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Signetics

FAST
Data
Manual

Signetics

FAST Products

Data
Manual
1987

FAST:
The World's Leading High-Performance TTL Family

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Preface

Signetics would like to thank you for your interest in our FAST product line. Because of its wide customer acceptance, FAST has become the world's leading high-performance logic family. We are proud to participate in and contribute to the dynamic growth of this product family. With over 150 part types released to production, Signetics now offers the broadest selection of FAST products.

Each data sheet contained in this manual is designed to stand alone and reflect the latest DC and AC specifications for a particular product. Several changes differentiate these data sheets from previous ones. First, all reference to military product has been deleted, specifically, to reflect recent government requirements imposed by Revision C of MIL-STD 883, including the general provisions of Paragraph 1.2. Specifications for military-grade FAST products are available in the latest Military Products Data Manual available from your nearest Signetics Sales Office, sales representative, or authorized distributor. Second, each commercial 74F product is specified over a 10% V_{CC} range, for both AC and DC parameters. Additionally, DC specifications for V_{OH} and V_{OL} are provided over the 5% V_{CC} range.

This 1987 FAST Data Manual updates a large number of data sheets which were "preliminary" in the 1986 Manual, and adds other newly defined products.

Features of this data manual include:

- Updated Availability and Functional Cross-Reference Guides
- An expanded Circuit Characteristics Section
- A User's Guide
- Selected Application Notes
- An expanded chapter on Surface Mounted Devices (SMD) and an Application Note on Thermal Considerations in SMD
- An expanded section on package outlines

New FAST part types are being released continuously. As you see new product announcements, please contact your nearest Signetics Sales Office, sales representative, or authorized distributor for the latest technical information.

In addition to FAST, Signetics Standard Products Division offers the industry's broadest line of commercially available Logic Products, spanning a wide speed/power spectrum from ECL (100K/10K) to TTL (74, 74LS, 74S, 74ALS, 8T, and 8200) to CMOS (4000 Series, 74HC/HCT, 74AC/ACT). Information on these product lines is also available from your nearest Signetics Sales Office, sales representative, or authorized distributor.

Signetics Standard Products Division — Logic Products

Product Status

DEFINITIONS

Data Sheet Identification	Product Status	Definition
Objective Specification	**Formative or In Design**	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	**Preproduction Product**	This data sheet contains preliminary data and supplementary data will be published at a later date. Signetics reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product Specification	**Full Production**	This data sheet contains Final Specifications. Signetics reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

Signetics

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Sales Offices 10-3

74F FAST TTL Introduction

THE HIGH-SPEED LOGIC OF THE '80s

Product Description

Signetics has combined advanced oxide-isolated fabrication techniques with standard TTL functions to create a new family designed for the '80s. The high operating speeds of FAST can push system operating speeds into areas previously reserved for 10K ECL, but with simple TTL design rules and single 5V power supplies. Low input loading allows the user to mix LS, ALS, and HCMOS in the same system without the need for translators and restrictive fanout requirements.

FAST circuits are pin-for-pin replacements for 74S types, but offer dissipation 3-4 times lower and higher operating speeds. Existing systems can achieve much lower power and improved performance by replacing the 74S types with the corresponding FAST devices.

The input structure provides better noise immunity because of higher thresholds, while the oxide-isolation and new circuit techniques create devices that have less variation with temperature or supply voltage than existing TTL logic families. Signetics guarantees all AC parameters under realistic system conditions – across the supply voltage spread and the temperature range, and with heavy 50pF output loads.

The use of high-capacitance PNP inputs has been avoided, and clamping diodes have been added to both the inputs and outputs to prevent negative overshoots. High input breakdown voltages allow unused inputs to be tied directly to V_{CC} without pull-up resistors.

Multiple sources and a complete family of powerful circuits combine to make Signetics FAST the logic choice of the '80s.

FEATURES

- **3ns propagation delays**
- **4m w/gate power dissipation**
- **Guaranteed AC performance over temperature and extended V_{CC} Range: 5V ± 10%**
- **High-impedance NPN base input structure on many types for reduced bus loading in Low state ($I_{IL} = 20\mu A$)**
- **Standard TTL functions and pinouts**
- **Replacement for "S" types...1/4 the power**
- **Designer's choice for new system designs**

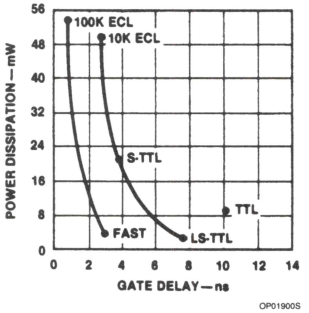

Figure 1. The Speed/Power Spectrum

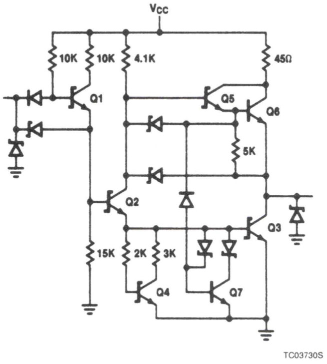

Figure 2. Basic FAST Gate

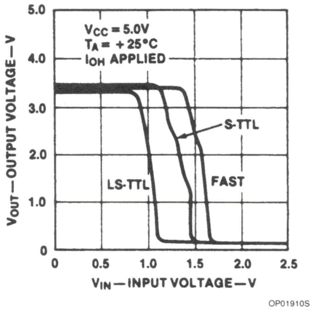

Figure 3. Transfer Functions At Room Temperature

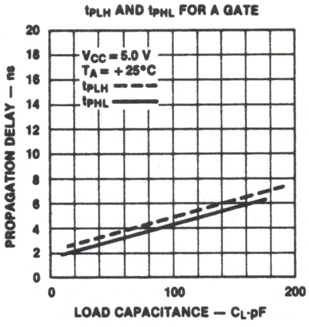

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Figure 4. Propagation Delay VS Load Capacitance

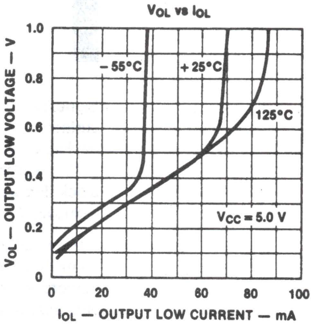

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Figure 5. Output LOW Characteristics

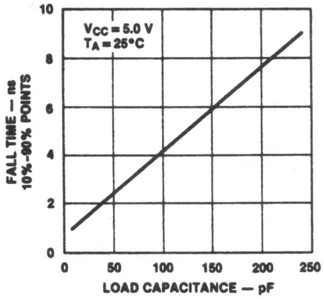

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Figure 6. Fall Time VS Load Capacitance

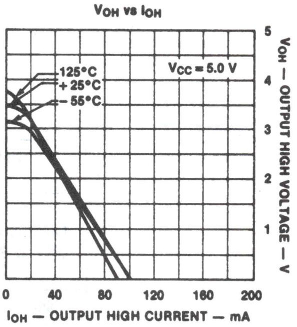

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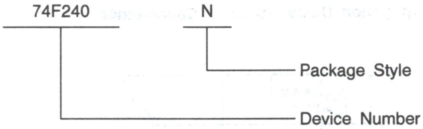
Figure 7. Output HIGH Characteristics

Ordering Information

Signetics commercial FAST products are generally available in both standard dual-in-line and surface mounted options. The ordering code specifies temperature range, device number, and package style as shown below. For commercial product, the standard temperature range is 0-70°C. Available package options are shown on individual data sheets in the "Ordering Code" block. For surface mounted devices the S.O. plastic dual-in-line package is supplied up to and including 28 pins. Above 28 pins, the plastic leaded chip carrier is utilized.

A wide variety of functions and package options is available for military products. Information on military products is available from the nearest Signetics sales office, sales representative, or authorized distributor. The Signetics Military Products Data Manual contains specifications, package, and ordering information for all military-grade products.

ORDERING CODE EXAMPLES



TEMPERATURE RANGE	DEVICE NUMBER	PACKAGE STYLE
Commercial Range 0°C to 70°C	74FXXX	N = Plastic DIP D = Plastic S.O. DIP (surface mounted) A = Plastic Leaded Chip Carrier
Military Range −55°C to 125°C	See Military Products Data Manual	

Section 1
Indices

FAST Products

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Function Selection Guide 1-7

Availability Guide

FAST Products

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74F02	Quad 2-Input NOR Gate	A
74F04	Hex Inverter	A
74F08	Quad 2-Input AND Gate	A
74F10	Triple 3-Input NAND Gate	A
74F11	Triple 3-Input AND Gate	A
74F13	Dual 4-Input NAND Schmitt Trigger	A
74F14	Hex Inverter Schmitt Trigger	A
74F20	Dual 4-Input NAND Gate	A
74F27	Triple 3-Input NOR Gate	A
74F30	8-Input NAND Gate	A
74F32	Quad 2-Input OR Gate	A
74F37	Quad 2-Input NAND Buffer	A
74F38	Quad 2-Input NAND Buffer (O.C.)	A
74F40	Dual 4-Input NAND Buffer	A
74F51	Dual 2-Wide 3-Input, 2-Wide 2-Input AND-OR-INVERT Gate	A
74F64	4-2-3-2 Input AND/OR Invert Gate	A
74F74	Dual D-Type Flip-Flop	A
74F83	4-Bit Binary Adder with Fast Carry (Center Power 'F283)	A
74F85	4-Bit Magnitude Comparator	A
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74F109	Dual J$\overline{K}$ Positive Edge Triggered Flip-Flop	A
74F112	Dual JK Negative Edge Triggered Flip-Flop	A
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74F126	Quad Buffer (3-State)	A
74F132	Quad 2-Input NAND Schmitt Trigger	A
74F133	13-Input NAND Gate	A
74F138	1-of-8 Decoder/Demultiplexer	A
74F139	Dual 1-of-4 Decoder/Demultiplexer	A
74F148	8-Line to 3-Line Priority Encoder	A

DEVICE	DESCRIPTION	AVAILA-BILITY
74F151	8-Input Multiplexer	A
74F151A	8-Input Multiplexer	A
74F153	Dual 4-Input Multiplexer	A
74F154	1-of-16 Decoder/Demultiplexer	A
74F157	Quad 2-Input Multiplexer, NINV	A
74F157A	Quad 2-Input Multiplexer, NINV	A
74F158	Quad 2-Input Multiplexer, INV	A
74F158A	Quad 2-Input Multiplexer, INV	A
74F161A	4-Bit Binary Counter, Asynch Reset	A
74F162A	BCD Decade Counter, Synch Reset	A
74F163A	4-Bit Binary Counter, Synch Reset	A
74F164	8-Bit Serial-In Parallel-Out Shift Register	A
74F166	8-Bit Serial/Parallel-In, Serial Out Shift Register	A
74F168	4-Bit Up/Down BCD Decade Synch Counter (3-State)	A
74F169	4-Bit Up/Down Binary Synch Counter (3-State)	A
74F173	Quad D Flip-Flop (3-State)	A
74F174	Hex D Flip-Flop with Master Reset	A
74F175	Quad D Flip-Flop with Master Reset	A
74F181	4-Bit Arithmetic Logic Unit	A
74F182	Carry Look-Ahead Generator	A
74F189	64-Bit Random Access Memory (3-State)	2H 87
74F190	Asynch Presettable Up/Down BCD Decade Counter	A
74F191	Asynch Presettable 4-Bit Binary Up/Down Counter	A
74F192	Synch Presettable BCD Decade Up/Down Counter	A
74F193	Synch Presettable 4-Bit Binary Up/Down Counter	A
74F194	4-Bit Bidirectional Universal Shift Register	A
74F195	4-Bit Parallel Access Shift Register	A
74F198	8-Bit Bidirectional Universal Shift Register	A
74F199	8-Bit Parallel Access Shift Register	A
74F240	Octal Bus/Line Driver, INV (3-State)	A

Availability Guide

DEVICE	DESCRIPTION	AVAILABILITY
74F241	Octal Bus/Line Driver, NINV (3-State)	A
74F242	Quad Bus Transceiver, INV (3-State)	A
74F243	Quad Bus Transceiver, NINV (3-State)	A
74F244	Octal Bus/Line Driver, NINV (3-State)	A
74F245	Octal Bus Transceiver (3-State)	A
74F251	8-Input Multiplexer (3-State)	A
74F251A	8-Input Multiplexer (3-State)	A
74F253	Dual 4-Input Multiplexer (3-State)	A
74F256	Dual 4-Bit Addressable Latch	A
74F257	Quad 2-Input Multiplexer, NINV (3-State)	A
74F257A	Quad 2-Input Multiplexer, NINV (3-State)	A
74F258	Quad 2-Input Multiplexer, INV (3-State)	A
74F258A	Quad 2-Input Multiplexer, INV (3-State)	A
74F259	8-Bit Addressable Latch	A
74F260	Dual 5-Input NOR Gate	A
74F269	8-Bit Bidirectional Binary Counter (3-State)	A
74F273	Octal D Flip-Flop	A
74F280A	9-Bit Odd/Even Parity Generator/ Checker	A
74F280B	9-Bit Odd/Even Parity Generator/ Checker	A
74F283	4-Bit Binary Adder with Fast Carry	A
74F298	Quad 2-Input Multiplexer with Storage	A
74F299	Octal Shift/Storage Register (3-State)	A
74F322	Octal Shift/Storage Register (3-State)	A
74F323	Octal Shift/Storage Register (3-State)	A
74F350	4-Bit Shifter (3-State)	A
74F352	Dual 4-Input Multiplexer (Inverted '153)	A
74F353	Dual 4-Input Multiplexer (Inverted '253) (3-state)	A
74F365	Hex Buffer with Common Enable (3-State)	A
74F366	Hex Inverter with Common Enable (3-State)	A
74F367	Hex Buffer, 4-Bit and 2-Bit (3-State)	A
74F368	Hex Inverter, 4-Bit and 2-Bit (3-State)	A
74F373	Octal D Latch (3-State)	A
74F374	Octal D Flip-Flop (3-State)	A
74F377	Octal D-Type Flip-Flop with Enable	A
74F378	Hex D Flip-Flop with Enable	A
74F379	Quad D Flip-Flop with Enable	A
74F381	4-Bit Arithmetic Logic Unit	A

DEVICE	DESCRIPTION	AVAILABILITY
74F382	4-Bit Arithmetic Logic Unit	A
74F385	Quad Serial Adder/Subtractor	A
74F393	Dual 4-Bit Binary Ripple Counter	A
74F395	4-Bit Cascadable Shift Register (3-State)	A
74F398	Quad 2-Port Register with Complementary Outputs	A
74F399	Quad 2-Port Register with True Outputs	A
74F412	Octal Multi-Mode Buffered Latch	A
74F432	Octal Multi-Mode Buffered Latch	A
74F455	Octal Buffer w/Parity Generator Checker, INV (3-State)	A
74F456	Octal Buffer w/Parity Generator Checker, NINV (3-State)	A
74F521	Octal Comparator	A
74F524	8-Bit Register Comparator (O.C.)	A
74F533	Octal Inverting D Latch (3-State)	A
74F534	Octal Inverting D Flip-Flop (3-State)	A
74F537	1-of-10 Decoder (3-State)	A
74F538	1-of-8 Decoder (3-State)	A
74F539	Dual 1-of-4 Decoder (3-State)	A
74F540	Octal Inverting Buffer (3-State) Broadside Pinout 'F240	A
74F541	Octal Buffer (3-State) Broadside Pinout 'F244	A
74F543	Octal Transparent Bidirectional Latch, NINV (3-State)	A
74F544	Octal Transparent Bidirectional Latch, INV (3-State)	A
74F545	Octal Bus Transceiver (3-State)	A
74F547	Octal Decoder/MUX w/Addr Latches and Acknowledge	A
74F548	Octal Decoder/Multiplexer with Acknowledge	A
74F550	Octal Registered Transceiver with Status Flags, NINV (3-State)	2H 87
74F551	Octal Registered Transceiver with Status Flags, INV (3-State)	2H 87
74F552	Octal Registered Transceiver with Parity and Status flags (3-State)	2H 87
74F563	Octal D Latch (3-State) Broadside Pinout 'F533	2H 87
74F564	Octal D Flip-Flop (3-State) Broadside Pinout 'F534	2H 87
74F568	4-Bit Decade Up/Down Counter (3-State)	A
74F569	4-Bit Binary Up/Down Counter (3-State)	A

Availability Guide

DEVICE	DESCRIPTION	AVAILA-BILITY
74F573	Octal D Latch (3-State) Broadside Pinout 'F373	2H 87
74F574	Octal D Flip-Flop (3-State) Broadside Pinout 'F374	2H 87
74F579	8-Bit Up/Down Counter, Common I/O (3-State)	A
74F582	4-Bit BCD Arithmetic Logic Unit	A
74F583	4-Bit BCD Adder	A
74F588	GPIB Compatible Octal Transceiver	A
74F595	8-Bit Shift Register with Output Latch	2H 87
74F597	8-Bit Shift Register with Input Latch	2H 87
74F598	8-Bit Shift Register with Input Latch	2H 87
74F604	Dual 8-Bit Latch (3-State)	A
74F605	Dual 8-Bit Latch (O.C.)	A
74F620	Octal Bus Transceiver, INV (3-State)	A
74F621	Octal Bus Transceiver, NINV (O.C.)	A
74F622	Octal Bus Transceiver, INV (O.C.)	A
74F623	Octal Bus Transceiver, NINV (3-State)	A
74F630	Memory Error Detector/Corrector (3-State)	2H 87
74F631	Memory Error Detector/Corrector (O.C.)	2H 87
74F640	Octal Bus Transceiver, Inverting (3-State)	A
74F641	Octal Bus Transceiver (O.C.)	A
74F642	Octal Bus Transceiver, Inverting (O.C.)	A
74F646	Octal Bus Transceiver and Register, NINV (3-State)	A
74F647	Octal Bus Transceiver and Register, NINV (O.C.)	A
74F648	Octal Bus Transceiver and Register, INV (3-State)	A
74F649	Octal Bus Transceiver and Register, INV (O.C.)	A
74F651	Octal Bus Transceiver and Register, INV (3-State)	A
74F652	Octal Bus Transceiver and Register, NINV (3-State)	A
74F653	Octal Bus Transceiver and Register, INV (O.C.)	A
74F654	Octal Bus Transceiver and Register, NINV (O.C.)	A
74F655A	Octal Inverting Buffer w/Parity Gen-Chk. (3-State)	A
74F656A	Octal Buffer w/Parity Generator-Checker (3-State)	A
74F657	Octal Bus Transceiver w/Parity Gen-Chk. (3-State)	A

DEVICE	DESCRIPTION	AVAILA-BILITY
74F670	4 × 4 Register File (3-State)	2H 87
74F673A	16-Bit Serial-In, Serial/Parallel-Out Shift Register (3-State)	2H 87
74F674	16-Bit Serial/Parallel-In, Serial-Out Shift Register (3-State)	2H 87
74F675	16-Bit Serial-In, Serial/Parallel-Out Shift Register (3-State)	2H 87
74F676	16-Bit Serial/Parallel-In, Serial-Out Shift Register (3-State)	A
74F711	Quint 2-Input Multiplexer	2H 87
74F712	Quint 3-Input Multiplexer	2H 87
74F723	Quad 3-Input Multiplexer	2H 87
74F725	Quad 3-Input Multiplexer	2H 87
74F732	Quad Data Multiplexer, NINV	2H 87
74F733	Quad Data Multiplexer, INV	2H 87
74F764	DRAM Dual Ported Controller with Latch (100 MHz)	A
74F764A	DRAM Dual Ported Controller with Latch (150 MHz)	A
74F764-1	DRAM Dual Ported Controller with Latch	A
74F765	DRAM Dual Ported Controller without Latch (100 MHz)	A
74F765A	DRAM Dual Ported Controller without Latch (150 MHz)	A
74F765-1	DRAM Dual Ported Controller without Latch	A
74F779	8-Bit Up/Down Counter, Common I/O (3-State)	A
74F786	4-Input Asynchronous Bus Arbiter	A
74F804	Hex 2-Input NAND Driver	2H 87
74F805	Hex 2-Input NOR Driver	2H 87
74F808	Hex 2-Input AND Driver	2H 87
74F821	10-Bit Register, NINV (3-State)	2H 87
74F822	10-Bit Register, INV (3-State)	2H 87
74F823	9-Bit Register, NINV (3-State)	2H 87
74F824	9-Bit Register, INV (3-State)	2H 87
74F825	8-Bit Register, NINV (3-State)	2H 87
74F826	8-Bit Register, INV (3-State)	2H 87
74F827	10-Bit Buffer, NINV (3-State)	A
74F828	10-Bit Buffer, INV (3-State)	A
74F832	Hex 2-Input OR Driver	2H 87
74F835	Microprogram Sequence Controller	2H 87
74F841	10-Bit Latch, NINV (3-State)	A
74F842	10-Bit Latch, INV (3-State)	A

Availability Guide

DEVICE	DESCRIPTION	AVAILA-BILITY
74F843	9-Bit Latch, NINV (3-State)	A
74F844	9-Bit Latch, INV (3-State)	A
74F845	8-Bit Latch, NINV (3-State)	A
74F846	8-Bit Latch, INV (3-State)	A
74F861	10-Bit Transceiver, NINV (3-State)	A
74F862	10-Bit Transceiver, INV (3-State)	A
74F863	9-Bit Transceiver, NINV (3-State)	A
74F864	9-Bit Transceiver, INV (3-State)	A
74F881	4-Bit Arithmetic Logic Unit/Function Generator	A
74F882	32 Bit Look-Ahead Carry Generator	A
74F1240	Octal Buffer (3-State) Light Load 'F240	A
74F1241	Octal Buffer (3-State) Light Load 'F241	A
74F1242	Quad Transceiver, Inverting (3-State) Light Load 'F242	A
74F1243	Quad Transceiver (3-State) Light Load 'F243	A
74F1244	Octal Buffer (3-State) Light Load 'F244	A
74F1245	Octal Bus Transceiver (3-State) Light Load 'F245	A
74F1761	DRAM and Interrupt Vector Controller	2H 87
74F1762	1 MBit Memory Address Controller	2H 87
74F1763	1 MBit Intelligent DRAM Controller	2H 87

DEVICE	DESCRIPTION	AVAILA-BILITY
74F1764	1 MBit DRAM Dual Ported Controller w/Latch	2H 87
74F1764A	1 MBit DRAM Dual Ported Controller w/Latch	2H 87
74F1765	1 MBit DRAM Dual Ported Controller w/o Latch	2H 87
74F1765A	1 MBit DRAM Dual Ported Controller w/o Latch	2H 87
74F2952	Octal Registered Transceiver, NINV (3-State)	2H 87
74F2953	Octal Registered Transceiver, INV (3-State)	2H 87
74F3037	Quad 2-Input 30Ω Transmission Line Driver, NINV	A
74F3038	Quad 2-Input 30Ω Transmission Line Driver, NINV (O.C.)	A
74F3040	Dual 4-Input 30Ω Transmission Line Driver, NINV	A
74F30240	Octal 30Ω Transmission Line/Backplane Driver, INV (O.C.)	A
74F30244	Octal 30Ω Transmission Line/Backplane Driver, NINV (O.C.)	A
74F30245	Octal 30Ω Xmission Line/Backplane Transceiver, NINV Transceiver, NINV (O.C.)	A
74F30640	Octal 30Ω Xmission Line/Backplane Transceiver, NINV Transceiver, INV (O.C.)	A

Signetics

Function Selection Guide

FAST Products

GATES

FUNCTION	DEVICE NUMBER
Inverters	
Hex Inverter	74F04
Hex Inverter Schmitt Trigger	74F14
NAND	
Quad 2-Input	74F00
Triple 3-Input	74F10
Dual 4-Input, Schmitt Trigger	74F13
Dual 4-Input	74F20
8-Input	74F30
Quad 2-Input, Schmitt Trigger	74F132
13-Input	74F133
AND	
Quad 2-Input	74F08
Triple 3-Input	74F11
NOR	
Quad 2-Input	74F02
Triple 3-Input	74F27
Dual 5-Input	74F260
OR	
Quad 2-Input	74F32
Exclusive-OR	
Quad	74F86
Combination Gates	
Dual 2-Wide, 2-Input AND-OR-Invert	74F51
4-2-3-2 Input AND-OR-Invert	74F64

DUAL FLIP-FLOPS

FUNCTION	DEVICE NUMBER	CLOCK EDGE	SET	CLEAR
D	74F74	↑	LOW	LOW
JK	74F109	↑	LOW	LOW
JK	74F112	↓	LOW	LOW
JK	74F113	↓	LOW	
JK	74F114	↓	LOW	LOW

MULTIPLE FLIP-FLOPS

FUNCTION	DEVICE NUMBER	RESET LEVEL	CLOCK EDGE	OUTPUT
Quad D	74F175	LOW	↑	NINV INV
Quad D with Enable	74F379		↑	NINV INV
Hex D	74F174	LOW	↑	NINV
Hex D with Enable	74F378		↑	NINV
Quad D	74F173	HIGH	↑	NINV
Octal D	74F273	LOW	↑	NINV
Octal D, 3-State	74F374		↑	NINV
Octal D, 3-State	74F534		↑	INV
Octal D with Enable	74F377		↑	NINV
Octal D, 3-State	74F564		↑	INV
Octal D, 3-State	74F574		↑	NINV

Function Selection Guide

OTHER REGISTERS, REGISTER FILES

FUNCTION	DEVICE NUMBER	BITS	SERIAL ENTRY	PARALLEL ENTRY	CLOCK
Quad 2 Port	74F398	4 × 2		2D (mux)	↑
Quad 2 Port	74F399	4 × 2		2D (mux)	↑
Dual Octal Register	74F604	8		8D	↑
Dual Octal Register	74F605	8		8D	↑
Register file	74F670	4 × 4		4D	
10-Bit, Non-Inverting	74F821	10		2D	↑
10-Bit, Inverting	74F822	10		2D	↑
9-Bit, Non-Inverting	74F823	9		2D	↑
9-Bit, Inverting	74F824	9		2D	↑
8-Bit, Non-Inverting	74F825	8		2D	↑
8-Bit, Inverting	74F826	8		2D	↑

LATCHES

FUNCTION	DEVICE NUMBER	COMMON CLEAR (LEVEL)	ENABLE INPUT (LEVEL)	OUTPUT
Dual 4-Bit Addressable	74F256	LOW	1(L)	NINV
Dual 4-Bit Addressable	74F259	LOW	1(H)	NINV
Octal, 3-State	74F373		1(H)	NINV
Octal Inverting, 3-State	74F533		1(H)	INV
Octal Transparent, Inverting, 3-State	74F563		1(H)	INV
Octal Transparent, 3-State	74F573		1(H)	NINV
Multi-Mode Buffered, 3-State	74F412	LOW	1(L), 2(H)	NINV
Multimode Buffered	74F432	LOW		INV
10-Bit, Non-Inverting	74F841		1(H)	NINV
10-Bit, Inverting	74F842		1(H)	INV
9-Bit, Non-Inverting	74F843	LOW	1(H)	NINV
9-Bit, Inverting	74F844	LOW	1(H)	INV
8-Bit, Non-Inverting	74F845	LOW	1(H)	NINV
8-Bit, Inverting	74F846	LOW	1(H)	INV

MULTIPLEXERS

FUNCTION	DEVICE NUMBER	ENABLE INPUT (LEVEL)	SELECT INPUTS	OUTPUT
Quad 2-Input	74F157	1(L)	1	NINV
Quad 2-Input	74F158	1(L)	1	NINV
Quint 2-Input	74F711	1	1	NINV
Quad 2-Input, 3-State	74F257		1	NINV
Quad 2-Input, 3-State	74F258		1	INV
Quad 2-Input	74F298		1	NINV
Quad 3-Input	74F732		3	INV
Quad 3-Input	74F733		3	NINV
Quint 3-Input	74F712		2	NINV
Quad 3-Input	74F723	1	2	NINV
Quad 3-Input	74F723	1	2	NINV
Quad 3-Input	74F132		3	INV
Quad 3-Input	74F133		3	NINV
Quad 4-Input	74F725		1	NINV
Quad 4-Input	74F725		1	NINV
Dual 4-Input	74F153	2(L)	2	NINV INV
Dual 4-Input	74F352	2	2	INV
Dual 4-Input, 3-State	74F253		2	NINV
Dual 4-Input, 3-State	74F353	2	2	INV
Quint 2-Input Multiplexer	74F711	1	1	NINV
Quint 3-Input Multiplexer	74F712		2	NINV
8-Input	74F151	1(L)	3	NINV INV
8-Input, 3-State	74F251		1	NINV INV

Function Selection Guide

DECODER/DEMULTIPLEXERS

FUNCTION	DEVICE NUMBER	ADDRESS INPUTS	ENABLE LEVEL	OUTPUT LEVEL
Dual 1-of-4	74F139	2 + 2	1(L) + 1(L)	4(L) + 4(L)
Dual 1-of-4	74F539	2 + 2	1(L) + 1(L)	4(H) + 4(H)
1-of-8	74F138	3	2(L), 1(H)	8(L)
1-of-8	74F538	3	2(L), 2(H)	8(H)
1-of-10	74F537	4	1(L), 1(H)	10(H)
1-of-16	74F154	4	2(L)	16(L)
Octal, with Address Latches and Acknowledge	74F547	3	1(L), 2(H)	8(L)
Octal with Acknowledge	74F548	3	2(L), 2(H)	8(L)

BUFFERS, DRIVERS AND TRANSCEIVERS

FUNCTION	DEVICE NUMBER	OUTPUT
Quad 2-Input NAND Buffer	74F37	INV
Quad 2-Input NAND Buffer, OC	74F38	INV
Dual 4-Input NAND Buffer	74F40	INV
Quad 2-Input NAND Transmission Line Driver	74F3037	INV
Quad 2-Input Transmission Line Driver	74F3038	NINV
Dual 4-Input NAND Transmission Line Driver	74F3040	INV
Octal 30Ω Transmission Line/Backplane Driver, OC	74F30240	INV
Octal 30Ω Transmission Line/Backplane Driver, OC	74F30244	NINV
Octal 30Ω Transmission Line/Backplane Transceiver	74F30245	NINV
Octal 30Ω Transmission Line/Backplane Transceiver	74F30640	INV
Octal Transceiver	74F621	NINV
Octal Transceiver	74F623	NINV
Octal Transceiver	74F641	NINV
Octal Transceiver	74F642	INV
Octal Transceiver and Registers	74F647	NINV
Octal Transceiver and Registers	74F649	INV
Octal Transceiver and Registers	74F653	INV
Octal Transceiver and Registers	74F654	NINV

SHIFT REGISTERS

FUNCTION	DEVICE NUMBER	BITS	SERIAL ENTRY	PARALLEL ENTRY	CLOCK
Serial-In/Parallel-Out	74F164	8	D_{sa}, D_{sb}		↑
Serial-In/Parallel-Out Output Latch, 3-State	74F595	8	D_s		↑
Serial-In/Serial-Out/Parallel-Out, 3-State	74F673	16	SI/O		↓
Serial-In/Serial-Out/Parallel-Out	74F675	16	D		⎍
Serial-In/Parallel-In/Serial-Out, Parallel-Out	74F195	4	J,K	4D	↑
Serial-In/Parallel-In/Parallel-Out, Shift Right	74F199	8	J,K	8D	↑
Serial-In/Parallel-In/Serial-Out, Parallel-Out	74F598	8	D_{s0}, D_{s1}	8 I/O	↑
Serial-In/Parallel-In/Serial-Out	74F674	16	SI/O	SI/O, 16D	↓
Serial-In/Parallel-In/Serial-Out	74F676	16	SI	16D	↑
Serial-In/Parallel-In/Parallel-Out Shift Right, 3-State	74F395	4	D_s	4D	↑
Serial-In/Parallel-In/Serial-Out, Parallel-Out, 3-State	74F322	8	D_0, D_1	8 I/O	↑
Serial-In/Parallel-In/Parallel-Out	74F194	4	D_{sr}, D_{sl}	4D	↑
Serial-In/Parallel-In/Parallel-Out, Shift Right	74F199	8	$J, \overline{K}$	$D_0 - D_7$	↑
Serial-In/Parallel-In/Serial-Out	74F166	8	D_S	$D_0 - D_7$	↑
Serial-In/Parallel-In/Parallel-Out, Bidirectional	74F198	8	D_{sr}, D_{sl}	8D	↑
Serial-In/Parallel-In/Serial-Out, Parallel-Out, 3-State	74F299	8	D_{s0}, D_{s7}	8 I/O	↑
Serial-In/Parallel-In/Serial-Out, Parallel-Out, 3-State	74F323	8	D_{s0}, D_{s7}	8 I/O	↑
Parallel-In/Serial-Out Input Latch	74F597	8	D_s	8D	↑
Parallel-In/Parallel-Out, 3-State	74F350	4	$I_{-3} - I_{+3}$	4Y	
Parallel-In/Parallel-Out, 3-State	74F604	16		$A_1 - A_8$, $B_1 - B_8$	↑
Parallel-In/Parallel-Out, OC	74F605	16		$A_1 - A_8$, $B_1 - B_8$	↑
Parallel-In/Parallel-Out, True and Complement Output	74F398	8	S	$I_{0a} - I_{0d}$, $I_{1a} - I_{1d}$	↑
Parallel-In/Parallel-Out	74F399	8	S	$I_{0a} - I_{0d}$, $I_{1a} - I_{1d}$	↑

Function Selection Guide

COUNTERS

FUNCTION	DEVICE NUMBER	MODULUS	PARALLEL ENTRY	PRESETTABLE	CLOCK EDGE
Synchronous	74F160A	10	S	X	↑
Synchronous	74F161A	16	S	X	↑
Synchronous	74F162A	10	S	X	↑
Synchronous	74F163A	16	S	X	↑
Up/Down	74F168	10	S	X	↑
Up/Down	74F169	16	S	X	↑
Up/Down	74F190	10	A	X	↑
Up/Down	74F191	16	A	X	↑
Up/Down	74F192	10	A	X	↑
Up/Down	74F193	16	A	X	↑
Up/Down	74F269	256	S	X	↑
Up/Down, 3-State	74F568	10	S	X	↑
Up/Down, 3-State	74F569	16	S	X	↑
Up/Down	74F579	256	S (I/O)	X	↑
Up/Down, 3-State Multiplexed	74F779	256	S (I/O)	X	↑
Ripple	74F393	16			↓

Function Selection Guide

THREE-STATE BUFFERS, DRIVERS AND TRANSCEIVERS

FUNCTION	DEVICE NUMBER	OUTPUT
Quad Buffer	74F125	NINV
Quad Buffer	74F126	NINV
Quad Bus Transceiver	74F242	INV
Quad Bus Transceiver	74F243	NINV
Quad Bus Transceiver	74F1242	INV
Quad Bus Transceiver	74F1243	NINV
Hex Buffer	74F365	NINV
Hex Inverter	74F366	INV
Hex Buffer, 4-Bit and 2-Bit	74F367	NINV
Hex Inverter, 4-Bit and 2-Bit	74F368	INV
Octal Buffer	74F240	INV
Octal Buffer	74F241	NINV
Octal Buffer	74F244	NINV
Octal Buffer	74F1240	INV
Octal Buffer	74F1241	NINV
Octal Buffer	74F1244	NINV
Octal Buffer with Parity	74F455	INV
Octal Buffer with Parity	74F456	NINV
Octal Buffer with Parity	74F655A	INV
Octal Buffer with Parity	74F656A	NINV
Octal Driver	74F540	INV
Octal Driver	74F541	NINV
Octal Transceiver	74F245	NINV
Octal Transceiver	74F545	NINV
Octal Transceiver with IEEE-488 Termination Resistors	74F588	NINV
Octal Transceiver	74F620	INV
Octal Transceiver	74F622	INV
Octal Transceiver	74F640	INV
Octal Transceiver	74F651	INV
Octal Transceiver	74F652	NINV
Octal Transceiver with Parity	74F657	NINV
Octal Transceiver/Register	74F646	NINV
Octal Transceiver/Register	74F648	INV
Octal Transceiver	74F1245	NINV
10-Bit Buffer	74F827	NINV
10-Bit Buffer	74F828	INV
10-Bit Transceiver	74F861	NINV
10-Bit Transceiver	74F862	INV
9-Bit Tranceiver	74F863	NINV
9-Bit Tranceiver	74F864	INV
Octal Registered Transceiver	74F543	NINV
Octal Registered Transceiver	74F544	INV
8-Bit Registered Transceiver	74F2952	NINV
8-Bit Registered Transceiver	74F2953	INV
Octal Registered Transceiver with Status Flags	74F550	NINV
Octal Registered Transceiver with Status Flags	74F551	INV
Octal Registered Transceiver with Parity and Status Flags	74F552	INV

PRIORITY ENCODERS

FUNCTION	DEVICE NUMBER	INPUT ENABLE (LEVEL)	INPUT/OUTPUT (LEVEL)
8-to-3	74F148	LOW	Active-Low

Function Selection Guide

ARITHMETIC FUNCTIONS

FUNCTION	DEVICE NUMBER
4-Bit ALU	74F181
4-Bit ALU	74F381
4-Bit ALU with Overflow Output for Two's Complement	74F382
ALU/Function Generator	74F881
4-Bit Binary Full Adder with Ripple Carry	74F83
4-Bit Binary Full Adder with FAST Carry	74F283
Look-ahead Carry Generator	74F182
Look-ahead Carry Generator	74F882
Quad Serial Adder/Subtractor	74F385
4-Bit BCD Arithmetic Logic Unit	74F582
4-Bit BCD Adder	74F583

COMPARATORS

FUNCTION	DEVICE NUMBER
4-Bit Comparator	74F85
8-Bit Comparator	74F521
8-Bit Register Comparator	74F524

PARITY

FUNCTION	DEVICE NUMBER
9-Bit Odd/Even Parity Generator/Checker	74F280A/280B

SPECIAL FUNCTIONS

FUNCTION	DEVICE NUMBER
16-Bit Error Detection	74F630
16-Bit Error Detection/Correction Circuit	74F631
64-Bit RAM	74F189
8-Bit Serial Multiplier with Adder/Subtractor	74F784
DRAM Dual-ported Controller with Refresh	74F764
DRAM Dual-ported Controller without Latch	74F765
4-Input Asynchronous Arbitor	74F786
DRAM Interrupt Vector Controller	74F1761
1 MBit Memory Address Controller	74F1762
1 MBit Intelligent DRAM Controller	74F1763
1 MBit DRAM Dual Ported Controller with Latch	74F1764
1 MBit DRAM Dual Ported Controller without Latch	74F1765

Signetics

FAST Products

Section 2
Quality And Reliability

Quality And Reliability

FAST Products

SIGNETICS LOGIC PRODUCTS QUALITY

Signetics has put together a winning process for manufacturing Logic Products. Our standard is zero defects, and current customer quality statistics demonstrate our commitment to this goal.

The products produced in the Standard Products Division must meet rigid criteria as defined by our design rules and evaluated with a thorough product characterization and quality process. The capabilities of our manufacturing process are measured and the results evaluated and reported through our corporate-wide QA05 data base system. The SURE (Systematic And Uniform Reliability Evaluation) Program monitors the performance of our product in a variety of accelerated environmental stress conditions. All of these programs and systems are intended to prevent problems and to inform our customers and employees of our progress in achieving zero defects.

RELIABILITY BEGINS WITH THE DESIGN

Quality and reliability must begin with design. No amount of extra testing or inspection will produce reliable ICs from a design that is inherently unreliable. Signetics follows very strict design and layout practices with its circuits. To eliminate the possibility of metal migration, current density in any path cannot exceed 2×10^5 A/cm^2. Layout rules are followed to minimize the possibility of shorts, circuit anomalies, and SCR type latch-up effects. Numerous ground-to-substrate connections are required to ensure that the entire chip is at the same ground potential, thereby precluding internal noise problems.

PRODUCT CHARACTERIZATION

Before a new design is released, the characterization phase is completed to ensure that the distribution of parameters resulting from lot-to-lot variations is well within specified limits. Such extensive characterization data also provides a basis for identifying unique application-related problems which are not part of normal data sheet guarantees. Characterization takes place from −55°C to +125°C and at ±10% supply voltage.

QUALIFICATION

Formal qualification procedures are required for all new or changed products, processes, and facilities. These procedures ensure the high level of product reliability our customers expect. New facilities are qualified by corporate groups as well as by the quality organizations of specific units that will operate in the facility. After qualification, products manufactured by the new facility are subjected to highly accelerated environmental stresses to ensure that they can meet rigorous failure rate requirements. New or changed processes are similarly qualified.

QA05 – QUALITY DATA BASE REPORTING SYSTEM

The QA05 data reporting system collects the results of product assurance testing on all finished lots and feeds this data back to concerned organizations where appropriate action can be taken. The QA05 reports EPQ (Estimated Process Quality) results for electrical, visual/mechanical, hermeticity, and documentation audits. Data from this system is available on request.

THE SURE PROGRAM

The SURE (Systematic And Uniform Reliability Evaluation) Program audits/monitors products from all Signetics' divisions under a variety of accelerated environmental stress conditions. This program, first introduced in 1964, has evolved to suit changing product complexities and performance requirements.

The SURE Program has two major functions: Long-term accelerated stress performance audit and a short-term accelerated stress monitor. In the case of Logic products, samples are selected that represent all generic product groups in all wafer fabrication and assembly locations.

THE LONG-TERM AUDIT

One hundred devices from each generic family are subjected to each of the following stresses every eight weeks:

- High Temperature Operating Life: $T_J = 150$°C, 1000 hours, static biased or dynamic operation, as appropriate (worst case bias configuration is chosen)
- High Temperature Storage: $T_J = 150$°C, 1000 hours
- Temperature Humidity Biased Life: 85°C, 85% relative humidity, 1000 hours, static biased
- Temperature Cycling (Air-to-Air): −65°C to +150°C, 1000 cycles

THE SHORT-TERM MONITOR

Every other week a 50-piece sample from each generic family is run to 168 hours of pressure pot (15psig, 121°C, 100% saturated steam) and 300 cycles of thermal shock (−65°C to +150°C)

In addition, each Signetics assembly plant performs SURE product monitor stresses weekly on each generic family and molded package by pin count and frame type. Fifty-piece samples are run on each stress, pressure pot to 96 hours, thermal shock to 300 cycles.

SURE REPORTS

The data from these test matrices provides a basic understanding of product capability, an indication of major failure mechanisms, and an estimated failure rate resulting from each stress. This data is published quarterly and is available to customers upon request.

Many customers use this information in lieu of running their own qualification tests, thereby eliminating time-consuming and costly additional testing.

Quality And Reliability

RELIABILITY ENGINEERING

In addition to the product performance monitors encompassed in the corporate SURE Program, Signetics' Corporate and Division Reliability Engineering departments sustain a broad range of evaluation and qualification activities.

The engineering process includes:

- Evaluation and qualification of new or changed materials, assembly/wafer-fab processes and equipment, product designs, facilities and subcontractors.
- Device or generic group failure rate studies.
- Advanced environmental stress development.
- Failure mechanism characterization and corrective action/prevention reporting.

The environmental stresses utilized in the engineering programs are similar to those utilized for the SURE monitor; however, more highly-accelerated conditions and extended durations typify the engineering projects. Additional stress systems such as biased pressure pot, power-temperature cycling, and cycle-biased temperature-humidity, are also included in the evaluation programs.

FAILURE ANALYSIS

The SURE Program and the Reliability Engineering Program both include failure analysis activities and are complemented by corporate, divisional, and plant failure analysis departments. These engineering units provide a service to our customers who desire detailed failure analysis support and, who in turn provide Signetics with the technical understanding of the failure modes and mechanisms actually experienced in service. This information is essential in our ongoing effort to accelerate and improve our understanding of product failure mechanisms and their prevention.

ZERO DEFECTS PROGRAM

In recent years, United States industry has increasingly demanded improved product quality. We at Signetics believe that the customer has every right to expect quality products from a supplier. The benefits derived from quality products can best be summed up in the words, *lower cost of ownership.*

Those of you who invest in costly test equipment and engineering to assure that incoming products meet your specifications have a special understanding of the cost of ownership. And your cost does not end there; you are also burdened with inflated inventories, lengthened lead times, and more rework.

SIGNETICS UNDERSTANDS CUSTOMERS' NEEDS

Signetics has long had an organization of quality professionals inside all operating units, coordinated by a corporate quality department. This broad decentralized organization provides leadership, feedback, and direction for achieving a high level of quality. Special programs are targeted on specific quality issues.

In 1980 we recognized that in order to achieve outgoing levels on the order of 100PPM (parts per million), down from an industry practice of 10,000PPM, we needed to supplement our traditional quality programs with one that encompassed all activities and all levels of the company. Such unprecedented low defect levels could only be achieved by contributions from all employees; from the R and D laboratory to the shipping dock. In short, we needed a program that would effect a total cultural change within Signetics in our attitude toward quality.

QUALITY PAYS OFF FOR OUR CUSTOMERS

Signetics' dedicated programs in product quality improvement, supplemented by close working relationships with many of our customers, have improved outgoing product quality more than twenty-fold since 1980. Signetics' high quality levels have allowed us a "ship-to-stock" program where many major customers no longer need to perform incoming inspection. Incoming product moves directly from the receiving dock to the production line, greatly accelerating throughput and reducing inventories. Other customers have pared significantly the amount of sampling done on our products. Others are beginning to adopt these cost-saving practices.

We closely monitor the electrical, visual, and mechanical quality of all our products and review each return to find and correct the cause. Since 1981, over 90% of our customers have reported a significant improvement in overall quality (see Figure 1).

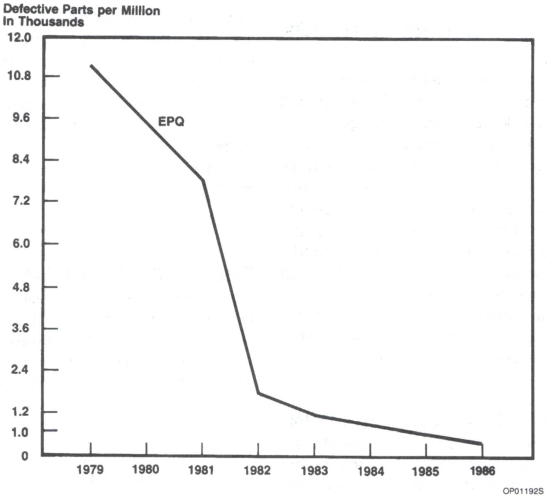


Figure 1. Signetics Quality Progress

Quality And Reliability

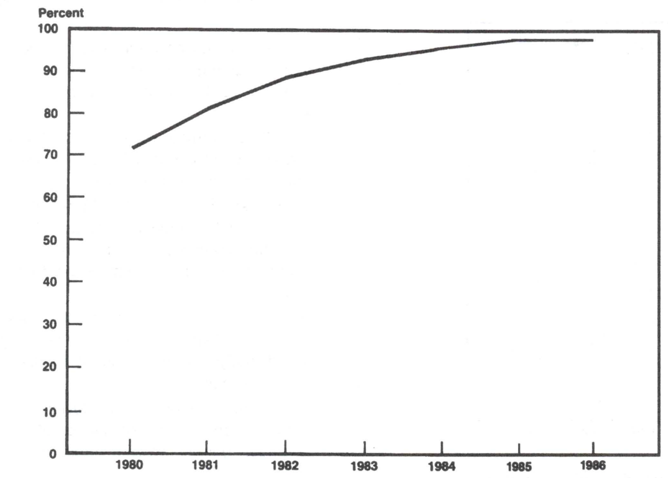


Figure 2. Performance To Schedule On-Time Delivery

At Signetics, quality means more than working circuits. It means on-time delivery of the right product at the agreed upon price (see Figure 2).

ONGOING QUALITY PROGRAM

The Quality Improvement Program at Signetics is based on "Do it Right the First Time". The intent of this innovative program is to change the perception of Signetics' employees that somehow quality is solely a manufacturing issue where some level of defects is inevitable. This attitude has been replaced by one of acceptance of the fact that all errors and defects are preventable, a point of view shared equally by all technical and administrative functions.

This program extends into every area of the company and more than 40 quality improvement teams throughout the organization drive its ongoing refinement and progress.

Key components of the program are the Quality College, the "Make Certain" Program, Corrective Action Teams, and the Error Cause Removal System.

The core concepts of doing it right the first time are embodied in the four absolutes of quality:

1. The definition of quality is conformance to requirements.
2. The system to achieve quality improvement is prevention.
3. The performance standard is zero defects.
4. The measurement system is the cost of quality.

QUALITY COLLEGE

Almost continuously in session, Quality College is a prerequisite for all employees. The intensive curriculum is built around the four absolutes of quality; colleges are conducted at company facilities throughout the world.

"MAKING CERTAIN" – ADMINISTRATIVE QUALITY IMPROVEMENT

Signetics' experience has shown that the largest source of errors affecting product and service quality is found in paperwork and in other administrative functions. The "Make Certain" Program focuses the attention of management and administrative personnel on error prevention, beginning with each employee's own actions.

This program promotes defect prevention in three ways: by educating employees as to the impact and cost of administrative errors, by changing attitudes from accepting occasional errors to one of accepting a personal work standard of zero defects, and by providing a formal mechanism for the prevention of errors.

CORRECTIVE ACTION TEAMS

Employees with the perspective, knowledge, and necessary skills to solve a problem are formed into ad hoc groups called Corrective Action Teams. These teams, a major force within the company for quality improvement, resolve administrative, technical and manufacturing problems.

ECR SYSTEM (ERROR CAUSE REMOVAL)

The ECR System permits employees to report to management any impediments to doing the job right the first time. Once such an impediment is reported, management is obliged to respond promptly with a corrective program. Doing it right the first time in all company activities produces lower cost of ownership through defect prevention.

VENDOR CERTIFICATION PROGRAM

Our vendors are taking ownership of their own product quality by establishing improved process control and inspection systems. They subscribe to the zero defects philosophy. Progress has been excellent.

Quality And Reliability

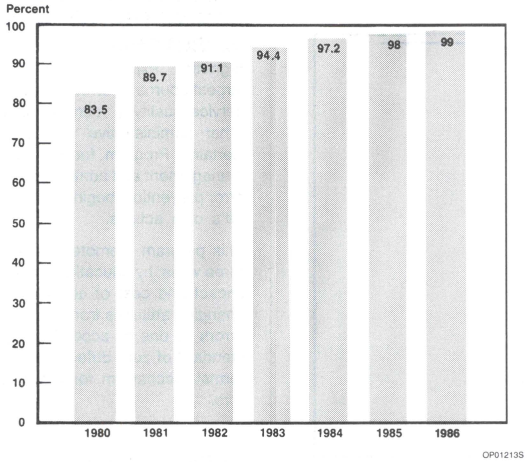


Figure 3. Lot Acceptance Rate From Signetics Vendors

Through intensive work with vendors, we have improved our lot acceptance rate on incoming materials as shown in Figure 3. Simultaneously, waivers of incoming material have been eliminated.

MATERIAL WAIVERS

1986 – 0
1985 – 0
1984 – 0
1983 – 0
1982 – 2
1981 – 134

Higher incoming quality material ensures higher outgoing quality products.

QUALITY AND RELIABILITY ORGANIZATION

Quality and reliability professionals at the divisional level are involved with all aspects of the product, from design through every step in the manufacturing process, and provide product assurance testing of outgoing product. A separate corporate-level group provides direction and common facilities.

Quality and Reliability Functions

- Manufacturing quality control
- Product assurance testing
- Laboratory facilities – failure analysis, chemical, metallurgy, thin film, oxides
- Environmental stress testing
- Quality and reliability engineering
- Customer liaison

COMMUNICATING WITH EACH OTHER

For information on Signetics' quality programs or for any question concerning product quality, the field salesperson in your area will provide you with the quickest access to answers. Or, write on your letter-head directly to the corporate director of quality at the corporate address shown at the back of this manual.

We are dedicated to preventing defects. When product problems do occur, we want to know about them so we can eliminate their causes. Here are some ways we can help each other:

- Provide us with one informed contact within your organization. This will establish continuity and build confidence levels.
- Periodic face-to-face exchanges of data and quality improvement ideas between your engineers and ours can help prevent problems before they occur.
- Test correlation data is very useful. Line-pull information and field failure reports also help us improve product performance.
- Provide us with as much specific data on the problem as soon as possible to speed analysis and enable us to take corrective action.
- An advance sample of the devices in question can start us on the problem resolution before physical return of shipment.

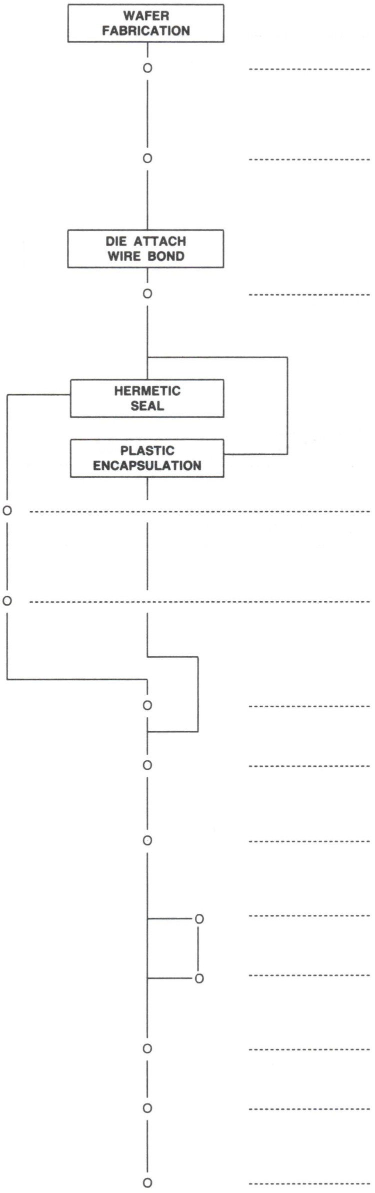
This team work with you will allow us to achieve our mutual goal of improved product quality.

MANUFACTURING: DOING IT RIGHT THE FIRST TIME

In dealing with the standard manufacturing flows, it was recognized that significant improvement would be achieved by "doing every job right the first time", a key concept of the Quality Improvement Program. During the development of the program many profound changes were made. Figure 4, *Logic Products Generic Process Flow*, shows the result. Some of the other changes and additions were to tighten the outgoing QA lot acceptance criteria to the tightest in the industry, with zero defect lot acceptance sampling across all three temperatures.

The achievements resulting from the improved process flow have helped Signetics to be recognized as the leading Quality supplier of Logic products. These achievements have also led to our participation in several Ship-to-Stock programs, which our customers use to eliminate incoming inspection. Such programs reduce the user *cost of ownership* by saving both time and money.

Quality And Reliability



SCANNING ELECTRON MICROSCOPE CONTROL

Wafers are sampled daily by the Quality Control Laboratory from each fabrication area and subjected to SEM analysis. This process control reveals manufacturing defects such as contact and oxide step coverage in the metalization process which may result in early failures.

DIE SORT VISUAL ACCEPTANCE

Product is inspected for defects caused during fabrication, wafer testing, or the mechanical scribe and break operation. Defects such as scratches, smears and glassivated bonding pads are included in the lot acceptance criteria.

PRE-SEAL VISUAL ACCEPTANCE

Product is inspected to detect any damage incurred at the die attach and wire bonding stations. Defects such as scratches, contamination and smeared ball bonds are included in the lot acceptance criteria.

STABILIZATION BAKE PRECONDITIONING

Plastic molded devices are baked to stress wire and die bonds and help eliminate marginal devices. It also ensures an optimum plastic seal to enhance moisture resistance. Hermetic devices are baked to ensure the elimination of any remaining cavity moisture.

TEMPERATURE CYCLING

Using MIL-STD-883 Method 1010.1 Condition C devices are cycled from cold to hot temperatures imposing a very severe stress which weakens loose bonds and package seals without degrading good devices. A loosened bond is later detected during 100% electrical tests.

SEAL TESTS

Hermetic package seal integrity is ensured by 100% gross leak testing.

SYMBOL

Devices are marked with the Signetics Logo, device number, and date code or custom symbol per individual specification requirements.

100% ELECTRICAL TEST

Every device is tested for functional and AC/DC parameters at room temperature with guard bands and product assurance sampling to assure performance to data sheet limits.

BURN-IN (SUPR II LEVEL B OPTION)

Devices are burned-in for 21 hours at 155°C junction temperature.

POST-BURN-IN ELECTRICAL TEST

Test to the same stringent test programs and conditions as those used at the pre-burn-in, but, also includes 100% High Temp Electrical Testing

VISUAL

All products are 100% visually inspected per the requirements specified in Signetics or customer documents.

PRODUCT ASSURANCE TESTING

Each lot is sampled and tested for functional and DC at 0°C and + 70°C, and AC/DC and functional at 25°C to assure device performance to data sheet limits.

FINAL QUALITY ASSURANCE GATE

The final QA inspection step guarantees that the specified mechanical and electrical requirements have been met. Every shipment is sealed with the craftsman's stamp.

NOTE: The items on this flowchart do not all happen in the same sequence for all products.

Figure 4. Logic Products Generic Process Flow

Quality And Reliability

As time goes on, the drive for a product line that has *zero defects* will grow in intensity. These efforts will provide both Signetics and their customers with the ability to achieve the mutual goal of improved product quality.

The Logic Products Quality Assurance department has monitored PPM progress, which can be seen in Figure 5. We are pleased with the progress that has been made, and expect to achieve even more impressive results as the procedures for accomplishing these tasks are fine tuned.

The real measure of any quality improvement program is the result that the customer sees. The meaning of *Quality* is more than just working circuits. It means commitment to *On-Time Delivery* to the *Right Place,* of the *Right Quantity,* of the *Right Product,* at the *Agreed Upon Price.*

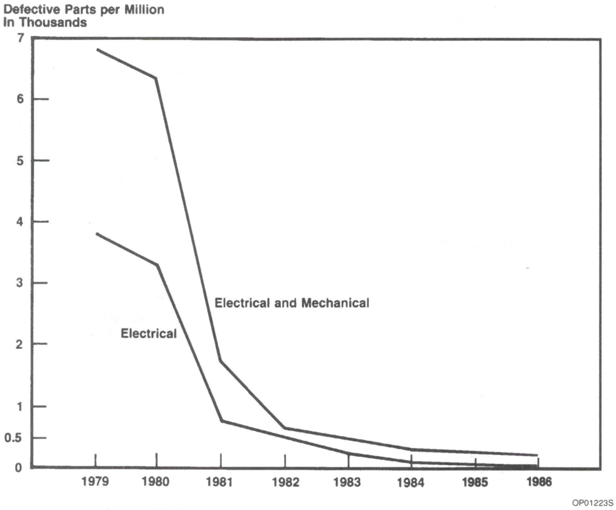


Figure 5. Logic Products EPQ

Section 3
Circuit Characteristics

Signetics

Circuit Characteristics

FAST Products

INPUT STRUCTURES

There are three types of input structures used in FAST circuits: diffusion diode, PNP vertical transistor, and NPN transistor. Each of these are discussed below.

The diffusion diode input is most often used with FAST circuits. The input diode is labeled as D1 in Figure 1. There can be more than one if NAND logic is to be performed. In the oxide-isolated processes these are base-collector diffusions. Each input pin also has a Schottky clamp diode D2. This diode is standard for most TTL circuits, and is included to limit negative input voltage excursions that are generally the result of inductive undershoot.

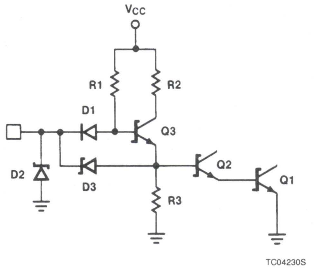


Figure 1. Diode Input

The static diode input function of voltage versus current is shown in Figure 2. If the pin voltage is negative, most of the relatively high negative current flows through the clamp Schottky D2. At 0V the current flows from V_{CC} through R1 and D1 to the pin. Switching from a logic Low level to a logic High level occurs when the input pin voltage rises high enough to force the current from the D1 path to the Q3 – Q2 – Q1 path. This happens when the base voltage of transistor Q3 is at three base-emitter drops ($3V_{BE}$), and the pin is at $2V_{BE}$, which is the standard FAST threshold switching voltage. At this voltage the input current is very small, just the leakage currents of diodes D1, D3, and clamp diode D2. The current remains at this small, positive value until breakdown voltage is reached.

Transistor Q3 and resistor R2 provide a current gain by increasing the amount of current available to Q2 and Q1 when the pin voltage is high. R3 bleeds current off the base of Q2 to pull it low when the pin voltage is low. D3 speeds up this process during the High-to-Low pin transition. When the switching transients are over, D3 is reverse biased.

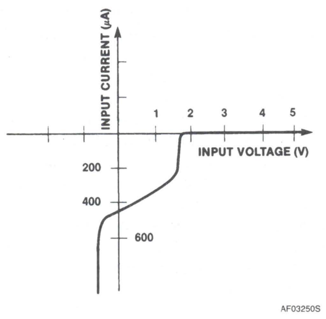


Figure 2. Static Diode Input Function of Voltage VS Current

The current of Figure 2 is scaled for the case where the pin is required to pull down a single 10KΩ resistor R1 (20µA maximum in the High state and 0.6mA maximum in the Low state), which is defined as a standard FAST Unit Load (UL). For some parts, pin current can exceed a UL, especially in the logic Low state. This will happen if the pin must sink the current from more than one R1 resistor, or if the value of R1 is less than 10KΩ, which will be the case if the capacitance at the base of the transistor Q3 is too large for the required switching speed. In this event, the actual number of ULs is listed for each input in the specification sheet for the part. Note: UL, as defined here, is less than the normally defined Schottky TTL Unit Load. The correlation is one Schottky Unit Load = 1.67 ULs. This is an important point to remember for fan-in and fan-out calculations in systems that mix FAST with other TTL families.

The PNP vertical transistor has found wide acceptance in its various forms in low power Schottky logic because it provides a high-impedance input which is usually desirable. It was not used with early FAST circuits because the original oxide-isolated processes did not provide a fully suitable PNP vertical structure. It is now frequently the input of choice for new parts built with improved processes. The PNP transistor Q3 is fabricated with the P-type substrate as the grounded collector, the N-type Epi as the base, and the P-type normal base diffusion as the emitter. The process must be tailored to provide a suitable current gain for this vertical structure and must have provision to remove the considerable substrate current without an appreciable rise in substrate voltage. Referring to Figure 3, Q3 functions as an emitter follower for pin voltages low enough to provide an emitter-base forward bias. This occurs at an emitter voltage below the $3V_{BE}$ value provided by the D3 – Q2 – Q1 stack, and gives the desired $2V_{BE}$ pin threshold. At pin voltages above this value, Q3 turns off and the current through R1 is directed to Q2 – Q1 through D3. The Schottky diode D2 speeds up the High to Low transition if the pin voltage falls more rapidly than the base of Q2; otherwise, D2 is off. The PNP input characteristics are shown in Figure 4. If the input voltage is negative with respect to ground, a large clamp current flows through D_1. As the voltage rises, D_1 turns off and the input current falls to the base current of Q3; for the usual values of R_1, this is in the range of about 10µA. This decreases as the lead voltage rises. At threshold, Q3 turns off and the input current drops to a low value determined by the leakage of D_1, D_2, and Q3. The current remains at this low value until the onset of breakdown. Since all PNP inputs are protected with ESD structures, the breakdown current is set by this, and not the actual PNP device.

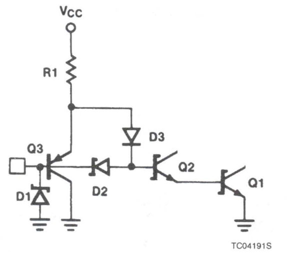


Figure 3. PNP Input

The NPN input is shown with two variations in Figures 5 and 6. It has limited use in standard TTL circuits, and is used in selected FAST devices, especially where its superior high-impedance input characteristics are useful. A typical plot of static input current versus input voltage is shown in Figure 7. There are some significant differences between this function and that of the diffusion diode input shown in Figure 2, the most important being the much lower input current in the region from 0V to threshold and the controlled increase of input current above V_{CC}.

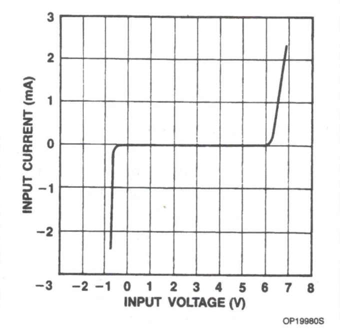


Figure 4. PNP Input Characteristics

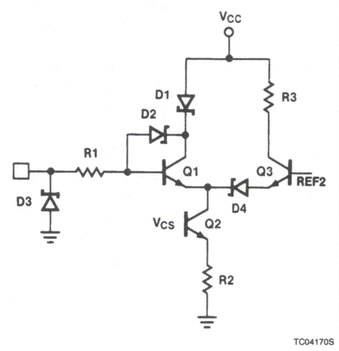


Figure 5. NPN Input

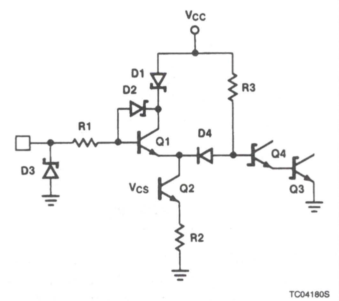


Figure 6. NPN Input

When the pin voltage is negative, the large negative clamp current is supplied through the clamp Schottky diode D3. For positive voltages, from 0V to the switching threshold of $2V_{BE}$, Q1 is off, and the input current I_{IL} is very small, just the leakage current of Q1, D2, and D3 with low reverse bias. As the input voltage rises above $2V_{BE}$, Q1 turns on, and the current that had been flowing through D4 now flows through Q1, blocking Schottky diode D1 to V_{CC}. The value of this current is determined by the current source transistor Q2 with its base connected to voltage reference V_{CS}, and by the size of the emitter resistor R2. The current is nearly constant within the normal operating range of input voltages and has a typical value of 0.1mA to 1.0mA. The pin must supply only a small fraction of this bias current, the ratio of Q1 collector current to base current being the bipolar β factor. Typically, I_{IH} base input current is less than 20μA in the voltage range from 0V to V_{CC}. This value is the specification for a standard FAST NPN Unit Load. As in the diode input case, if larger currents are needed to reduce delay times or to provide for multiple-input transistors connected to the same pin, the specification sheet for the particular device will identify the input pins which have NPN ULs larger than one, and will list their values.

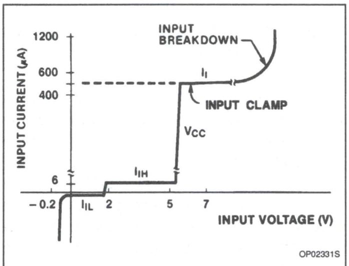


Figure 7. NPN Input Characteristics (Not to Scale)

In normal operation, the pin voltage will be limited in the negative direction by the diode clamp D3, and will be less than V_{CC} in the positive direction. The actual input voltage may exceed V_{CC} for three reasons: there may be inductive overshoot in badly terminated systems; the V_{CC} pin may be floating or grounded; or the input pin may be forced high by electrostatic discharge or incoming inspection testing.

For the inductive overshoot case, when the pin voltage exceeds V_{CC}, part of the Q1 collector current begins to flow from the pin through limiting resistor R1 and Schottky diode D2. The current from V_{CC} through D1 decreases by exactly this amount, since Q2 is a constant current source. As the voltage continues to rise, D1 becomes reverse biased and prevents high currents flowing from the pin into V_{CC}. All the Q2 current flows into the pin through the R1 – D2 – Q1 – Q2 – R2 path to ground. As stated before, this current is typically small, in the range of 0.1mA to 1.0mA, and nearly independent of pin voltage, as shown by the I_I plateau in Figure 7. I_I provides a clamping action to ground for pin voltages in excess of V_{CC}, which is usually desirable to reduce overshoot.

For the case where V_{CC} is grounded or floating, the input current is nearly zero for positive voltages between zero and approximately 7V. The conducting path through R1 – D2 – Q1 is available, but the current source Q2 will be shut off because, without V_{CC} drive, the Q2 base reference V_{CS} will be at 0V. This is the specified standard setup for incoming inspection. For the incoming inspection testing case where V_{CC} is connected to a 5V source, the response is shown in Figure 7. The current remains on the Q2-limited plateau until the pin voltage is high enough to cause non-destructive collector-emitter reach-through of Q2. At this point, input current increases as the pin voltage rises, and R1 functions to limit this current and prevent damage to Q2.

The electrostatic discharge case is similar to the incoming inspection case except that Q2 may be off if the V_{CC} pad is floating, in which case it breaks down at a slightly higher voltage. The NPN input produces reach-through at a relatively low voltage compared with the diode input. The effect of this non-destructive reach-through is to greatly increase the ability of the device to survive electrostatic discharge. The discharge current is passed through the chip at a relatively low power dissipation, and this is shared by elements R1, D2, Q1, Q2 and R2, so that none of them dissipate enough power to do damage. By way of contrast, with a diode input, the clamp Schottky diode breaks down at high voltage with high dissipation in a localized area, and may suffer damage.

Another advantage of the NPN input is its ability to interface on the chip to either a conventional TTL interior design, or to the increasingly popular current-mode interior logic. The conventional TTL interface is shown in Figure 6. In this case the Q2 current source is designed to provide sufficient current to insure that in the Low state, with current flowing through the R3 – D4 – Q2 path, the base-emitter stack of Q3 – Q4 is shut off. The $2V_{BE}$ input threshold is set by the forward drops of Q1, D4, Q4 and Q3.

The current-mode logic interface is shown in Figure 5. The output voltage is the drop across R3, and is referenced to V_{CC} (or some on-chip regulated voltage lower than V_{CC}) as is required for current-mode logic. For this case, voltage reference REF2 is normally fixed at $2V_{BE}$ + 1 Schottky drop to provide a pin threshold voltage of $2V_{BE}$. In fact, REF2 can be tailored to set the switching threshold voltage to any desirable level; it can be set to something other than an integral number of

Circuit Characteristics

base emitter drops, or it can be designed to reduce the sometimes undesirable temperature variations of input threshold.

INPUT CONSIDERATIONS

Static Input Current

A comparison of input current for various input voltage ranges for each of the three types of inputs is shown in Figure 8.

INPUT VOLTAGE RANGE	INPUT CURRENT		
	Diode	PNP	NPN
Below Ground	Schottky Clamp	Schottky Clamp	Schottky Clamp
Ground to V_T	High (to 600μA)	Low (to 20μA)	Leakage
V_T to V_{CC}	Leakage	Leakage	Low (to 20μA)
Above V_{CC}	Leakage	Leakage	Clamp 100 to 1000μA

Figure 8. Input Current for Input Voltage Ranges

The majority of FAST devices available to date have diode inputs and supply current to their drivers that may be as large as 600μA at V_{IN} of 0.5V for a single unit load input. If a driver cannot sink the necessary current for a particular number of loads, the system designer must either add a buffer circuit designed to drive with higher current, or switch to devices that have high-impedance inputs. These are available on many Signetics FAST designs, and are specified to have input current less than 20μA over the full switching range from 0V to V_{CC}. Typical input current for the NPN structure at room temperature is less than 1μA below switching threshold voltage and 3μA above threshold. Typical PNP input current is less than 10μA below threshold voltage and 1μA above threshold.

Input Capacitance

Input capacitance, measured using a small-signal variation about a static DC operating point, is usually the least for the NPN. When one includes the added capacitance of the elements common to each input, such as the pin, pad, bond wire, and clamp Schottky diode, the percentage difference for total static input capacitance for any of the three types of inputs is not very large.

Dynamic Input Current

In many applications the total current an input pin draws during a switching transition is a more important consideration than its input capacitance. This dynamic input current is often larger than the value of static capacitance would predict because each of the three types of input structure normally includes some sort of speed-up mechanism, usually a "kicker" Schottky diode, connected to an internal node of the circuit. The kickers deliver current, related in a non-linear way to input edge-rates. High-dynamic input current does not always equate to fast circuit switching. NPN inputs are usually faster than diode or PNP inputs, but in general have the lowest total dynamic current. The percentage differences for dynamic current tend to be larger than the respective differences for static capacitance.

Switching Threshold Voltage

The FAST input switching threshold voltage is set quite high for TTL at two base-emitter junction forward-bias drops. FAST input structures have enough gain that the voltage range in which they switch from one state to the other, as shown by a static DC transfer function curve, is completed within about 100mV of the $2V_{BE}$ threshold. For a typical part at room temperature, V_{BE} is about 800mV, and the switching threshold is nominally at 1.6V; the static transfer range uncertainty of about 100mV gives a nominal threshold for solid Lows and Highs of about 1.55V and 1.65V respectively. The FAST threshold voltage was chosen higher than other TTL families to give a larger noise margin with respect to ground, and to be more nearly centered in the region where a FAST output driver stage switches with maximum edge rates, which occurs between about 0.6V and 2.6V.

Because the FAST threshold is set by the base-emitter junction voltage, it is dependent on junction temperature and current density. V_{BE} increases by about 1.2mV for each degree C drop in junction temperature; current density changes by about a decade for a 60mV change in V_{BE}. The total variation due to processing differences, temperature, and current density is about 150mV per junction, or 300mV total change in input threshold to give limits of 1.25V Low and 1.95V High. The FAST V_{IL} and V_{IH} limits are 0.8V and 2.0V respectively, a tight spec for V_{IH}.

HYSTERESIS CONSIDERATIONS

Hysteresis has frequently been added to the inputs of TTL circuits in the past. The purpose is to increase noise immunity, which is accomplished by adjusting threshold voltages in a direction to reinforce an input level once a critical value has been reached. The procedure works well for slow circuits where the likelihood of slow, noisy inputs is high. It does not accomplish what is intended for FAST parts. There are several reasons: FAST threshold is already high and well centered so noise problems are automatically minimized. Inductive ground bounce, which is discussed at length later, causes problems with fast edge rates that completely swamp the typical benefits of hysteresis. It thus becomes a further complication in an already complicated picture and is more apt to hurt noise margin than to help it. Because of this, the two major supplies of FAST have eliminated hysteresis from all circuits except those specifically designed as Schmidt triggers; the 'F13, 'F14, and 'F132.

ELECTRO-STATIC DISCHARGE (ESD) CONSIDERATIONS

It is universally true that no bipolar integrated circuit process can provide devices with such high breakdown voltages that they are able to withstand ESD without some structure punching through or breaking down. The necessary condition for survival when this occurs is that the energy dissipation in any volume of the chip must be kept low enough so that neither the silicon nor the interconnecting metal can melt. This can be accomplished in two ways: the breakdown voltage should be as low as practical, consistent with normal circuit operation, and the energy should be dissipated in as large a volume as is possible. Circuit components that are particularly sensitive to charge damage must be protected by structures that are less fragile. All Signetics FAST parts are designed with these requirements in mind, and although, as a rule of thumb, a sophisticated oxide isolated process used to fabricate these parts tends to be more ESD damage-prone than a junction isolated process, FAST is about as rugged as other TTL families in general. If FAST parts are handled with the same care afforded any other high-technology parts, they will not be damaged.

ESD sources usually fit into one of two categories: people or other objects that have accumulated static charge and touch the parts; or, they generate their own charge, as is the case when a circuit makes sliding contact with an insulator. In the first instance, static voltages tend to be high, over 10000V, and discharge is usually limited by relatively high series resistance. In the second case, voltages are lower, around 200V, but there is very little series resistance to limit discharge current. Both possibilities are simulated with discharge models that are used in the majority of the test setups, and parts are designed in a way to improve survival for both ESD conditions.

Circuit Characteristics

Experience has shown that inputs of TTL circuits are much more likely to suffer ESD damage than outputs. Since negative voltages are discharged through clamp ground diodes with low chip dissipation, only voltages positive with respect to substrate ground are apt to produce input damage.

Circuits with diode inputs have a positive voltage breakdown in the relatively high range of from 15V to 25V. Schottky diodes connected to an input pin usually break down before junction diodes, and if they are stressed beyond their limits the Schottky diodes usually sustain damage in the corners. A diffusion guard-ring around the diode increases the uniformity of the breakdown, and as a result maximizes the dissipation volume at breakdown and increases the ability of the device to survive ESD. All Signetics FAST circuits have guard-rings on Schottky diodes that connect to input or output pins.

NPN inputs are designed to have low holdoff voltage for positive voltages in excess of V_{CC}. Under static discharge the input structure forward biases, and the current-source transistor conducts the ESD current to substrate with a relatively low collector-emitter reach-through voltage. The input current for normal operation is low enough that a series limiting resistor can be added; this limits ESD current, especially for the case where the ESD source has no appreciable series resistance itself.

As processes improve, it is often possible to improve ESD protection. Most new releases and many parts that have been recently redesigned onto new processes have specific ESD structures included which protect up to 2000V for the standard resistance limited case — the human body model.

FLOATING INPUTS

FAST inputs should not be allowed to float. All unused inputs, even those on unused gates, should be tied to a voltage source of relatively low impedance that will get them out of the logic picture and out of trouble. For a Low input this can be ground, or the output of a permanently low driver. For a High input this can be V_{CC}, protected by a series resistor if circuit damaging voltage spikes are possible in the system, or a permanently high driver.

Properly tied High or Low inputs will not pick up enough spurious noise to cause problems. If they are allowed to float, the results can be disastrous. Floating diode inputs usually pull to within a few Mv of $3V_{BE}$ above ground, a V_{BE} above threshold. The input voltage will fall about 1V per 0.1mA of current that is capacitively coupled from an adjacent Low-going pin. Since pin-to-pin input capacitance is in the order of one pF for an IC in a PC environment, an adjacent pin falling at 1.0V/ns couples in about 1.0mA of current, enough to switch the input to a Low state for as long as the current lasts. The normal FAST circuit response will be to switch or oscillate. The problem is even worse for high-impedance low-capacitance NPN or PNP inputs. In this case the static voltage to which they float is determined in part by leakage, and is not predictable.

To reiterate, FAST inputs must not be allowed to float. To do so is to invite serious system problems.

OUTPUT CONSIDERATIONS

The purpose of the output stage is to supply current to a load to force it to a High state or to sink current from the load to force it to a Low state. The speed at which the load can be switched from one state to the other depends on how much supply current or sink current is available from the output driver. There must be an amount in excess of that which is required to maintain the static load voltage, and it is the excess current that is available to charge or discharge the load capacitance. Most FAST circuits are designed to fit into one of those categories, based on output drive capability; the normal output stage, the buffer driver which can supply approximately twice as much current, and the high current drivers designed to drive low-impedance terminations.

Both normal drivers and buffers may be 3-State, which means that, in addition to Low and High states, they can be forced to a high-impedance OFF state as a third possible choice. This allows multiple components to be connected to a bus simultaneously, with only the single-selected device providing actual drive capability.

The basic components of an output stage are shown in Figure 9.

The pull-down driver components sink load currents to force a Low state at the output pin; the pull-up driver components supply current to force a High state. The control components turn on the selected driver and turn off the nonselected driver in response to the logic input signal. For 3-State parts, the control components turn off both drivers if the 3-State control signal is active. The output Schottky clamp is included to suppress inductive undershoots, and is a part of every FAST circuit. The load requires a static current to keep it in either a logic High or Low state. The drivers must also charge and discharge the load capacitance C_L, which is generally one of the major factors that influence switching speed.

Since, to a large extent, they function independently of each other, the pull-up driver, pull-down driver, and control blocks are discussed independently.

PULL-UP DRIVERS

Open-Collector

The simplest pull-up driver consists of no more than a fixed pull-up resistor tied to V_{CC}. For this case, the control stage interacts only with the pull-down driver. In the Low state, this must sink the current from both the pull-up resistor and load. In the High state, the pull-up resistor must supply all of the load current. Most often, the pull-up resistor is not physically part of the integrated circuit chip itself, but is added externally. In this case the only circuit element connected to the output pad (in addition to the ever-present Schottky clamp) is the collector of the pull-down driver transistor, hence the name "Open-Collector." Parts with this output stage can be tied together for bus applications. If any of the connected pull-down stages is active, it will pull the bus Low; only if all of them are off can the external resistor pull the bus High. This action provides a "wired" logical function that is free in the sense that no additional components are required to achieve it. Some Open-Collector FAST parts also have 3-State inputs that serve to disable output pull-down stages regardless of the action of the normal logic function.

The Open-Collector output voltage depends on the load, the value of the pull-up resistor, and the voltage to which this is connected. If the resistor value is low, the output will rise to nearly the full value of the pull-up source voltage; in particular, the Open-Collector output can rise to V_{CC}, a voltage higher than that obtainable with a standard Darlington totem-pole pull-up.

High-drive Open-Collector parts are ideal as drivers for terminated transmission lines. In this application the line is terminated at the receiving end with a resistor network that provides the proper impedance and an equivalent source voltage of about 3V. The circuit pull-down drive sinks the termination current through the line at relatively low chip power dissipation when it is on. When it is turned off, the line pulls the output high, charging the stray capacitance from an impedance equal to the line characteristic impedance. Since the current is supplied by the line, the chip power dissipation falls. Very fast rise times approaching 1ns can be obtained with this scheme. Rise times, in general, for open-collector outputs are determined by the RC product of the pull-up resistor and the stray capacitance, and are limited only by the ability of the chip to pull the load low.

Signetics has a new family of parts designed specifically for driving heavy loads in termi-

Circuit Characteristics

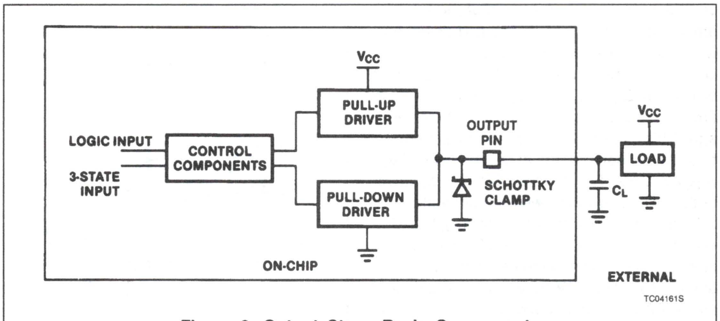


Figure 9. Output Stage Basic Components

nated or unterminated environments. The majority of these are Open-Collector functions. They are discussed in detail later.

Standard Darlington

Most FAST pull-up drivers use dual transistors, connected as shown in Figure 10, with the emitter of the first device Q_b delivering current to the base of the driver Q_a. This configuration is called a Darlington circuit and provides a composite current gain nearly as large as the product of the current gains of Q_b and Q_a.

The major advantage of the Darlington pull-up, as compared to the Open-Collector, is that the pin is actively pulled high by the emitter-follower action of Q_a which is capable of supplying large currents to quickly charge output capacitance. Despite the large output current that is available, the drive requirements of Q_b are low, so that the voltage drop across R_c is small, and the pad will pull up to a voltage nearly as high as $V_{CC} - 2V_{BE}$.

For the case where the output pin voltage is High, the phase-splitter transistor Q_c is off, and the base of Q_b is pulled high by resistor R_c. The current which flows through R_c is just sufficient to provide base drive to Q_b. The base voltage of Q_b will be just slightly below V_{CC}, and the output pin voltage will be less than this by the sum of the V_{BE} drops of Q_b and Q_a, both of which are on. Most of the base current for Q_a and the current through pull-down resistor R_b is supplied from V_{CC} through R_a and Q_b. Q_b has a Schottky clamp to prevent saturation when the current through R_a is large. Resistor R_a limits the amount of current flowing from V_{CC} through Q_a to a value small enough that Q_a will not be damaged if the output pin is accidentally grounded for a short period of time. This short circuit output current is called I_{OS}, and its value is approximately the maximum current available to charge the output capacitance at the beginning of a Low-to-High transition. The minimum current available when the pin has reached the minimum guaranteed high voltage V_{OH} is called output high current (I_{OH}), and is specified to be either 1mA or 3mA, depending on the type of driver. The maximum output voltage that the pull-up driver can achieve occurs at maximum V_{CC}, and at high temperatures with corresponding low values of transistor V_{BE} and high current gain. Conversely, the minimum high voltage occurs at low V_{CC} and low temperatures.

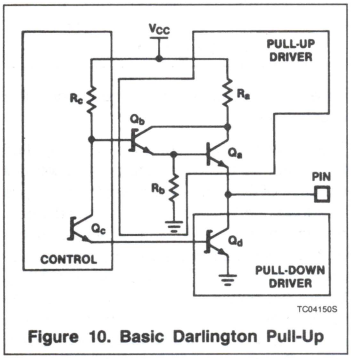


Figure 10. Basic Darlington Pull-Up

In the Low state, the pull-down driver Q_d is on and the pin voltage is the Q_d saturation voltage V_{SAT}. Q_c is on and its collector resistor R_c is pulled down to $V_{BE} + V_{SAT}$; the V_{BE} of Q_d, V_{SAT} of Q_c. Q_b is also on, with its emitter at V_{SAT}, and the current through R_b is low. The base-emitter voltage of Q_a is nearly zero and Q_a is off.

The rate at which the pull-up driver can force a Low-to-High transition depends on a number of factors. The first, and obvious, consideration is that the control components must turn off the pull-down driver very quickly. During the short time that both pull-up and pull-down are on, there is a large feed-through current spike that is wasted as far as switching the load is concerned; it also increases chip power dissipation and produces undesirable voltage spikes in V_{CC} and ground. Assuming the pull-down is off, the Low-to-High transition speed is governed by: 1) the rate at which R_c can pull-up the base of Q_b; 2) the amount of pin current required to drive the load and charge the load capacitance; 3) the value of R_a; 4) the physical size and current gain of Q_a; and 5) the amount of Q_a base drive current that is lost through R_b to ground. The amount of R_b drive current lost can be reduced by connecting R_b to the output pin instead of ground, and this is done in a number of FAST parts. For this case, the static current through R_b with the pin high is less than if R_b is grounded, but switching feed-through current spike for a High-to-Low transition may be increased because R_b cannot effectively pull-down the base of Q_a until after the pin voltage falls.

The pin can be driven above its maximum high value by an external pull-up or by positive reflections from a transmission line. When this happens, Q_a and Q_b do not have sufficient base-emitter drive to keep them on. If the pin voltage rises significantly above V_{CC}, Q_a will begin to leak current into V_{CC}. For the case where R_b is tied to the pin instead of ground, the reverse transistor action of Q_a allows a high pin-to-V_{CC} current. This is not usually a problem in normal operation, but should be avoided in system applications where the V_{CC} pin may be intentionally grounded.

3-State

For all 3-State FAST parts, the leakage paths to a grounded V_{CC} pin are blocked with Schottky diodes. A typical 3-State pull-up is shown in Figure 11. S_a is the series Schottky blocking diode. 3-State Schottkys S_{t1} and S_{t2} serve to simultaneously turn off the pull-up and pull-down drivers. The 3-State control is active when it is pulled low to within V_{SAT} of ground. In this state it sinks all the available drive current for Q_b and Q_c, and pulls their bases down to ($V_{SAT} + V_{Schottky}$), which is essentially one V_{BE}. The voltage drop across R_c is large and 3-State power dissipation is typically high. Q_a and Q_b are off for normal TTL voltage ranges of the output pin; a negative undershoot large enough to drive the pin about one V_{BE} below ground will allow them to turn on and supply current from V_{CC}; this action aids the clamping Schottky diode in preventing the pin voltage from falling lower.

Circuit Characteristics

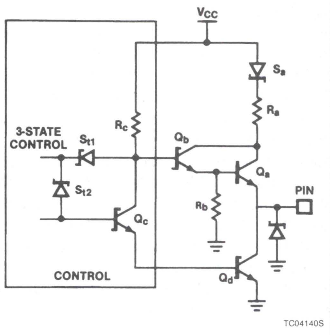


Figure 11. Basic 3-State Pull-Up

PULL-DOWN DRIVERS

The basic FAST pull-down driver is shown in Figure 12. Q_d is the pull-down driver transistor, a big Schottky-clamped device capable of sinking large currents. C_d is the stray base-collector capacitance of Q_d, and its unavoidable presence has an important effect on the performance of the pull-down driver. Q_c is the Schottky-clamped phase splitter. It functions as a current-limited, low-impedance driver for Q_d when the logic input voltage V_{IN} is high, and as an inverting driver for pull-up Q_b by virtue of the current through R_c when V_{IN} is low and Q_C is off. Z_d is the pull-down impedance network which insures that Q_d is off when V_{IN} is low.

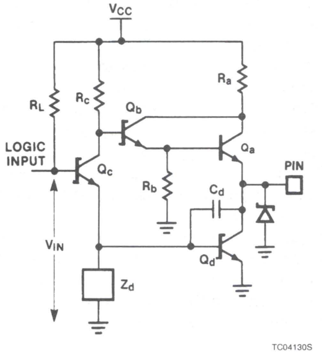


Figure 12. Basic FAST Pull-Down

Switching to the logic Low state occurs when V_{IN} is larger than the V_{BE} drops of Q_c plus Q_d, both of which are initially on. Part of the total emitter current available from Q_c comes from R_c, which has a voltage drop of $V_{CC} - V_{BE} - V_{SAT}$. The remainder of the Q_c emitter current is supplied through its base Schottky clamp or by other components not shown in Figure 12 but discussed in the section on control components. A portion of the total Q_c emitter current is lost in the pull-down network Z_d; the remainder is available as base current for pull-down driver Q_d. The amount of current Q_d can sink depends on its base drive, its current gain, and its collector voltage. This current is specified on a per-part basis in the data sheets at output low voltage (V_{OL}) of 0.5V. The current which Q_d can sink in the switching range with the pin voltage at 2.5V is called available current (I_{AVL}), and is usually at least 70mA for FAST. The manner in which this current varies as the pin voltage decreases from 2.5V to V_{OL} is not specified as a FAST family parameter, since it is critically dependent on circuit design for a particular part, but is included as a specification for selected parts, especially those tailored to drive transmission lines. Several innovative circuit improvements that increase I_{AVL} by increasing the drive current for Q_d are shown in Figures 19a and 19b. Speed-up Schottky diodes S_{s1} and S_{s2} have been added to the standard pull-down circuit as shown in Figure 13a. Both are reverse-biased and off in the High state, since R_c pulls the collector of Q_c nearly to V_{CC}. Both connect the collector of Q_c to nodes that need to be discharged during a High-to-Low transition. S_{s1} to the base of Q_a, S_{s2} to the pin. They will conduct if these node voltages are higher than $V_{BE} + V_{SAT} + V_{Schottky}$, or approximately $2V_{BE}$; they are quite effective above $2V_{BE}$. Other networks are available which function down to lower voltages; these are especially useful for transmission line drivers. Figure 13b shows a dynamic kicker that gives an impulse of current which is especially useful in discharging high capacitive loads.

The network of elements labeled Z_d in Figure 12 is the pull-down impedance which insures that Q_d is off when the value of V_{IN} falls below $2V_{BE}$. When the voltage at the base of Q_d is being pulled high by Q_c or low by Z_d, the output pin voltage responds by moving in the opposite direction. This produces a change in voltage across C_d, which is the sum of the base voltage change and the collector voltage change, so the amount of charge required by C_d is magnified by a factor which is larger than unity.

This well-known Miller-effect causes the apparent value of C_d, as perceived by the drivers, to be a factor of about five times larger than the already large physical junction capacitance, all of which means that the drivers Q_c and Z_d need to supply or sink much more current during an output transition than is necessary to maintain static conditions. When static conditions do exist internally in the circuit, noise voltage spikes on the output pin, V_{CC}, or ground can momentarily force the base of Q_d in the direction to produce a serious output glitch, and the drivers must respond quickly to counter this coupled noise.

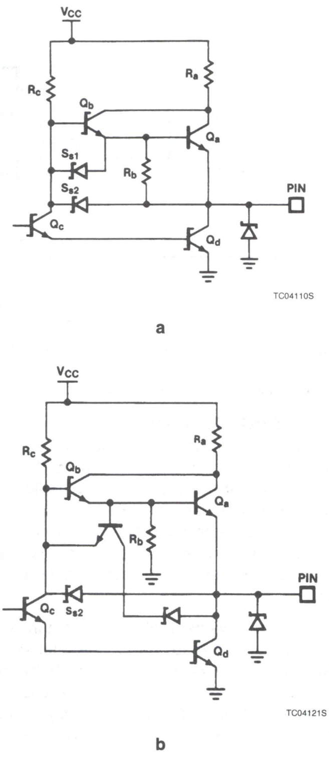


Figure 13

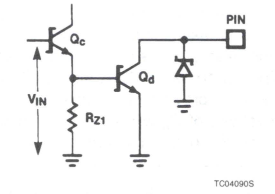


Figure 14

The simplest Z_d element is a resistor R_{Z1} tied to ground, as shown in Figure 14. It will pull the base of Q_d all the way down to 0V if V_{IN} is less than one V_{BE}. This provides good immunity to coupled noise, but slows down the High-to-Low pad transition somewhat because the base of Q_d must rise a full V_{BE} before the output can begin to change. The value of R_{Z1} needs to be relatively large to prevent a serious loss of base drive current when Q_d is on, which makes it easier to

Circuit Characteristics

capacitively couple voltage spikes to the base of Q_d and, in part, nullifies the good noise immunity the full V_{BE} swing provides.

The addition of a series Schottky diode solves most of the problems. This is shown in Figure 15. The Q_d base voltage cannot pull below a Schottky drop, so the switching speed is unimpaired. The value of R_{Z2} can be less than R_{Z1} for the same current when the base is high, so the effect of coupled charge is less and the noise margin is acceptable.

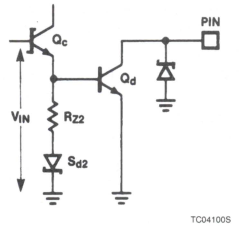


Figure 15

The circuit of Figure 16 is standard with many TTL families. It pulls the base of Q_d down even less than does $R_{Z2} - S_{d2}$, but it has a relatively high dynamic impedance and is somewhat noise sensitive. It has the advantage that it tends to "square up" the input voltage-to-output voltage transfer function, hence its popular name "squaring circuit." It is frequently used in simple gates where the shape of the transfer function may be important. For more complicated circuits, where there are one or more stages of logic with gain between input and output pins, the squaring ability is pretty much lost; in fact, it is likely that high-gain, multiple-logic-level FAST circuits will oscillate if the input voltage is held at near threshold for any length of time.

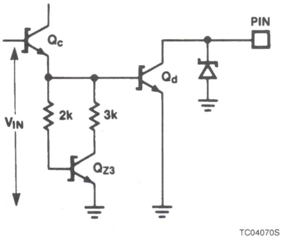


Figure 16

Figure 17 shows a popular dynamic circuit that is used in conjunction with a resistor or squaring circuit pull-down, and which insures that C_d cannot couple enough charge to the base of Q_d to slow down a Low-to-High transition. In operation, as the emitter of Q_b rises, charge is coupled through C_{Z4} into the base of Q_{Z4} which turns on and shunts the Miller current flowing through C_d to ground. When the transition is finished, the current through C_{Z4} stops and Q_{Z4} turns off. When the High-to-Low transition of Q_b occurs, C_{Z4} discharges through S_{d4}. Because Q_{Z4} reduces the problems associated with Miller current, the circuit is called a "Miller Killer."

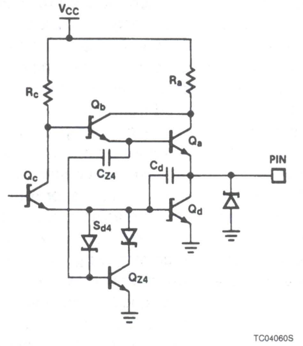


Figure 17

Figure 18 shows an active pull-down for the base of Q_d. The drive for Q_{Z5} (not shown) must be generated from the same signal that drives the base of Q_c. When Q_c is on, Q_{Z5} must be off, and when Q_c is off, Q_{Z5} turns on to hold the base of Q_d low. The impedance is very low, eliminating the capacitive-coupling noise problem.

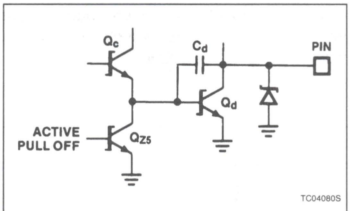


Figure 18

CONTROL COMPONENTS

This section covers 3-State control drivers, special 3-State problems, and V_{CC} turn-on current and 3-State glitches during power-up.

3-State Control Drivers

The normal TTL 3-State scheme is shown in Figure 11. The 3-State control voltage in the OFF state is high enough that S_{t1} and S_{t2} are reverse-biased; in the active state the control voltage is low, usually V_{sat}, so that the $Q_a - Q_b$ base emitter stack is off, as is the $Q_c - Q_d$ stack. In the 3-State mode, R_c is dissipating maximum power. Blocking Schottky diode S_a prevents current from flowing backwards through Q_a if the V_{CC} pin is grounded; the output pin high voltage can be about 4.5V before there is any significant 3-State leakage current. The only exception to this general rule with FAST is for the diode input transceiver function, where the same pin acts as an input or an output. In this case, the pin supplies one or more normal FAST unit loads of current if it is Low, and tends to pull to $2V_{BE}$ if it is floating. NPN and PNP input transceivers have normal low 3-State leakage.

There are several innovative improvements to the basic 3-State circuit, as shown in Figure 19. The addition of inverter $Q_{c2} - R_{c2}$ with a blocking Schottky S_{c2} allows the addition of feedback diodes S_{s1} and S_{s2} to increase I_{AVL}; S_{c2} cannot be included in series with R_{c1} because its forward voltage drop would lower V_{OH}. 3-State power is not increased, since only one R_{c1} is pulled low. The current through Q_{c2} is available as added base drive to Q_d, so nothing is wasted. An additional transistor may be paralleled with Q_{c1} and Q_{c2} to control an active pull-down version of impedance Z_d which, discussed in a previous section, eliminates the Miller turn-on problem of Q_d.

I_{CC} Considerations

There is no formal family specification that limits the amount of V_{CC} current a FAST circuit may draw during turn-on as V_{CC} rises from zero to 4.5V. However, for most new designs, and especially for circuits that have high I_{CC} requirements, an effort has been made to limit maximum turn-on I_{CC} to 110% of I_{CCmax}. This precaution prevents an undesirable system situation where the V_{CC} power supply is large enough to drive the devices, but can't power them up. The major component of turn-on current is V_{CC} to ground feedthrough of output stages. Unless specific steps are taken to prevent it, the pull-up Darlington turns on if V_{CC} is greater than $2V_{BE}$, and remains on until the on-chip voltage is high enough to set the phase splitter solidly in one or the other of its two states. The solution is to incorporate extra circuit components that will set the phase splitter at voltages nearly as low as $2V_{BE}$, or turn off the top device with a separate 3-State type structure which activates at low V_{CC} voltages and becomes inoperative when V_{CC} is high.

The amount of current that can be fed from an output pin back into a grounded V_{CC} pin, or through the chip to ground for an open V_{CC} pin, depends on the design. Generally, 3-State feedback current is specifically limited to low values which are leakage or breakdown related. Other parts have medium to high current. Those with Darlington pull-downs connected to the output pin conduct the most.

Some 3-State parts, especially selected buffer functions, have additional circuit elements to insure that as they power on they source or sink no appreciable output current, provided that the 3-State control pins are in the active state as V_{CC} rises. This means that V_{CC} can be turned on or off at will in the system to conserve power, and bus voltages will not be affected. Parts with this capability are identified in the specific data sheets.

GROUND VOLTAGE AND OTHER NOISE PROBLEMS

Ground Voltage As A Serious Problem

Excessive ground noise voltage in a system usually produces serious degradation of switching speed. It may also produce unwanted glitches on outputs, or spurious clocks which cause flip-flops to lose data, or relaxation oscillations that completely disrupt a system. It is, without doubt, one of the major causes of logic systems failure ... difficult to accommodate, and difficult to eliminate.

The problem is not unique with FAST, but is greatly aggravated by the high transition rates and large currents for which FAST is designed. Because of this, FAST can optimally replace other TTL families only in systems that have been carefully designed at the PC board level. Well planned layout is vital, and multilayer boards with ground and V_{CC} planes are often necessary. Great care must be taken to insure adequate bypassing for V_{CC}. The problems are not trivial, but they can be solved satisfactorily to yield systems whose performance is not exceeded in the TTL world.

Sources Of Ground Noise

Ground lead inductance is the source of most ground noise voltage; it causes a voltage drop proportional to the rate at which the current through it changes.

Inductance is a measure of the amount of energy stored in the magnetic field associated with a current. Low values of inductance imply low energy, which means low voltage required to affect a change in current. As a general rule, inductance decreases as current is allowed to spread out in space, and current interactions decrease. The inductance of a thin wire far removed from the return current path is high; that of a large conductor coaxially encircled by the return path is low. Inductance tends to increase faster than linearly with conductor length, but only approximately logarithmically with decreasing cross-section dimensions. From a logic system viewpoint, ground planes are better than ground traces; wide lines are better than narrow lines; close spacing to planes is good; loops that allow magnetic flux linkages are bad; wire lengths of fractions of inches count; and sockets with long pins add significant inductance to a PC card.

Ground noise voltage is increased by feed-through current spikes. These occur when both top and bottom devices of the output totem-pole driver are on simultaneously, and heavy currents are allowed to flow directly from V_{CC} to ground. They can be minimized in one of two ways: drive the devices such that one is turned off before the other can turn on, or more commonly, drive them together, but very fast, so the feed-through current can flow for only a short time.

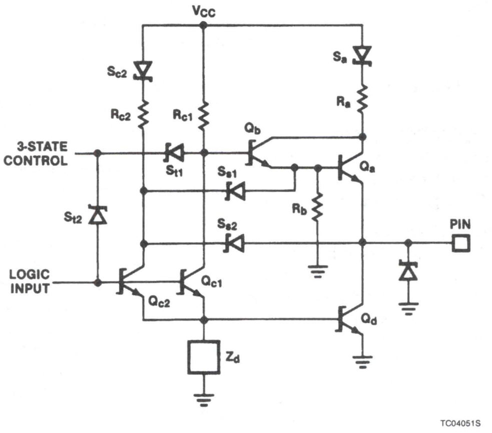


Figure 19. Improved 3-State Circuit

Although most ground noise results from ground inductance, resistance also contributes. Static ground offsets unrelated to rates of current change occur, and add to the total ground voltage. Generally speaking, those measures which reduce ground inductance also reduce ground resistance.

Estimating The Magnitude Of Ground Noise

The accurate modeling of ground noise-related problems in logic design is a complex procedure that requires numerical analysis to determine system currents and voltages as a function of time. This can only be accomplished in a satisfactory manner if one has reasonable electrical models, especially for input stages and output drivers of the integrated circuits used in the system. These data are available on request for many of the FAST logic functions. Signetics is prepared to assist customers in solving the sometimes formidable problems associated with large system simulation.

The following discussion derives the minimum peak-value of ground noise that will occur as an integrated circuit discharges a capacitor through ground lead inductance. It points out the minimum problems that will exist. In the real world, the peak ground voltage will always be larger than the simple derivation predicts.

The load capacitor C and its discharge path are shown in Figure 20. The capacitor has been previously charged to a positive voltage, and is discharging through pull-down transistor Q_d and lead ground inductance L_g. As the current changes, it develops a ground voltage V_g across L_g that is equal to the product of L_g times the rate at which it changes.

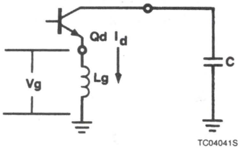


Figure 20

The discharge current I_d will vary with time; starting from zero, it will increase to a maximum value, and then eventually return to zero. There are an infinite number of ways I_d can vary, depending on how the transistor allows charge to flow at any instant in time, but each of the possible current-vs-time discharge curves must define the same area, equal in value to the total charge Q that is removed from the capacitor as its voltage falls by an amount V.

The voltage drop V_g across the inductor at any instant in time will be determined by the

Circuit Characteristics

slope of the current-vs-time curve, that is, by the rate at which current is changing. The unique curve that has the required area and minimum slope is triangular, as shown in Figure 21. The ground voltage for this case is a square wave as shown in Figure 22. It will be positive while the current is increasing, and negative when the current is decreasing.

The equations of interest in estimating V_g are:

$$\text{Charge} = Q = CV = I_{MAX}\frac{T}{2} = \text{triangle area}$$

$$\text{Ground voltage} = V_g = (\text{triangle slope})(L) = \frac{2\ I_{MAX}\ L}{T}$$

Combining the two equations to eliminate I_{MAX} gives:

$$V_g = \frac{4CVL}{T^2}$$

This lower limit of peak ground voltage will always be exceeded in the real world, where ground voltages are usually spikes, not square waves. If a spike is large enough and long enough, the chip will erroneously recognize it as a valid input, and respond either by glitching, slowing down, clocking incorrectly, or oscillating.

An example using values typical for a FAST circuit in a 16-pin DIP illustrates the potential for trouble. If the circuit discharges one standard FAST load of 50pF in 2ns with a voltage change of 3V through a ground inductance of 10nH, the minimum ground voltage will be:

$$V_g = \frac{4 \times 50 \times 10^{-12} \times 3 \times 10 \times 10^{-9}}{(2 \times 10^{-9})^2}$$

$$= 1.5\text{V}$$

This value is high, and suggests that if transition times are not to be seriously degraded, inductances must be kept as small as possible, and loads must be minimized.

Effects Of Ground Noise On Input Stages

FAST TTL input voltages are referenced to system ground as illustrated in Figure 23 which shows an equivalent input and output stage. The equivalent input circuit is represented by R_{IN} and the four diodes D1 through D4. These components establish an input switching threshold voltage of 2 V_{BE} relative to chip ground. The on-chip voltage V_{IN} must be different from this value by a margin large enough to guarantee a static Low or High with sufficient overdrive to insure switching speed. The on-chip voltage V_{IN} that is actually available is the difference between the input pin voltage V_{PIN} and the total ground voltage noise V_g. V_g is the sum of the steady state voltage due to ground current flowing through R_g, and the inductive voltage drop across L_g. The inductive voltage is usually the larger of the two, and since it depends on current changes, it will have both positive and negative polarities for each switching cycle. This means that either Low or High input voltages which are too close to switching threshold will allow the noise margin to be exceeded, and if the ground voltage noise persists long enough, the input will switch erroneously. The result of this depends on the chip function. Combinatorial logic usually slows down or produces output glitches. Latches and flip-flops may be clocked inadvertently, and stored data will be lost. Complex circuits that have multiple outputs may oscillate, particularly if one polarity of ground noise results in a rapid change of ground current that produces the opposite polarity ground noise.

Ground noise adds a dimension of difficulty in measuring input threshold voltage. FAST parts are guaranteed to have input thresholds between the limits 0.8V and 2.0V. A typical method of verifying this is to determine the voltage at which the input actually switches. This requires some care, since the true threshold voltage is masked by any noise voltage contributed by the test system or ground inductance. For accurate results, the input pin voltage should approach the switching threshold slowly and smoothly. At threshold the input will switch. Sensing this point is easy for those circuits where an output also switches, glitches, or oscillates. It is much harder to sense this point for those circuits where an input change produces no output change, for example, with flip-flops which change state only when clocked. The input switch point for these devices can be inferred by measuring the input current as a function of input voltage. Clocking the part may produce enough ground noise to distort the measurement, even if the output doesn't switch.

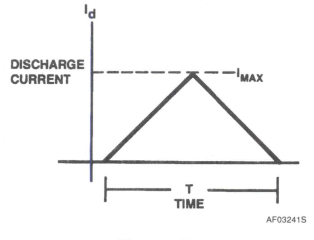


Figure 21

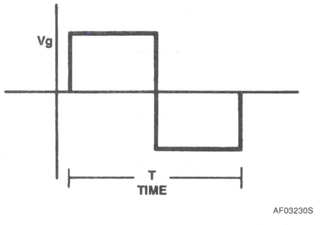


Figure 22

Effects Of Ground Noise On Output Stages

The most obvious effect that ground noise has on output stages is to directly change the voltage available to force discharge current through the pull-down device. If the only source of ground voltage is from the particular output of interest, the ground and output pin inductances will always slow down a High-to-Low transition. They produce a voltage in opposition to the output pin voltage at the

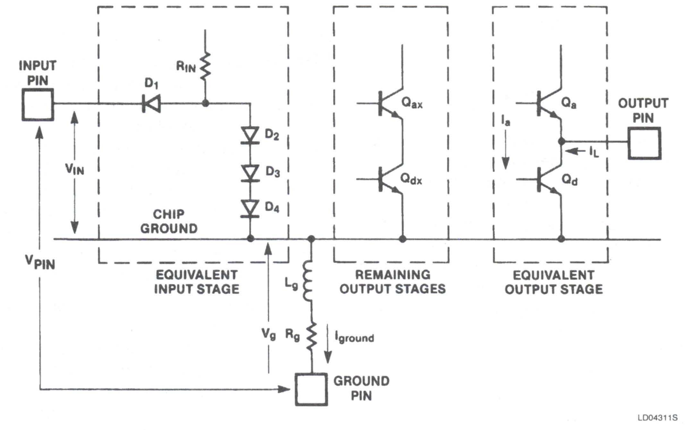


Figure 23. Equivalent Input and Output Stage

Circuit Characteristics

beginning of the discharge when currents tend to be high and voltage changes rapidly. As discharge continues, the available drive decreases, and currents increase less rapidly. Eventually the current begins to fall, and the ground voltage reverses polarity, which tends to limit the rate at which the current decreases. If currents have been high, and the inductances are large, there may be substantial undershoot at the end of the switching cycle which can drive the output pin below ground.

If multiple outputs are switching simultaneously, the total ground noise needs to be considered to determine the result for a particular output. For this case, it can happen that ground noise will, in fact, speed up an output; on the other hand, it may introduce delays that are much larger than those possible with single output switching. This behavior makes it difficult to predict, except on a case by case basis, what the actual effects of multiple output switching will be. Curves of delay vs multiple switching have been published, but these serve only as rough guides to indicate potential problems, and need to be backed up with actual analysis for any particular application.

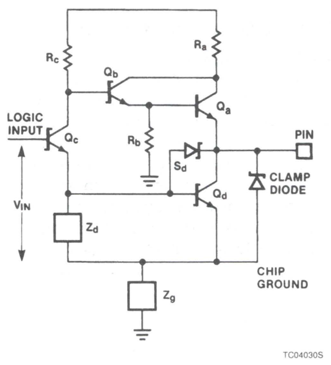


Figure 24

In addition to the direct influence on discharge voltage, excessive ground noise can affect the operation of the control components, and alter both rise and fall times by driving pull-up or pull-down stages incorrectly. One example of this can be understood with reference to Figure 24. The scenario is that the output pin is Low, but on the verge of switching High, with V_{IN} falling and Q_c ready to turn off. A problem occurs if, at the instant before the pull-up transistor Q_a turns on to pull the output pin high, the voltage from output pin to chip ground falls. This can happen as a result of inductive undershoot driving the output pin down, or by a rise in ground voltage caused by currents completely unrelated to the output of interest. The low output-pin-to-chip-ground voltage pulls down the emitter of Q_c through Schottky clamp diode S_d, and if V_{IN} is not low enough to counteract this, Q_c will not turn off. The net result is that R_c cannot rise, and the transition is delayed until the noise voltage from output to ground disappears.

V_{CC} Noise As An Additional Problem

Inductance in the V_{CC} lead produces noise in the on-chip V_{CC} voltage that is entirely analogous to ground voltage. The effects of V_{CC} noise can be nearly as harmful as those produced by ground noise, the only significant difference being the fact that TTL input voltages are referenced to ground instead of V_{CC}.

The first symptom of excessive V_{CC} inductive voltage drop is a change in the edge rate for a Low-to-High transition. This will decrease if the on-chip V_{CC} falls, and increase if it rises. If the ground to V_{CC} voltage falls below a minimum value, internal circuit delays or glitches can occur, and functions with flip-flops or other storage elements may lose data. As is the case with excessive ground noise, FAST circuits may break into relaxation oscillation.

Because V_{CC} to ground voltage must remain above a minimum value to avoid logic errors and glitches, it is absolutely vital that V_{CC} to ground bypassing is adequate. This requires low inductance V_{CC} and ground PC traces, and low inductance bypass capacitors. FAST parts are guaranteed to function properly for low V_{CC} of 4.5V. This means that pin voltages must not fall below this value for any appreciable time: fractions of nanoseconds. V_{CC} system voltage should be close to the maximum guaranteed value for safe system design.

Designing To Reduce The Effects Of Ground Noise

The typical 1.5V minimum value for ground noise, calculated in the preceeding example, points out the possibility of noise-related problems when only one standard 50pF load is being driven by an output stage. Simultaneous switching of more than one such load obviously increases the risk of trouble, and raises the question of how an octal part can work at all. Fortunately, the real world, with careful PC layout, is not usually so grim.

The standard 50pF load is a lot of capacitance, chosen so one can estimate the chip response for a single output switching under conditions that approach worst case. On a modern PC board a wire trace that has 50pF stray capacitance is several feet long and looks like a resistive delay line instead of a lumped capacitor.

Traces on a PC card must be short to behave like lumped capacitance for an output stage. For this case, a major contributor to driver current is the load presented by the input stages of the driven circuits, and the associated stray capacitance. As previously mentioned, the input current for FAST parts is related to edge rates, and is generally larger than the measured static value of input capacitance would predict. Because of this, the useful fan-out of FAST circuits may be more dependent on ground noise of drivers with heavy capacitive loads than on the amount of current available to a static DC load, which is the guaranteed data sheet value.

Most of Signetics' FAST parts are available in surface mount packages, and these have lower ground inductance than the standard DIP parts.

Inductance of output signal pins reduces the rate at which associated ground current can change, and this reduces ground noise voltage without a corresponding reduction of static output voltage. This inductance may be intentionally increased by adding trace length on the PC board; one needs to be careful, and anticipate the increase in output ringing during switching transitions.

In summary, there are many potential problems that one can anticipate in logic systems with fast edge rates. Some of these are dependent on the available components and their respective packages, and the system designer must be certain that the demands made of them are not more than they can handle. A second major consideration is the system layout, especially from the standpoint of ground, V_{CC}, and signal lead inductance. If one is careful with PC design and layout, and chooses components wisely, FAST systems deliver performance second to none in the TTL world.

Heavy Current Drivers

Signetics has a new family of parts defined that are capable of driving currents much larger than those achieved with standard FAST parts.

The parts presently available are:

F3037	Quad 2 – Input NAND
F3038	Quad 2 – Input NAND Open-Collector
F3040	Dual 4 – Input NAND
F30240	Octal Line Driver, Open-Collector
F30244	Octal Line Driver, Open-Collector
F30245	Octal Transceiver, Open-Collector
F30640	Octal Transceiver, Open-Collector

Others are in the planning stage.

Circuit Characteristics

The drivers are husky enough to assure incident wave-switching driving transmission lines with impedance levels as low as 30Ω. They are the best choice available for applications that need the ultimate in speed and drive capability.

All the parts use multiple center ground and V_{CC} pins. Special precautions have been taken to insure minimum feed-through current during switching, and this, coupled with the low V_{CC} and ground inductance, results in minimum V_{CC} and ground noise, and allows maximum edge-rate and speed.

The parts are available on several different packages, including ceramic. Because the power dissipation is application dependent, the user needs to choose a package and an environment carefully to be sure the maximum temperature ratings are not exceeded. These maximum ratings are part of the individual data sheets.

Signetics

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FAST User's Guide

FAST Products

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Data Sheet Specification Guide

FAST Products

INTRODUCTION

Signetics' FAST data sheets have been configured for quick usability.

They are self-contained and should require minimum reference to other sections for amplifying information.

All references to military products have been deleted from this manual, specifically to reflect recent government requirements imposed via Revision C of MIL-STD-883, including the general provisions of Paragraph 1.2. Specifications for military-grade FAST products are included in the Military Products Data Manual available from the nearest Signetics Sales Office or Sales Representative.

TYPICAL PROPAGATION DELAY AND SUPPLY CURRENT

The typical propagation delays listed at the top of the data sheets are the average between t_{PLH} and t_{PHL} for the most significant data path through the part.

In the case of clocked products, this is sometimes the maximum frequency of operation. In any event, this number is under the operating conditions of $V_{CC} = 5.0V$ and $T_A = 25°C$.

The typical I_{CC} current shown in that same specification block is the average current (in the case of gates, this will be the average of the I_{CCH} and I_{CCL} currents) at $V_{CC} = 5.0V$ and $T_A = 25°C$. It represents the total current through the package, not the current through the individual functions.

LOGIC SYMBOLS

There are two types of logic symbols. The conventional one, "Logic Symbol," explicitly shows the internal logic (except for complex logic). The other is "Logic Symbol (IEEE/IEC)" as developed by the IEC and IEEE. The International Electrotechnical Commission (IEC) has developed a very powerful symbolic language than can show the relationship of each input of a digital logic circuit to each output without explicitly showing the internal logic. Internationally, Working Group 2 of IEC Technical Committee TC-3 is preparing a new document (Publication 817-12) that will consolidate the original work started in the mid-1960's and published in 1972 (Publication 117-15), and the amendments and supplements that have followed. Similarly, for the U.S.A., IEEE Committee SCC 11 has revised the publication IEEE Std 91/ANSI Y32.14-1973.

The updated version IEEE Standard Graphic Symbols for Logic Functions ANSI/IEEE Std 91-1984 (Revision of ANSI/IEEE Std 91-1973 [ANSI Y32.14-1973]) can be ordered through:

IEEE Service Center
445 Hoes Lane
Piscataway, New Jersey 08854
Phone (201) 981-0060

ABSOLUTE MAXIMUM RATINGS

The Absolute Maximum Ratings table carries the maximum limits to which the part can be subjected without damaging it. There is no implication that the part will function at these extreme conditions. Thus, specifications such as the most negative voltage that may be applied to the outputs only guarantees that if less than −0.5V is applied to the output pin, after that voltage is removed, the part will still be functional and its useful life will not have been shortened.

Input and output voltage specifications in this table reflect the device breakdown voltages in the positive direction (+7.0V) and the effect of the clamping diodes in the negative direction (−0.5V).

Absolute maximum ratings imply that any transient voltages, currents, and temperatures will not exceed the maximum ratings. Absolute maximum ratings are shown in Table 1.

RECOMMENDED OPERATING CONDITIONS

The Recommended Operating Conditions table has a dual purpose. It sets environmental conditions (operating free-air temperature), and it sets the conditions under which the limits set forth in the DC Electrical Characteristics table and AC Electrical Characteristics table will be met. Another way of looking at this table is to think of it not as a set of limits guaranteed by Signetics, but as the conditions Signetics uses to test the parts and guarantee that they will then meet the limits set forth in the DC and AC Electrical Characteristics tables.

Some care must be used in interpreting the numbers in these tables. Signetics feels strongly that the specifications set forth in a data sheet should reflect as accurately as possible the operation of the part in an actual system. In particular, the input threshold values of V_{IH} and V_{IL} can be tested by the user with parametric test equipment ... if V_{IH} and V_{IL} are applied to the inputs, the outputs will

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		74F	UNIT
V_{CC}	Supply voltage		−0.5 to +7.0	V
V_{IN}	Input voltage		−0.5 to +7.0	V
I_{IN}	Input current		−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		−0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	Standard outputs	40	mA
		3-State outputs	48	mA
		All buffer outputs	128	mA
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature range		−65 to +150	°C

be at the voltages guaranteed by DC Electrical Characteristics table. There is a tendency on the part of some users to use V_{IH} and V_{IL} as conditions applied to the inputs to test the part for functionality in a "truth-table exerciser" mode. This frequently causes problems because of the noise present at the test head of automated test equipment. Parametric tests, such as those used for the output levels under the V_{IH} and V_{IL} conditions are done fairly slowly, on the order of milliseconds, and any noise present at the inputs has settled out before the outputs are measured. But in functionality testing, the outputs are examined much faster, before the noise on the inputs has settled out and the part has assumed its final and correct output state. Thus, V_{IH} and V_{IL} should never be used in testing the functionality of any FAST part type. For these types of tests, input voltages of +4.5V and 0.0V should be used for the High and Low states, respectively.

In no way does this imply that the devices are noise sensitive in the final system. The use of "hard" Highs and Lows during functional testing is done primarily to reduce the effects of the large amounts of noise typically present at the test heads of automated test equipment with cables that may at times reach several feet. The situation in a system on a PC board is less severe than in a noisy production environment. Typical recommended operating conditions are shown in Table 2.

DC ELECTRICAL CHARACTERISTICS

This table reflects the DC limits used by Signetics during their testing operations conducted under the conditions set forth in the Recommended Operating Conditions table. V_{OH}, for example, is guaranteed to be no less than 2.7V when tested with $V_{CC} = +4.75V$, $V_{IH} = 0.8V$ across the temperature range of 0°C to +70°C, and with an output current of $I_{OH} = -1.0mA$. In this table, one sees the heritage of the original junction-isolated Schottky family ... $V_{OL} = 0.5V$ at $I_{OL} = 20mA$. This gives the user a guaranteed worst-case Low-state noise immunity of 0.3V. In the High state the noise immunity is 0.7V worst case. Although at first glance it would seem one-sided to have greater noise immunity in the High state than in the Low, this is a useful state of affairs. Because the impedance of an output in the High state is generally much higher than in the Low state, more noise immunity in the High state is needed. This is because the noise source couples noise onto the output connection of the device. That output tries to pull the noise source down by sinking the energy to ground or to V_{CC}, depending on the state. The ability of the output to do that is determined by its output impedance. The lower half of the output stage is a very low-impedance transistor which can effectively pull the noise source down. Because of the higher impedance of the upper stage of the output, it is not as effective in shunting the noise energy to V_{CC}, so that an extra 0.4V of noise immunity in the High state compensates for the higher impedance. The result is a nice balance of sink-and-drive current capabilities with the optimum amount of noise immunity in both states.

V_{OH} and V_{OL} values may vary depending on whether 5% or 10% V_{CC} swings are specified. The type of output structure, standard: 3-State, or buffer will also affect the value of V_{OH} and V_{OL}. Generally, as the output current and V_{CC} variations increase, the guaranteed minimum V_{OH} decreases and the maximum V_{OL} increases. Signetics specifies and tests V_{OH} and V_{OL} for both 5% and 10% V_{CC} swings.

I_I, the maximum input current at maximum input voltage, is a measure of the input leakage current at a guaranteed minimum input breakdown voltage. The test conditions for I_I vary according to the type of input structure being tested. Diode inputs are tested with $V_{CC} = MAX$ and 7.0V at the input. NPN inputs are tested with $V_{CC} = 0.0V$ and 7.0V at the input. It is necessary to turn V_{CC} off for the NPN input test to measure leakage. Otherwise, the current source is on and the leakage is undetectable. When I_I is being measured on transceiver I/O pins, both V_{CC} and the input voltage are 5.5V. The reduced input voltage is necessary because of the output structure connected to the input structure. Output structures break down sooner than input structures and it is impossible to test the input without testing the output also.

I_{IH} for both Diode and NPN input structures is less than 20μA typically. I_{IL} is less than 20μA for NPN inputs and less than 600μA for Diode inputs. If multiple input structures are tied together in the design, then the input current values also multiply. The fan-out for devices with NPN inputs is 30 times greater than those with Diode inputs. This means the output current sinking ability of the device driving the input to the Low state could be 30 times less when driving NPN devices.

For transceiver I/O pins the outputs are in the High-impedance state when the inputs are tested. Therefore, a maximum of 50μA extra leakage is allowed and combined with the I_{IH} and I_{IL} values. These tests are called

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
V_{OH}	High-level output voltage	Open-Collector			4.5	V
I_{OH}	High-level output current	Standard			−1	mA
		3-State			−3	mA
		Buffers			−15	mA
I_{OL}	Low-level output current	Standard			20	mA
		3-State			24	mA
		Buffers			64	mA
T_A	Operating free-air temperature		0		70	°C

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$I_{IH} + I_{OZH}$ and $I_{IL} + I_{OZL}$ to more accurately describe the true measurement being made.

I_{OZH} is tested with setup conditions that would put the output in the High state if it were not in the 3-State High-impedance condition. I_{OZL} is similar except the setup condition is for the Low state.

I_{OH} is tested only on Open-Collector outputs as a leakage test for the lower output transistor structure. Both V_{CC} and V_{OH} are at the same value so that there is not a current path to or from V_{CC} that would mask the leakage.

Short-circuit output current is a parameter that has appeared on digital data sheets since the inception of integrated circuit logic devices, but the meaning and implications of that specification has totally changed. Originally, I_{OS} was an attempt to reassure the user that if a stray oscilloscope probe accidentally shorted an output to ground, the device would not be damaged. In this manner, an extremely long time was associated with the I_{OS} test. However, thermally-induced malfunctions could occur after several seconds of sustained test.

Over a period of time, I_{OS} became a measure of the ability of an output to charge line capacitance. Assume a device is driving a long line and is in the Low state. When the output is switched High, the rise time of the output waveform is limited by the rate at which the line capacitance can be charged to its new state of V_{OH}. At the instant the output switches, the line capacitance looks like a short to ground. I_{OS} is the current demanded by the capacitive load as the voltage begins to rise and the demand decreases. We now reach the critical point in our discussion. The full value of I_{OS} need only be supplied for a few hundred microseconds at most, even with 1.0μFd of line capacitance tied to the output; a load that is unrealistically high by several orders of magnitude.

The effect of a large I_{OS} surge through the relatively small transistors that make up the upper part of the output stage is not serious — AS LONG AS THAT CURRENT IS LIMITED TO A SHORT DURATION. If the hard short is allowed to remain, the full I_{OS} current will flow through that output state and may cause functional failure or damage to the structure. A test-induced failure may occur if the I_{OS} test time is excessive. As long as the I_{OS} condition is very brief, typically 50ms or less with ATE equipment, the local heating does not reach the point where damage or functional failures might occur. As we have already seen, this is considerably longer than the time of the effective current surge that must be supplied by the device in the case of charging line capacitance. The Signetics data sheet limits for I_{OS} reflect the conditions that the part will see in the system — full I_{OS} spikes for extremely short periods of time. Problems could occur if slow test equipment or test methods ground an output for too long a time, causing functional failure or damage. DC electrical characteristics are shown in Table 3.

AC ELECTRICAL CHARACTERISTICS

The AC Electrical Characteristics table (see Table 4) contains the guaranteed limits when tested under the conditions set forth in the AC Test Circuits and Waveforms section. In some cases, the test conditions are further defined by the AC setup requirements (see Table 5) — this is generally the case with counters and flip-flops where setup and hold times are involved.

All of the AC characteristics are guaranteed with 50pF load capacitance. The reason for choosing 50pF over 15pF as load capacitance is that it allows more leeway in dealing with stray capacitance, and also loads the device during rising or falling output transitions, which more closely resembles the loading to be expected in average applications, thus giving the designer more useful delay figures.

Although the 50pF load capacitance will increase the propagation delay by an average of about 1ns for FAST devices, it will increase several ns for standard Schottky devices.

The load resistor of 500Ω is conveniently specified as both a pull-up and pull-down load resistor.

FAST products are being released in the surface-mounted SO package as a commercial option. Because of the reduced inductance inherent in this package, minimum propagation delays are being derated by 0.2ns. This is reflected by a note at the bottom of Table 4.

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DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER[1]			CONDITIONS[2]	LIMITS[2]			UNITS	V_{CC}[4]
					Min	Typ[3]	Max		
V_{IH}	Input High voltage			Recognized as a High signal over recommended V_{CC} and T_A range	2.0			V	
V_{IL}	Input Low voltage			Recognized as a Low signal over recommended V_{CC} and T_A range			0.8	V	
V_{IK} (V_{CD})	Input clamp diode voltage			$I_{IN} = -18mA$			−1.2	V	MIN
V_{OH}	Output High voltage	Std.[5]	±10%	$I_{OH} = -1mA$	2.5	3.4		V	MIN
			±5%	$I_{OH} = -1mA$	2.7	3.4		V	MIN
		3-State	±10%	$I_{OH} = -3mA$	2.4	3.3		V	MIN
			±5%	$I_{OH} = -3mA$	2.7	3.3		V	MIN
		Buffers	±10%	$I_{OH} = -15mA$	2.0	3.1		V	MIN
			±5%	$I_{OH} = -15mA$	2.0	3.1		V	MIN
V_{OL}	Output Low voltage	Std.[5]	±10%	$I_{OL} = 20mA$		0.35	0.5	V	MIN
			±5%	$I_{OL} = 20mA$		0.35	0.5	V	MIN
		3-State	±10%	$I_{OL} = 24mA$		0.35	0.5	V	MIN
			±5%	$I_{OL} = 24mA$		0.35	0.5	V	MIN
		Buffers	±10%	$I_{OL} = 64mA$		0.35	0.5	V	MIN
			±5%	$I_{OL} = 64mA$		0.40	0.55	V	MIN
I_I	Input High current breakdown test	Diode inputs		$V_{IN} = 7.0V$			100	μA	MAX
		NPN inputs		$V_{IN} = 7.0V$			100	μA	0.0V
		Transceiver I/O pins		$V_{IN} = 5.5V$			1.0	mA	5.5V
I_{IH}	Input High current			$V_{IH} = 2.7V$ (20μA × n High U.L.)			n(20)	μA	MAX
I_{IL}	Input Low current	Diode inputs		$V_{IL} = 0.5V$ (−0.6mA × n Low U.L.)			n(−0.6)	mA	MAX
		NPN inputs		$V_{IL} = 0.5V$ (−20μA × n Low U.L.)			n(−20)	μA	MAX
I_{IH} + I_{OZH}	Input High current (I/O pins)			$V_{IH} = 2.7V$ (20μA × n High U.L.)			n(20) +50	μA	MAX
I_{IL} + I_{OZL}	Input Low current (I/O pins)	Diode inputs		$V_{IL} = 0.5V$ (−0.6mA × n Low U.L.)			n(−0.6)	mA	MAX
		NPN inputs		$V_{IL} = 0.5V$ (−20μA × n Low U.L.)			n(−20) −50	μA	MAX
I_{OZH}	3-State OFF current High			$V_{OUT} = 2.7V$			50	μA	MAX
I_{OZL}	3-State OFF current Low			$V_{OUT} = 0.5V$			−50	μA	MAX
I_{OH}	Open-Collector output leakage			$V_{OH} = 4.5V$			250	μA	MIN
I_{OS}[6]	Output short-circuit current	Std.[5] 3-State		$V_{OUT} = 0V$	−60		−150	mA	MAX
		Buffer driver		$V_{OUT} = 0V$	−100		−225	mA	MAX

NOTES:

1. Unless otherwise noted, conditions and limits apply throughout the temperature range for which the particular device type is rated. The ground pin is the reference level for all applied and resultant voltages.
2. Unless otherwise stated on individual data sheets.
3. Typical characteristics refer to $T_A = +25°C$ and $V_{CC} = +5.0V$.
4. MIN and MAX refer to the values listed in the data sheet table of recommended operating conditions.
5. Standard refers to the totem-pole pull-up circuitry commonly used for the particular family, as distinguished from buffers, line drivers or 3-State outputs.
6. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operation values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} test should be performed last.

Data Sheet Specification Guide

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	74F373, 74F374					UNIT
				$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	'F373	Waveform 3	3.0 2.0	5.3 3.7	7.0 5.0	3.0 2.0	8.0 6.0	ns
t_{PLH} t_{PHL}	Propagation delay E to $\overline{Q}_n$		Waveform 2	5.0 3.0	9.0 4.0	11.5 7.0	5.0 3.0	13.0 8.0	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level		Waveform 6 Waveform 7	2.0 2.0	5.0 5.6	11.0 7.5	2.0 2.0	12.0 8.5	ns
t_{PHZ} t_{PLZ}	Output Disable time High or Low level		Waveform 6 Waveform 7	2.0 2.0	4.5 3.8	6.5 5.0	2.0 2.0	7.5 6.0	ns
f_{MAX}	Maximum clock frequency	'F374	Waveform 1	100			70		MHz
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{Q}_n$		Waveform 1	4.0 4.0	6.5 6.5	8.5 8.5	4.0 4.0	10.0 10.0	ns
t_{PZH} t_{PZL}	Output enable time to High or Low level		Waveform 6 Waveform 7	2.0 2.0	9.0 5.3	11.5 7.5	2.0 2.0	12.5 8.5	ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level		Waveform 6 Waveform 7	2.0 2.0	5.3 4.3	7.0 5.5	2.0 2.0	8.0 6.5	ns

AC SETUP REQUIREMENTS

SYMBOL	PARAMETER		TEST CONDITIONS	74F373, 74F374					UNIT
				$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
				Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time D_n to E	'F373	Waveform 4	2.0 2.0			2.0 2.0		ns
$t_h(H)$ $t_h(L)$	Hold time, D_n to E		Waveform 4	3.0 3.0			3.0 3.0		ns
$t_w(H)$	E pulse width, High or Low		Waveform 2	6.0			6.0		ns
$t_s(H)$ $t_s(L)$	Setup time D_n to CP	'F374	Waveform 5	2.0 2.0			2.0 2.0		ns
$t_h(H)$ $t_h(L)$	Hold time, D_n to CP		Waveform 5	2.0 2.0			2.0 2.0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low		Waveform 1	7.0 6.0			7.0 6.0		ns

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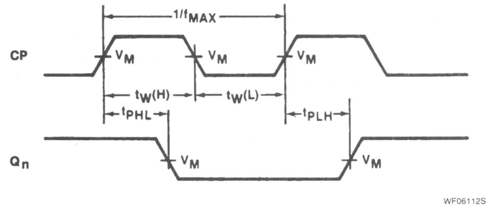
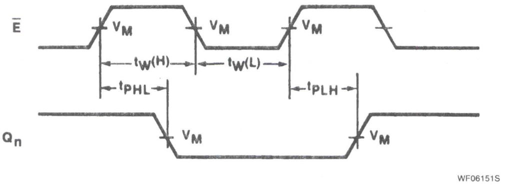
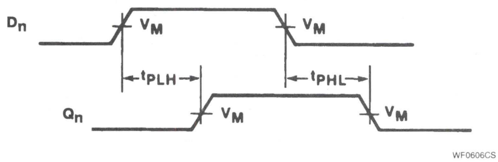
AC WAVEFORMS


CP
Qn
1/fMAX
VM
tW(H)
tW(L)
tPHL
tPLH
WF06112S

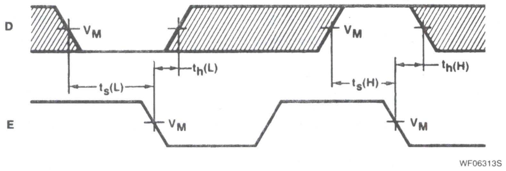
Waveform 1. Clock to Output Delays and Pulse Width


E̅
Qn
VM
tW(H)
tW(L)
tPHL
tPLH
WF06151S

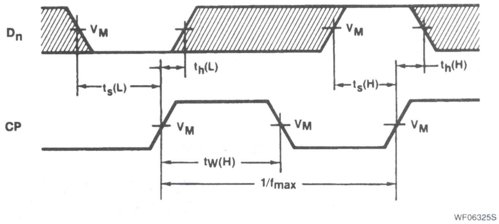
Waveform 2. Latch Enable to Output Delays and Latch Enable Pulse Width


Dn
Qn
VM
tPLH
tPHL
WF0606CS

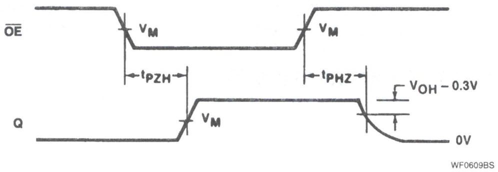
Waveform 3. Propagation Delay Data to Q Outputs


D
E
VM
th(L)
ts(L)
ts(H)
th(H)
WF06313S

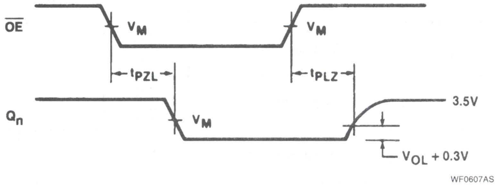
Waveform 4. Data Setup and Hold Times


Dn
CP
VM
th(L)
ts(L)
ts(H)
th(H)
tW(H)
1/fmax
WF06325S

Waveform 5. Data Setup and Hold Times


OE̅
Q
VM
tPZH
tPHZ
VOH − 0.3V
0V
WF0609BS

Waveform 6. 3-State Output Enable Time to High Level and Output Disable Time from High Level


OE̅
Qn
VM
tPZL
tPLZ
3.5V
VOL + 0.3V
WF0607AS

Waveform 7. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

Figure 3. AC Waveforms for FAST 74F373, 74F374

Data Sheet Specification Guide

TEST CIRCUITS AND WAVEFORMS

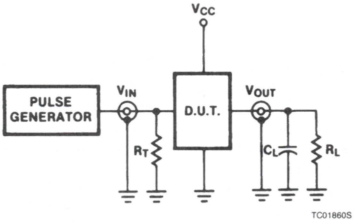
The 500Ω load resistor, R_L to ground, as described in Figure 1, acts as a ballast to slightly load the totem-pole pull-up and limit the quiescent High state voltage to about +3.5V. Otherwise, an output would rise quickly to about +3.5V, but then continue to rise very slowly up to about +4.4V. On the subsequent High-to-Low transition, the observed t_{PHL} would vary slightly with duty cycle, depending on how long the output voltage was allowed to rise before switching to the Low state. Perhaps, more importantly, the 500Ω resistor to ground can be a high-frequency, passive probe for a sampling scope, which costs much less than the equivalent high-impedance probe. Alternatively, the 500Ω load to ground can simply be a 450Ω resistor feeding into a 50Ω coaxial cable leading to a sampling scope input connector, with the internal 50Ω termination of the scope completing the path to ground. Note that with this scheme there should be a matching cable from the device input pin to the other input of the sampling scope; this also serves as a 50Ω termination for the pulse generator that supplies the input signal.

Figure 2, Test Circuit for 3-State Outputs, shows a second 500Ω resistor from the device output to a switch. For most measurements this switch is open; it is closed for measuring a device with Open-Collector outputs and for measuring one set of the Enable/Disable parameters (Low-to-OFF and OFF-to-Low) of a 3-State output. With the switch closed, the pair of 500Ω resistors and the +7.0V supply establish a quiescent High level of +3.5V, which correlates with the High level discussed in the preceding paragraph.

As shown in Figure 3, AC Waveforms for FAST 74F373, 74F374, the disable times are measured at the point where the output voltage has risen or fallen by 0.3V from the quiescent level (i.e., Low for $t_{PLH}{}^2$ or High for $t_{PHL}{}^2$).

Since the rising or falling waveform is RC-controlled, the 0.3V of change is more linear and is less susceptible to external influences.

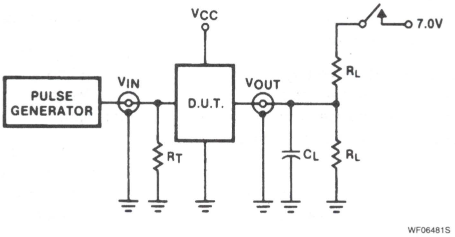
More importantly, from the system designer's point of view, 0.3V is adequate to ensure that a device output has turned OFF. It also gives system designers more realistic delay times to use in calculating minimum cycle times.



DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Figure 1. Test Circuit for Totem-Pole Outputs, 74F00



SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PLZ}	closed
OC	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Figure 2. Test Circuit for 3-State and Open-Collector (OC) Outputs

Good, high-frequency wiring practices should be used in constructing test jigs. Leads on the load capacitor should be as short as possible to minimize ripples on the output waveform transitions and to minimize undershoot. Generous ground metal (preferably a ground plane) should be used for the same reasons. A V_{CC} bypass capacitor should be provided at the test socket, also with minimum lead lengths. Input signals should have rise and fall times of 2.5ns, and signal swing of 0V to +3.0V, 1.0MHz square wave is recommended for most propagation delay tests. The repetition rate must necessarily be increased for testing f_{MAX}. Two pulse generators are usually required for testing such parameters as setup time, hold time, recovery time, etc.

Data Sheet Specification Guide

DC SYMBOLS AND DEFINITIONS

Voltages — All voltages are referenced to ground. Negative-voltage limits are specified as absolute values (i.e., $-10V$ is greater than $-1.0V$).

V_{CC}	**Supply voltage:** The range of power supply voltage over which the device is guaranteed to operate within the specified limits.
V_{IKMax}	**Input clamp diode voltage:** The most negative voltage at an input when the specified current is forced out of that input terminal. This parameter guarantees the integrity of the input diode intended to clamp negative ringing at the input terminal.
V_{IH}	**Input High voltage:** The range of input voltages recognized by the device as a logic High.
V_{IHMin}	**Minimum input High voltage:** This value is the guaranteed input High threshold for the device. The minimum allowed input High in a logic system.
V_{IL}	**Input Low voltage:** The range of input voltages recognized by the device as a logic Low.
V_{ILMax}	**Maximum input Low voltage:** This value is the guaranteed input Low threshold for the device. The maximum allowed input Low in a logic system.
V_M	**Measurement voltage:** The reference voltage level on AC waveforms for determining AC performance. Usually specified as 1.5V for the FAST family.
V_{OHMin}	**Output High voltage:** The minimum guaranteed High voltage at an output terminal for the specified output current I_{OH} and at the minimum V_{CC} value.
V_{OLMax}	**Output Low voltage:** The maximum guaranteed Low voltage at an output terminal sinking the specified load current I_{OL}.
V_{T+}	**Positive-going threshold voltage:** The input voltage of a variable threshold device which causes operation according to specification as the input transition rises from below V_{T-} (Min).
V_{T-}	**Negative-going threshold voltage:** The input voltage of a variable threshold device which causes operation according to specification as the input transition falls from above V_{T+} (Max).

Currents — Positive current is defined as conventional current flow into a device. Negative current is defined as conventional current flow out of a device. All current limits are specified as absolute values.

I_{CC}	**Supply current:** The current flowing into the V_{CC} supply terminal of the circuit with specified input conditions and open outputs. Input conditions are chosen to guarantee worst-case operation unless specified.
I_I	**Input leakage current:** The current flowing into an input when the maximum allowed voltage is applied to the input. This parameter guarantees the minimum breakdown voltage for the input.
I_{IH}	**Input High current:** The current flowing into an input when a specified High-level voltage is applied to that input.
I_{IL}	**Input Low current:** The current flowing out of an input when a specified Low-level voltage is applied to that input.
I_O	**Output current:** The output current that is approximately one half of the true short-circuit output current (I_{OS}).
I_{OH}	**Output High current:** The leakage current flowing into a turned off Open-Collector output with a specified High output voltage applied. For devices with a pull-up circuit, the I_{OH} is the current flowing out of an output which is in the High state.
I_{OH1}	**Output High current:** The current necessary to guarantee the Low to High transition in a 30Ω transmission line on the incident wave.
I_{OL}	**Output Low current:** The current flowing into an output which is the Low state.
I_{OL1}	**Output Low current:** The current necessary to guarantee the High to Low transition in a 30Ω transmission line on the incident wave.
I_{OS}	**Output short-circuit current:** The current flowing out of an output which is in the High state when that output is short circuit to ground.
I_{OZH}	**Output off current High:** The current flowing into a disabled 3-State output with a specified High output voltage applied.
I_{OZL}	**Output off current Low:** The current flowing out of a disabled 3-State output with a specified Low output voltage applied.

AC SYMBOLS AND DEFINITIONS

f_{MAX}	**Maximum clock frequency:** The maximum input frequency at a Clock input for predictable performance. Above this frequency the device may cease to function.
t_{PLH}	**Propagation delay time:** The time between the specified reference points on the input and output waveforms with the output changing from the defined Low level to the defined High level.
t_{PHL}	**Propagation delay time:** The time between the specified reference points on the input and output waveforms with the output changing from the defined High level to the defined Low level.
t_{PHZ}	**Output disable time from High level of a 3-State output:** The delay time between the specified reference points on the input and output voltage waveforms with the 3-State output changing from the High level to a high-impedance "OFF" state.
t_{PLZ}	**Output disable time from Low level of a 3-State output:** The delay time between the specified reference points on the input and output voltage waveforms with the 3-State output changing from the Low level to a high-impedance "OFF" state.
t_{PZH}	**Output enable time to a High level of a 3-State output:** The delay time between the specified reference points on the input and output voltage waveforms with the 3-State output changing from a high-impedance "OFF" state to High level.
t_{PZL}	**Output enable time to a Low level of a 3-State output:** The delay time between the specified reference points on the input and output voltage waveforms with the 3-State output changing from a high-impedance "OFF" state to Low level.

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t_h	**Hold time:** The interval immediately following the active transition of the timing pulse (usually the Clock pulse) or following the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure its continued recognition. A negative hold time indicates that the correct logic level may be released prior to the active transition of the timing pulse and still be recognized.
t_s	**Setup time:** The interval immediately preceding the active transition of the timing pulse (usually the Clock pulse) or preceding the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure its recognition. A negative setup time indicates that the correct logic level may be initiated sometime after the active transition of the timing pulse and still be recognized.
t_W	**Pulse width:** The time between the specified reference points on the leading and trailing edges of a pulse.
t_{REC}	**Recovery time:** The time between the reference point on the trailing edge of an asynchronous input control pulse and the reference point on the activating edge of a synchronous (Clock) pulse input such that the device will respond to the synchronous input.
t_{TLH}	**Transition time, Low-to-High:** The time between two specified reference points on a waveform, normally 10% and 90% points, that is changing from Low to High.
t_{THL}	**Transition time, High-to-Low:** The time between two specified reference points on a waveform, normally 90% and 10% points, that is changing from High to Low.
t_r, t_f	**Clock input rise and fall times:** 10% to 90% value.

Design Considerations

FAST Products

INTRODUCTION

The properties of high-speed FAST logic circuits dictate that care be taken in the design and layout of a system.

Some general design considerations are included in this section. This is not intended to be a thorough guideline for designing FAST systems, but a reference for some of the constraints and techniques to be considered when designing a high-speed system.

HANDLING PRECAUTIONS

As described in the Circuit Characteristics section, FAST devices are susceptible to damage from electrostatic discharge (ESD).

- Signetics FAST devices are shipped in conducting foam or anti-static tubes and foil-lined boxes to minimize ESD during shipment and unloading.
- Before opening the shipment of FAST devices, make sure that the individual is grounded and all handling means (such as tools, fixtures, and benches) are grounded.
- After removal from the shipping material, the leads of the FAST devices should always be grounded. In other words, FAST devices should be placed leads-down on a grounded surface, since ungrounded leads will attract static charge.
- Do not insert or remove devices in sockets with power applied. Ensure that power supply transients, such as occur during power turn on-off, do not exceed absolute maximum ratings.
- After assembly on PC boards, ensure that ESD is minimized during handling, storage or maintenance.
- FAST inputs should never be left floating on a PC board. This precaution applies to any TTL family. As a temporary measure, a resistor with a resistance greater than 10kΩ should be soldered on the open input. The resistor will limit accidental damage if the PC board is removed and brought into contact with static-generating materials.

INPUT CLAMPING

FAST circuits are provided with clamp diodes on the device inputs to minimize negative ringing effects. These diodes should not be used to clamp negative DC voltages or long-duration, negative pulses. Certain FAST part types with the NPN base input structure also provide clamping of positive overshoots.

UNUSED INPUTS

Proper digital design rules dictate that all unused inputs on TTL devices be tied either High or Low. This is especially important with FAST logic.

Electrically-open inputs can degrade AC noise immunity as well as the switching speed of the device. Small geometries make FAST more susceptible to damage by electrostatic discharge than other TTL families. Tying inputs to V_{CC} or GND, directly or through a resistor, protects the device from in-circuit electrostatic damage. Additionally, while most unconnected TTL inputs float High, FAST devices with NPN inputs float Low.

FAST devices do not require an input resistor to tie the input High. Inputs can be connected directly to V_{CC} as well as ground.

Possible ways of handling unused inputs are:

1. Unused active-High NAND or AND inputs to V_{CC}. The inputs should be maintained at a voltage greater than 2.7V, but should not exceed the absolute maximum rating.
2. Connect unused active-High NOR or OR inputs to ground.
3. Tie unused active-High NAND or AND inputs to a used input of the same gate, provided that the High-level fanout of the driving circuit is not impaired.
4. Connect the unused active-High NAND or AND inputs to the output of an unused gate that is forced High.

MIXING FAST WITH OTHER TTL FAMILIES

Mixing the slower TTL families such as 74 and 74LS with the higher speed families such as 74F is possible but must be done with caution. Each family of TTL devices has unique input and output characteristics optimized to achieve the desired speed or power features.

The unique speed/power characteristics of the FAST devices are achieved partially by the internal fast rise and fall times, as well as those at input and output nodes. These fast transitions can cause noise of various types in a system. Power and ground line noise are generated by the faster transitions of the current in the output load capacitance. Signal line noise can also be generated by the fast output transitions.

The noise generated by 74F devices can be minimized in systems designed with shorter signal lines, good ground planes, well-by-passed power distribution networks, layouts that minimize adjacent signal lines that run parallel, and improved impedance matching in signal lines to reduce transmission line-type reflections.

INPUT LOADING AND OUTPUT DRIVE COMPARISON

The logic levels of all TTL products are fully compatible with each other. However, the input loading and output drive characteristics of each family are different and must be taken into consideration when mixing them in a system. Table 1 shows the relative drive capabilities of each family for commercial temperature and voltage ranges.

INPUT-OUTPUT LOADING AND FAN-OUT TABLE

For convenience in system design, the input-output loading and fan-out characteristics of each circuit are specified in terms of unit loads and actual load value. One FAST Unit Load (U.L.) in the High state is defined as 20μA; thus both the input High leakage current, I_{IH}, and output High current-sourcing capability, I_{OH}, are normalized to 20μA.

Similarly, one FAST Unit Load (U.L.) in the Low state is defined as 0.6mA and both the input Low current, I_{IL}, and input Low current/TL, and the output Low current-sinking capability, I_{OL}, are normalized to 0.6mA.

For added convenience, the actual load value in amperes is listed in the column adjacent to U.L.

On some FAST devices, high-impedance NPN base input structure has been utilized.

With this structure, the Low level input current, I_{IL}, has been reduced to 20μA. This characteristic is 30 times lower than the requirement of devices using the conventional input structure. This feature improves fan-out in the Low state and can help reduce part count in system design by eliminating buffers in some applications.

Table 1. Loading Comparisons

DRIVEN DEVICE FAMILY		74F	74F (NPN)	74LS	74	74S	8200/9300	82S00
Driving Device Family	**I_{OL} (Min)**	**I_{IL} (Max)**						
		0.6mA	**20μA**	**0.4mA**	**1.6mA**	**2.0mA**	**1.6mA**	**0.4mA**
		Maximum Number of Loads Driven						
74F	20mA	33	1,000	50	12.5	10	12	50
74F (NPN)	64mA	106	3,200	160	40	32	40	160
74LS	8mA	13	400	20	5	4	5	20
74LS Buffer	24mA	40	1,200	60	15	12	15	60
74	16mA	26	800	40	10	8	10	40
74 Buffer	40mA	78	2,400	120	30	24	30	120
74S	20mA	33	1,000	50	12.5	10	12	50
74S Buffer	60mA	100	3,000	150	37.5	30	37	150
8200/9300	16mA	26	800	40	10	8	10	40
82S00	20mA	33	1,000	50	12	10	12	50

CLOCK PULSE REQUIREMENTS

All FAST Clock inputs are buffered to increase their tolerance of slow positive-clock edges and heavy ground noise. Nevertheless, the rise time on positive-edge-triggered devices should be less than the nominal clock-to-output delay time measured between 0.8V to 2.0V levels of the clock driver for added safety margin against heavy ground noise. Not only a fast rising, clean Clock pulse is required, but the path between the clock drive and clock input of the device should be well-shielded from electromagnetic noise.

FAST OUTPUTS TIED TOGETHER

The only FAST outputs that are designed to be tied together are Open-Collector and 3-State outputs. Standard FAST outputs should not be tied together unless their logic levels will always be the same; either all High or all Low. When connecting Open-Collector or 3-State outputs together, some general guidelines must be observed.

Open-Collector Outputs

These devices must be used whenever two or more OR-tied outputs will be at opposite logic levels at the same time. These devices must have a pull-up resistor (or resistors) added between the OR-tie connector and V_{CC} to establish an active-High level. Only special high-voltage buffers can be tied to a higher voltage than V_{CC}. The minimum and maximum size of the pull-up resistor is determined as follows:

$$R\ (\text{Min}) = \frac{V_{CC}\ (\text{Max}) - V_{OL}}{I_{OL} - N_2\ (I_{IL})}$$

$$R\ (\text{Max}) = \frac{V_{CC}\ (\text{Min}) - V_{OH}}{N_1\ (I_{OH}) + N_2\ (I_{IH})}$$

where: I_{OL} = Minimum I_{OL} guarantee or OR-tied elements.

$N_2\ (I_{IL})$ = Cumulative maximum input Low current for all inputs tied to OR-tie connection.

$N_1\ (I_{OH})$ = Cumulative maximum output High leakage current for all outputs tied to OR-tie connection.

$N_2\ (I_{IH})$ = Cumulative maximum input High leakage current for all inputs tied to OR-tie connection.

If a resistor divider network is used to provide the High level, the R (Max) must be decreased enough to provide the required [(V_{OH}/R (pull-down)] current.

3-State Outputs

3-State outputs are designed to be tied together, but are not designed to be active simultaneously. In order to minimize noise and protect the outputs from excessive power dissipation, only one 3-State output should be active at any time. This generally requires that the output enable signals be non-overlapping. When TTL decoders are used to enable 3-State outputs, the decoder should be disabled while the address is being changed. Since all TTL decoder outputs are subject to decoding spikes, non-overlapping signals cannot normally guarantee when the address is changing.

Since most 3-State output enable signals are active-Low, shift registers or edge-triggered storage registers provide good output enable buffers. Shift registers with one circulating Low bit, such as the 'F164 or 'F194, are ideal for sequential enable signals. The 'F174 or 'F273 can be used to buffer enable signals from TTL decoders or microcode (ROM) devices. Since the outputs of these registers will change from Low-to-High faster than from High-to-Low, the selection of one device at a time is assured.

GND

Good system design starts with a well thought out ground layout. Try to use ground plane if possible. This will save headaches later on. If ground strip is used, try to reduce ground path in order to minimize ground inductance. This prevents crosstalk problems. Quite often, jumper wire is used for connecting to ground at the breadboarding stage, but a solid ground must be used even at the breadboarding stage.

V_{CC}

Typical dynamic impedance of un-bypassed V_{CC} runs from 50Ω to 100Ω, depending on V_{CC} and GND configuration. This is why a sudden current demand, due to an IC output switching, can cause momentary reduction in V_{CC} unless a bypass (decoupling) capacitor is located near V_{CC}.

Not only is there a sudden current demand due to output switching transient, there is also a heavy current demand by the buffer driver. Assuming the buffer output sees a 50Ω dynamic load and the buffer Low-to-High transition is 2.5V, the current demand is 50mA per buffer. If it is an octal buffer, the current demand could be 0.4mA per package in 3ns time!

The next step is to figure out the capacitance requirement for each bypass capacitor. Using the previously-mentioned octal buffer and assuming the V_{CC} droop is 0.1V, then C is:

$$C = \frac{0.4A \times 3 \times 10^{-9}\ \text{sec}}{0.1V} = 12 \times 10F^{-9}$$

$$= 0.012\mu F$$

This formula is derived as follows:
cQ = CV

by differentiation:

$$\frac{\Delta Q}{\Delta t} = C\frac{\Delta V}{\Delta t}$$

Since $\frac{\Delta Q}{\Delta t} = I$

the equation becomes $I = C\frac{\Delta t}{\Delta t}$

hence, $C = \frac{I\Delta t}{\Delta V}$

Select the C bypass ⩾0.02μF and try to use a high-quality RF capacitor. Place one bypass capacitor for each buffer and one bypass capacitor every two other types of IC packages. Make sure that the leads are cut as short as possible.

In addition, place bypass capacitors on a board to take care of board-level current transients.

CROSS-TALK

The best way to handle cross-talk is to prevent it from occurring in the first place; quick-fixes are troublesome and costly. To prevent cross-talk, maximize spacing between signal lines and minimize spacing between signal lines and ground lines. Preferably, place ground lines between signal lines. For added precaution, add a ground trace alongside either the potential cross-talker or the cross-listener.

For backplane or wire-wrap, use twisted pair for sensitive functions such as clocks, asynchronous set or reset, or asynchronous parallel load. In flat cable, make every other conductor ground.

For multilayer P.C. boards, run signal lines in adjacent planes perpendicular to prevent magnetic coupling, and limit capacitive coupling. Use power shield (V_{CC} or ground plane) in between signal planes.

Since any voltage change, noise or otherwise, arriving at the unterminated end of transmission lines double in amplitude, even a partially terminated line reduces the amplitude of the signal (noise or otherwise) appearing at the end of the line; therefore, using a terminating resistor whose value is equal to the line characteristics impedance will help reduce cross-talk.

Section 5
Military Information

5

Military Information

FAST Products

Effective January 1, 1985, this section has been superseded by the 1985 Military Products Data Manual. Information regarding this manual can be obtained from the Military Division in Sacramento. (916) 925-6700.

MILITARY STANDARD PRODUCTS

The Signetics Military product line offering includes JAN Qualified Class S and B, and Class B vendor standard products. These products are designed to offer our customers the optimum of quality, reliability, delivery and cost. The benefits of these products provide our customers:

- Industry-wide standardization.
- Fewer custom specifications.
- Cost savings associated with larger lots.
- Better lead times by reducing specification negotiation time and allowing off-the-shelf procurement.
- Industry standard marking.

JAN QUALIFIED PRODUCT

JAN Qualified products are offered to give our customers the highest quality and reliability. The JAN processing levels (Class S and B) are a result of the Governments product standardization programs, and our JAN production lines are certified by the qualifying activity, the Defense Electronics Supply Center (DESC). Signetics strongly recommends the use of JAN products, which are listed on the MIL-M-38510 Qualified Products List (QPL).

JAN qualified products are fabricated, assembled, tested, and inspected in U.S. Government certified facilities in Sunnyvale, California (wafer fab); Orem, Utah (wafer fab, assembly); and in Sacramento, California (burn-in, test, quality conformance inspection).

Testing and inspection to MIL-M-38510 is monitored by resident Government Source Inspection (GSI) personnel representing the Defense Contract Administration Services (DCAS).

DESC prohibits any customer imposed additions, deviations, omissions, or waivers on procurement of JAN products. Products must conform completely to Government specifications prior to shipment and are verified by Signetics Quality Control. A Certificate of Conformance and Procurement Traceability is supplied with each lot shipped.

JAN Qualified products are listed in QPL-38510, issued periodically by DESC. For current QPL information, customers may contact their local sales representative, Military Marketing in Sacramento, or directly with DESC-EQM at (513) 296-6355. The JAN products listed herein should be considered valid only on its date of publication.

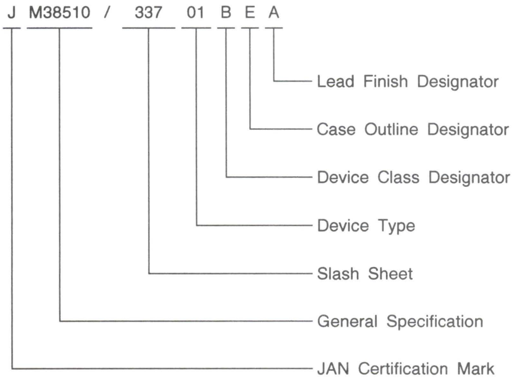
These categories of product conform to Quality Levels A and B of MIL-HDBK-217 ($\pi_Q = 0.5$ Class S, 1.0 for Class B).

The example at the bottom of this page illustrates the part numbering system for JAN products, the part number is per MIL-M-38510.

SIGNETICS CLASS B STANDARD PRODUCT (RB)

Signetics Class B Standard product is offered for use when no JAN product is qualified on the QPL, DESC Drawing product is not available, or when program requirements allow the use of vendor standard product.

Class B standard product conforms to MIL-STD-883, general provisions Paragraph 1.2.1 (and its sub-paragraphs), except where noted. (See Product Noncompliance Section of Military Data Book and/or Hand Book). No other claims, expressed or implied, are made of equivalence to JAN product or to MIL-M-38510. Signetics compliant product also conforms with JEDEC Publication 101, except for marking content.



Electrical test requirements are as stated in the most current **Signetics Military Data Manual only.**

- 100% final electrical tests include all Data Manual parameter limits, test conditions, and temperatures applicable to Subgroups 1, 2, 3, 7, and 9 of MIL-STD-883, Method 5004 for digital products, or to Subgroups 1, 2, 3, 4, and 9 for Linear Products.
- Group A sample electrical inspection tests include all final electrical subgroups as well as all other Data Manual parameters with specified minimum or maximum limits.
- End point electrical tests used for QCI inspection sampling (Groups C and D) are those Data Manual parameter limits, test conditions, and temperatures applicable to Group A Subgroups 1, 2, and 3 per MIL-STD-883, Method 5005, or to Subgroup 1 for Linear Products.

Data Manual parameters which have no specified minimum or maximum limits (typical performance only) are not tested. Parameters which have limits specified at 25°C only, are tested only at that temperature. Detailed parameter assignment to subgroups and other test detail are contained in documented Signetics internal Product Electrical specifications, and are available upon request. Actual test program symbolics are available for customer review at the factory, but are considered proprietary and will not be copied or otherwise distributed outside of Signetics.

QCI Groups A and B testing are performed on all products and packages per MIL-M-38510

Military Information

and MIL-STD-883, Method 5005. Signetics utilizes inline Group A and alternate Group B for all lines. QCI Groups C and D are routinely performed on all compliant families and package types.

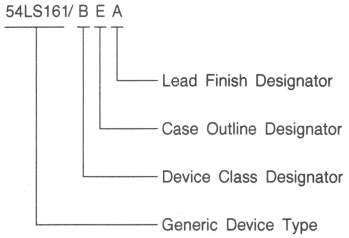
Waivers, deviations, or exceptions of any kind deemed necessary in the course of the contracts must be issued in accordance with DOD-STD-480. Should Signetics have knowledge of the need for waivers at the time of response to quote (RFQ) or order entry, that information will be transmitted prior to order entry.

Package types which do not have case outlines letters assigned in MIL-M-38510, Appendix C, will be assigned case outline letters per JEDEC Publication 101.

The Signetics standard Product Assurance Plan documentation is available for customer review at the factory, and is considered proprietary.

This category of product conforms to quality level B-2 of MIL-HDBK-217 ($\pi_Q = 6.5$).

For Class B Standard Product, the part number is listed as follows:



Signetics

FAST Products

Section 6

74 Series Data Sheets

Signetics

FAST 74F00
Gate

Quad Two-Input NAND Gate
Product Specification

FAST Products

FUNCTION TABLE

INPUT		OUTPUT
A	B	$\overline{Y}$
L	L	H
L	H	H
H	L	H
H	H	L

H = High voltage level
L = Low voltage level

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F00	3.4ns	4.4mA

ORDERING INFORMATION

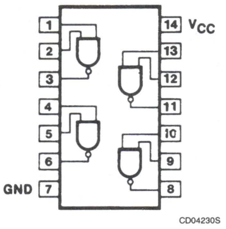
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ± 10%; T_A = 0°C to +70°C
14-Pin Plastic DIP	N74F00N
14-Pin Plastic SO	N74F00D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

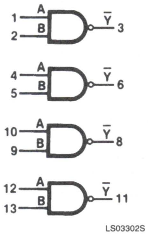
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A, B	Inputs	1.0/1.0	20μA/0.6mA
$\overline{Y}$	Output	50/33	1.0mA/20mA

NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

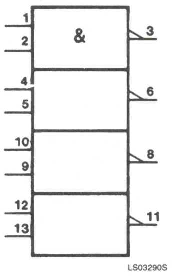
PIN CONFIGURATION


1
2
3
4
5
6
GND 7
14 VCC
13
12
11
10
9
8
CD04230S

LOGIC SYMBOL


1 A
2 B
Y 3
4 A
5 B
Y 6
10 A
9 B
Y 8
12 A
13 B
Y 11
LS03302S

LOGIC SYMBOL (IEEE/IEC)


1
2
&
3
4
5
6
10
9
8
12
13
11
LS03290S

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS Min	LIMITS Nom	LIMITS Max	UNIT
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS Min	LIMITS Typ[2]	LIMITS Max	UNIT
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX V_{IH} = MIN,	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OL} = MAX V_{IH} = MIN,	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		-60		−150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_{IN} = GND		1.9	2.8	mA
		I_{CCL}		V_{IN} = 4.5V		6.8	10.2	mA

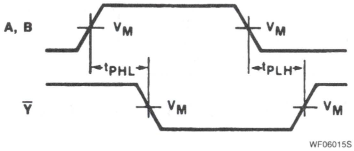
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A, B to $\overline{Y}$	Waveform 1	2.4 2.0	3.7 3.2	5.0 4.3	2.4 2.0	6.0 5.3	ns

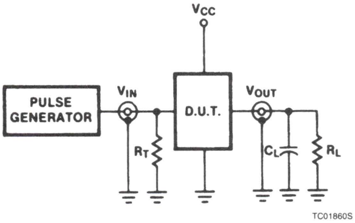
AC WAVEFORM


A, B
V_M
V_M
t_{PHL}
t_{PLH}
$\overline{Y}$
V_M
V_M
WF06015S

NOTE: For all waveforms, $V_M = 1.5V$.

Waveform 1. For Inverting Outputs

TEST CIRCUIT AND WAVEFORM


V_{CC}
PULSE GENERATOR
V_{IN}
D.U.T.
V_{OUT}
R_T
C_L
R_L
TC01860S

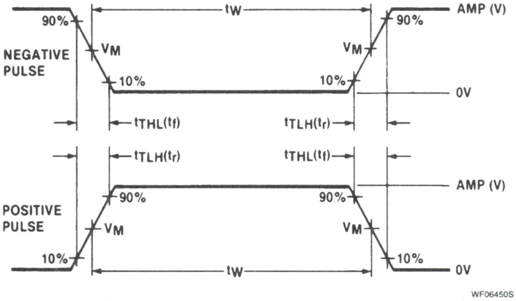
Test Circuit for Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.


tw
90%
90%
AMP (V)
NEGATIVE PULSE
VM
VM
10%
10%
0V
tTHL(tf)
tTLH(tr)
tTLH(tr)
tTHL(tf)
AMP (V)
90%
90%
POSITIVE PULSE
VM
VM
10%
10%
0V
tw
WF06450S

$V_M = 1.5V$

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F02
Gate

Quad Two-Input NOR Gate
Product Specification

FAST Products

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F02	3.4ns	4.4mA

FUNCTION TABLE

INPUTS		OUTPUT
A	B	$\overline{Y}$
L	L	H
L	H	L
H	L	L
H	H	L

H = High voltage level
L = Low voltage level

ORDERING INFORMATION

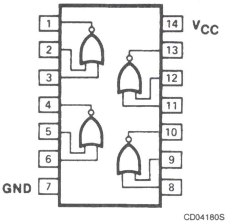
PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
14-Pin Plastic DIP	N74F02N
14-Pin Plastic SO	N74F02D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A, B	Inputs	1.0/1.0	20μA/0.6mA
$\overline{Y}$	Output	50/33	1.0mA/20mA

NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



1
2
3
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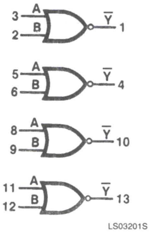
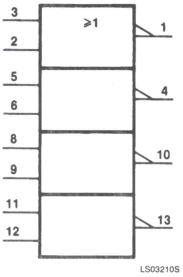
5
6
GND 7
14 V_{CC}
13
12
11
10
9
8
CD04180S

LOGIC SYMBOL



3 A
2 B
$\overline{Y}$ 1
5 A
6 B
$\overline{Y}$ 4
8 A
9 B
$\overline{Y}$ 10
11 A
12 B
$\overline{Y}$ 13
LS03201S

LOGIC SYMBOL (IEEE/IEC)



≥1
3
2
1
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6
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8
9
10
11
12
13
LS03210S

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX V_{IH} = MIN,	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OL} = MAX V_{IH} = MIN,	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				−0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current[4] (total)	I_{CCH}	V_{CC} = MAX			3.0	5.6	mA
		I_{CCL}				7.0	13	mA

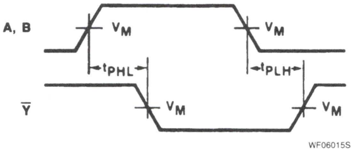
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. I_{CC} is measured with outputs open.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F02					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A, B to $\overline{Y}$	Waveform 1	2.5 2.0	4.4 3.2	5.5 4.3	2.5 2.0	6.5 5.3	ns

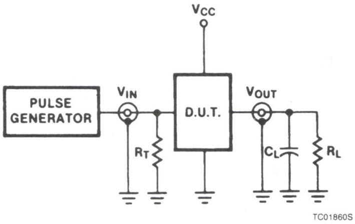
AC WAVEFORM


A, B
V_M
V_M
t_{PHL}
t_{PLH}
$\overline{Y}$
V_M
V_M
WF06015S

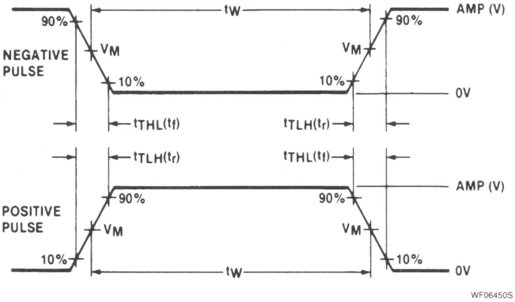
NOTE: For all waveforms, $V_M = 1.5V$.

Waveform 1. For Inverting Outputs

TEST CIRCUIT AND WAVEFORM


V_{CC}
PULSE GENERATOR
V_{IN}
D.U.T.
V_{OUT}
R_T
C_L
R_L
TC01860S

Test Circuit for Totem-Pole Outputs


NEGATIVE PULSE
POSITIVE PULSE
90%
10%
V_M
t_W
AMP (V)
0V
$t_{THL}(t_f)$
$t_{TLH}(t_r)$
WF06450S

$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS
R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F04
Inverter

Hex Inverter
Product Specification

FAST Products

FUNCTION TABLE

INPUT	OUTPUT
A	**$\overline{Y}$**
L H	H L

H = High voltage level
L = Low voltage level

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F04	3.5ns	6.9mA

ORDERING INFORMATION

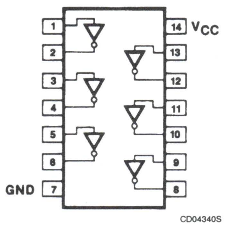
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ± 10%; T_A = 0°C to +70°C
14-Pin Plastic DIP	N74F04N
14-Pin Plastic SO	N74F04D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

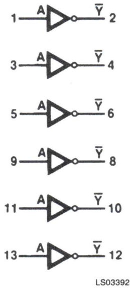
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A	Input	1.0/1.0	20μA/0.6mA
$\overline{Y}$	Output	50/33	1.0mA/20mA

NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

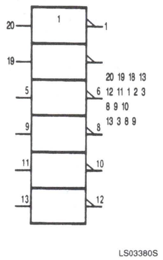
PIN CONFIGURATION


1
2
3
4
5
6
GND 7
14 V_{CC}
13
12
11
10
9
8
CD04340S

LOGIC SYMBOL


1 A $\overline{Y}$ 2
3 A $\overline{Y}$ 4
5 A $\overline{Y}$ 6
9 A $\overline{Y}$ 8
11 A $\overline{Y}$ 10
13 A $\overline{Y}$ 12
LS03392S

LOGIC SYMBOL (IEEE/IEC)


1
20
19
5
9
11
13
1
6
8
10
12
20 19 18 13
12 11 1 2 3
8 9 10
13 3 8 9
LS03380S

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX V_{IH} = MIN,	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OL} = MAX V_{IH} = MIN,	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				−0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_{IN} = GND		2.8	4.2	mA
		I_{CCL}		V_{IN} = 4.5V		10.2	15.3	mA

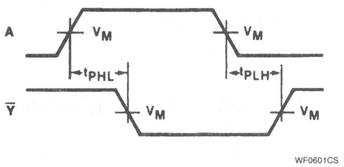
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F04					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH}	Propagation delay A, B to $\overline{Y}$	Waveform 1	2.4	3.7	5.0	2.4	6.0	ns
t_{PHL}			1.5	3.2	4.3	1.5	5.3	

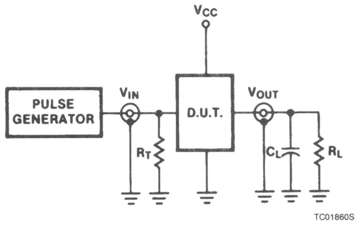
AC WAVEFORM


A
V_M
V_M
t_{PHL}
t_{PLH}
$\overline{Y}$
V_M
V_M
WF0601CS

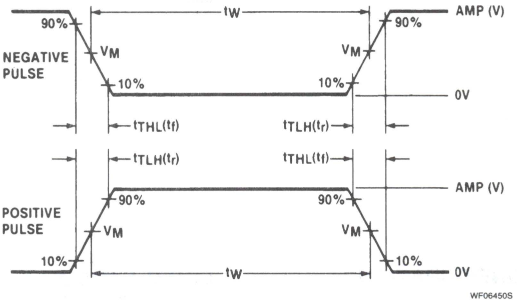
NOTE: For all waveforms, $V_M = 1.5V$.

Waveform 1. For Inverting Outputs

TEST CIRCUIT AND WAVEFORM


V_{CC}
PULSE GENERATOR
V_{IN}
D.U.T.
V_{OUT}
R_T
C_L
R_L
TC01860S

Test Circuit for Totem-Pole Outputs


NEGATIVE PULSE
90%
V_M
10%
t_W
90%
V_M
10%
AMP (V)
0V
$t_{THL}(t_f)$
$t_{TLH}(t_r)$
$t_{TLH}(t_r)$
$t_{THL}(t_f)$
POSITIVE PULSE
90%
V_M
10%
90%
V_M
10%
t_W
AMP (V)
0V
WF06450S

V_M=1.5V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F08
Gate

Quad Two-Input AND Gate
Product Specification

FAST Products

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F08	4.1ns	7.1mA

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

H = High voltage level
L = Low voltage level

ORDERING INFORMATION

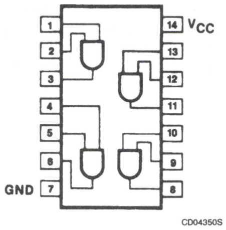
PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
14-Pin Plastic DIP	N74F08N
14-Pin Plastic SO	N74F08D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

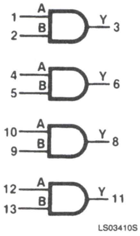
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A, B	Inputs	1.0/1.0	20μA/0.6mA
Y	Output	50/33	1.0mA/20mA

NOTE:
1. One (1.0) FAST Unit Load (U.L.) is defined as: 20μA in the High state and 0.6mA in the Low state.

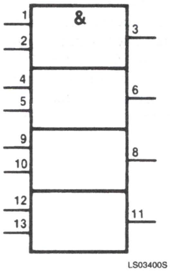
PIN CONFIGURATION


1
2
3
4
5
6
GND 7
14 VCC
13
12
11
10
9
8
CD04350S

LOGIC SYMBOL


1 A
2 B
Y 3
4 A
5 B
Y 6
10 A
9 B
Y 8
12 A
13 B
Y 11
LS03410S

LOGIC SYMBOL (IEEE/IEC)


&
1
2
3
4
5
6
9
10
8
12
13
11
LS03400S

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX V_{IH} = MIN,	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OL} = MAX V_{IH} = MIN,	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				−0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_{IN} = GND		5.5	8.3	mA
		I_{CCL}		V_{IN} = 4.5V		8.6	12.9	mA

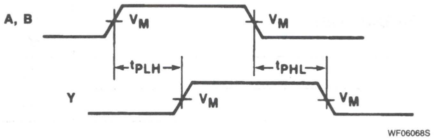
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F08 $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		UNIT
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A, B to Y	Waveform 1	3.0 2.5	4.2 4.0	5.6 5.3	3.0 2.5	6.6 6.3	ns

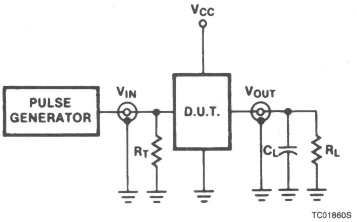
AC WAVEFORM


A, B
V_M
V_M
t_PLH
t_PHL
Y
V_M
V_M
WF06068S

NOTE: For all waveforms, $V_M = 1.5V$.

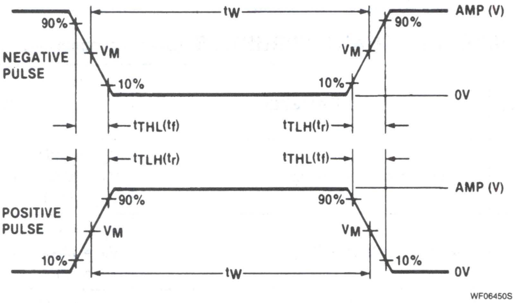
Waveform 1. For Non-Inverting Outputs

TEST CIRCUIT AND WAVEFORM


V_CC
PULSE GENERATOR
V_IN
D.U.T.
V_OUT
R_T
C_L
R_L
TC01860S

Test Circuit for Totem-Pole Outputs

DEFINITIONS
R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.


NEGATIVE PULSE
90%
V_M
10%
t_W
AMP (V)
0V
t_THL(t_f)
t_TLH(t_r)
POSITIVE PULSE
AMP (V)
0V
WF06450S

$V_M = 1.5V$

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST Products

FAST 74F10, 74F11
Gates

Triple Three-Input NAND ('F10), AND ('F11) Gates
Product Specification

FUNCTION TABLE

INPUTS			OUTPUTS	
A	B	C	$\overline{Y}$('F10)	Y('F11)
L	L	L	H	L
L	L	H	H	L
L	H	L	H	L
L	H	H	H	L
H	L	L	H	L
H	L	H	H	L
H	H	L	H	L
H	H	H	L	H

H = High voltage level
L = Low voltage level

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F10	3.5ns	3.3mA
74F11	4.2ns	5.3mA

ORDERING INFORMATION

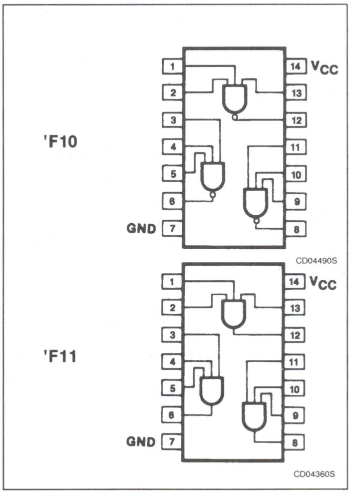
PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
14-Pin Plastic DIP	N74F10N, N74F11N
14-Pin Plastic SO	N74F10D, N74F11D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

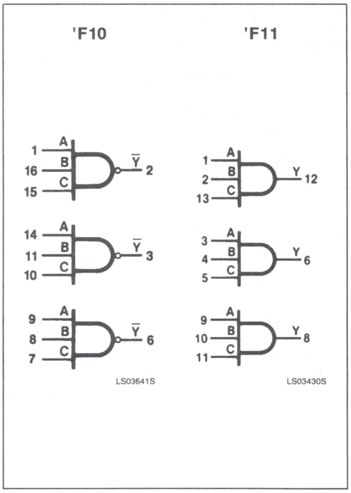
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A – C	Inputs	1.0/1.0	20μA/0.6mA
Y, $\overline{Y}$	Outputs	50/33	1.0mA/20mA

NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

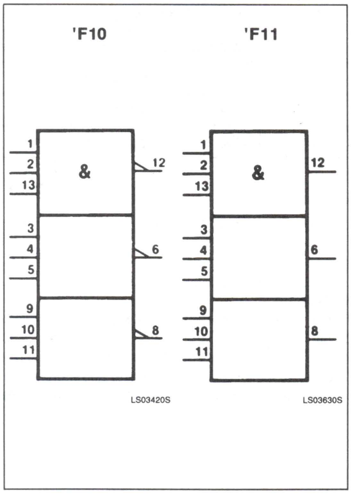
PIN CONFIGURATION


'F10
1
2
3
4
5
6
GND 7
14 VCC
13
12
11
10
9
8
CD04490S
'F11
1
2
3
4
5
6
GND 7
14 VCC
13
12
11
10
9
8
CD04360S

LOGIC SYMBOL


'F10
'F11
1 A
16 B
15 C
$\overline{Y}$ 2
14 A
11 B
10 C
$\overline{Y}$ 3
9 A
8 B
7 C
$\overline{Y}$ 6
LS03641S
1 A
2 B
13 C
Y 12
3 A
4 B
5 C
Y 6
9 A
10 B
11 C
Y 8
LS03430S

LOGIC SYMBOL (IEEE/IEC)


'F10
'F11
&
1
2
13
12
3
4
5
6
9
10
11
8
LS03420S
&
1
2
13
12
3
4
5
6
9
10
11
8
LS03630S

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]		74F10, 11			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage			V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX V_{IH} = MIN,	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage			V_{CC} = MIN, V_{IL} = MAX, I_{OL} = MAX V_{IH} = MIN,	±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, $I_I = I_{IK}$			−0.73	−1.2	V
I_I	Input current at maximum input voltage			V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	High-level input current			V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current			V_{CC} = MAX, V_I = 0.5V				−0.6	mA
I_{OS}	Short-circuit output current[3]			V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current (total)	'F10	I_{CCH}	V_{CC} = MAX	V_{IN} = GND		1.8	2.1	mA
			I_{CCL}		V_{IN} = 4.5V		6.0	7.7	mA
		'F11	I_{CCH}		V_{IN} = 4.5V		4.7	6.2	mA
			I_{CCL}		V_{IN} = GND		7.2	9.7	mA

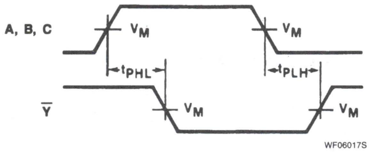
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

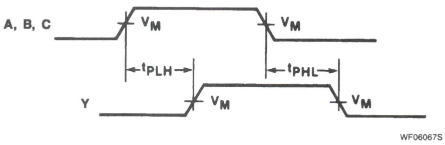
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F10, 11					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A, B, C to $\overline{Y}$	Waveform 1 'F10	2.4 1.5	3.7 3.2	5.0 4.3	2.4 1.5	6.0 5.3	ns
t_{PLH} t_{PHL}	Propagation delay A, B, C to Y	Waveform 2 'F11	3.0 2.5	4.2 4.1	5.6 5.5	3.0 2.5	6.6 6.5	ns

AC WAVEFORMS


A, B, C
VM
VM
tPHL
tPLH
Y
VM
VM
WF06017S

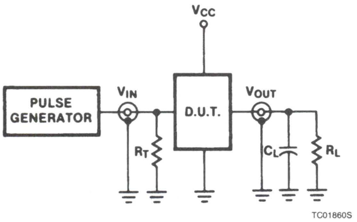
'F10
Waveform 1. For Inverting Outputs


A, B, C
VM
VM
tPLH
tPHL
Y
VM
VM
WF06067S

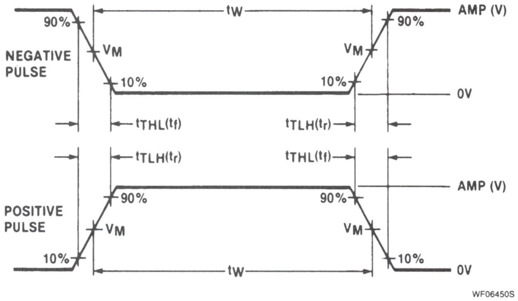
'F11
Waveform 2. For Non-Inverting Outputs

NOTE: For all waveforms, V_M=1.5V.

TEST CIRCUIT AND WAVEFORM


VCC
PULSE GENERATOR
VIN
D.U.T.
VOUT
RT
CL
RL
TC01860S

Test Circuit for Totem-Pole Outputs


90%
tW
90%
AMP (V)
NEGATIVE PULSE
VM
VM
10%
10%
0V
tTHL(tf)
tTLH(tr)
tTLH(tr)
tTHL(tf)
AMP (V)
90%
90%
POSITIVE PULSE
VM
VM
10%
tW
10%
0V
WF06450S

V_M = 1.5V
Input Pulse Definition

DEFINITIONS
R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F13
Schmitt Trigger

Dual 4-Input NAND Schmitt Trigger
Product Specification

FAST Products

DESCRIPTION

The F13 contains two 4-input NAND gates which accept standard TTL input signals and provide standard TTL output levels. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. In addition, they have greater noise margin than conventional NAND gates.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F13	7.8ns	5.5mA

FUNCTION TABLE

INPUTS				OUTPUT
A	B	C	D	$\overline{Y}$
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

H = High voltage level
L = Low voltage level
X = Don't care

ORDERING INFORMATION

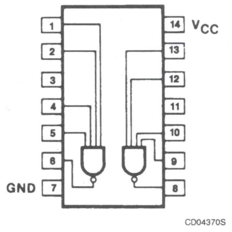
PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%; T_A = 0°C$ to $+70°C$
14-Pin Plastic DIP	N74F13N
14-Pin Plastic SO	N74F13D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

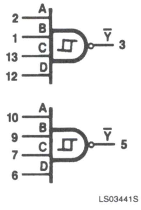
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A, B, C, D	Inputs	1.0/1.0	20μA/0.6mA
$\overline{Y}$	Output	50/33	1.0mA/20mA

NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

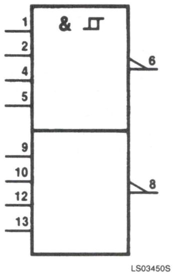
PIN CONFIGURATION


1
2
3
4
5
6
GND 7
14 V_{CC}
13
12
11
10
9
8
CD04370S

LOGIC SYMBOL


2 A
1 B
13 C
12 D
$\overline{Y}$ 3
10 A
9 B
7 C
6 D
$\overline{Y}$ 5
LS03441S

LOGIC SYMBOL (IEEE/IEC)


&
1
2
4
5
6
9
10
12
13
8
LS03450S

Schmitt Trigger FAST 74F13

Each circuit contains a 4-input Schmitt trigger followed by a Darlington level shifter and a phase splitter driving a TTL totem-pole output. The Schmitt trigger uses positive feedback to effectively speed-up slow input transitions, and provide different input threshold voltages for positive and negative-going transitions. This hysteresis between the positive-going and negative-going input threshold (typically 800mV) is determined by resistor ratios and is essentially insensitive to temperature and supply voltage variations. As long as three inputs remain at a more positive voltage than V_{T+MAX}, the gate will respond in the transitions of the other input as shown in Waveform 1.

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		74F13			UNIT
					Min	Typ[2]	Max	
V_{T+}	Positive-going threshold		$V_{CC} = 5.0V$		1.5	1.7	2.0	V
V_{T-}	Negative-going threshold		$V_{CC} = 5.0V$		0.7	0.9	1.1	V
ΔV_T	Hysteresis ($V_{T+} - V_{T-}$)		$V_{CC} = 5.0V$		0.4	0.8		V
V_{OH}	High-level output voltage		V_{CC} = MIN, $V_I = V_{T-MIN}$, I_{OH} = MAX	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, $V_I = V_{T+MAX}$, I_{OH} = MAX	±10%V_{CC}		.35	.50	V
				±5%V_{CC}		.35	.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$			−0.73	−1.2	V
I_{T+}	Input current at positive-going threshold		$V_{CC} = 5.0V$, $V_I = V_{T+}$			0		μA
I_{T-}	Input current at negative-going threshold		$V_{CC} = 5.0V$, $V_I = V_{T-}$			−350		μA
I_I	Input current at maximum input voltage		V_{CC} = MAX, $V_I = 7.0V$				100	μA
I_{IH}	High-level input current		V_{CC} = MAX, $V_I = 2.7V$				20	μA
I_{IL}	Low-level input current		V_{CC} = MAX, $V_I = 0.5V$				−0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_{IN} = GND		4.5	8.5	mA
		I_{CCL}		$V_{IN} = 4.5V$		7.0	10.0	mA

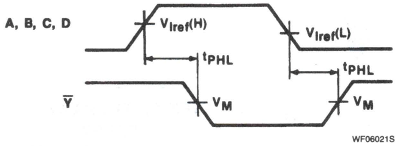
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at $V_{CC} = 5V$, $T_A = 25°C$.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F13					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A, B, C, D to $\overline{Y}$	Waveform 1	4.0 9.0	5.5 11.0	7.0 13.5	4.0 9.0	8.0 13.5	ns

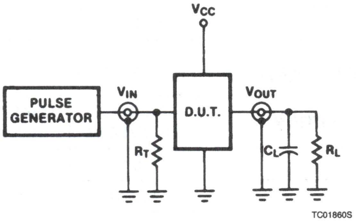
AC WAVEFORM


A, B, C, D
$V_{Iref}(H)$
$V_{Iref}(L)$
t_{PHL}
t_{PHL}
$\overline{Y}$
V_M
V_M
WF06021S

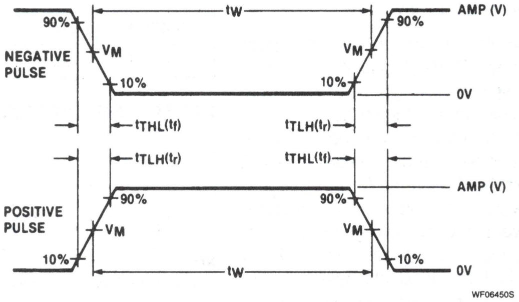
NOTE: For all waveforms, V_M = 1.5V.

Waveform 1. For Inverting Outputs

TEST CIRCUIT AND WAVEFORM


V_{CC}
PULSE GENERATOR
V_{IN}
D.U.T.
V_{OUT}
R_T
C_L
R_L
TC01860S

Test Circuit for Totem-Pole Outputs


t_W
AMP (V)
90%
90%
NEGATIVE PULSE
V_M
V_M
10%
10%
0V
$t_{THL}(t_f)$
$t_{TLH}(t_r)$
$t_{TLH}(t_r)$
$t_{THL}(t_f)$
AMP (V)
90%
90%
POSITIVE PULSE
V_M
V_M
10%
10%
0V
t_W
WF06450S

V_M = 1.5V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

FAST 74F14
Schmitt Trigger

Hex Inverter Schmitt Trigger
Product Specification

FAST Products

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F14	5.0ns	18mA

DESCRIPTION

The 'F14 contains six logic inverters which accept standard TTL input signals and provide standard TTL output levels. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. In addition, they have greater noise margin than conventional inverters.

Each circuit contains a Schmitt trigger followed by a Darlington level shifter and a phase splitter driving a TTL totem-pole output. The Schmitt trigger uses positive feedback to effectively speed-up slow input transition, and provide different input threshold voltages for positive and negative-going transitions. This hysteresis between the positive-going and negative-going input thresholds (typically 800mV) is determined internally by resistor ratios and is essentially insensitive to temperature and supply voltage variations.

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
14-Pin Plastic DIP	N74F14N
14-Pin Plastic SO	N74F14D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

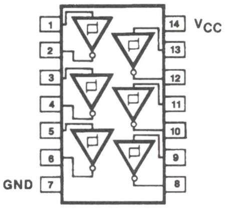
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A	Input	1.0/1.0	20μA/0.6mA
$\overline{Y}$	Output	50/33	1.0mA/20mA

NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

FUNCTION TABLE

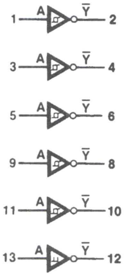
INPUT	OUTPUT
A	$\overline{Y}$
0	1
1	0

PIN CONFIGURATION



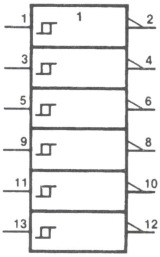
CD04380S

LOGIC SYMBOL



LS03481S

LOGIC SYMBOL (IEEE/IEC)



LS03470S

Schmitt Trigger

FAST 74F14

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

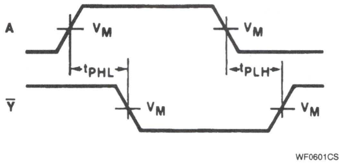
SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{T+}	Positive-going threshold		$V_{CC} = 5.0V$		1.4	1.7	2.0	V
V_{T-}	Negative-going threshold		$V_{CC} = 5.0V$		0.7	0.9	1.1	V
ΔV_T	Hysteresis ($V_{T+} - V_{T-}$)		$V_{CC} = 5.0V$		0.4	0.8		V
V_{OH}	High-level output voltage		$V_{CC} = MIN$, $V_I = V_{T-MIN}$, $I_{OH} = MAX$	$\pm10\%V_{CC}$	2.5			V
				$\pm5\%V_{CC}$	2.7	3.4		V
V_{OL}	Low-level output voltage		$V_{CC} = MIN$, $V_I = V_{T+MAX}$, $I_{OH} = MAX$	$\pm10\%V_{CC}$		0.35	0.50	V
				$\pm5\%V_{CC}$		0.35	0.50	V
V_{IK}	Input clamp voltage		$V_{CC} = MIN$, $I_I = I_{IK}$			−0.73	−1.2	V
I_{T+}	Input current at positive-going threshold		$V_{CC} = 5.0V$, $V_I = V_{T+}$			0.0		μA
I_{T-}	Input current at negative-going threshold		$V_{CC} = 5.0V$, $V_I = V_{T-}$			175		μA
I_I	Input current at maximum input voltage		$V_{CC} = MAX$, $V_I = 7.0V$				100	μA
I_{IH}	High-level input current		$V_{CC} = MAX$, $V_I = 2.7V$				20	μA
I_{IL}	Low-level input current		$V_{CC} = MAX$, $V_I = 0.5V$				−0.6	mA
I_{OS}	Short-circuit output current[3]		$V_{CC} = MAX$		−60		−150	mA
I_{CC}	Supply current (total)	I_{CCH}	$V_{CC} = MAX$	$V_{IN} = GND$		13	22	mA
		I_{CCL}		$V_{IN} = 4.5V$		23	32	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at $V_{CC} = 5V$, $T_A = 25°C$.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

SYMBOL	PARAMETER	TEST CONDITIONS	74F14					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A to $\overline{Y}$	Waveform 1	4.0 3.5	6.5 5.0	8.5 6.5	4.0 3.5	9.5 7.0	ns

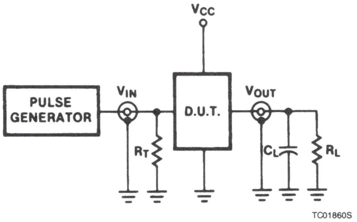
AC WAVEFORM


A
V_M
V_M
t_{PHL}
t_{PLH}
$\overline{Y}$
V_M
V_M
WF0601CS

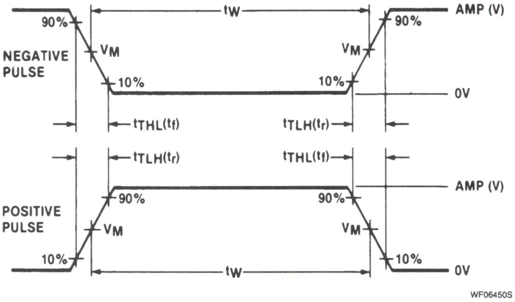
NOTE: For all waveforms, $V_M = 1.5V$.

Waveform 1. For Inverting Outputs

TEST CIRCUIT AND WAVEFORM


V_{CC}
PULSE GENERATOR
V_{IN}
D.U.T.
V_{OUT}
R_T
C_L
R_L
TC01860S

Test Circuit for Totem-Pole Outputs


NEGATIVE PULSE
90%
V_M
10%
t_W
90%
V_M
10%
AMP (V)
0V
$t_{THL}(t_f)$
$t_{TLH}(t_r)$
$t_{TLH}(t_r)$
$t_{THL}(t_f)$
POSITIVE PULSE
90%
V_M
10%
90%
V_M
10%
AMP (V)
0V
t_W
WF06450S

$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F20
Gate

Dual Four-Input NAND Gate
Product Specification

FAST Products

FUNCTION TABLE

INPUTS				OUTPUT
A	B	C	D	$\overline{Y}$
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

H = High voltage level
L = Low voltage level
X = Don't care

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F20	3.5ns	2.2mA

ORDERING INFORMATION

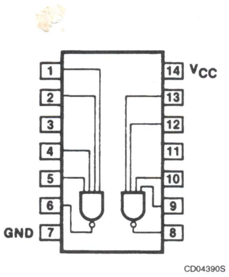
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ± 10%; T_A = 0°C to +70°C
14-Pin Plastic DIP	N74F20N
14-Pin Plastic SO	N74F20D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

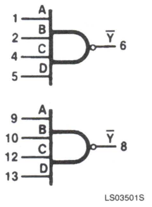
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A, B, C, D	Inputs	1.0/1.0	20μA/0.6mA
$\overline{Y}$	Output	50/33	1.0mA/20mA

NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

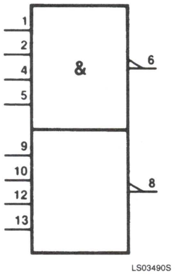
PIN CONFIGURATION


1
2
3
4
5
6
7
GND
14
V_{CC}
13
12
11
10
9
8
CD04390S

LOGIC SYMBOL


1
2
4
5
A
B
C
D
$\overline{Y}$
6
9
10
12
13
A
B
C
D
$\overline{Y}$
8
LS03501S

LOGIC SYMBOL (IEEE/IEC)


1
2
4
5
&
6
9
10
12
13
8
LS03490S

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX V_{IH} = MIN,	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OL} = MAX V_{IH} = MIN,	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				−0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_{IN} = GND		0.9	1.4	mA
		I_{CCL}		V_{IN} = 4.5V		3.4	5.1	mA

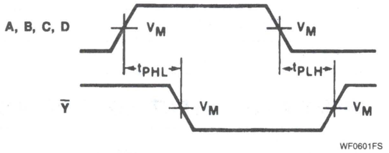
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F20					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A, B, C, D to $\overline{Y}$	Waveform 1	2.4 2.0	3.7 3.2	5.0 4.3	2.4 2.0	6.0 5.3	ns

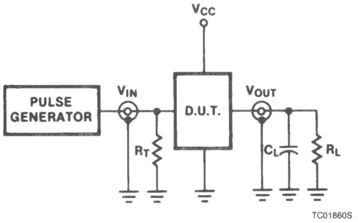
AC WAVEFORM


A, B, C, D
V_M
V_M
t_{PHL}
t_{PLH}
$\overline{Y}$
V_M
V_M
WF0601FS

NOTE: For all waveforms, $V_M = 1.5V$.

Waveform 1. For Inverting Outputs

TEST CIRCUIT AND WAVEFORM


V_{CC}
PULSE GENERATOR
V_{IN}
D.U.T.
V_{OUT}
R_T
C_L
R_L
TC01860S

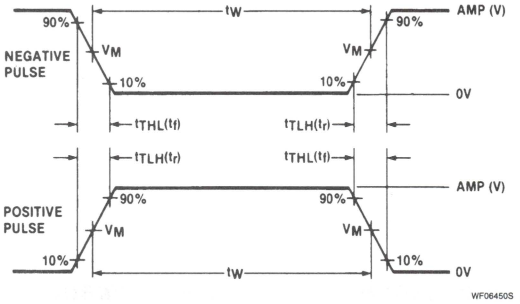
Test Circuit for Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.


NEGATIVE PULSE
90%
V_M
10%
t_W
90%
V_M
10%
AMP (V)
0V
$t_{THL}(t_f)$
$t_{TLH}(t_r)$
$t_{TLH}(t_r)$
$t_{THL}(t_f)$
POSITIVE PULSE
90%
V_M
10%
90%
V_M
10%
AMP (V)
0V
t_W
WF06450S

$V_M = 1.5V$

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

FAST 74F27
Gate

Triple Three-Input NOR Gate
Product Specification

FAST Products

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F27	3.0ns	6.5mA

FUNCTION TABLE

INPUTS			OUTPUT
A	B	C	$\overline{Y}$
L	L	L	H
X	X	H	L
X	H	X	L
H	X	X	L

H = High voltage level
L = Low voltage level
X = Don't care

ORDERING INFORMATION

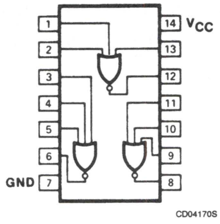
PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
14-Pin Plastic DIP	N74F27N
14-Pin Plastic SO	N74F27D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A, B, C	Data inputs	1.0/1.0	20μA/0.6mA
$\overline{Y}$	Data output	50/33	1mA/20mA

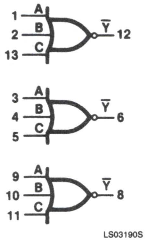
NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



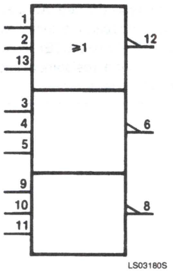
1
2
3
4
5
6
GND 7
14 VCC
13
12
11
10
9
8
CD04170S

LOGIC SYMBOL



1 A
2 B
13 C
$\overline{Y}$ 12
3 A
4 B
5 C
$\overline{Y}$ 6
9 A
10 B
11 C
$\overline{Y}$ 8
LS03190S

LOGIC SYMBOL (IEEE/IEC)



1
2
13
≥1
12
3
4
5
6
9
10
11
8
LS03180S

Gate

FAST 74F27

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

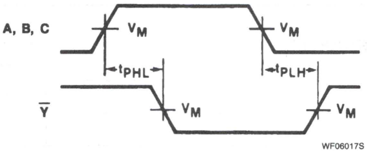
SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX V_{IH} = MIN,	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OL} = MAX V_{IH} = MIN,	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		-60		−150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_{IN} = GND		4.0	5.5	mA
		I_{CCL}		V_{IN} = 4.5V		8.5	12.0	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F27					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH}	Propagation delay A, B, C to $\overline{Y}$	Waveform 1	2.0	3.5	5.0	1.5	5.5	ns
t_{PHL}			1.0	2.5	4.5	1.0	4.5	

AC WAVEFORM

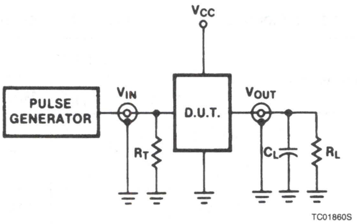


A, B, C
V_M
V_M
t_{PHL}
t_{PLH}
$\overline{Y}$
V_M
V_M
WF06017S

NOTE: For all waveforms, $V_M = 1.5V$.

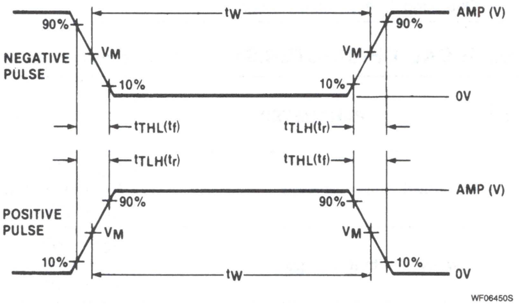
Waveform 1. Propagation Delay Input to Output

TEST CIRCUIT AND WAVEFORM



V_{CC}
PULSE GENERATOR
V_{IN}
D.U.T.
V_{OUT}
R_T
C_L
R_L
TC01860S

Test Circuit for Totem-Pole Outputs



90%
t_W
90%
AMP (V)
NEGATIVE PULSE
V_M
V_M
10%
10%
0V
$t_{THL}(t_f)$
$t_{TLH}(t_r)$
$t_{TLH}(t_r)$
$t_{THL}(t_f)$
AMP (V)
90%
90%
POSITIVE PULSE
V_M
V_M
10%
t_W
10%
0V
WF06450S

$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS

R_L = Load resistor to GND; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F30
Gate

Eight-Input NAND Gate
Product Specification

FAST Products

FUNCTION TABLE

INPUTS								OUTPUT
A	B	C	D	E	F	G	H	$\overline{Y}$
L	X	X	X	X	X	X	X	H
X	L	X	X	X	X	X	X	H
X	X	L	X	X	X	X	X	H
X	X	X	L	X	X	X	X	H
X	X	X	X	L	X	X	X	H
X	X	X	X	X	L	X	X	H
X	X	X	X	X	X	L	X	H
X	X	X	X	X	X	X	L	H
H	H	H	H	H	H	H	H	L

H = High voltage level
L = Low voltage level
X = Don't care

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F30	3.2ns	1.7mA

ORDERING INFORMATION

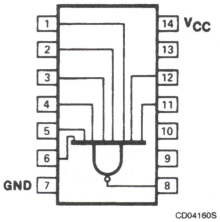
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ± 10%; T_A = 0°C to +70°C
14-Pin Plastic DIP	N74F30N
14-Pin Plastic SO	N74F30D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

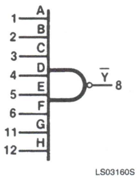
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A – H	Data inputs	1.0/1.0	20μA/0.6mA
$\overline{Y}$	Data output	50/33	1.0mA/20mA

NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

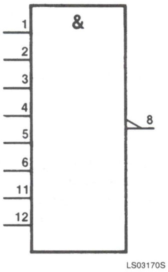
PIN CONFIGURATION


1
2
3
4
5
6
GND 7
14 VCC
13
12
11
10
9
8
CD04160S

LOGIC SYMBOL


1 A
2 B
3 C
4 D
5 E
6 F
11 G
12 H
$\overline{Y}$ 8
LS03160S

LOGIC SYMBOL (IEEE/IEC)


&
1
2
3
4
5
6
11
12
8
LS03170S

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX V_{IH} = MIN,	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OL} = MAX V_{IH} = MIN,	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_{IN} = GND		0.6	1.5	mA
		I_{CCL}		V_{IN} = 4.5V		2.8	4.0	mA

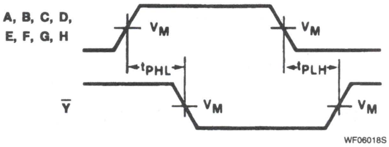
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F30					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A, B, C, D, E, F, G, H to $\overline{Y}$	Waveform 1	1.5 1.0	3.5 3.0	5.0 4.5	1.5 1.0	5.5 5.0	ns

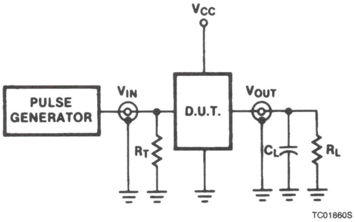
AC WAVEFORM


A, B, C, D,
E, F, G, H
V_M
V_M
t_{PHL}
t_{PLH}
$\overline{Y}$
V_M
V_M
WF06018S

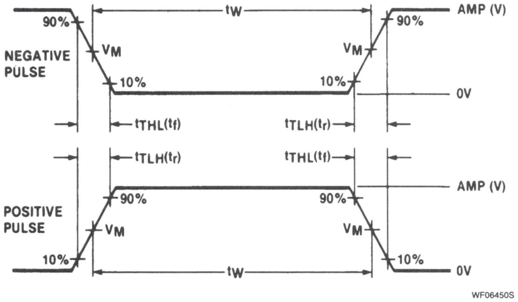
NOTE: For all waveforms, $V_M = 1.5V$.

Waveform 1. Propagation Delay Input to Output

TEST CIRCUIT AND WAVEFORM


V_{CC}
PULSE GENERATOR
V_{IN}
D.U.T.
V_{OUT}
R_T
C_L
R_L
TC01860S

Test Circuit for Totem-Pole Outputs


tW
90%
90%
AMP (V)
NEGATIVE PULSE
V_M
V_M
10%
10%
0V
$t_{THL}(t_f)$
$t_{TLH}(t_r)$
$t_{TLH}(t_r)$
$t_{THL}(t_f)$
AMP (V)
90%
90%
POSITIVE PULSE
V_M
V_M
10%
10%
0V
tW
WF06450S

$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS
R_L = Load resistor to GND; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F32
Gate

Quad Two-Input OR Gate
Product Specification

FAST Products

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	H

H = High voltage level
L = Low voltage level

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F32	4.1ns	8.2mA

ORDERING INFORMATION

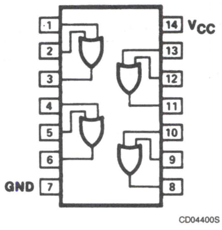
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ± 10%; T_A = 0°C to +70°C
14-Pin Plastic DIP	N74F32N
14-Pin Plastic SO	N74F32D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

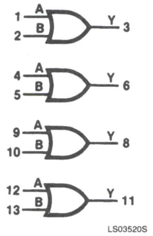
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A, B	Inputs	1.0/1.0	20μA/0.6mA
Y	Output	50/33	1.0mA/20mA

NOTE:
1. One (1.0) FAST Unit Load (U.L.) is defined as: 20μA in the High state and 0.6mA in the Low state.

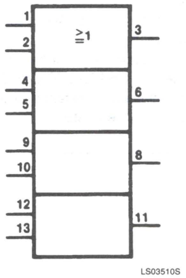
PIN CONFIGURATION


1
2
3
4
5
6
GND 7
14 V_{CC}
13
12
11
10
9
8
CD04400S

LOGIC SYMBOL


1 A
2 B
Y 3
4 A
5 B
Y 6
9 A
10 B
Y 8
12 A
13 B
Y 11
LS03520S

LOGIC SYMBOL (IEEE/IEC)


≥1
1
2
3
4
5
6
9
10
8
12
13
11
LS03510S

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX V_{IH} = MIN,	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OL} = MAX V_{IH} = MIN,	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				0.60	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_{IN} = GND		6.1	9.2	mA
		I_{CCL}		V_{IN} = 4.5V		10.3	15.5	mA

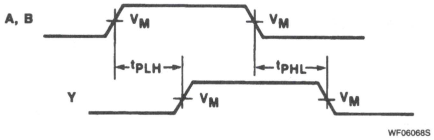
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F32					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH}	Propagation delay A, B to Y	Waveform 1	3.0	4.2	5.6	3.0	6.6	ns
t_{PHL}			3.0	4.0	5.3	3.0	6.3	

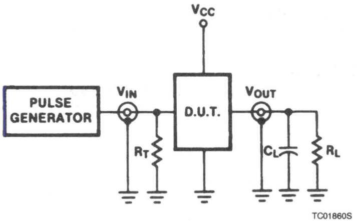
AC WAVEFORM


A, B
V_M
V_M
t_PLH
t_PHL
Y
V_M
V_M
WF06068S

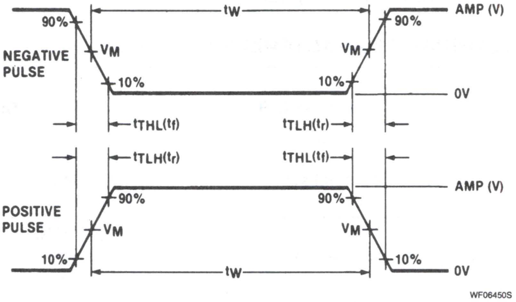
NOTE: For all waveforms, $V_M = 1.5V$.

Waveform 1. For Non-Inverting Outputs

TEST CIRCUIT AND WAVEFORM


V_CC
PULSE GENERATOR
V_IN
D.U.T.
V_OUT
R_T
C_L
R_L
TC01860S

Test Circuit for Totem-Pole Outputs


90%
NEGATIVE PULSE
V_M
10%
t_W
V_M
90%
10%
AMP (V)
0V
t_THL(t_f)
t_TLH(t_r)
t_TLH(t_r)
t_THL(t_f)
AMP (V)
POSITIVE PULSE
90%
V_M
10%
90%
V_M
10%
t_W
0V
WF06450S

$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F37
Buffer

Quad Two-Input NAND Buffer
Product Specification

FAST Products

FUNCTION TABLE

INPUTS		OUTPUT
A	**B**	**$\overline{Y}$**
L	L	H
L	H	H
H	L	H
H	H	L

H = High voltage level
L = Low voltage level
X = Don't care

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F37	3.5ns	13mA

ORDERING INFORMATION

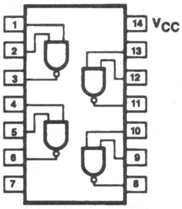
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ± 10%; T_A = 0°C to +70°C
14-Pin Plastic DIP	N74F37N
14-Pin Plastic SO	N74F37D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A, B	Data inputs	1.0/2.0	20µA/1.2mA
$\overline{Y}$	Data output	750/106.6	15mA/64mA

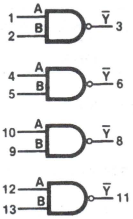
NOTE:
1. One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



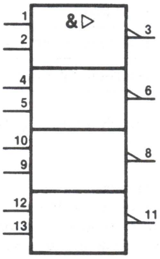
CD04410S

LOGIC SYMBOL



LS03541S

LOGIC SYMBOL (IEEE/IEC)



LS03530S

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−15	mA
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = −1mA	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7	3.4		V
				I_{OH} = −15mA	±10%V_{CC}	2.0			V
					±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 48mA	±10%V_{CC}		0.35	0.50	V
				I_{OL} = 64mA	±5%V_{CC}		0.40	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V					100	μA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					−1.2	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX			100		−225	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX		V_{IN} = GND		3	6	mA
		I_{CCL}			V_{IN} = 4.5V		23	33	mA

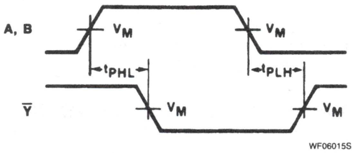
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F37					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A, B to $\overline{Y}$	Waveform 1	2.5 1.5	3.5 2.5	5.5 4.5	2.0 1.5	6.5 5.0	ns

AC WAVEFORM

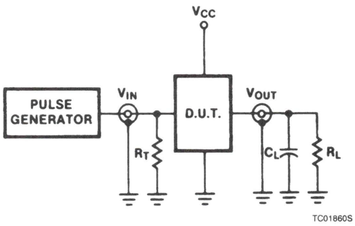


A, B
V_M
V_M
t_{PHL}
t_{PLH}
$\overline{Y}$
V_M
V_M
WF06015S

NOTE: For all waveforms, $V_M = 1.5V$.

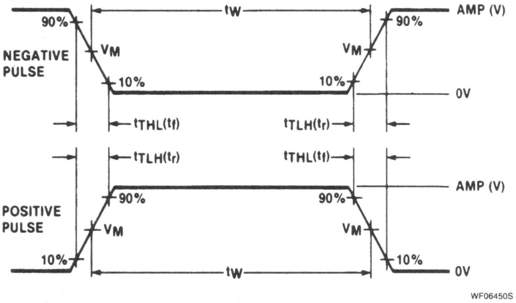
Waveform 1. For Inverting Outputs

TEST CIRCUIT AND WAVEFORM



V_{CC}
PULSE GENERATOR
V_{IN}
D.U.T.
V_{OUT}
R_T
C_L
R_L
TC01860S

Test Circuit for Totem-Pole Outputs



tw
90%
AMP (V)
NEGATIVE PULSE
V_M
10%
0V
$t_{THL}(t_f)$
$t_{TLH}(t_r)$
$t_{TLH}(t_r)$
$t_{THL}(t_f)$
POSITIVE PULSE
AMP (V)
0V
WF06450S

$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS

R_L = Load resistor to GND; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F38

Buffer

Quad Two-Input NAND Buffer (Open-Collector)
Product Specification

FAST Products

FUNCTION TABLE

INPUTS		OUTPUT
A	B	$\overline{Y}$
L	L	H
L	H	H
H	L	H
H	H	L

H = High voltage level
L = Low voltage level
X = Don't care

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F38	7.0ns	13mA

ORDERING INFORMATION

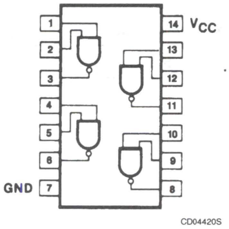
PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
14-Pin Plastic DIP	N74F38N
14-Pin Plastic SO	N74F38D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

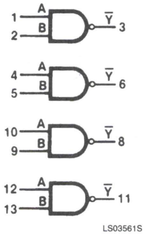
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A, B	Inputs	1.0/2.0	20μA/1.2mA
$\overline{Y}$	Output	OC*/106.7	OC*/64mA

NOTES:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.
2. *OC = Open-Collector.

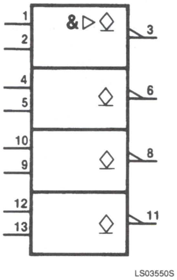
PIN CONFIGURATION


1
2
3
4
5
6
GND 7
14 VCC
13
12
11
10
9
8
CD04420S

LOGIC SYMBOL


1 A
2 B
$\overline{Y}$ 3
4 A
5 B
$\overline{Y}$ 6
10 A
9 B
$\overline{Y}$ 8
12 A
13 B
$\overline{Y}$ 11
LS03561S

LOGIC SYMBOL (IEEE/IEC)


&▷◇
1
2
3
4
5
6
10
9
8
12
13
11
LS03550S

Buffer

FAST 74F38

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	128	mA
T_A	Operating free-air temperature range	0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			4.5	mV
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
I_{OH}	High-level output current		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, V_{OH} = MAX					250	μA
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 48mA	±10%V_{CC}		0.35	0.50	V
				I_{OL} = 64mA	±5%V_{CC}		0.40	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$				−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V					100	μA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					−1.2	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX		V_{IN} = GND		4	7	mA
		I_{CCL}			V_{IN} = 4.5V		22	30	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.

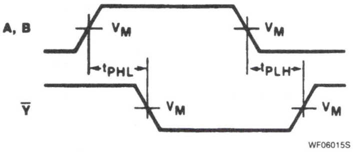
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F38					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A, B to $\overline{Y}$	Waveform 1	7.5 1.5	10 3.0	12.5 5.0	7.5 1.5	13 5.5	ns

NOTE:

1. When using open-collector parts, the value of the pull-up resistor greatly affects the value of the t_{PLH}. For example, changing the specified pull-up resistor value from 500Ω will improve the t_{PLH} up to 50% with only a slight increase in the t_{PHL}. However, if the value of the pull-up resistor is changed, the user must make certain that the total I_{OL} current through the resistor, plus the total IIL s of the receivers does not exceed the I_{OL} maximum specification.

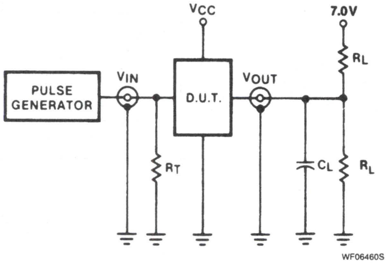
AC WAVEFORM


A, B
VM
VM
tPHL
tPLH
Y
VM
VM
WF06015S

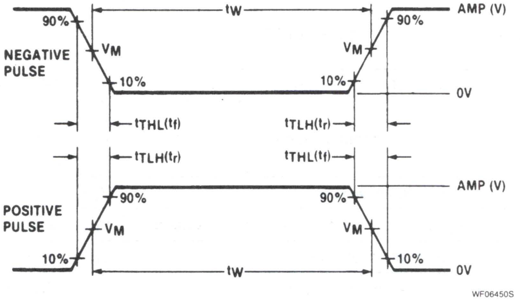
NOTE: For all waveforms, $V_M = 1.5V$.

Waveform 1. Propagation Delay Input to Output

TEST CIRCUIT AND WAVEFORM


VCC
7.0V
RL
PULSE GENERATOR
VIN
D.U.T.
VOUT
RT
CL
RL
WF06460S

Test Circuit for Open-Collector Outputs


90%
tW
90%
AMP (V)
NEGATIVE PULSE
VM
VM
10%
10%
0V
tTHL(tf)
tTLH(tr)
tTLH(tr)
tTHL(tf)
AMP (V)
90%
90%
POSITIVE PULSE
VM
VM
10%
10%
tW
0V
WF06450S

$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS
R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST Products

FAST 74F40
Buffer

Dual Four-Input NAND Buffer
Product Specification

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F40	3.5ns	6mA

FUNCTION TABLE

INPUTS				OUTPUT
A	B	C	D	$\overline{Y}$
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

H = High voltage level
L = Low voltage level
X = Don't care

ORDERING INFORMATION

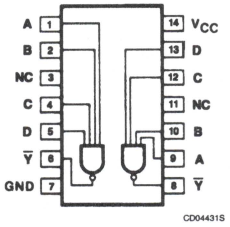
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ± 10%; T_A = 0°C to +70°C
14-Pin Plastic DIP	N74F40N
14-Pin Plastic SO	N74F40D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

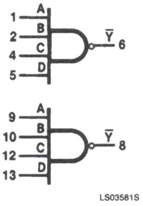
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A, B, C, D	Data inputs	1.0/2.0	20μA/1.2mA
$\overline{Y}$	Data output	750/106.7	15mA/64mA

NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

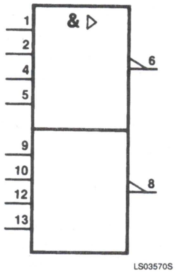
PIN CONFIGURATION


A 1
B 2
NC 3
C 4
D 5
$\overline{Y}$ 6
GND 7
14 V_{CC}
13 D
12 C
11 NC
10 B
9 A
8 $\overline{Y}$
CD04431S

LOGIC SYMBOL


1 A
2 B
4 C
5 D
$\overline{Y}$ 6
9 A
10 B
12 C
13 D
$\overline{Y}$ 8
LS03581S

LOGIC SYMBOL (IEEE/IEC)


& ▷
1
2
4
5
6
9
10
12
13
8
LS03570S

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	128	mA
T_A	Operating free-air temperature range	0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−15	mA
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = −1mA	$\pm10\%V_{CC}$	2.5			V
					$\pm5\%V_{CC}$	2.7	3.4		V
				I_{OH} = −15mA	$\pm10\%V_{CC}$	2.0			V
					$\pm5\%V_{CC}$	2.0			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 48mA	$\pm10\%V_{CC}$		0.35	0.50	V
				I_{OL} = 64mA	$\pm5\%V_{CC}$		0.40	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$				−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V					100	μA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					−1.2	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX			−100		−225	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX		V_{IN} = GND		1.75	4	mA
		I_{CCL}			V_{IN} = 4.5V		11	17	mA

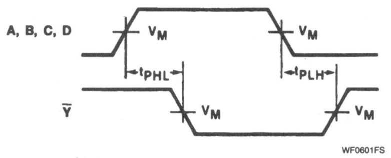
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F40 $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			74F40 $T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		UNIT
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A, B, C, D to $\overline{Y}$	Waveform 1	2.0 1.5	4.0 3.0	6.0 5.0	1.5 1.0	7.0 5.5	ns

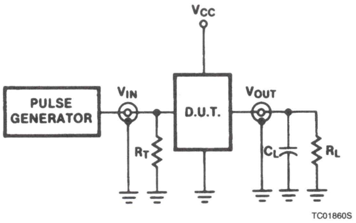
AC WAVEFORM


A, B, C, D
V_M
V_M
t_{PHL}
t_{PLH}
$\overline{Y}$
V_M
V_M
WF0601FS

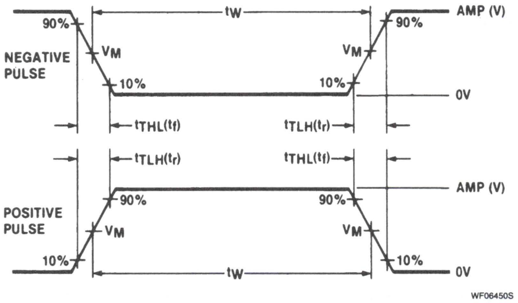
NOTE: For all waveforms, $V_M = 1.5V$.

Waveform 1. Inverting Outputs

TEST CIRCUIT AND WAVEFORM


V_{CC}
PULSE GENERATOR
V_{IN}
D.U.T.
V_{OUT}
R_T
C_L
R_L
TC01860S

Test Circuit for Totem-Pole Outputs


t_W
AMP (V)
90%
90%
NEGATIVE PULSE
V_M
V_M
10%
10%
0V
$t_{THL}(t_f)$
$t_{TLH}(t_r)$
$t_{TLH}(t_r)$
$t_{THL}(t_f)$
AMP (V)
90%
90%
POSITIVE PULSE
V_M
V_M
10%
10%
t_W
0V
WF06450S

$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS

R_L = Load resistor to GND; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{THL}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

FAST 74F51
Gate

Dual 2-Wide 2-Input, 2-Wide 3-Input AND-OR-Invert Gate
Product Specification

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F51	3.0ns	3.5mA

FUNCTION TABLE
For 3-Input Gates

INPUTS						OUTPUT
A	B	C	D	E	F	$1\overline{Y}$
H	H	H	X	X	X	L
X	X	X	H	H	H	L
All other combinations						H

FUNCTION TABLE
For 2-Input Gates

INPUTS				OUTPUT
A	B	C	D	$2\overline{Y}$
H	H	X	X	L
X	X	H	H	L
All other combinations				H

H = High voltage level
L = Low voltage level
X = Don't care

ORDERING INFORMATION

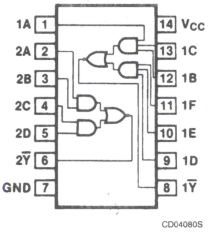
PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
14-Pin Plastic DIP	N74F51N
14-Pin Plastic SO	N74F51D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

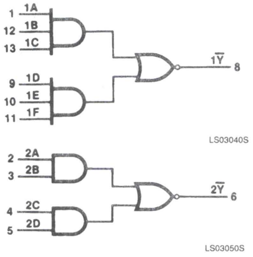
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A, B, C, D, E, F	Data inputs	1.0/1.0	20μA/0.6mA
$1\overline{Y}$, $2\overline{Y}$	Data outputs	50/33	1mA/20mA

NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

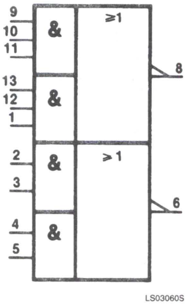
PIN CONFIGURATION


1A 1
2A 2
2B 3
2C 4
2D 5
$2\overline{Y}$ 6
GND 7
14 Vcc
13 1C
12 1B
11 1F
10 1E
9 1D
8 $1\overline{Y}$
CD04080S

LOGIC SYMBOL


1 1A
12 1B
13 1C
9 1D
10 1E
11 1F
$1\overline{Y}$ 8
LS03040S
2 2A
3 2B
4 2C
5 2D
$2\overline{Y}$ 6
LS03050S

LOGIC SYMBOL (IEEE/IEC)


9
10
11
&
≥1
8
13
12
1
&
2
3
&
≥1
6
4
5
&
LS03060S

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX V_{IH} = MIN,	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OL} = MAX V_{IH} = MIN,	±10%V_{CC}		0.35	0.5	V
				±5%V_{CC}		0.35	0.5	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				−0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_{IN} = GND		1.8	3.0	mA
		I_{CCL}		V_{IN} = 4.5V		5.5	7.5	mA

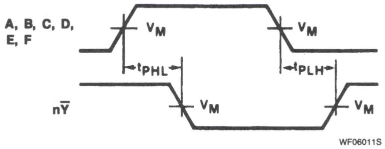
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F51					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A, B, C, D, E, F to $n\overline{Y}$	Waveform 1	2.0 1.0	3.5 2.5	5.5 4.0	1.5 1.0	6.5 4.5	ns

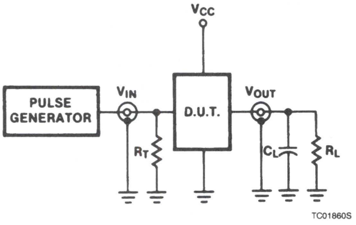
AC WAVEFORM


A, B, C, D, E, F
VM
VM
tPHL
tPLH
nȲ
VM
VM
WF06011S

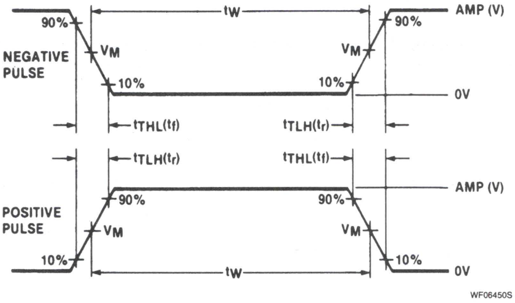
NOTE: For all waveforms, $V_M = 1.5V$.

Waveform 1. Propagation Delay Input to Output

TEST CIRCUIT AND WAVEFORM


VCC
PULSE GENERATOR
VIN
D.U.T.
VOUT
RT
CL
RL
TC01860S

Test Circuit for Totem-Pole Outputs


tW
90%
AMP (V)
NEGATIVE PULSE
VM
VM
10%
10%
0V
tTHL(tf)
tTLH(tr)
tTLH(tr)
tTHL(tf)
AMP (V)
POSITIVE PULSE
90%
90%
VM
VM
10%
10%
tW
0V
WF06450S

$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS

R_L = Load resistor to GND; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST Products

FAST 74F64
Gate

Four-Two-Three-Two-Input AND-OR-Invert Gate
Product Specification

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F64	4.0ns	2.5mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ± 10%; T_A = 0°C to +70°C
14-Pin Plastic DIP	N74F64N
14-Pin Plastic SO	N74F64D

FUNCTION TABLE

INPUTS											OUTPUT
A	B	C	D	E	F	G	H	J	K	L	$\overline{Y}$
H	H	X	X	X	X	X	X	X	X	X	L
X	X	H	H	H	H	X	X	X	X	X	L
X	X	X	X	X	X	H	H	H	X	X	L
X	X	X	X	X	X	X	X	X	H	H	L
All other combinations											H

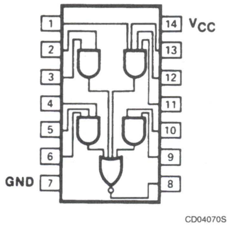
H = High voltage level
L = Low voltage level
X = Don't care

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

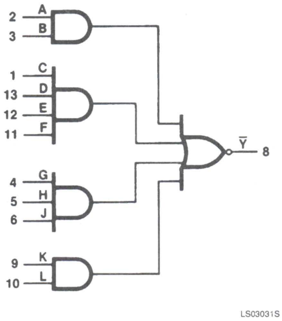
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A – L	Inputs	1.0/1.0	20μA/0.6mA
$\overline{Y}$	Output	50/33	1.0mA/20mA

NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

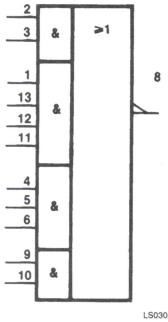
PIN CONFIGURATION


1
2
3
4
5
6
GND 7
14 VCC
13
12
11
10
9
8
CD04070S

LOGIC SYMBOL


2 A
3 B
1 C
13 D
12 E
11 F
4 G
5 H
6 J
9 K
10 L
Y̅ 8
LS03031S

LOGIC SYMBOL (IEEE/IEC)


2
3
&
≥1
1
13
12
11
&
8
4
5
6
&
9
10
&
LS03020S

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX V_{IH} = MIN,	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OL} = MAX V_{IH} = MIN,	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				−0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_{IN} = GND		1.9	2.8	mA
		I_{CCL}		V_{IN} = 4.5V		3.1	4.7	mA

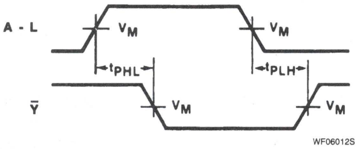
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F64 $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$ Min	Typ	Max	$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$ Min	Max	UNIT
t_{PLH} t_{PHL}	Propagation delay A – L to $\overline{Y}$	Waveform 1	2.5 2.0	4.6 3.2	6.0 4.5	2.5 2.0	7.0 5.5	ns

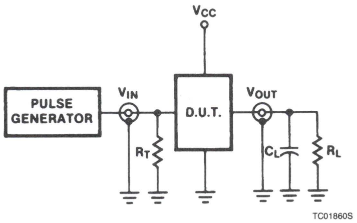
AC WAVEFORM


A - L
V_M
V_M
t_{PHL}
t_{PLH}
$\overline{Y}$
V_M
V_M
WF06012S

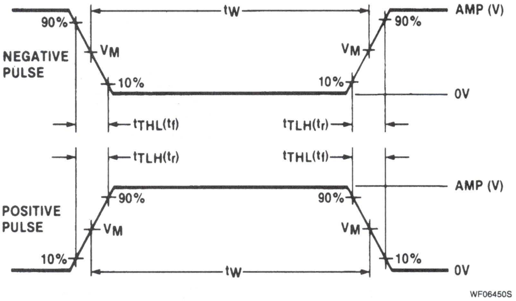
NOTE: For all waveforms, $V_M = 1.5V$.

Waveform 1. For Inverting Outputs

TEST CIRCUIT AND WAVEFORM


V_{CC}
PULSE GENERATOR
V_{IN}
D.U.T.
V_{OUT}
R_T
C_L
R_L
TC01860S

Test Circuit for Totem-Pole Outputs


t_W
AMP (V)
90%
90%
NEGATIVE PULSE
V_M
V_M
10%
10%
0V
$t_{THL}(t_f)$
$t_{TLH}(t_r)$
$t_{TLH}(t_r)$
$t_{THL}(t_f)$
AMP (V)
90%
90%
POSITIVE PULSE
V_M
V_M
10%
10%
0V
t_W
WF06450S

$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

FAMILY	INPUT PULSE REQUIREMENTS Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F74
Flip-Flop

Dual D-Type Flip-Flop
Product Specification

FAST Products

DESCRIPTION

The 'F74 is a dual-positive edge-triggered D-type flip-flop featuring individual Data, Clock, Set and Reset inputs, and complementary Q and $\overline{Q}$ outputs.

Set ($\overline{S}_D$) and Reset ($\overline{R}_D$) are asynchronous active-Low inputs and operate independently of the Clock input. Information on the Data (D) input is transferred to the Q output on the Low-to-High transition of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. The D inputs must be stable one set-up time prior to the Low-to-High clock transition for predictable operation.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F74	125MHz	11.5mA

ORDERING INFORMATION

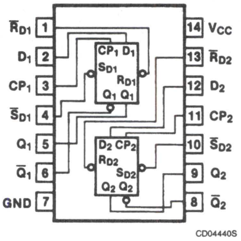
PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
14-Pin Plastic DIP	N74F74N
14-Pin Plastic SO	N74F74D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

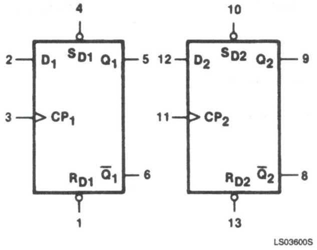
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_1, D_2	Data inputs	1.0/1.0	20μA/0.6mA
CP_1, CP_2	Clock pulse inputs (active rising edge)	1.0/1.0	20μA/0.6mA
$\overline{R}_{D1}$, $\overline{R}_{D2}$	Reset inputs (active-Low)	1.0/3.0	20μA/1.8mA
$\overline{S}_{D1}$, $\overline{S}_{D2}$	Set inputs (active-Low)	1.0/3.0	20μA/1.8mA
Q_1, $\overline{Q}_1$, Q_2, $\overline{Q}_2$	Outputs	50/33	1.0mA/20mA

NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

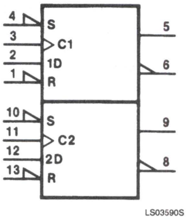
PIN CONFIGURATION


$\overline{R}_{D1}$ 1
D_1 2
CP_1 3
$\overline{S}_{D1}$ 4
Q_1 5
$\overline{Q}_1$ 6
GND 7
14 V_{CC}
13 $\overline{R}_{D2}$
12 D_2
11 CP_2
10 $\overline{S}_{D2}$
9 Q_2
8 $\overline{Q}_2$
CP_1 D_1
S_{D1}
R_{D1}
Q_1 Q_1
D_2 CP_2
R_{D2}
S_{D2}
Q_2 Q_2
CD04440S

LOGIC SYMBOL


4
10
2
D_1
S_{D1}
Q_1
5
12
D_2
S_{D2}
Q_2
9
3
CP_1
11
CP_2
R_{D1}
$\overline{Q}_1$
6
R_{D2}
$\overline{Q}_2$
8
1
13
LS03600S

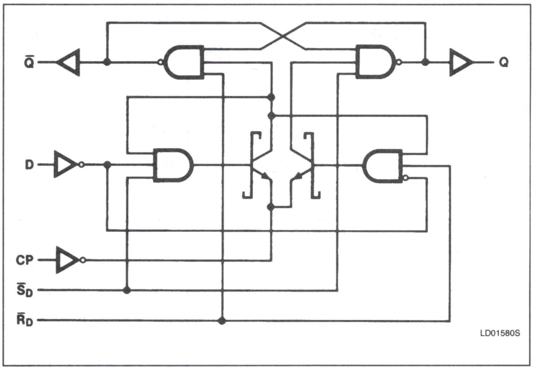
LOGIC SYMBOL (IEEE/IEC)


4
S
3
C1
2
1D
1
R
5
6
10
S
11
C2
12
2D
13
R
9
8
LS03590S

Flip-Flop

FAST 74F74

LOGIC DIAGRAM



MODE SELECT — FUNCTION TABLE

OPERATING MODE	INPUTS				OUTPUTS	
	$\overline{S}_D$	$\overline{R}_D$	CP	D	Q	$\overline{Q}$
Asynchronous Set	L	H	X	X	H	L
Asynchronous Reset (Clear)	H	L	X	X	L	H
Undetermined(1)	L	L	X	X	H	H
Load "1" (Set)	H	H	↑	h	H	L
Load "0" (Reset)	H	H	↑	l	L	H

H = High voltage level steady state.
h = High voltage level one set-up time prior to the Low-to-High clock transition.
L = Low voltage level steady state.
l = Low voltage level one set-up time prior to the Low-to-High clock transition.
X = Don't care.
↑ = Low-to-High clock transition.

NOTE:

(1) Both outputs will be High if both $\overline{S}_D$ and $\overline{R}_D$ go Low simultaneously.

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	–0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			–18	mA
I_{OH}	High-level output current			–1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		74F74			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX V_{IH} = MIN,	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OL} = MAX V_{IH} = MIN,	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current	D, CP inputs	V_{CC} = MAX, V_I = 0.5V				−0.6	mA
		$\overline{R}_D$, $\overline{S}_D$ inputs					−1.8	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current[4] (total)		V_{CC} = MAX			11.5	16	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Measure I_{CC} with the Clock inputs grounded and all outputs open, with the Q and $\overline{Q}$ outputs High in turn.

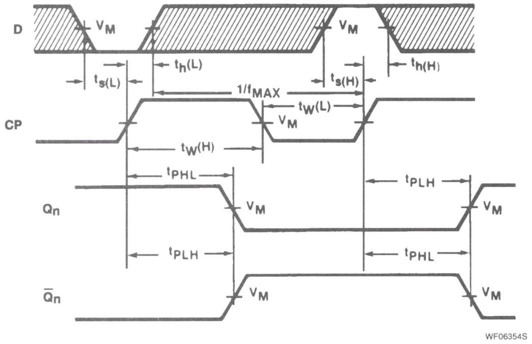
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F74					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	100	125		100		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n, $\overline{Q}_n$	Waveform 1	3.8 4.4	5.3 6.2	6.8 8.0	3.8 4.4	7.8 9.2	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{SD}_n$ or $\overline{RD}_n$ to Q_n, $\overline{Q}_n$	Waveform 2	3.2 3.5	4.6 7.0	6.1 9.0	3.2 3.5	7.1 10.5	ns

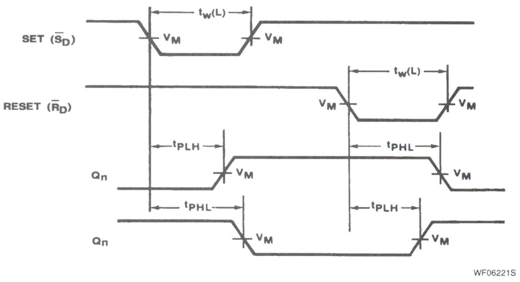
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	74F74					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_s (H) t_s (L)	Setup time High or Low, D_n to CP	Waveform 1	2.0 3.0			2.0 3.0		ns
t_h (H) t_h (L)	Hold time High or Low, D_n to CP	Waveform 1	1.0 1.0			1.0 1.0		ns
t_W (H) t_W (L)	Clock pulse width, High or Low	Waveform 1	4.0 5.0			4.0 5.0		ns
t_W (L)	$\overline{R}_D$ or $\overline{S}_D$ pulse width, Low	Waveform 2	4.0			4.0		ns
t_{rec}	Recovery time, $\overline{R}_D$ or $\overline{S}_D$ to CP	Waveform 3	2.0			2.0		ns

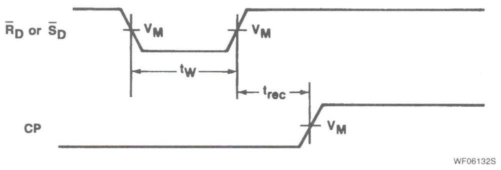
AC WAVEFORMS


D
VM
th(L)
ts(L)
1/fMAX
ts(H)
th(H)
CP
tW(L)
tW(H)
tPHL
tPLH
Qn
tPLH
tPHL
Q̄n
WF06354S

Waveform 1. Clock to Output Delays, Data Setup and Hold Times, Clock Pulse Width


tW(L)
SET (S̄D)
VM
RESET (R̄D)
tPLH
tPHL
Qn
tPHL
tPLH
Q̄n
WF06221S

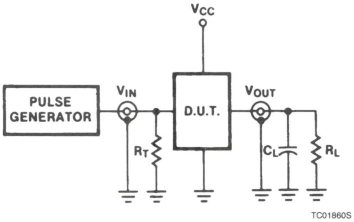
Waveform 2. Set and Reset to Output Delays, Set and Reset Pulse Widths


R̄D or S̄D
VM
tW
trec
CP
WF06132S

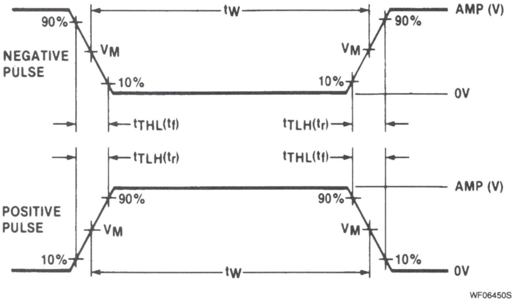
Waveform 3. Recovery Time

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable performance.

TEST CIRCUIT AND WAVEFORM


V_{CC}
PULSE GENERATOR
V_{IN}
D.U.T.
V_{OUT}
R_T
C_L
R_L
TC01860S

Test Circuit for Totem-Pole Outputs


90%
NEGATIVE PULSE
V_M
10%
t_W
AMP (V)
0V
$t_{THL}(t_f)$
$t_{TLH}(t_r)$
POSITIVE PULSE
WF06450S

$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F83
4-Bit Adder

Product Specification

FAST Products

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F83	7.0ns	36mA

FEATURES
- **High-speed 4-bit binary addition**
- **Cascadable in 4-bit increments**
- **Functionally equivalent to 'F283 but with center power pins**

DESCRIPTION
The 'F83 adds two 4-bit binary words (A_n plus B_n) plus the incoming carry. The binary sum appears on the Sum outputs ($\Sigma 1 - \Sigma 4$) and the outgoing carry (C_{OUT}) according to the equation:

$$C_{IN} + (A_1 + B_1) + 2(A_2 + B_2) + 4(A_3 + B_3) + B(A_4 + B_4) = \Sigma_1 + 2\Sigma_2 + 4\Sigma_3 + 8\Sigma_4 + 16C_{OUT}$$

where (+) = plus.

Due to the symmetry of the binary add function, the 'F83 can be used with either all active-High operands (positive logic) or with all active-Low operands (negative logic). See Function Table. With active-High inputs, C_{IN} cannot be left open; it must be held Low when no "carry in" is intended. Interchanging inputs of equal weight does not affect the operation, thus A_1, B_1, C_{IN} can arbitrarily be assigned to pins 10, 11, 13, etc.

ORDERING INFORMATION

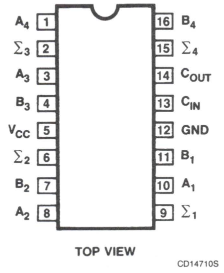
PACKAGE	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$, $T_A = 0°C$ to $+70°C$
16-Pin Plastic DIP	N74F83N
16-Pin Plastic SO	N74F83D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

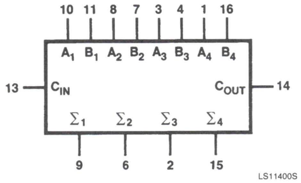
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$A_1 - A_4$	A operand inputs	1.0/2.0	20µA/1.2mA
$B_1 - B_4$	B operand inputs	1.0/2.0	20µA/1.2mA
C_{IN}	Carry input	1.0/1.0	20µA/0.6mA
$\Sigma_1 - \Sigma_4$	Sum outputs	50/33	1.0mA/20mA
C_{OUT}	Carry output	50/33	1.0mA/20mA

NOTE:
1. One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION

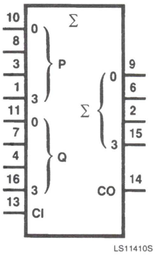

A4 1
Σ3 2
A3 3
B3 4
VCC 5
Σ2 6
B2 7
A2 8
16 B4
15 Σ4
14 COUT
13 CIN
12 GND
11 B1
10 A1
9 Σ1
TOP VIEW
CD14710S

LOGIC SYMBOL


10 11 8 7 3 4 1 16
A1 B1 A2 B2 A3 B3 A4 B4
13 CIN
COUT 14
Σ1 Σ2 Σ3 Σ4
9 6 2 15
LS11400S

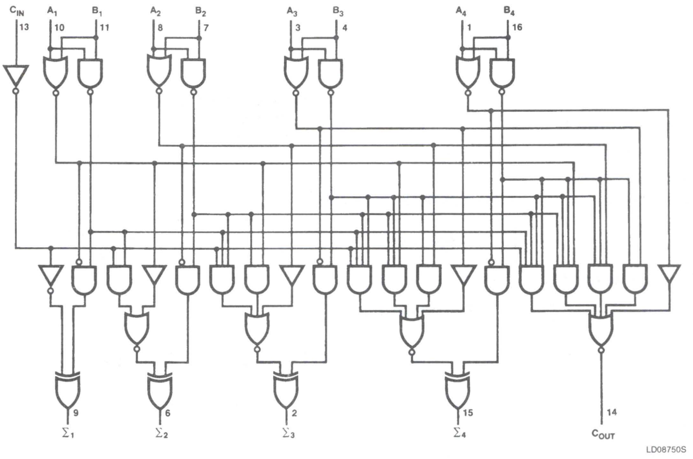
V_{CC} = Pin 5
GND = Pin 12

LOGIC SYMBOL


Σ
10
8
3
1
11
7
4
16
13
0
P
3
0
Q
3
CI
0
Σ
3
9
6
2
15
CO
14
LS11410S

4-Bit Adder FAST 74F83

LOGIC DIAGRAM



C_{IN}
13
A_1
10
B_1
11
A_2
8
B_2
7
A_3
3
B_3
4
A_4
1
B_4
16
9
Σ_1
6
Σ_2
2
Σ_3
15
Σ_4
14
C_{OUT}
LD08750S

V_{CC} = Pin 16
GND = Pin 8
( ) = Pin numbers

FUNCTION TABLE

PINS	C_{IN}	A_1	A_2	A_3	A_4	B_1	B_2	B_3	B_4	Σ_1	Σ_2	Σ_3	Σ_4	C_{OUT}
Logic levels	L	L	H	L	H	H	L	L	H	H	H	L	L	H
Active High	0	0	1	0	1	1	0	0	1	1	1	0	0	1
Active Low	1	1	0	1	0	0	1	1	0	0	0	1	1	0

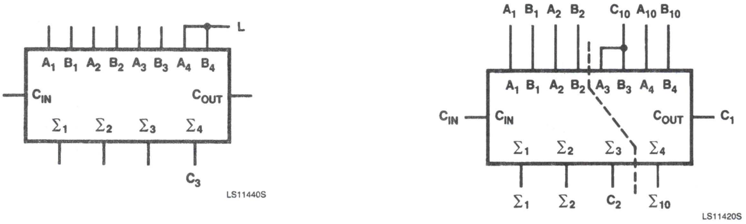
Example:
1001
1010
10011
(10 + 9 = 19)
(Carry + 5 + 6 = 12)

H = High voltage level
L = Low voltage level

Due to pin limitations, the intermediate carries of the 'F83 are not brought out for use as inputs or outputs. However, other means can be used to effectively insert a carry into, or bring a carry out from, an intermediate stage.

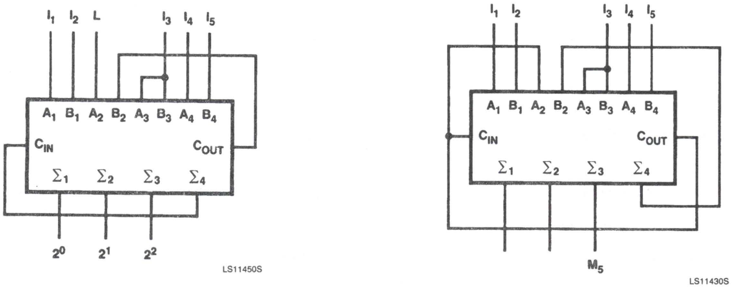
Figure 1a shows how to make a 3-bit adder. Tying the operand inputs of the fourth adder (A_4, B_4) Low makes Σ_4 dependent only on, and equal to, the carry from the third adder.

Using somewhat the same principle, Figure 1b shows a way of dividing the 'F83 into a 2-bit and a 1-bit adder. The third stage adder (A_3, B_3, Σ_3) is used merely as a means of getting a carry (C_{10}) signal into the fourth stage (via A_3 and B_3) and bringing out the carry from the second stage on Σ_3. Note that as long as A_3 and B_3 are the same, whether High or Low, they do not influence Σ_3. Similarly, when A_3 and B_3 are the same, the carry into the third stage does not influence the carry out of the third stage. Figure 1c shows a method of implementing a 5-input encoder where the inputs are equally weighted. The outputs Σ_1, Σ_2, and Σ_3 present a binary number equal to the number of inputs $I_1 - I_5$ that are true. Figure 1d shows one method of implementing a 5-input majority gate. When three or more of the inputs $I_1 - I_5$ are true, the output M_5 is true.


L
A1 B1 A2 B2 A3 B3 A4 B4
CIN
COUT
Σ1 Σ2 Σ3 Σ4
C3
LS11440S
A1 B1 A2 B2 C10 A10 B10
A1 B1 A2 B2 A3 B3 A4 B4
CIN
COUT
C1
Σ1 Σ2 Σ3 Σ4
Σ1 Σ2 C2 Σ10
LS11420S

a. 3-Bit Adder

b. 2-Bit and 1-Bit Adders


I1 I2 L I3 I4 I5
A1 B1 A2 B2 A3 B3 A4 B4
CIN
COUT
Σ1 Σ2 Σ3 Σ4
2^0 2^1 2^2
LS11450S
I1 I2 I3 I4 I5
A1 B1 A2 B2 A3 B3 A4 B4
CIN
COUT
Σ1 Σ2 Σ3 Σ4
M5
LS11430S

c. 5-Input Encoder

d. 5-Input Majority Gate

Figure 1

ABSOLUTE MAXIMUM RATINGS

(Operating beyond the limits set forth in this table may impair th useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	–0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature range	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			–18	V
I_{OH}	High-level output current			–1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX V_{IH} = MIN	±10% V_{CC}	2.5			V
				±5% V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OL} = MAX V_{IH} = MIN	±10% V_{CC}		0.35	0.50	V
				±5% V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	$A_1 - A_4$, $B_1 - B_4$	V_{CC} = MAX, V_I = 0.5V				-1.2	mA
		C_{IN}					-0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current		V_{CC} = MAX			36	55	mA

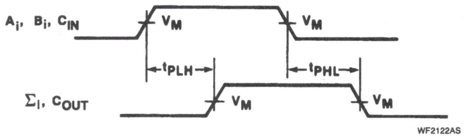
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value under the recommended operating conditions for the applicable conditions.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} should be performed last.

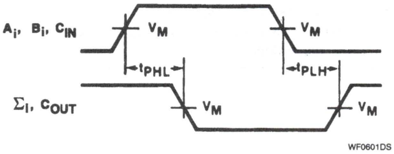
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			$T_A = +25°C$ $V_{CC} = 5.0V$ $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$, $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay C_{IN} to Σ_i	Waveform 1, 2	3.5 4.0	7.0 7.0	9.5 9.5	3.0 3.5	10.5 10.5	ns
t_{PLH} t_{PHL}	Propagation delay A_i or B_i to Σ_i	Waveform 1, 2	3.5 3.5	7.0 7.0	9.5 9.5	2.5 3.5	10.5 10.5	ns
t_{PLH} t_{PHL}	Propagation delay C_{IN} to C_{OUT}	Waveform 2	3.5 3.0	5.7 5.4	7.5 7.0	3.5 2.5	8.5 8.0	ns
t_{PLH} t_{PHL}	Propagation delay A_i or B_i to C_{OUT}	Waveform 1, 2	3.5 2.5	5.7 5.3	7.5 7.0	3.0 2.5	8.5 8.0	ns

AC WAVEFORMS


A_i, B_i, C_{IN}
V_M
V_M
t_{PLH}
t_{PHL}
Σ_i, C_{OUT}
V_M
V_M
WF2122AS

Waveform 1. Propagation Delay Operands and Carry Inputs to Outputs

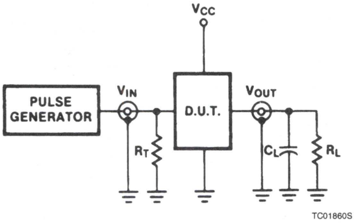

A_i, B_i, C_{IN}
V_M
V_M
t_{PHL}
t_{PLH}
Σ_i, C_{OUT}
V_M
V_M
WF0601DS

Waveform 2. Propagation Delay Operands and Carry Inputs to Outputs

NOTE: $V_M = 1.5V$.

4-Bit Adder FAST 74F83

TEST CIRCUIT AND WAVEFORMS


VCC
PULSE GENERATOR
VIN
D.U.T.
VOUT
RT
CL
RL
TC01860S

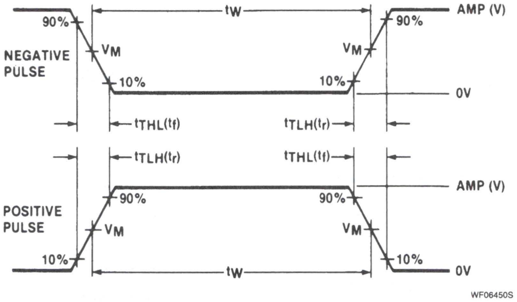
Test Circuit for Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.


NEGATIVE PULSE
90%
VM
10%
tW
AMP (V)
0V
tTHL(tf)
tTLH(tr)
POSITIVE PULSE
tTLH(tr)
tTHL(tf)
90%
VM
10%
tW
AMP (V)
0V
WF06450S

V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F85
Comparator

4-Bit Magnitude Comparator
Product Specification

FAST Products

FEATURES

- **High-impedance NPN base inputs for reduced loading (20μA in High and Low states)**
- **Magnitude comparison of any binary words**
- **Serial or parallel expansion without extra gating**

DESCRIPTION

The 'F85 is a 4-bit magnitude comparator that can be expanded to almost any length. It compares two 4-bit binary, BCD, or other monotonic codes and presents the three possible magnitude results at the outputs. The 4-bit inputs are weighted ($A_0 \rightarrow A_3$) and ($B_0 \rightarrow B_3$), where A_3 and B_3 are the most significant bits.

The operation of the 'F85 is described in the Function Table, showing all possible logic conditions. The upper part of the table describes the normal operation under all conditions that will occur in a single device or in a series expansion scheme. In the upper part of the table the three outputs are mutually exclusive. In the lower part of the table, the outputs reflect the feed-forward conditions that exist in the parallel expansion scheme.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F85	7.0ns	40mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
16-Pin Plastic DIP	N74F85N
16-Pin Plastic SOL	N74F85D

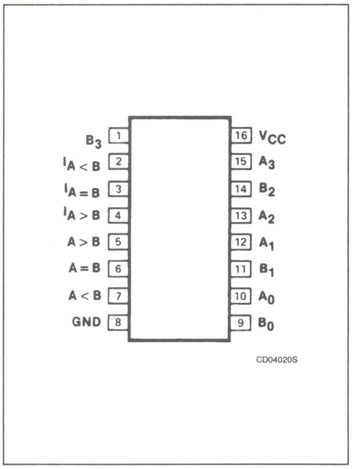
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$A_0 - A_3$	Comparing Inputs	1.0/0.033	20μA/20μA
$B_0 - B_3$	Comparing Inputs	1.0/0.033	20μA/20μA
$I_{A<B}$, $I_{A=B}$ $I_{A>B}$	Expansion Inputs	1.0/0.033	20μA/20μA
A > B, A = B A < B	Data Outputs	50/33	1.0mA/20mA

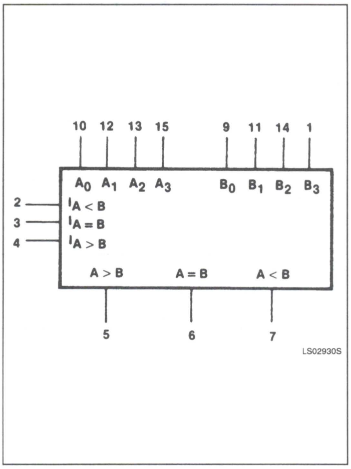
NOTE:

1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

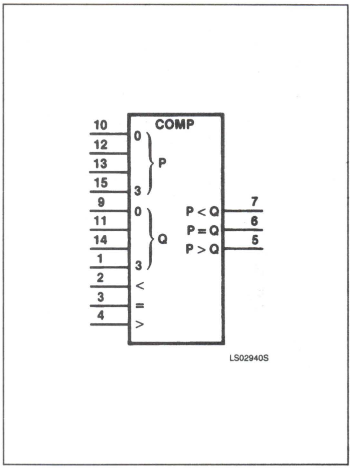
PIN CONFIGURATION


B3 1
IA<B 2
IA=B 3
IA>B 4
A>B 5
A=B 6
A<B 7
GND 8
16 VCC
15 A3
14 B2
13 A2
12 A1
11 B1
10 A0
9 B0
CD04020S

LOGIC SYMBOL


10 12 13 15
9 11 14 1
A0 A1 A2 A3
B0 B1 B2 B3
2 IA<B
3 IA=B
4 IA>B
A>B
A=B
A<B
5
6
7
LS02930S

LOGIC SYMBOL (IEEE/IEC)

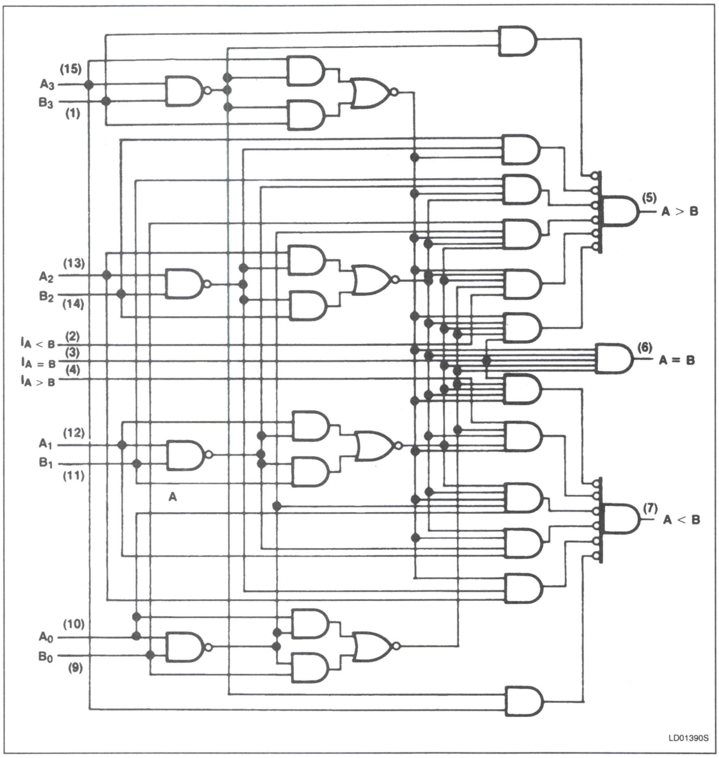

COMP
10
12
13
15
0
P
3
9
11
14
1
0
Q
3
2 <
3 =
4 >
P<Q 7
P=Q 6
P>Q 5
LS02940S

Comparator

FAST 74F85

The expansion inputs $I_{A>B}$, $I_{A=B}$, and $I_{A<B}$ are the least significant bit positions. When used for series expansion, the A > B, A = B and A < B outputs of the least significant word are connected to the corresponding $I_{A>B}$, $I_{A=B}$, and $I_{A<B}$ inputs of the next higher stage. Stages can be added in this manner to any length, but a propagation delay penalty of about 15ns is added with each additional stage. For proper operation the expansion inputs of the least significant word should be tied as follows: $I_{A>B}$ = Low, $I_{A=B}$ = High, and $I_{A<B}$ = Low.

LOGIC DIAGRAM


(15)
A_3
B_3
(1)
(13)
A_2
B_2
(14)
$I_{A<B}$ (2)
$I_{A=B}$ (3)
$I_{A>B}$ (4)
(12)
A_1
B_1
(11)
A
(10)
A_0
B_0
(9)
(5) A > B
(6) A = B
(7) A < B
LD01390S

FUNCTION TABLE

COMPARING INPUTS				EXPANSION INPUTS			OUTPUTS		
A_3, B_3	A_2, B_2	A_1, B_1	A_0, B_0	$I_{A>B}$	$I_{A<B}$	$I_{A=B}$	A > B	A < B	A = B
$A_3 > B_3$	X	X	X	X	X	X	H	L	L
$A_3 < B_3$	X	X	X	X	X	X	L	H	L
$A_3 = B_3$	$A_2 > B_2$	X	X	X	X	X	H	L	L
$A_3 = B_3$	$A_2 < B_2$	X	X	X	X	X	L	H	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 > B_1$	X	X	X	X	H	L	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 < B_1$	X	X	X	X	L	H	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 > B_0$	X	X	X	H	L	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 < B_0$	X	X	X	L	H	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	H	L	L	H	L	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	L	H	L	L	H	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	L	L	H	L	L	H
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	X	X	H	L	L	H
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	H	H	L	L	L	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	L	L	L	H	H	L

H = High voltage level
L = Low voltage level
X = Don't care

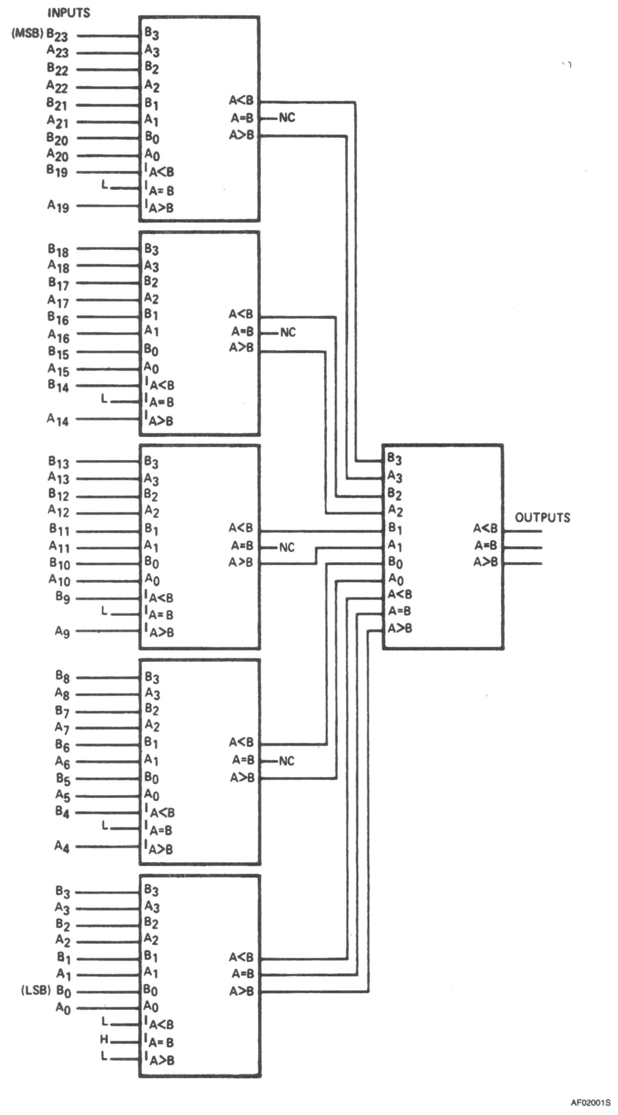

INPUTS
(MSB) B23
A23
B22
A22
B21
A21
B20
A20
B19
L
A19
B18
A18
B17
A17
B16
A16
B15
A15
B14
A14
B13
A13
B12
A12
B11
A11
B10
A10
B9
A9
B8
A8
B7
A7
B6
A6
B5
A5
B4
A4
B3
A3
B2
A2
B1
A1
(LSB) B0
A0
H
B3
A3
B2
A2
B1
A1
B0
A0
IA<B
IA=B
IA>B
A<B
A=B
A>B
NC
OUTPUTS
AF02001S

Figure 1. Comparison Of Two 24-Bit Words

The parallel expansion scheme shown in Figure 1 demonstrates the most efficient general use of these comparators. In the parallel expansion scheme, the expansion inputs can be used as a fifth input bit position except on the least significant device which must be connected as in the serial scheme. The expansion inputs are used by labeling $I_{A>B}$ as an "A" input, $I_{A<B}$ as a "B" input and setting $I_{A=B}$ Low. The 'F85 can be used as a 5-bit comparator only when the outputs are used to drive the ($A_0 - A_3$) and ($B_0 - B_3$) inputs of another 'F85 device. The parallel technique can be expanded to any number of bits as shown in Table 1.

Table 1

WORD LENGTH	NUMBER OF PACKAGES	TYPICAL SPEEDS 74F
1 – 4 Bits	1	12ns
5 – 25 Bits	2 – 6	22ns
25 – 120 Bits	8 – 31	34ns

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			+0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		74F85			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX V_{IH} = MIN,	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OL} = MAX V_{IH} = MIN,	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = 0.0V, V_I = 7.0V				100	μA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				−20	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_{IN} = GND		36	50	mA
		I_{CCL}		$A_n = B_n = I_{A-B}$ = GND, $I_{A>B} = I_{A<B}$ = 4.5V		40	54	mA

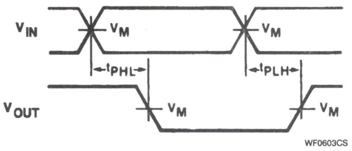
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F85					UNIT
			T_A = +25°C V_{CC} = +5.0V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A or B input to A < B, A > B output	Waveform 1 3 logic levels	6.0 7.0	8.5 9.5	11.0 14.0	5.5 6.5	13.0 15.5	ns
t_{PLH} t_{PHL}	Propagation delay A or B input to A = B output	Waveform 1 4 logic levels	6.5 7.0	9.0 9.5	11.5 14.0	6.0 6.5	14.0 14.5	ns
t_{PLH} t_{PHL}	Propagation delay $I_{A<B}$ and $I_{A=B}$ input to A > B output	Waveform 1 1 logic level	3.0 3.0	5.0 6.0	7.5 9.0	2.5 2.5	9.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay $I_{A=B}$ input to A = B output	Waveform 1 2 logic levels	2.5 3.5	4.5 7.5	7.0 10.0	2.0 2.5	9.0 12.0	ns
t_{PLH} t_{PHL}	Propagation delay $I_{A>B}$ and $I_{A=B}$ input to A < B output	Waveform 1 1 logic level	3.0 3.0	5.0 6.0	8.0 9.0	3.0 2.0	9.5 9.5	ns

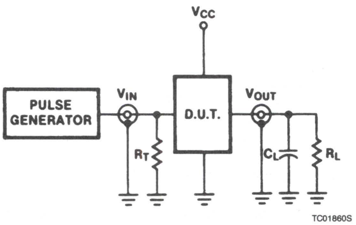
AC WAVEFORM


VIN
VM
VM
tPHL
tPLH
VOUT
VM
VM
WF0603CS

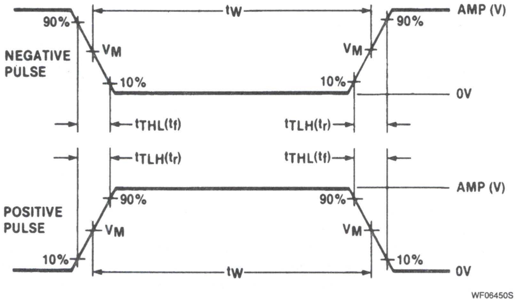
NOTE: For all waveforms, $V_M = 1.5V$.

Waveform 1. Propagation Delay Input to Output

TEST CIRCUIT AND WAVEFORM


VCC
PULSE GENERATOR
VIN
D.U.T.
VOUT
RT
CL
RL
TC01860S

Test Circuit for Totem-Pole Outputs


90%
tW
AMP (V)
90%
NEGATIVE PULSE
VM
VM
10%
10%
0V
tTHL(tf)
tTLH(tr)
tTLH(tr)
tTHL(tf)
AMP (V)
90%
90%
POSITIVE PULSE
VM
VM
10%
10%
tW
0V
WF06450S

$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS

R_L = Load resistor to GND; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F86
Gate

Quad Two-Input Exclusive-OR Gate
Product Specification

FAST Products

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

H = High voltage level
L = Low voltage level

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F86	4.3ns	16.5mA

ORDERING INFORMATION

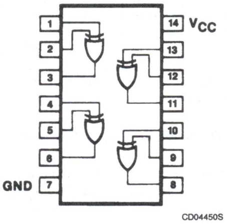
PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
14-Pin Plastic DIP	N74F86N
14-Pin Plastic SO	N74F86D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A, B	Inputs	1.0/1.0	20μA/0.6mA
Y	Output	50/33	1.0mA/20mA

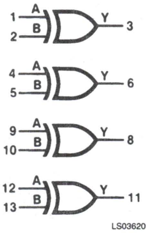
NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



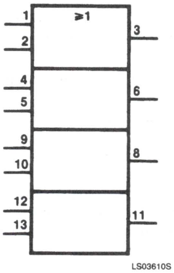
1
2
3
4
5
6
GND 7
14 VCC
13
12
11
10
9
8
CD04450S

LOGIC SYMBOL



1 A
2 B
Y 3
4 A
5 B
Y 6
9 A
10 B
Y 8
12 A
13 B
Y 11
LS03620S

LOGIC SYMBOL (IEEE/IEC)



≥1
1
2
3
4
5
6
9
10
8
12
13
11
LS03610S

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	05.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX V_{IH} = MIN,	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OL} = MAX V_{IH} = MIN,	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				−0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	A = GND B = 4.5V		15	23	mA
		I_{CCL}		V_{IN} = 4.5V		18	28	mA

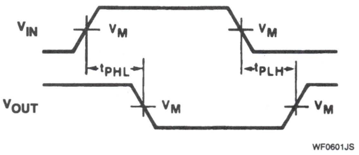
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

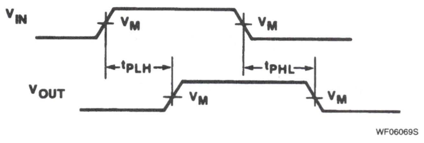
SYMBOL	PARAMETER	TEST CONDITIONS	74F86					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A or B to Y	Other input Low Waveform 2	3.0 3.0	4.0 4.2	5.5 5.5	3.0 3.0	6.5 6.5	ns
t_{PLH} t_{PHL}	Propagation delay A or B to Y	Other input High Waveform 1	3.5 3.0	5.3 4.7	7.0 6.5	3.5 3.0	8.0 7.5	ns

AC WAVEFORMS



V_IN
V_M
V_M
t_PHL
t_PLH
V_OUT
V_M
V_M
WF0601JS

Waveform 1. For Inverting Outputs

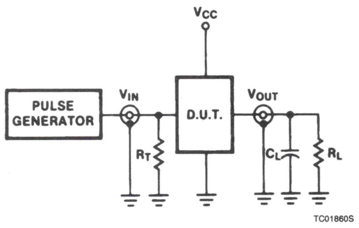


V_IN
V_M
V_M
t_PLH
t_PHL
V_OUT
V_M
V_M
WF06069S

Waveform 2. For Non-Inverting Outputs

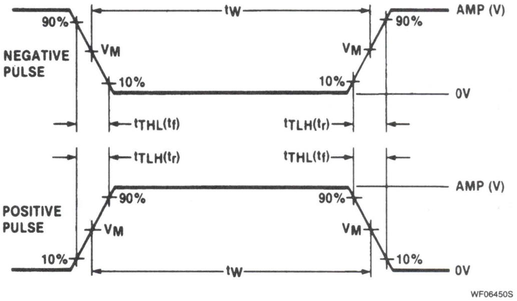
NOTE: For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORM



V_CC
PULSE GENERATOR
V_IN
D.U.T.
V_OUT
R_T
C_L
R_L
TC01860S

Test Circuit for Totem-Pole Outputs



NEGATIVE PULSE
90%
V_M
10%
tw
90%
V_M
10%
AMP (V)
0V
t_THL(t_f)
t_TLH(t_r)
t_TLH(t_r)
t_THL(t_f)
POSITIVE PULSE
90%
V_M
10%
90%
V_M
10%
tw
AMP (V)
0V
WF06450S

$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS
R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST Products

FAST 74F109
Flip-Flop

Dual J-$\overline{K}$ Positive Edge-Triggered Flip-Flop
Product Specification

DESCRIPTION

The 'F109 is a dual positive edge-triggered J$\overline{K}$-type flip-flop featuring individual J, $\overline{K}$, Clock, Set and Reset inputs, and complementary $\overline{Q}$ outputs.

Set ($\overline{S}_D$) and Reset ($\overline{R}_D$) are asynchronous active-Low inputs and operate independently of the Clock input.

The J and $\overline{K}$ are edge-triggered inputs which control the state changes of the flip-flops as described in the Function Table. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition of the positive-going pulse.

The J and $\overline{K}$ inputs must be stable just one set-up time prior to the Low-to-High transition of the Clock for predictable operation. The J$\overline{K}$ design allows operation as a D flip-flop by tying the J and $\overline{K}$ inputs together.

Although the Clock input is level sensitive, the positive transition of the Clock pulse between the 0.8V and 2.0V levels should be equal to or less than the Clock to output delay time for reliable operation.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F109	125MHz	12.3mA

ORDERING INFORMATION

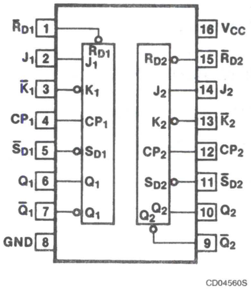
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F109N
16-Pin Plastic SO	N74F109D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

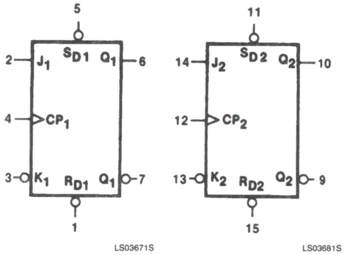
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
J_1, J_2, $\overline{K}_1$, $\overline{K}_2$	Data inputs	1.0/1.0	20μA/0.6mA
CP_1, CP_2	Clock Pulse inputs (active rising edge)	1.0/1.0	20μA/0.6mA
$\overline{R}_{D1}$, $\overline{R}_{D2}$	Reset inputs (active-Low)	1.0/3.0	20μA/1.8mA
$\overline{S}_{D1}$, $\overline{S}_{D2}$	Set inputs (active-Low)	1.0/3.0	20μA/1.8mA
Q_1, Q_2, $\overline{Q}_1$, $\overline{Q}_2$	Outputs	50/33	1.0mA/20mA

NOTE:
1. One (1.0) FAST Unit Load (U.L.) is defined as: 20μA in the High state and 0.6mA in the Low state.

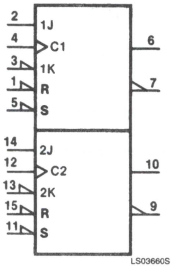
PIN CONFIGURATION


R̄D1 1
J1 2
K̄1 3
CP1 4
S̄D1 5
Q1 6
Q̄1 7
GND 8
16 VCC
15 R̄D2
14 J2
13 K̄2
12 CP2
11 S̄D2
10 Q2
9 Q̄2
R̄D1
J1
K1
CP1
SD1
Q1
Q1
RD2
J2
K2
CP2
SD2
Q2
Q2
CD04560S

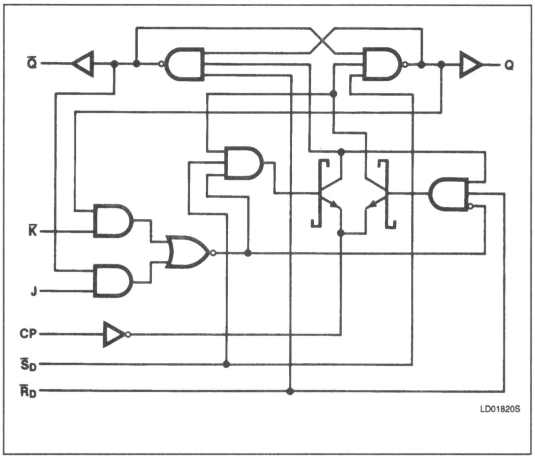
LOGIC SYMBOL


5
2
J1
SD1
Q1
6
4
CP1
3
K1
RD1
Q1
7
1
LS03671S
11
14
J2
SD2
Q2
10
12
CP2
13
K2
RD2
Q2
9
15
LS03681S

LOGIC SYMBOL (IEEE/IEC)


2
1J
4
C1
3
1K
1
R
5
S
6
7
14
2J
12
C2
13
2K
15
R
11
S
10
9
LS03660S

LOGIC DIAGRAM



FUNCTION TABLE

OPERATING MODE	INPUTS					OUTPUTS	
	$\overline{S}_D$	$\overline{R}_D$	CP	J	$\overline{K}$	Q	$\overline{Q}$
Asynchronous Set	L	H	X	X	X	H	L
Asynchronous Reset (Clear)	H	L	X	X	X	L	H
Undetermined (Note)	L	L	X	X	X	H	H
Toggle	H	H	↑	h	l	$\overline{q}$	q
Load "0" (Reset)	H	H	↑	l	l	L	H
Load "1" (Set)	H	H	↑	h	h	H	L
Hold "no change"	H	H	↑	l	h	q	$\overline{q}$

H = High voltage level steady state.
L = Low voltage level steady state.
h = High voltage level one set-up time prior to the Low-to-High Clock transition.
l = Low voltage level one set-up time prior to the Low-to-High Clock transition.
X = Don't care.
q = Lower case letters indicate the state of the referenced output prior to the Low-to-High Clock transition.
↑ = Low-to-High Clock transition.

NOTE:
Both outputs will be High if both $\overline{S}_D$ and $\overline{R}_D$ go Low simultaneously.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		74F109			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX V_{IH} = MIN,	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OL} = MAX V_{IH} = MIN,	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	High-level input current	J, $\overline{K}$, CP inputs	V_{CC} = MAX, V_I = 2.7V				20	μA
		$\overline{S}_D$, $\overline{R}_D$ inputs					20	μA
I_{IL}	Low-level input current	J, $\overline{K}$, CP inputs	V_{CC} = MAX, V_I = 2.7V				−0.6	mA
		$\overline{S}_D$, $\overline{R}_D$ inputs					−1.8	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current[4] (total)		V_{CC} = MAX			12.3	17	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. With the Clock input grounded and all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs High in turn.

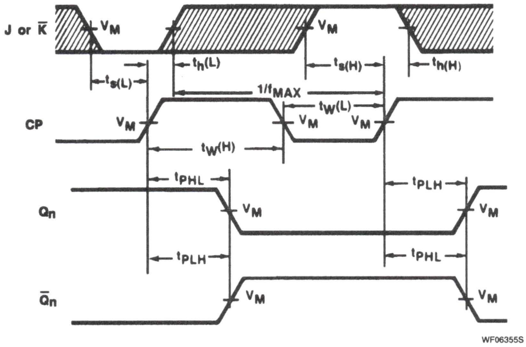
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F109					UNIT
			T_A = +25°C V_{CC} = +5.0V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	90	125		90		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n, $\overline{Q}_n$	Waveform 1	3.8 4.4	5.3 6.2	7.0 8.0	3.8 4.4	8.0 9.2	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{S}_{Dn}$ or $\overline{R}_{Dn}$ to Q_n, $\overline{Q}_n$	Waveform 2	3.2 3.5	5.2 7.0	7.0 9.0	3.2 3.5	8.0 10.5	ns

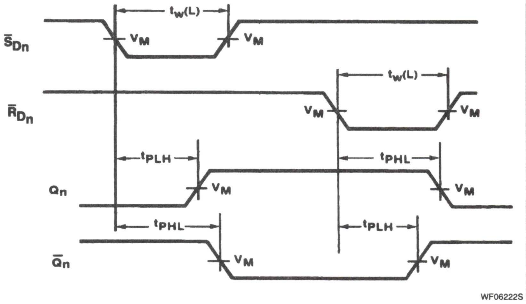
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	74F109					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Set-up time High or Low, J or $\overline{K}$ to CP	Waveform 1	3.0 3.0			3.0 3.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low, J or $\overline{K}$ to CP	Waveform 1	1.0 1.0			1.0 1.0		ns
$t_w(H)$ $t_w(L)$	Clock pulse width, High or Low	Waveform 1	4.0 5.0			4.0 5.0		ns
$t_w(L)$	Set or Reset pulse width, Low	Waveform 2	4.0			4.0		ns
t_{rec}	Recovery time, Set or Reset to clock	Waveform 3	2.0			2.0		ns

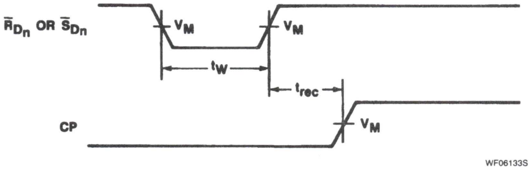
AC WAVEFORMS


J or K̄
V_M
t_s(L)
t_h(L)
t_s(H)
t_h(H)
1/f_MAX
CP
t_w(L)
t_w(H)
t_PHL
t_PLH
Q_n
Q̄_n
WF06355S

Waveform 1. Clock to Output Delays, Data Set-up and Hold Times, Clock Pulse Width


S̄_Dn
R̄_Dn
t_w(L)
V_M
t_PLH
t_PHL
Q_n
Q̄_n
WF06222S

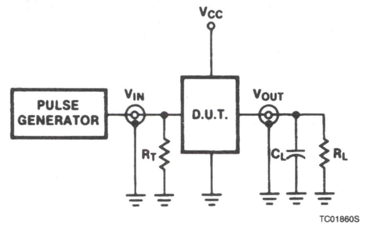
Waveform 2. Set and Reset to Output Delays, Set and Reset Pulse Widths


R̄_Dn OR S̄_Dn
V_M
t_w
t_rec
CP
WF06133S

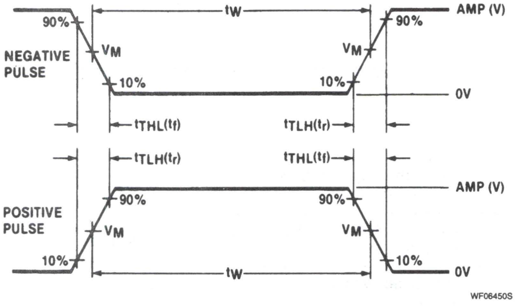
Waveform 3. Recovery Time

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORM


V_{CC}
PULSE GENERATOR
V_{IN}
D.U.T.
V_{OUT}
R_T
C_L
R_L
TC01860S

Test Circuit for Totem-Pole Outputs


90%
tW
AMP (V)
NEGATIVE PULSE
VM
10%
0V
$t_{THL}(t_f)$
$t_{TLH}(t_r)$
POSITIVE PULSE
WF06450S

V_M = 1.5V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F112
Flip-Flop

Dual J-K Negative Edge-Triggered Flip-Flop
Product Specification

FAST Products

DESCRIPTION

The 'F112 is a dual J-K negative edge-triggered flip-flop featuring individual J, K, Clock, Set and Reset inputs. The Set ($\overline{S}_D$) and Reset ($\overline{R}_D$) inputs, when Low, set or reset the outputs as shown in the Function Table regardless of the levels at the other inputs.

A High level on the Clock ($\overline{CP}$) input enables the J and K inputs and data will be accepted. The logic levels at the J and K inputs may be allowed to change while the $\overline{CP}$ is High and the flip-flop will perform according to the Function Table as long as minimum setup and hold times are observed. Output state changes are initiated by the High-to-Low transition of $\overline{CP}$.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F112	100MHz	15mA

ORDERING INFORMATION

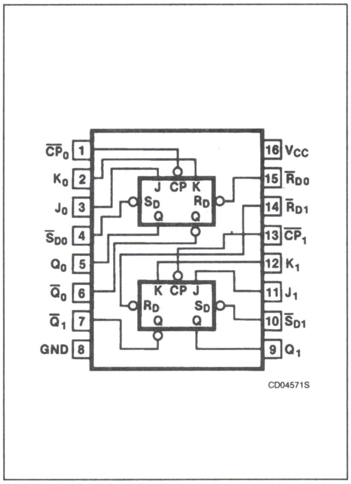
PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
16-Pin Plastic DIP	N74F112N
16-Pin Plastic SO	N74F112D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

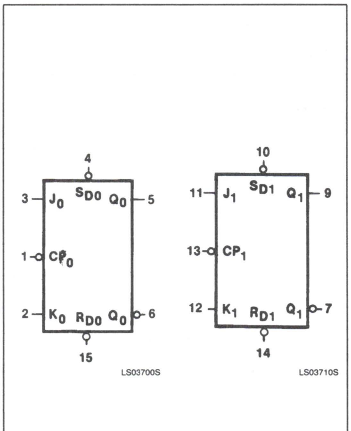
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$\overline{CP}_0$, $\overline{CP}_1$	Clock inputs (Active falling edge)	1.0/4.0	20μA/2.4mA
$\overline{S}_{D0}$, $\overline{S}_{D1}$	Set inputs (active-Low)	1.0/5.0	20μA/3.0mA
$\overline{R}_{D0}$, $\overline{R}_{D1}$	Reset inputs (active-Low)	1.0/5.0	20μA/3.0mA
J_0, J_1	J inputs	1.0/1.0	20μA/0.6mA
K_0, K_1	K inputs (active-Low)	1.0/1.0	20μA/0.6mA
Q_0, $\overline{Q}_0$, Q_1, $\overline{Q}_1$	Data outputs	50/33	1.0mA/20mA

NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION

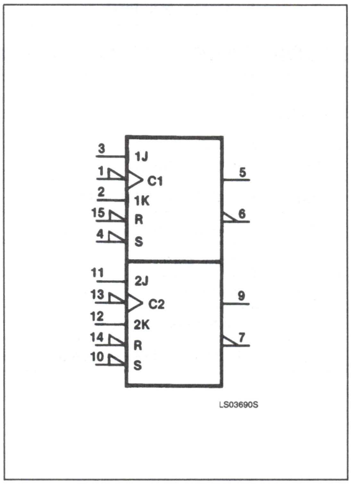

CP̄0 1
K0 2
J0 3
S̄D0 4
Q0 5
Q̄0 6
Q̄1 7
GND 8
16 VCC
15 R̄D0
14 R̄D1
13 CP̄1
12 K1
11 J1
10 S̄D1
9 Q1
J CP K
SD RD
Q Q
K CP J
RD SD
Q Q
CD04571S

LOGIC SYMBOL


4
3
J0
SD0
Q0
5
1
CP0
2
K0
RD0
Q0
6
15
LS03700S
10
11
J1
SD1
Q1
9
13
CP1
12
K1
RD1
Q1
7
14
LS03710S

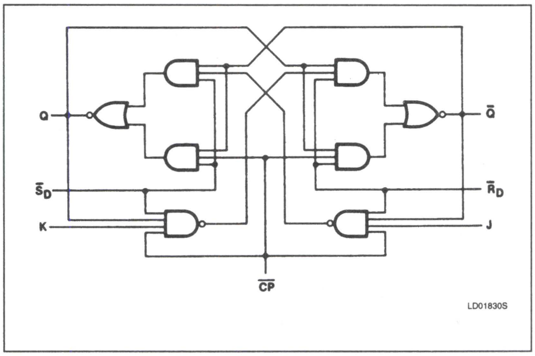
V_{CC} = Pin 16
GND = Pin 8

LOGIC SYMBOL (IEEE/IEC)


3
1J
1
C1
2
1K
15
R
4
S
5
6
11
2J
13
C2
12
2K
14
R
10
S
9
7
LS03690S

Flip-Flop FAST 74F112

LOGIC DIAGRAM



FUNCTION TABLE

OPERATING MODE	INPUTS					OUTPUTS	
	$\overline{S}_D$	$\overline{R}_D$	$\overline{CP}$	J	K	Q	$\overline{Q}$
Asynchronous set	L	H	X	X	X	H	L
Asynchronous reset (clear)	H	L	X	X	X	L	H
Undetermined*	L	L	X	X	X	H*	H*
Toggle	H	H	↓	h	h	$\overline{q}$	q
Load "0" (reset)	H	H	↓	l	h	L	H
Load "1" (set)	H	H	↓	h	l	H	L
Hold "no change"	H	H	↓	l	l	q	$\overline{q}$
Hold "no change"	H	H	H	X	X	Q	$\overline{Q}$

H = High voltage level steady state.
h = High voltage level one setup time prior to the High-to-Low Clock transition.
L = Low voltage level steady state.
l = Low voltage level one setup time prior to the High-to-Low Clock transition.
q = Lower case letters indicate the state of the referenced output one setup time prior to the High-to-Low Clock transition.
X = Don't care.
↓ = High-to-Low Clock transition.

Undetermined* = Both outputs will be High while both $\overline{S}_D$ and $\overline{R}_D$ are Low, but the output states are unpredictable if $\overline{S}_D$ and $\overline{R}_D$ go High simultaneously.

Asynchronous inputs: Low input to $\overline{S}_D$ sets Q to High level
Low input to $\overline{R}_D$ sets Q to Low level
Reset and Set are independent of clock
Simultaneous Low on both $\overline{S}_D$ and $\overline{R}_D$ makes both Q and $\overline{Q}$ High.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5.0	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−1.0	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		74F112			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX V_{IH} = MIN,	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OL} = MAX V_{IH} = MIN,	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	μA
							100	μA
							100	μA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	μA
							20	μA
							20	μA
I_{IL}	Low-level input current	J_n, K_n	V_{CC} = MAX, V_I = 0.5V				−0.6	mA
		$\overline{CP}$					−2.4	mA
		$\overline{S}_{Dn}$, $\overline{R}_{Dn}$					−3.0	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current[4] (total)		V_{CC} = MAX			15	21	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. With the Clock input grounded and all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs High in turn.

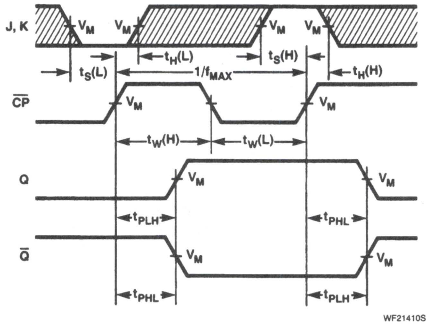
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F112					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum Clock frequency	Waveform 1	85	100		80		MHz
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}_n$ to Q_n, $\overline{Q}_n$	Waveform 1	2.0 2.0	5.0 5.0	6.5 6.5	2.0 2.0	7.5 7.5	ns
t_{PLH} t_{PHL}	Propagation delay S_{Dn} or R_{Dn} to Q_n, $\overline{Q}_n$	Waveform 2, 3	2.0 2.0	4.5 4.5	6.5 6.5	2.0 2.0	7.5 7.5	ns

AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	74F112					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low J_n or K_n to $\overline{CP}_n$	Waveform 1	4.0 3.5			5.0 4.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low J_n or K_n to $\overline{CP}_n$	Waveform 1	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	$\overline{CP}_n$ pulse width	Waveform 1	4.5 4.5			5.0 5.0		ns
$t_w(L)$	$\overline{S}_{Dn}$ or $\overline{R}_{Dn}$ pulse width Low	Waveform 2, 3	4.5			5.0		ns
t_{rec}	Recovery time $\overline{S}_{Dn}$ or $\overline{R}_{Dn}$ to $\overline{CP}$	Waveform 2, 3	4.0			5.0		ns

AC WAVEFORMS

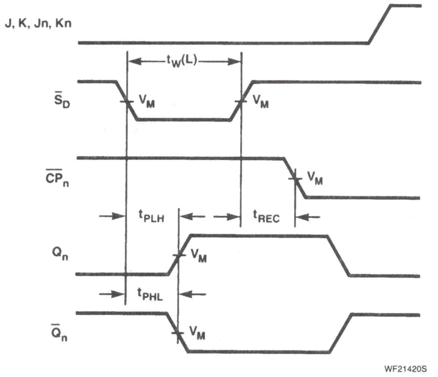


Waveform 1. Propagation Delay for Data to Output, Data Setup Time and Hold Times, and Clock Widths

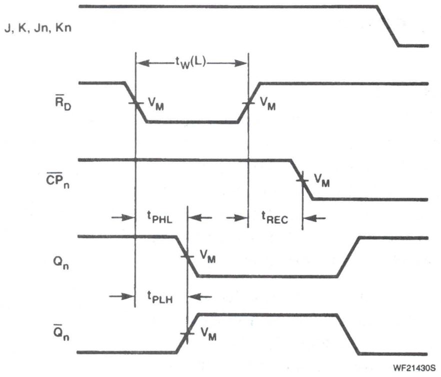
NOTE: $V_M = 1.5V$.

The shaded areas indicated when the input is permitted to change for predictable output performance.

AC WAVEFORMS


J, K, Jn, Kn
tW(L)
S̄D
VM
VM
C̄P̄n
VM
tPLH
tREC
Qn
VM
tPHL
Q̄n
VM
WF21420S

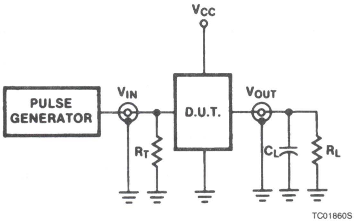
Waveform 2. Propagation Delay for Set to Output, Set Pulse Width, and Recovery Time for Set to Clock


J, K, Jn, Kn
tW(L)
R̄D
VM
VM
C̄P̄n
VM
tPHL
tREC
Qn
VM
tPLH
Q̄n
VM
WF21430S

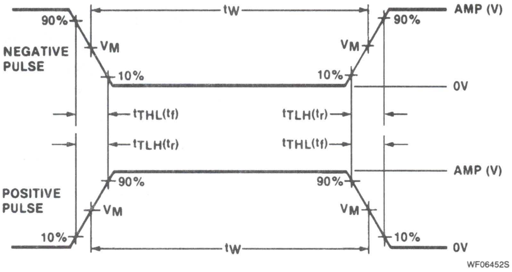
Waveform 3. Propagation Delay for Reset to Output, Reset Pulse Width, and Recovery Time for Reset to Clock

NOTE: $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORMS


VCC
PULSE GENERATOR
VIN
D.U.T.
VOUT
RT
CL
RL
TC01860S

Test Circuit for Totem-Pole Outputs


tW
90%
90%
AMP (V)
NEGATIVE PULSE
VM
VM
10%
10%
0V
tTHL(tf)
tTLH(tr)
tTLH(tr)
tTHL(tf)
AMP (V)
90%
90%
POSITIVE PULSE
VM
VM
10%
10%
0V
tW
WF06452S

$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS

R_L = Load resistor to GND; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F113
Flip-Flop

Dual J-K Negative Edge-Triggered Flip-Flop Without Reset
Product Specification

FAST Products

DESCRIPTION

The 'F113 is a dual J-K negative edge-triggered flip-flop featuring individual J, K, Set and Clock inputs. The asynchronous Set ($\overline{S}_D$) input, when Low, forces the outputs to the steady state levels as shown in the Function Table regardless of the levels at the other inputs.

A High level on the Clock ($\overline{CP}$) input enables the J and K inputs and data will be accepted. The logic levels at the J and K inputs may be allowed to change while the $\overline{CP}$ is High and the flip-flop will perform according to the Function Table as long as minimum setup and hold times are observed. Output state changes are intitiated by the High-to-Low transition of $\overline{CP}$.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F113	100MHz	15mA

ORDERING INFORMATION

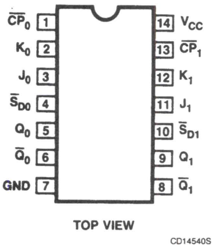
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V± 10%; T_A = 0°C to +70°C
14-Pin Plastic DIP	N74F113N
14-Pin Plastic SO	N74F113D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

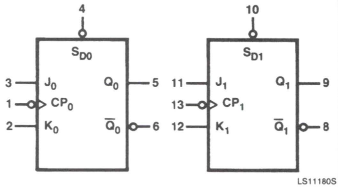
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
J_0, J_1	J inputs	1.0/1.0	20μA/0.6mA
K_0, K_1	K Inputs	1.0/1.0	20μA/0.6mA
$\overline{CP}_0$, $\overline{CP}_1$	Clock inputs (active falling edge)	1.0/4.0	20μA/2.4mA
$\overline{S}_{D0}$, $\overline{S}_{D1}$	Direct set inputs (active-Low)	1.0/5.0	20μA/3.0mA
Q_0, $\overline{Q}_0$, Q_1, $\overline{Q}_1$	Data Outputs	50/33	1.0mA/20mA

NOTE:
1. One (1) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION

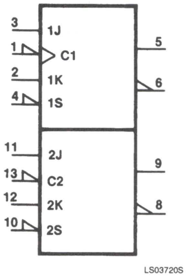

$\overline{CP}_0$ 1
K_0 2
J_0 3
$\overline{S}_{D0}$ 4
Q_0 5
$\overline{Q}_0$ 6
GND 7
14 V_{CC}
13 $\overline{CP}_1$
12 K_1
11 J_1
10 $\overline{S}_{D1}$
9 Q_1
8 $\overline{Q}_1$
TOP VIEW
CD14540S

LOGIC SYMBOL


4
S_{D0}
3 J_0
1 CP_0
2 K_0
Q_0 5
$\overline{Q}_0$ 6
10
S_{D1}
11 J_1
13 CP_1
12 K_1
Q_1 9
$\overline{Q}_1$ 8
LS11180S

V_{CC} = Pin 14
GND = Pin 7

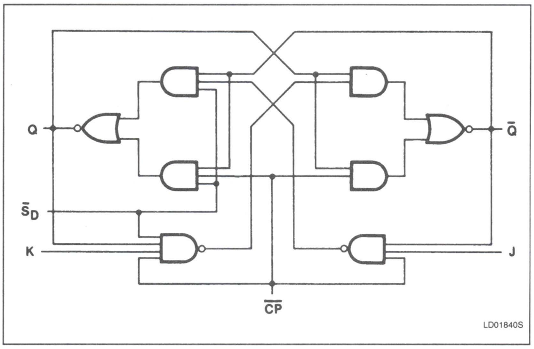
LOGIC SYMBOL (IEEE/IEC)


3 1J
1 C1
2 1K
4 1S
5
6
11 2J
13 C2
12 2K
10 2S
9
8
LS03720S

Flip-Flop

FAST 74F113

LOGIC DIAGRAM



FUNCTION TABLE

OPERATING MODE	INPUTS				OUTPUTS	
	$\overline{S}_D$	$\overline{CP}$	J	K	Q	$\overline{Q}$
Asynchronous Set	L	X	X	X	H	L
Toggle	H	↓	h	h	$\overline{q}$	q
Load "0" (Reset)	H	↓	l	h	L	H
Load "1" (Set)	H	↓	h	l	H	L
Hold "no change"	H	↓	l	l	q	$\overline{q}$

H = High voltage level steady state.
h = High voltage level one setup time prior to the High-to-Low Clock transition.
L = Low voltage level steady state.
l = Low voltage level one setup time prior to the High-to-Low Clock transition.
q = Lower case letters indicate the state of the referenced output one setup time prior to the High-to-Low Clock transition.
X = Don't care.
↓ = High-to-Low Clock transition.
Asynchronous input:
Low input to $\overline{S}_D$ sets Q to High level
Set is independent of clock

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			+0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX V_{IH} = MIN	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OL} = MAX V_{IH} = MIN	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	μA
							100	μA
							100	μA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	μA
							20	μA
							20	μA
I_{IL}	Low-level input current	J, K	V_{CC} = MAX, V_I = 0.5V				−0.6	mA
		$\overline{CP}_n$					−2.4	mA
		$\overline{S}_{Dn}$					−3.0	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current[4] (total)		V_{CC} = MAX			15	21	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of High-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. With the Clock input grounded and all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs High in turn.

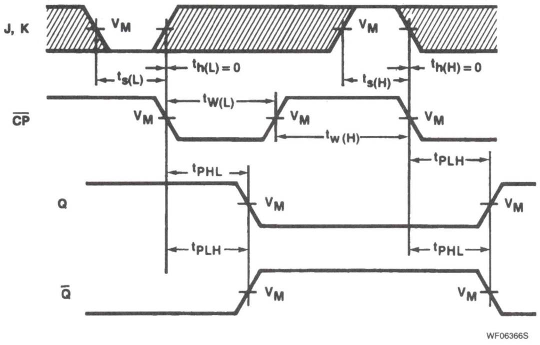
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C V_{CC} = +5.0V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = +5.0V± 10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	110	125		100		MHz
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}_n$ to Q_n, $\overline{Q}_n$	Waveform 1	2.0 2.0	4.0 4.0	6.0 6.0	2.0 2.0	7.0 7.0	ns
t_{PLH} t_{PHL}	Propagation delay S_{Dn} to Q_n, $\overline{Q}_n$	Waveform 2	2.0 2.0	4.5 4.5	6.5 6.5	2.0 2.0	7.5 7.5	ns

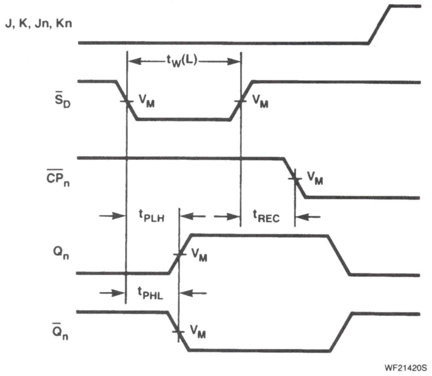
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low J_n or K_n to $\overline{CP}_n$	Waveform 1	4.0 3.0			5.0 4.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low J_n or K_n to $\overline{CP}_n$	Waveform 1	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	$\overline{CP}_n$ pulse width	Waveform 1	4.5 4.5			5.0 5.0		ns
$t_w(L)$	SD_n pulse width	Waveform 2	4.5			5.0		ns
t_{rec}	$\overline{SD}_n$ to $\overline{CP}_n$	Waveform 2	4.5			5.0		ns

AC WAVEFORMS


J, K
VM
VM
th(L) = 0
ts(L)
ts(H)
th(H) = 0
CP
tW(L)
VM
VM
VM
tw (H)
tPHL
tPLH
Q
VM
VM
tPLH
tPHL
Q̄
VM
VM
WF06366S

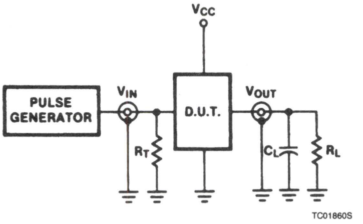
Waveform 1. Clock to Output Delays, Data Setup and Hold Times, Clock Pulse Width


J, K, Jn, Kn
tw(L)
S̄D
VM
VM
CPn
VM
tPLH
tREC
Qn
VM
tPHL
Q̄n
VM
WF21420S

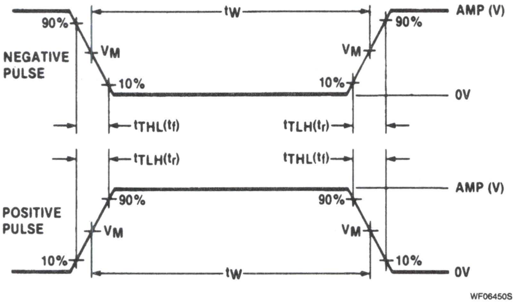
Waveform 2. Propagation Delay for Set to Output, Set Pulse Width, and Recovery Time for Set to Clock

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS


VCC
PULSE GENERATOR
VIN
D.U.T.
VOUT
RT
CL
RL
TC01860S

Test Circuit for Totem-Pole Outputs


AMP (V)
90%
tW
NEGATIVE PULSE
VM
10%
0V
tTHL(tf)
tTLH(tr)
POSITIVE PULSE
WF06450S

V_M = 1.5V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST Products

FAST 74F114
Flip-Flop

Dual J-K Negative Edge-Triggered Flip-Flop
(With Common Clock and Reset)
Product Specification

DESCRIPTION

The 'F114 is a Dual JK Negative Edge-Triggered Flip-Flop featuring individual J, K, and Set inputs and common Clock and Reset inputs. The Set ($\overline{S}_D$) and Reset ($\overline{R}_D$) inputs, when Low, set or reset the outputs as shown in the Function Table, regardless of the levels at the other inputs.

A High level on the Clock ($\overline{CP}$) input enables the J and K inputs and data will be accepted. The logic levels at the J and K inputs may be allowed to change while the $\overline{CP}$ is High and the flip-flop will perform according to the Function Table as long as minimum setup and hold times are observed. Output state changes are initiated by the High-to-Low transition of $\overline{CP}$.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F114	100	15mA

ORDERING INFORMATION

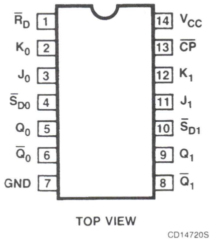
PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
14-Pin Plastic DIP	N74F114N
14-Pin Plastic SO	N74F114D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
J_0, J_1,	J inputs	1.0/1.0	20μA/0.6mA
K_0, K_1	K inputs	1.0/1.0	20μA/0.6mA
$\overline{CP}$	Clock pulse input (active falling edge)	1.0/8.0	20μA/4.8mA
$\overline{R}_D$	Direct clear input (active-Low)	1.0/10	20μA/6.0mA
$\overline{S}_{D0}$, $\overline{S}_{D1}$	Direct set inputs (active-Low)	1.0/5.0	20μA/3.0mA
Q_0, $\overline{Q}_0$, Q_1, $\overline{Q}_1$	Outputs	50/33	1.0mA/20mA

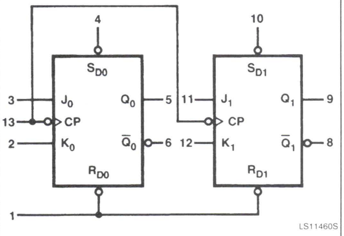
NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



$\overline{R}_D$ 1
K_0 2
J_0 3
$\overline{S}_{D0}$ 4
Q_0 5
$\overline{Q}_0$ 6
GND 7
14 V_{CC}
13 $\overline{CP}$
12 K_1
11 J_1
10 $\overline{S}_{D1}$
9 Q_1
8 $\overline{Q}_1$
TOP VIEW
CD14720S

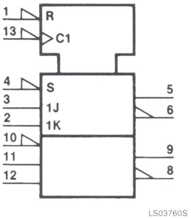
LOGIC SYMBOL



4
10
S_{D0}
S_{D1}
3
13
2
J_0
CP
K_0
Q_0
$\overline{Q}_0$
5
6
11
12
J_1
CP
K_1
Q_1
$\overline{Q}_1$
9
8
R_{D0}
R_{D1}
1
LS11460S

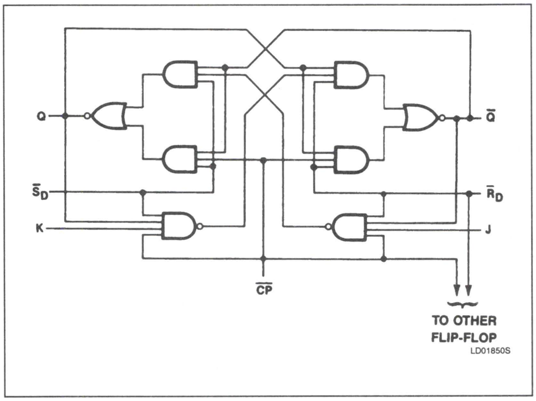
V_{CC} = Pin 14
GND = Pin 7

LOGIC SYMBOL (IEEE/IEC)



1
13
R
C1
4
3
2
S
1J
1K
10
11
12
5
6
9
8
LS03760S

LOGIC DIAGRAM



FUNCTION TABLE

OPERATING MODE	INPUTS					OUTPUTS	
	$\overline{S}_D$	$\overline{R}_D$	$\overline{CP}$	J	K	Q	$\overline{Q}$
Asynchronous Set	L	H	X	X	X	H	L
Asynchronous Reset (Clear)	H	L	X	X	X	L	H
Undetermined	L	L	X	X	X	H	H
Toggle	H	H	↓	h	h	$\overline{q}$	q
Load "0" (Reset)	H	H	↓	l	h	L	H
Load "1" (Set)	H	H	↓	h	l	H	L
Hold "no change"	H	H	↓	l	l	q	$\overline{q}$

H = High voltage level steady state.
h = High voltage level one setup time prior to the High-to-Low Clock transition.
L = Low voltage level steady state.
l = Low voltage level one setup time prior to the High-to-Low Clock transition.
q = Lower case letters indicate the state of the referenced output one setup time prior to the High-to-Low Clock transition.
X = Don't care.
Asynchronous inputs:
Low input to $\overline{S}_D$ sets Q to High level
Low input to $\overline{C}_D$ sets Q to Low level
Clear and Set are independent of clock
Simultaneous Low on $\overline{C}_D$ and $\overline{S}_D$ makes both Q and $\overline{Q}$ High
Undetermined* : Both outputs will be High while both $\overline{S}_D$ and R_D are Low, but the output states are unpredictable if $\overline{S}_D$ and R_D go High simultaneously.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX V_{IH} = MIN,	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OL} = MAX V_{IH} = MIN,	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current	J, K	V_{CC} = MAX, V_I = 0.5V				-0.6	mA
		$\overline{CP}$					-4.8	mA
		$\overline{S}_D$					-3.0	mA
		$\overline{R}_D$					-6.0	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current[4] (total)		V_{CC} = MAX			15	21	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of High-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. With the Clock input grounded and all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs High in turn.

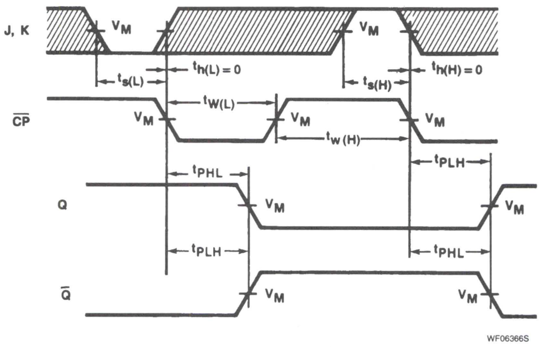
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C V_{CC} = +5.0V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = +5.0V±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	110	125		90		MHz
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}$ to Q_n, $\overline{Q}_n$	Waveform 1	3.0 3.0	5.0 5.5	6.5 7.5	3.0 3.0	7.5 8.5	ns
t_{PLH} t_{PHL}	Propagation delay SD_n or RD_n to Q_n, $\overline{Q}_n$	Waveform 2	3.0 3.0	4.5 4.5	6.5 6.5	3.0 3.0	7.5 7.5	ns

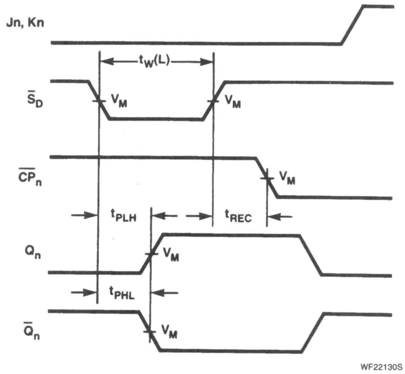
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low J_n or K_n to $\overline{CP}_n$	Waveform 1	4.0 3.5			5.0 4.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low J_n or K_n to $\overline{CP}_n$	Waveform 1	0 0			0 0		ns
$t_W(H)$ $t_w(L)$	$\overline{CP}_n$ pulse width	Waveform 1	4.5 4.5			5.0 5.0		ns
$t_w(L)$	SD_n or RD pulse width	Waveform 2	4.5			5.0		ns
t_{rec}	Recovery time $\overline{S}_{Dn}$ or $\overline{R}_D$ to $\overline{CP}$	Waveform 2, 3	4.5			5.0		ns

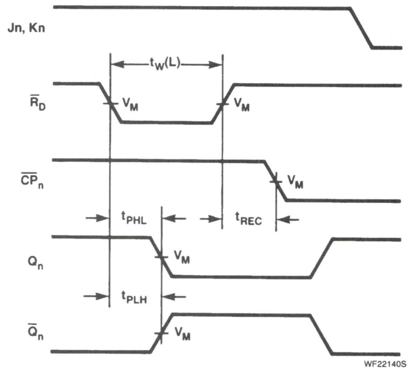
AC WAVEFORMS


J, K
V_M
$t_{s(L)}$
$t_{h(L)} = 0$
$t_{s(H)}$
$t_{h(H)} = 0$
$\overline{CP}$
$t_{W(L)}$
$t_{w(H)}$
t_{PHL}
t_{PLH}
Q
$\overline{Q}$
WF06366S

Waveform 1. Clock to Output Delays, Data Setup and Hold Times, Clock Pulse Width


Jn, Kn
$t_{w(L)}$
$\overline{S}_D$
V_M
$\overline{CP}_n$
t_{PLH}
t_{REC}
Q_n
t_{PHL}
$\overline{Q}_n$
WF22130S

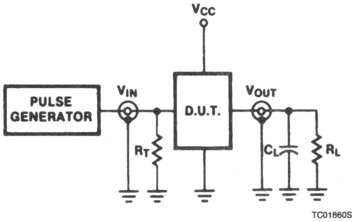
Waveform 2. Propagation Delay for Set to Output, Set Pulse Width, and Recovery time for Set to Clock


Jn, Kn
$t_{w(L)}$
$\overline{R}_D$
V_M
$\overline{CP}_n$
t_{PHL}
t_{REC}
Q_n
t_{PLH}
$\overline{Q}_n$
WF22140S

Waveform 3. Propagation Delay for Reset to Output, Reset Pulse Width, and Recovery Time for Reset to Clock

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS


VCC
PULSE GENERATOR
VIN
D.U.T.
VOUT
RT
CL
RL
TC01860S

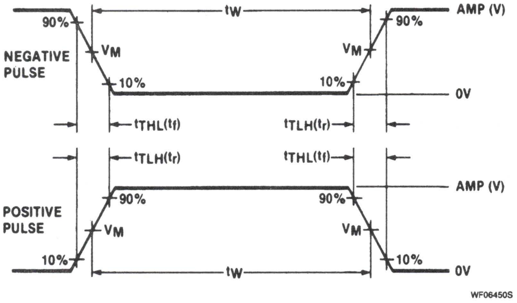
Test Circuit for Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.


NEGATIVE PULSE
POSITIVE PULSE
90%
10%
VM
tW
AMP (V)
0V
tTHL(tf)
tTLH(tr)
WF06450S

V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	**Rep. Rate**	**Pulse Width**	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F125, 74F126
Buffer

Quad Buffers (3-State)
Product Specification

FAST Products

FEATURES

- **High-impedance NPN base inputs for reduced loading (20µA in High and Low states)**

FUNCTION TABLE 'F125

INPUTS		OUTPUT
$\overline{C}$	A	Y
L	L	L
L	H	H
H	X	(Z)

FUNCTION TABLE 'F126

INPUTS		OUTPUT
C	A	Y
H	L	L
H	H	H
L	X	Z

H = High voltage level
L = Low voltage level
X = Don't care

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F125	5.0ns	23mA
74F126	5.0ns	26mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
14-Pin Plastic DIP	N74F125N, N74F126N
14-Pin Plastic SO	N74F125D, N74F126D

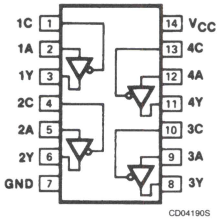
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
1A – 4A	Data inputs	1.0/0.033	20µA/20µA
$\overline{1C}$ – $\overline{4C}$	3-State output enable input (active-Low) 'F125	1.0/0.033	20µA/20µA
1C – 4C	3-State output enable input (active-High) 'F126	1.0/0.033	20µA/20µA
1Y – 4Y	Data outputs	750/106.7	15mA/64mA

NOTE:
1. One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

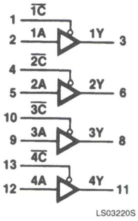
PIN CONFIGURATION

'F125


1C 1
1A 2
1Y 3
2C 4
2A 5
2Y 6
GND 7
14 V_{CC}
13 4C
12 4A
11 4Y
10 3C
9 3A
8 3Y
CD04190S

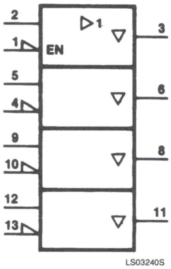
LOGIC SYMBOL

'F125


$\overline{1C}$
1
1A
2
1Y
3
$\overline{2C}$
4
2A
5
2Y
6
$\overline{3C}$
10
3A
9
3Y
8
$\overline{4C}$
13
4A
12
4Y
11
LS03220S

LOGIC SYMBOL (IEEE/IEC)

'F125

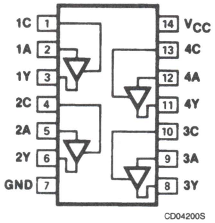

2
1
▷1
EN
3
5
4
6
9
10
8
12
13
11
LS03240S

Buffer

FAST 74F125, 74F126

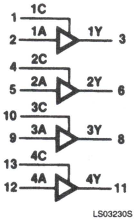
PIN CONFIGURATION

'F126


1C 1
1A 2
1Y 3
2C 4
2A 5
2Y 6
GND 7
14 V_{CC}
13 4C
12 4A
11 4Y
10 3C
9 3A
8 3Y
CD04200S

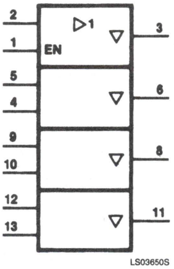
LOGIC SYMBOL

'F126


1 1C
2 1A
1Y 3
4 2C
5 2A
2Y 6
10 3C
9 3A
3Y 8
13 4C
12 4A
4Y 11
LS03230S

LOGIC SYMBOL (IEEE/IEC)

'F126


2
1
EN
▷1
3
5
4
6
9
10
8
12
13
11
LS03650S

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	–0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	128	mA
T_A	Operating free-air temperature range	0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			–18	mA
I_{OH}	High-level output current			–15	mA
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]			74F125, 74F126			UNIT
							Min	Typ[2]	Max	
V_{OH}	High-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = −3mA	±10%V_{CC}	2.4			V
						±5%V_{CC}	2.7	3.4		V
					I_{OH} = −15mA	±10%V_{CC}	2.0			V
						±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 48mA	±10%V_{CC}		0.35	0.50	V
					I_{OL} = 64mA	±5%V_{CC}		0.40	0.55	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, $I_I = I_{IK}$				−0.73	−1.2	V
I_I	Input current at maximum input voltage			V_{CC} = 0.0V, V_I = 7.0V					100	μA
I_{IH}	High-level input current			V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	Low-level input current			V_{CC} = MAX, V_I = 0.5V					−20	μA
I_{OZH}	Off-state output current, High-level voltage applied			V_{CC} = MAX, V_O = 2.7V					50	μA
I_{OZL}	Off-state output current, Low-level voltage applied			V_{CC} = MAX, V_O = 0.5V					−50	μA
I_{OS}	Short-circuit output current[3]			V_{CC} = MAX			−100		−225	mA
I_{CC}	Supply current (total)	'F125	I_{CCH}	V_{CC} = MAX	$\overline{nC}$ = GND, nA = 4.5V			17	24	mA
			I_{CCL}		$\overline{nC}$ = nA = GND			28	40	mA
			I_{CCZ}		$\overline{nC}$ = nA = 4.5V			25	35	mA
		'F126	I_{CCH}		nC = nA = 4.5V			20	30	mA
			I_{CCL}		nC = 4.5V, nA = GND			32	48	mA
			I_{CCZ}		nC = GND, nA = 4.5V			26	39	mA

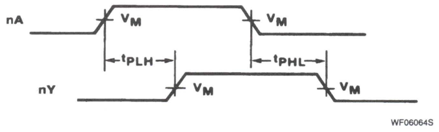
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

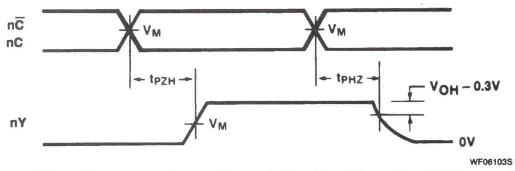
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	74F125, 74F126					UNIT
				T_A = +25°C V_{CC} = +5.0V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF R_L = 500Ω		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA to nY	'F125	Waveform 1	2.0 3.0	4.0 5.5	6.0 7.5	2.0 3.0	6.5 8.0	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level		Waveform 2 Waveform 3	3.5 4.0	5.5 6.0	7.5 8.0	3.5 4.0	8.5 9.0	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level		Waveform 2 Waveform 3	1.5 1.5	3.5 3.5	5.0 5.5	1.5 1.5	6.0 6.0	ns
t_{PLH} t_{PHL}	Propagation delay nA to nY	'F126	Waveform 1	2.0 3.0	4.0 5.5	6.5 8.0	2.0 3.0	7.0 8.5	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level		Waveform 2 Waveform 3	4.0 4.0	6.0 6.0	7.5 8.0	3.5 3.5	8.5 8.5	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level		Waveform 2 Waveform 3	2.0 3.0	4.5 5.5	6.5 7.5	2.0 3.0	7.5 8.0	ns

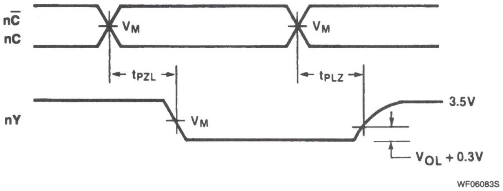
AC WAVEFORMS


nA
VM
VM
tPLH
tPHL
nY
VM
VM
WF06064S

Waveform 1. Propagation Delay For Input To Output


nC̄
nC
VM
VM
tPZH
tPHZ
VOH − 0.3V
nY
VM
0V
WF06103S

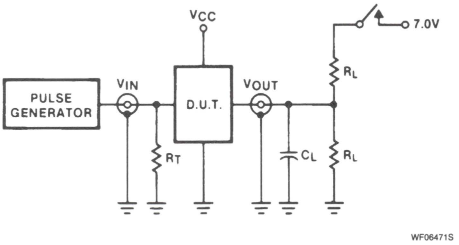
Waveform 2. 3-State Output Enable Time To High Level And Output Disable Time From High Level


nC̄
nC
VM
VM
tPZL
tPLZ
nY
VM
3.5V
VOL + 0.3V
WF06083S

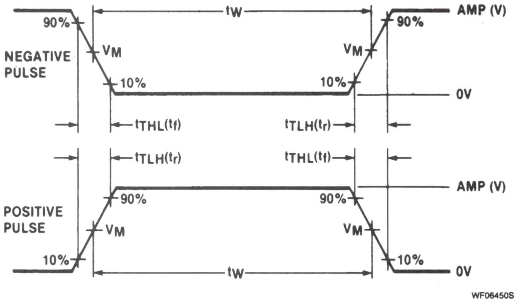
Waveform 3. 3-State Output Enable Time to Low Level and Output Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORM


VCC
7.0V
RL
PULSE GENERATOR
VIN
D.U.T.
VOUT
RT
CL
RL
WF06471S

Test Circuit for 3-State Outputs


90%
tW
90%
AMP (V)
NEGATIVE PULSE
VM
VM
10%
10%
0V
tTHL(tf)
tTLH(tr)
tTLH(tr)
tTHL(tf)
AMP (V)
90%
90%
POSITIVE PULSE
VM
VM
10%
10%
tW
0V
WF06450S

$V_M = 1.5V$

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor to GND; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F132
Schmitt Trigger

Quad 2-Input NAND Schmitt Trigger
Product Specification

FAST Products

DESCRIPTION

The 'F132 contains four 2-input NAND gates which accept standard TTL input signals and provide standard TTL output levels. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. In addition, they have greater noise margin than conventional NAND gates.

Each circuit contains a 2-input Schmitt trigger followed by a Darlington level shifter and a phase splitter driving a TTL totem-pole output. The Schmitt trigger uses positive feedback to effectively speed-up slow input transitions, and provide different input threshold voltages for positive and negative-going transitions. This hysteresis between the positive-going and negative-going input threshold (typically 800mV) is determined by resistor ratios and is essentially insensitive to temperature and supply voltage variations. As long as three inputs remain at a more positive voltage than V_{T+MAX}, the gate will respond in the transitions of the other input as shown in Waveform 1.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F132	6.3ns	13mA

ORDERING INFORMATION

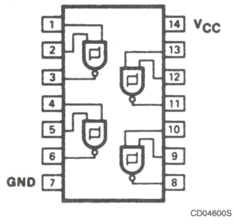
PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
14-Pin Plastic DIP	N74F132N
14-Pin Plastic SO	N74F132D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

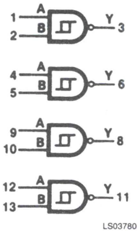
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A, B	Inputs	1.0/1.0	20µA/0.6mA
$\overline{Y}$	Output	50/33	1.0mA/20mA

NOTE:
1. One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

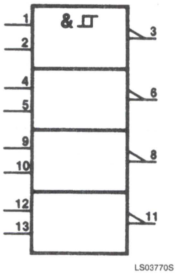
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Schmitt Trigger

FAST 74F132

FUNCTION TABLE

INPUTS		OUTPUT
A	B	$\overline{Y}$
L	L	H
L	H	H
H	L	H
H	H	L

H = High voltage level
L = Low voltage level

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		74F132			UNIT
					Min	Typ[2]	Max	
V_{T+}	Positive-going threshold		$V_{CC} = 5.0V$		1.5	1.7	2.0	V
V_{T-}	Negative-going threshold		$V_{CC} = 5.0V$		0.7	0.9	1.1	V
ΔV_T	Hysteresis ($V_{T+} - V_{T-}$)		$V_{CC} = 5.0V$		0.4	0.8		V
V_{OH}	High-level output voltage		V_{CC} = MIN, $V_I = V_{T-MIN}$, I_{OH} = MAX	± 10%V_{CC}	2.5			V
				± 5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, $V_I = V_{T+MAX}$, I_{OL} = MAX	± 10%V_{CC}		0.35	0.50	V
				± 5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$			−0.73	−1.2	V
I_{T+}	Input current at positive-going threshold		$V_{CC} = 5.0V$, $V_I = V_{T+}$			0.0		μA
I_{T-}	Input current at negative-going threshold		$V_{CC} = 5.0V$, $V_I = V_{T-}$			−350		μA
I_I	Input current at maximum input voltage		V_{CC} = MAX, $V_I = 7.0V$				100	μA
I_{IH}	High-level input current		V_{CC} = MAX, $V_I = 2.7V$				20	μA
I_{IL}	Low-level input current		V_{CC} = MAX, $V_I = 0.5V$				−0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_{IN} = GND		8.5	12	mA
		I_{CCL}		V_{IN} = 4.5V		13.0	19.5	mA

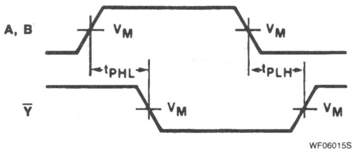
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at $V_{CC} = 5V$, $T_A = 25°C$.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F132					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH}	Propagation delay A, B to $\overline{Y}$	Waveform 1	4.0	5.5	7.0	3.5	8.5	ns
t_{PHL}			5.5	7.0	8.5	5	9.0	

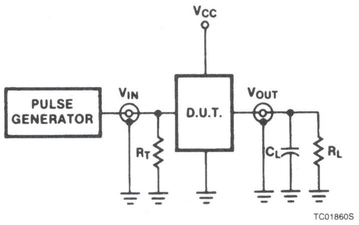
AC WAVEFORM


A, B
V_M
V_M
t_{PHL}
t_{PLH}
$\overline{Y}$
V_M
V_M
WF06015S

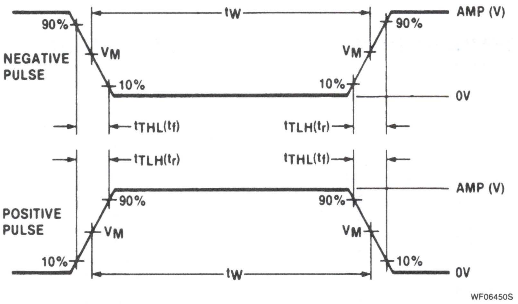
NOTE: For all waveforms, $V_M = 1.5V$.

Waveform 1. For Inverting Outputs

TEST CIRCUIT AND WAVEFORM


V_{CC}
PULSE GENERATOR
V_{IN}
D.U.T.
V_{OUT}
R_T
C_L
R_L
TC01860S

Test Circuit for Totem-Pole Outputs


t_W
90%
AMP (V)
NEGATIVE PULSE
V_M
V_M
90%
10%
10%
0V
$t_{THL}(t_f)$
$t_{TLH}(t_r)$
$t_{TLH}(t_r)$
$t_{THL}(t_f)$
AMP (V)
90%
90%
POSITIVE PULSE
V_M
V_M
10%
10%
0V
t_W
WF06450S

$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST Products

FAST 74F133
13-Input NAND Gate

Product Specification

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F133	4ns	2mA

ORDERING INFORMATION

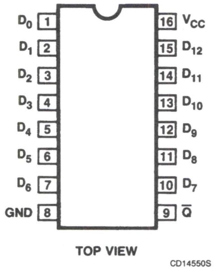
PACKAGE	COMMERCIAL RANGE V_{CC} = 5V± 10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	74F133N
16-Pin Plastic SOL	74F133D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

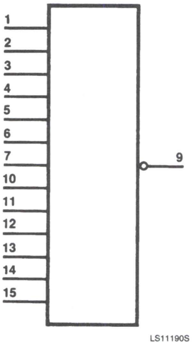
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$D_0 - D_{14}$	Data inputs	1.0/1.0	20μA/0.6mA
$\overline{Q}$	Data output	50/33.3	1mA/20mA

NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION

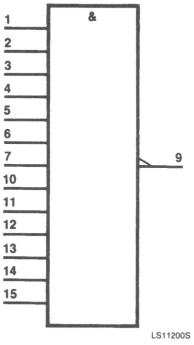

D_0 1
D_1 2
D_2 3
D_3 4
D_4 5
D_5 6
D_6 7
GND 8
16 V_{CC}
15 D_{12}
14 D_{11}
13 D_{10}
12 D_9
11 D_8
10 D_7
9 $\overline{Q}$
TOP VIEW
CD14550S

LOGIC SYMBOL


1
2
3
4
5
6
7
10
11
12
13
14
15
9
LS11190S

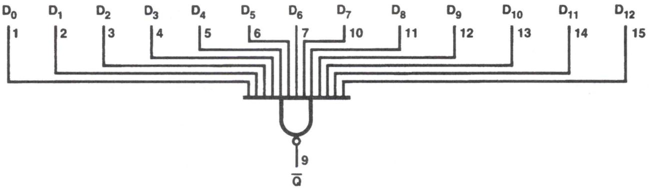
V_{CC} = Pin 16
GND = Pin 8

LOGIC SYMBOL (IEEE/IEC)


&
1
2
3
4
5
6
7
10
11
12
13
14
15
9
LS11200S

13-Input NAND Gate FAST 74F133

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8

FUNCTION TABLE

OUTPUT	INPUTS												
$\overline{Q}$	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_8	D_9	D_{10}	D_{11}	D_{12}
L	H	H	H	H	H	H	H	H	H	H	H	H	H
H	Any one input = L												

NOTES:
H = High voltage level
L = Low voltage level

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = MAX	±10% V_{CC}	2.5			V
					±5% V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = MAX	±10% V_{CC}		0.35	0.50	V
					±5% V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$				−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V					100	μA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					−0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX			−60		−150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				1.0	2.0	mA
		I_{CCL}					2.5	4.0	mA

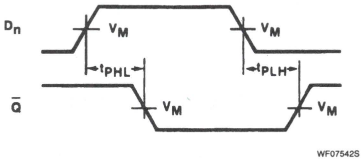
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value under the recommended operating conditions for the applicable conditions.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F133					UNIT
			$T_A = +25°C$ $V_{CC} = 5.0V$ $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$, $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_n to $\overline{Q}$	Waveform 1	2.0 2.5	4.0 4.5	7.0 7.5	1.5 2.0	7.5 8.0	ns

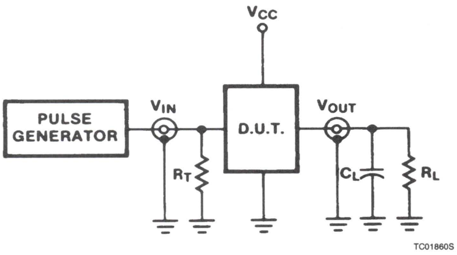
AC WAVEFORMS


D_n
V_M
V_M
t_{PHL}
t_{PLH}
$\overline{Q}$
V_M
V_M
WF07542S

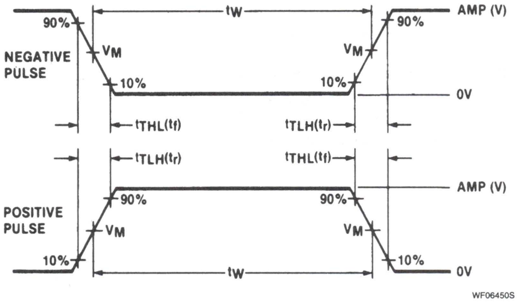
Waveform 1. Propagation Delay for Data to Output

NOTE: $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORMS


V_{CC}
PULSE GENERATOR
V_{IN}
D.U.T.
V_{OUT}
R_T
C_L
R_L
TC01860S

Test Circuit for Totem-Pole Outputs


NEGATIVE PULSE
90%
t_W
90%
AMP (V)
V_M
V_M
10%
10%
0V
$t_{THL}(t_f)$
$t_{TLH}(t_r)$
$t_{TLH}(t_r)$
$t_{THL}(t_f)$
AMP (V)
90%
90%
POSITIVE PULSE
V_M
V_M
10%
10%
0V
t_W
WF06450S

$V_M = 1.5V$

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F138

Decoder/Demultiplexer

1-Of-8 Decoder/Demultiplexer
Product Specification

FAST Products

FEATURES

- **Demultiplexing capability**
- **Multiple input enable for easy expansion**
- **Ideal for memory chip select decoding**
- **High-speed replacement for Intel 3205**

DESCRIPTION

The 'F138 decoder accepts three binary weighted inputs (A_0, A_1, A_2) and when enabled, provides eight mutually exclusive, active-Low outputs ($\overline{Q}_0 - \overline{Q}_7$). The device features three Enable inputs; two active-Low ($\overline{E}_1$, $\overline{E}_2$) and one active-High (E_3). Every output will be High unless $\overline{E}_1$ and $\overline{E}_2$ are Low and E_3 is High. This multiple enable function allows easy parallel expansion of the device to a 1-of-32 (5 lines to 32 lines) decoder with just four 'F138's and one inverter.

The device can be used as an eight output demultiplexer by using one of the active-Low Enable inputs as the Data input and the remaining Enable inputs as strobes. Enable inputs not used must be permanently tied to their appropriate active-High or active-Low state.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F138	5.8ns	13mA

ORDERING INFORMATION

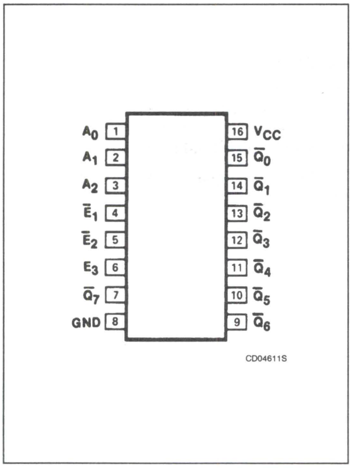
PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
16-Pin Plastic DIP	N74F138N
16-Pin Plastic SO	N74F138D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$A_0 - A_2$	Address inputs	1.0/1.0	20μA/0.6mA
$\overline{E}_1 - \overline{E}_2$	Enable inputs (active-Low)	1.0/1.0	20μA/0.6mA
E_3	Enable input (active-High)	1.0/1.0	20μA/0.6mA
$\overline{Q}_0 - \overline{Q}_7$	Outputs (active-Low)	50/33	1.0mA/20mA

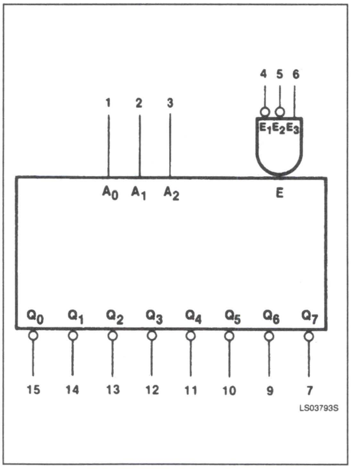
NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



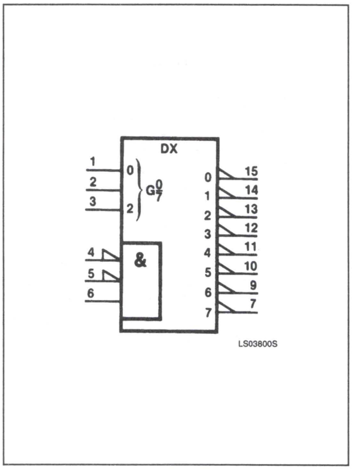
A0 1
A1 2
A2 3
Ē1 4
Ē2 5
E3 6
Q̄7 7
GND 8
16 VCC
15 Q̄0
14 Q̄1
13 Q̄2
12 Q̄3
11 Q̄4
10 Q̄5
9 Q̄6
CD04611S

LOGIC SYMBOL



1
2
3
4 5 6
Ē1Ē2E3
A0 A1 A2
E
Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
15 14 13 12 11 10 9 7
LS03793S

LOGIC SYMBOL (IEEE/IEC)



DX
1
2
3
0
2
G0/7
4
5
6
&
0 15
1 14
2 13
3 12
4 11
5 10
6 9
7 7
LS03800S

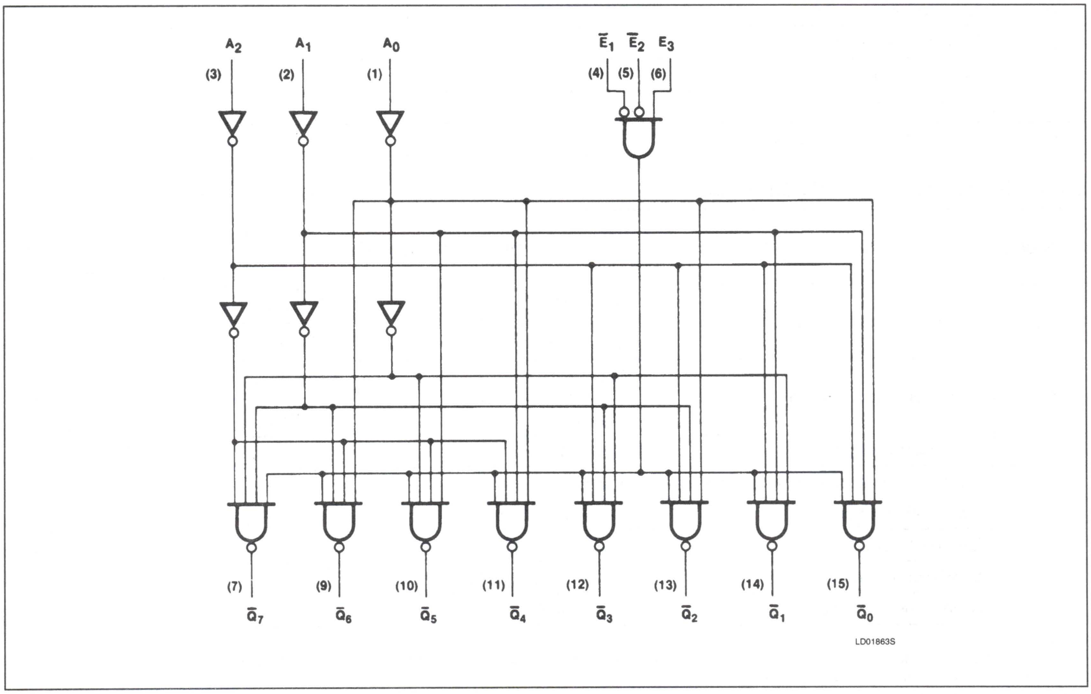
Decoder/Demultiplexer FAST 74F138

FUNCTION TABLE

INPUTS						OUTPUTS							
$\overline{E}_1$	$\overline{E}_2$	E_3	A_0	A_1	A_2	$\overline{Q_0}$	$\overline{Q_1}$	$\overline{Q_2}$	$\overline{Q_3}$	$\overline{Q_4}$	$\overline{Q_5}$	$\overline{Q_6}$	$\overline{Q_7}$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

NOTES:
H = High voltage level
L = Low voltage level
X = Don't care

LOGIC DIAGRAM


A_2
A_1
A_0
(3)
(2)
(1)
$\overline{E}_1$
$\overline{E}_2$
E_3
(4)
(5)
(6)
(7)
(9)
(10)
(11)
(12)
(13)
(14)
(15)
$\overline{Q}_7$
$\overline{Q}_6$
$\overline{Q}_5$
$\overline{Q}_4$
$\overline{Q}_3$
$\overline{Q}_2$
$\overline{Q}_1$
$\overline{Q}_0$
LD01863S

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to $+7.0$	V
V_{IN}	Input voltage	-0.5 to $+7.0$	V
I_{IN}	Input current	-30 to $+5$	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

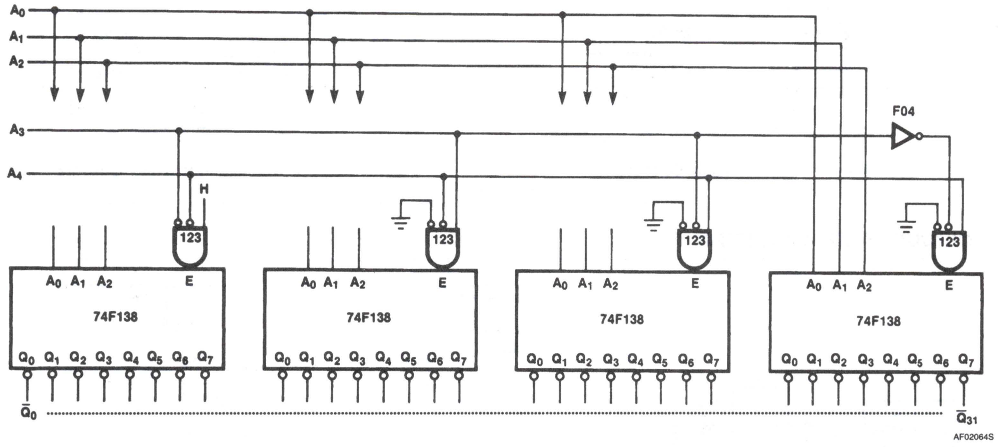
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX V_{IH} = MIN,	$\pm10\%V_{CC}$	2.5			V
			$\pm5\%V_{CC}$	2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, I_{OL} = MAX V_{IH} = MIN,	$\pm10\%V_{CC}$		0.35	0.50	V
			$\pm5\%V_{CC}$		0.35	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, $I_I = I_{IK}$			-0.73	-1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX, V_O = 0.0V		-60		-150	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX			13	20	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. To measure I_{CC}, outputs must be open, V_{IN} on all inputs = 4.5V.

APPLICATION

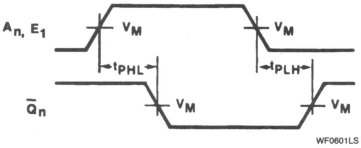

A0
A1
A2
A3
A4
H
F04
123
74F138
A0 A1 A2
E
Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
Q̄0
Q̄31
AF02064S

Expansion to 1-of-32 Decoding

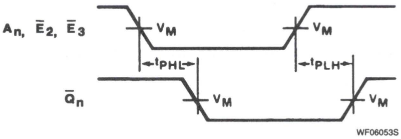
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F138					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay Address to output A_n to $\overline{Q}_n$	Waveforms 1 and 2	3.5 4.0	5.6 6.1	7.0 8.0	3.5 4.0	8.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}_1$ or $\overline{E}_2$ to $\overline{Q}_n$	Waveform 2	3.5 3.0	6.4 5.3	7.0 7.0	3.5 3.0	8.0 7.5	ns
t_{PLH} t_{PHL}	Propagation delay E_3 to $\overline{Q}_n$	Waveform 1	4.0 3.5	8.2 5.6	8.0 7.5	4.0 3.5	9.0 8.5	ns

AC WAVEFORMS


An, E1
VM
VM
tPHL
tPLH
Q̄n
VM
VM
WF0601LS

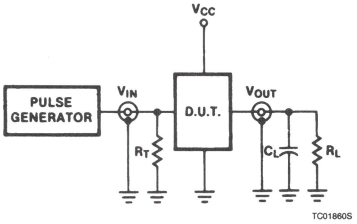
Waveform 1. For Inverting Outputs


An, Ē2, Ē3
VM
VM
tPHL
tPLH
Q̄n
VM
VM
WF06053S

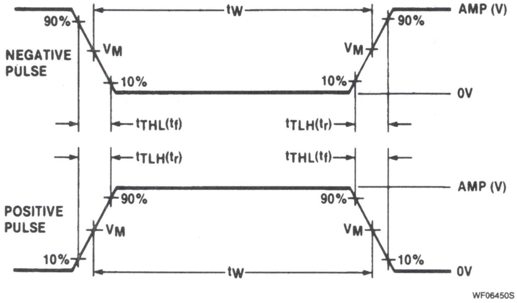
Waveform 2. For Non-Inverting Outputs

NOTE: For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORM


VCC
PULSE GENERATOR
VIN
VOUT
D.U.T.
RT
CL
RL
TC01860S

Test Circuit for Totem-Pole Outputs


tW
90%
VM
10%
NEGATIVE PULSE
AMP (V)
0V
tTHL(tf)
tTLH(tr)
tTLH(tr)
tTHL(tf)
POSITIVE PULSE
90%
VM
10%
AMP (V)
0V
WF06450S

$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F139
Decoder/Demultiplexer

Dual 1-of-4 Decoder/Demultiplexer
Product Specification

FAST Products

FEATURES
- **Demultiplexing capability**
- **Two independent 1-of-4 decoders**
- **Multifunction capability**

DESCRIPTION
The 'F139 is a high-speed, dual 1-of-4 decoder/demultiplexer. This device has two independent decoders, each accepting two binary weighted inputs (A_0, A_1) and providing four mutually exclusive active-Low outputs ($\overline{Q}_{0n}-\overline{Q}_{3n}$). Each decoder has an active-Low Enable ($\overline{E}$). When $\overline{E}$ is High, every output is forced High. The Enable can be used as the Data input for a 1-of-4 demultiplexer application.

FUNCTION TABLE

INPUTS			OUTPUTS			
$\overline{E}$	A_0	A_1	$\overline{Q}_0$	$\overline{Q}_1$	$\overline{Q}_2$	$\overline{Q}_3$
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

H = High voltage level
L = Low voltage level
X = Don't care

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F139	5.3ns	13mA

ORDERING INFORMATION

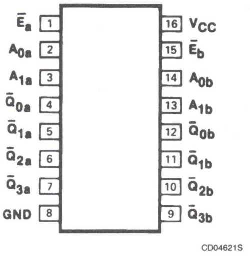
PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
16-Pin Plastic DIP	N74F139N
16-Pin Plastic SO	N74F139D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_{na}, A_{nb}	Address Inputs	1.0/1.0	20μA/0.6mA
$\overline{E}_a$, $\overline{E}_b$	Enable Inputs	1.0/1.0	20μA/0.6mA
$\overline{Q}_{0a}-\overline{Q}_{3a}$, $\overline{Q}_{0b}-\overline{Q}_{3b}$	Outputs	50/33	1.0mA/20mA

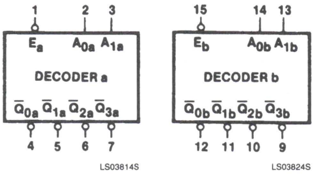
NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



$\overline{E}_a$ 1
A_{0a} 2
A_{1a} 3
$\overline{Q}_{0a}$ 4
$\overline{Q}_{1a}$ 5
$\overline{Q}_{2a}$ 6
$\overline{Q}_{3a}$ 7
GND 8
16 V_{CC}
15 $\overline{E}_b$
14 A_{0b}
13 A_{1b}
12 $\overline{Q}_{0b}$
11 $\overline{Q}_{1b}$
10 $\overline{Q}_{2b}$
9 $\overline{Q}_{3b}$
CD04621S

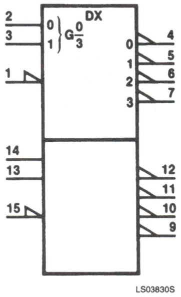
LOGIC SYMBOL



1 2 3
E_a A_{0a} A_{1a}
DECODER a
$\overline{Q}_{0a}$ $\overline{Q}_{1a}$ $\overline{Q}_{2a}$ $\overline{Q}_{3a}$
4 5 6 7
LS03814S
15 14 13
E_b A_{0b} A_{1b}
DECODER b
$\overline{Q}_{0b}$ $\overline{Q}_{1b}$ $\overline{Q}_{2b}$ $\overline{Q}_{3b}$
12 11 10 9
LS03824S

V_{CC} = Pin 16
GND = Pin 8

LOGIC SYMBOL (IEEE/IEC)

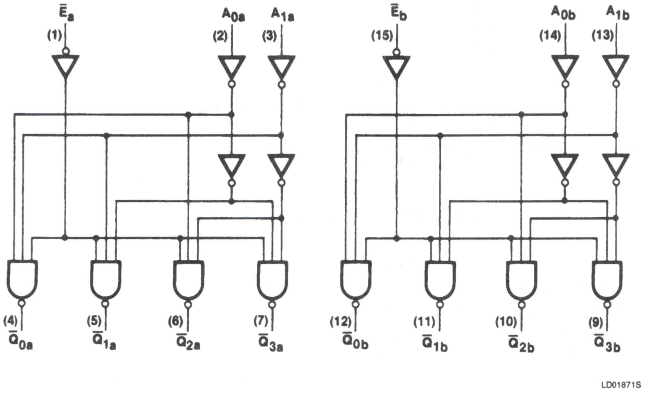


DX
2
3
0
1
G 0/3
1
0 4
1 5
2 6
3 7
14
13
15
12
11
10
9
LS03830S

Decoder/Demultiplexer

FAST 74F139

LOGIC DIAGRAM


$\overline{E}_a$
(1)
A_{0a}
(2)
A_{1a}
(3)
$\overline{E}_b$
(15)
A_{0b}
(14)
A_{1b}
(13)
(4)
$\overline{Q}_{0a}$
(5)
$\overline{Q}_{1a}$
(6)
$\overline{Q}_{2a}$
(7)
$\overline{Q}_{3a}$
(12)
$\overline{Q}_{0b}$
(11)
$\overline{Q}_{1b}$
(10)
$\overline{Q}_{2b}$
(9)
$\overline{Q}_{3b}$
LD01871S

V_{CC} = Pin 16
GND = Pin 8
( ) = Pin numbers

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		74F139			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX V_{IH} = MIN,	± 10%V_{CC}	2.5			V
			± 5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, I_{OL} = MAX V_{IH} = MIN,	± 10%V_{CC}		0.35	0.50	V
			± 5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, $I_I = I_{IK}$			−0.73	−1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V				−0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX			13	20	mA

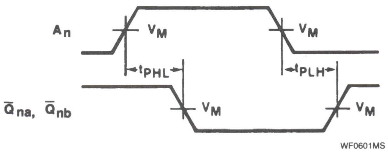
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. To measure I_{CC}, outputs must be open, V_{IN} on all inputs = 4.5V.

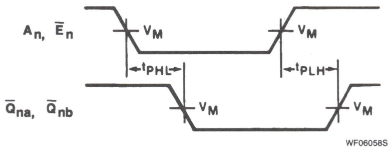
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F139					UNIT
			T_A = +25°C V_{CC} = +5.0V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_0 or A_1 to $\overline{Q}_{na}$, $\overline{Q}_{nb}$	Waveforms 1 and 2	3.5 4.0	5.3 6.1	7.0 8.0	3.0 4.0	8.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}_n$ to $\overline{Q}_{na}$, $\overline{Q}_{nb}$	Waveform 2	3.5 3.0	5.4 4.7	7.0 6.5	3.5 3.0	8.0 7.5	ns

AC WAVEFORMS



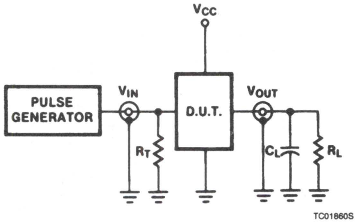
Waveform 1. For Inverting Outputs



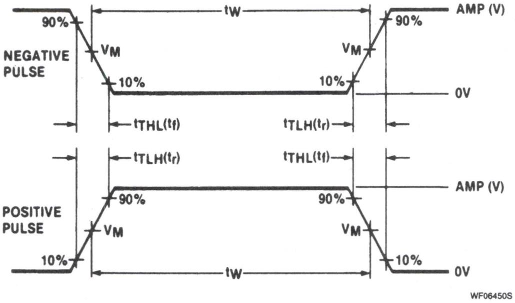
Waveform 2. For Non-Inverting Outputs

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORM


VCC
PULSE GENERATOR
VIN
D.U.T.
VOUT
RT
CL
RL
TC01860S

Test Circuit for Totem-Pole Outputs


tW
90%
AMP (V)
NEGATIVE PULSE
VM
10%
0V
tTHL(tf)
tTLH(tr)
tTLH(tr)
tTHL(tf)
POSITIVE PULSE
90%
AMP (V)
VM
10%
0V
tW
WF06450S

V_M = 1.5V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F148
Encoder

8-Input Priority Encoder
Product Specification

FAST Products

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F148	6.0ns	23mA

FEATURES
- Code conversions
- Multi-channel D/A converter
- Decimal-to-BCD converter
- Cascading for priority encoding of "N" bits
- Input enable capability
- Priority encoding — automatic selection of highest priority input line
- Output enable — active-Low when all inputs High
- Group signal output — active when any input is Low

DESCRIPTION
The 'F148 8-input priority encoder accepts data from eight active-Low inputs and provides a binary representation on the three active-Low outputs. A priority is assigned to each input so that when two or more inputs are simultaneously active, the input with the highest priority is represented on the output, with input line $\bar{I}_7$ having the highest priority.

A High on the Enable Input (EI) will force all outputs to the inactive (High) state and allow new data to settle without producing erroneous information at the outputs.

ORDERING INFORMATION

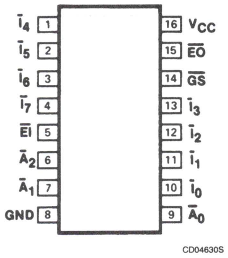
PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
16-Pin Plastic DIP	N74F148N
16-Pin Plastic SO	N74F148D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

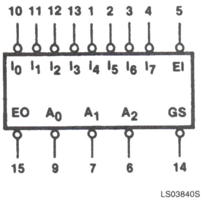
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$\bar{I}_1 - \bar{I}_7$	Priority inputs (active-Low)	1.0/2.0	20μA/1.2mA
$\bar{I}_0$	Priority input (active-Low)	1.0/1.0	20μA/0.6mA
$\overline{EI}$	Enable input (active-Low)	1.0/2.0	20μA/1.2mA
$\overline{EO}$	Enable output (active-Low)	50/33	1.0mA/20mA
$\overline{GS}$	Group select output (active-Low)	50/33	1.0mA/20mA
$\bar{A}_0 - \bar{A}_2$	Address outputs (active-Low)	50/33	1.0mA/20mA

NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

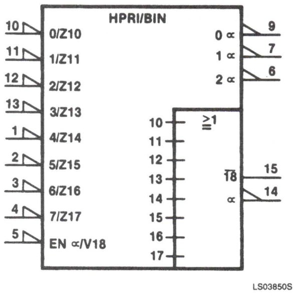
PIN CONFIGURATION


Ī4 1
Ī5 2
Ī6 3
Ī7 4
ĒI 5
Ā2 6
Ā1 7
GND 8
16 VCC
15 ĒO
14 GS
13 Ī3
12 Ī2
11 Ī1
10 Ī0
9 Ā0
CD04630S

LOGIC SYMBOL


10 11 12 13 1 2 3 4 5
I0 I1 I2 I3 I4 I5 I6 I7 EI
EO A0 A1 A2 GS
15 9 7 6 14
LS03840S

LOGIC SYMBOL (IEEE/IEC)


HPRI/BIN
10 0/Z10
11 1/Z11
12 2/Z12
13 3/Z13
1 4/Z14
2 5/Z15
3 6/Z16
4 7/Z17
5 EN α/V18
0 α 9
1 α 7
2 α 6
10 11 12 13 14 15 16 17
≥1
18 15
α 14
LS03850S

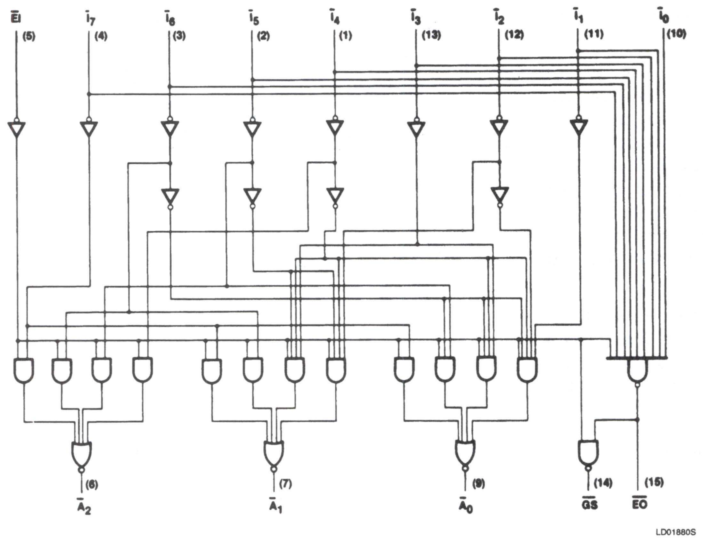
A Group Signal ($\overline{GS}$) output and an Enable Output ($\overline{EO}$) are provided with the three data outputs. The $\overline{GS}$ is active-Low when any input is Low; this indicates when any input is active. The $\overline{EO}$ is active-Low when all inputs are High. Using the Enable Output along with the Enable Input allows priority encoding of N input signals. Both $\overline{EO}$ and $\overline{GS}$ are active-High when the Enable Input is High.

FUNCTION TABLE

INPUTS									OUTPUTS				
EI	$\bar{I}_0$	$\bar{I}_1$	$\bar{I}_2$	$\bar{I}_3$	$\bar{I}_4$	$\bar{I}_5$	$\bar{I}_6$	$\bar{I}_7$	$\overline{GS}$	$\bar{A}_0$	$\bar{A}_1$	$\bar{A}_2$	$\overline{EO}$
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	H	L	L	H
L	X	X	X	X	X	L	H	H	L	L	H	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	L	L	L	H	H
L	X	X	L	H	H	H	H	H	L	H	L	H	H
L	X	L	H	H	H	H	H	H	L	L	H	H	H
L	L	H	H	H	H	H	H	H	L	H	H	H	H

H = High voltage level
L = Low voltage level
X = Don't care

LOGIC DIAGRAM


$\overline{EI}$ (5)
$\bar{I}_7$ (4)
$\bar{I}_6$ (3)
$\bar{I}_5$ (2)
$\bar{I}_4$ (1)
$\bar{I}_3$ (13)
$\bar{I}_2$ (12)
$\bar{I}_1$ (11)
$\bar{I}_0$ (10)
(6) $\bar{A}_2$
(7) $\bar{A}_1$
(9) $\bar{A}_0$
(14) $\overline{GS}$
(15) $\overline{EO}$
LD01880S

V_{CC} = Pin 16
GND = Pin 8

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		74F148			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX V_{IH} = MIN,	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OL} = MAX V_{IH} = MIN,	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current	$\overline{I}_0$, $\overline{EI}$	V_{CC} = MAX, V_I = 0.5V				−0.6	mA
		$\overline{I}_1 - \overline{I}_7$					−1.2	
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current (total)		V_{CC} = MAX			23	35	mA

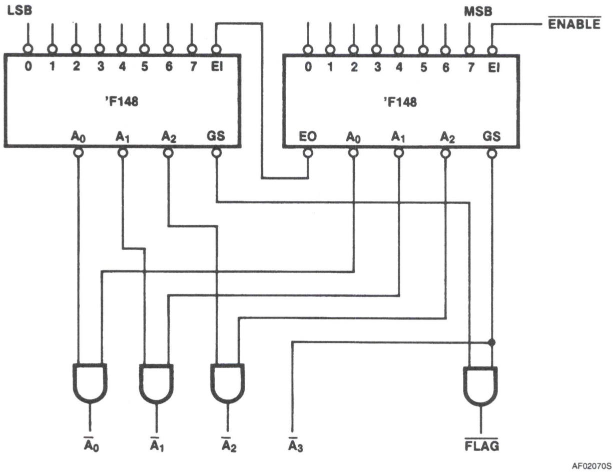
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

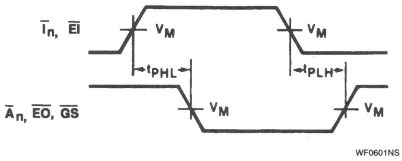
SYMBOL	PARAMETER	TEST CONDITIONS	74F148					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay $\overline{I}_n$ to $\overline{A}_n$	Waveform 2	3.5 4.0	6.0 6.0	9.0 10.5	3.5 4.0	10.0 12.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{I}_n$ to $\overline{EO}$	Waveform 1	2.0 2.5	3.5 4.5	6.5 7.5	2.0 2.5	7.5 8.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{I}_n$ to $\overline{GS}$	Waveform 2	2.0 2.0	4.0 6.0	9.0 8.0	2.0 2.0	10.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{EI}$ to $\overline{A}_n$	Waveform 2	3.5 3.0	6.0 5.5	8.5 8.0	3.5 3.0	9.5 9.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{EI}$ to $\overline{GS}$	Waveform 2	2.5 3.0	4.5 5.5	7.0 7.5	2.5 3.0	8.0 8.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{EI}$ to $\overline{EO}$	Waveform 2	3.0 4.5	5.0 7.0	7.0 10.5	3.0 4.5	8.0 12.0	ns

APPLICATION

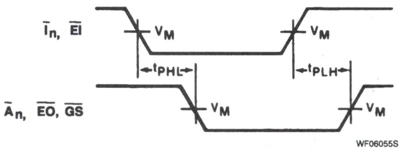

LSB
MSB
ENABLE
0 1 2 3 4 5 6 7 EI
'F148
A0 A1 A2 GS
0 1 2 3 4 5 6 7 EI
'F148
EO A0 A1 A2 GS
$\overline{A}_0$
$\overline{A}_1$
$\overline{A}_2$
$\overline{A}_3$
$\overline{FLAG}$
AF02070S

16-Input Priority Encoder

AC WAVEFORMS


$\overline{I}_n$, $\overline{EI}$
V_M
V_M
t_{PHL}
t_{PLH}
$\overline{A}_n$, $\overline{EO}$, $\overline{GS}$
V_M
V_M
WF0601NS

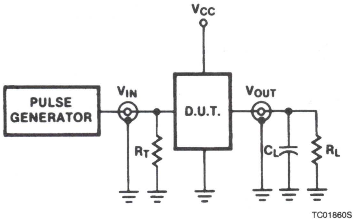
Waveform 1. For Inverting Outputs


$\overline{I}_n$, $\overline{EI}$
V_M
V_M
t_{PHL}
t_{PLH}
$\overline{A}_n$, $\overline{EO}$, $\overline{GS}$
V_M
V_M
WF06055S

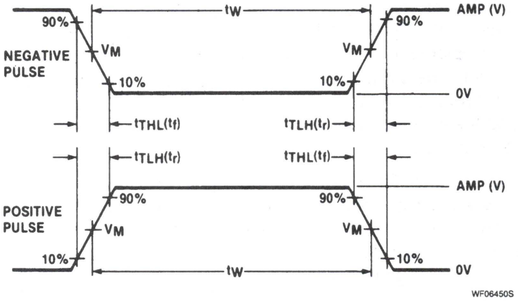
Waveform 2. For Non-Inverting Outputs

NOTE: For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORM


V_{CC}
PULSE GENERATOR
V_{IN}
D.U.T.
V_{OUT}
R_T
C_L
R_L
TC01860S

Test Circuit for Totem-Pole Outputs


90%
t_W
90%
AMP (V)
NEGATIVE PULSE
V_M
V_M
10%
10%
0V
$t_{THL}(t_f)$
$t_{TLH}(t_r)$
$t_{TLH}(t_r)$
$t_{THL}(t_f)$
AMP (V)
90%
90%
POSITIVE PULSE
V_M
V_M
10%
10%
t_W
0V
WF06450S

$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F151
Multiplexer

8-Input Multiplexer
Product Specification

FAST Products

FEATURES
- **Multifunction capability**
- **Complementary outputs**
- **See 'F251 for 3-state version**

DESCRIPTION
The 'F151 is a logical implementation of a single-pole, 8-position switch with the switch position controlled by the state of three Select inputs: S_0, S_1, and S_2. True (Y) and Complement ($\overline{Y}$) outputs are both provided. The Enable input ($\overline{E}$) is active-Low. When $\overline{E}$ is High, the $\overline{Y}$ output is High and the Y output is Low, regardless of all other inputs.

In one package the 'F151 provides the ability to select from eight sources of data or control information. The device can provide any logic function of four variables and its negation with correct manipulation.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F151	5.5ns	13.5mA

ORDERING INFORMATION

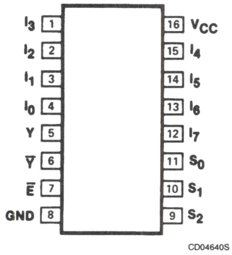
PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
16-Pin Plastic DIP	N74F151N
16-Pin Plastic SO	N74F151D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$I_0 - I_7$	Data inputs	1.0/1.0	20μA/0.6mA
$S_0 - S_2$	Select inputs	1.0/1.0	20μA/0.6mA
$\overline{E}$	Enable input (active-Low)	1.0/1.0	20μA/0.6mA
Y, $\overline{Y}$	Data outputs	50/33	1.0mA/20mA

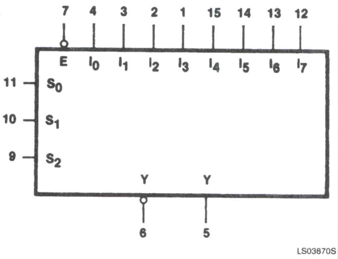
NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



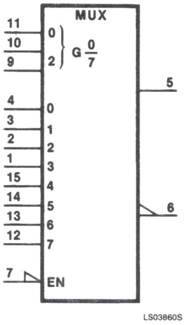
I_3 1
I_2 2
I_1 3
I_0 4
Y 5
$\overline{Y}$ 6
$\overline{E}$ 7
GND 8
16 V_{CC}
15 I_4
14 I_5
13 I_6
12 I_7
11 S_0
10 S_1
9 S_2
CD04640S

LOGIC SYMBOL



7
4
3
2
1
15
14
13
12
E
I_0
I_1
I_2
I_3
I_4
I_5
I_6
I_7
11
S_0
10
S_1
9
S_2
Y
Y
6
5
LS03870S

LOGIC SYMBOL (IEEE/IEC)

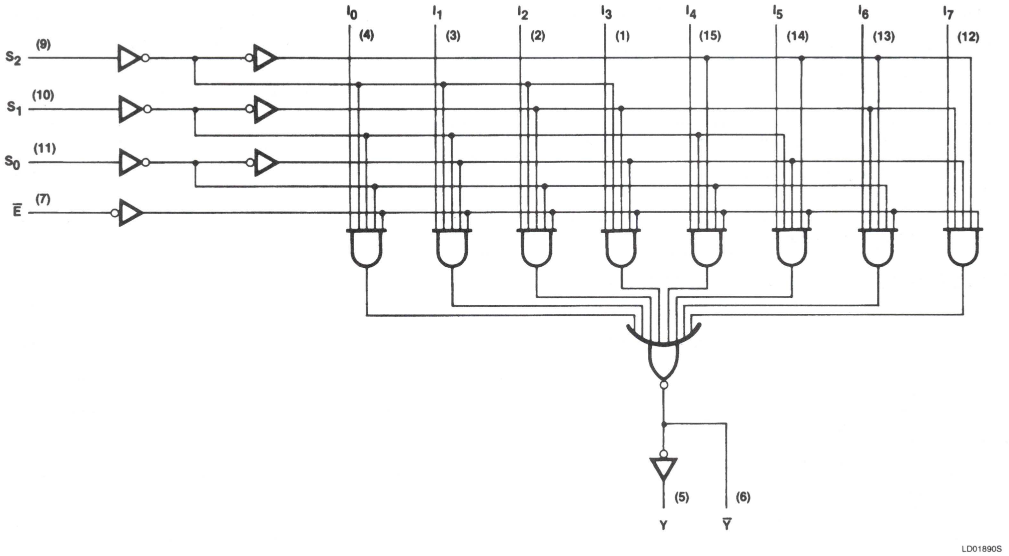


MUX
11
10
9
0
2
G $\frac{0}{7}$
4
3
2
1
15
14
13
12
0
1
2
3
4
5
6
7
5
6
7
EN
LS03860S

Multiplexer

FAST 74F151

LOGIC DIAGRAM


I_0 (4)
I_1 (3)
I_2 (2)
I_3 (1)
I_4 (15)
I_5 (14)
I_6 (13)
I_7 (12)
S_2 (9)
S_1 (10)
S_0 (11)
$\overline{E}$ (7)
(5) Y
(6) $\overline{Y}$
LD01890S

V_{CC} = Pin 16
GND = Pin 8
( ) = Pin numbers

FUNCTION TABLE

INPUTS				OUTPUTS	
S_2	S_1	S_0	$\overline{OE}$	Y	$\overline{Y}$
X	X	X	H	L	H
L	L	L	L	I_0	$\overline{I}_0$
L	L	H	L	I_1	$\overline{I}_1$
L	H	L	L	I_2	$\overline{I}_2$
L	H	H	L	I_3	$\overline{I}_3$
H	L	L	L	I_4	$\overline{I}_4$
H	L	H	L	I_5	$\overline{I}_5$
H	H	L	L	I_6	$\overline{I}_6$
H	H	H	L	I_7	$\overline{I}_7$

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		74F151			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX V_{IH} = MIN,	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OL} = MAX V_{IH} = MIN,	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				−0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			12	16	mA
		I_{CCL}				15	20	mA

NOTES:

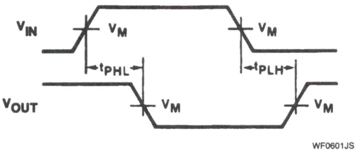
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

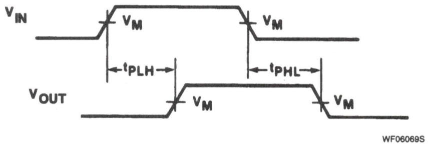
SYMBOL	PARAMETER	TEST CONDITIONS	74F151					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_n to Y	Waveform 2	3.0 3.0	4.5 4.5	6.5 6.5	2.5 3.0	9.0 7.5	ns
t_{PLH} t_{PHL}	Propagation delay I_n to $\overline{Y}$	Waveform 1	2.0 1.0	4.0 2.5	6.0 4.0	2.0 1.0	7.0 5.0	ns
t_{PLH} t_{PHL}	Propagation delay S_n to Y	Waveform 1, 2	4.0 4.5	7.0 7.0	9.5 9.0	4.0 4.5	12.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{Y}$	Waveform 1, 2	4.0 2.0	6.5 4.5	9.0 7.0	3.5 2.0	10.0 7.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}_n$ to Y	Waveform 1	6.0 4.0	8.0 5.5	10.0 7.0	5.5 4.0	11.5 8.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}_n$ to $\overline{Y}$	Waveform 2	3.5 4.0	5.0 5.5	6.5 7.5	3.5 4.0	7.5 8.0	ns

NOTE:
1. Subtract 0.2ns from minimum values for SO package.

AC WAVEFORMS



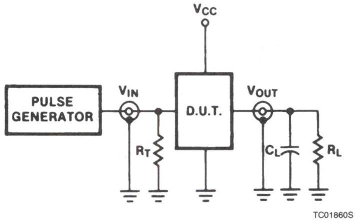
Waveform 1. Inverting



Waveform 2. Non-Inverting

NOTE: For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORMS


V_{CC}
PULSE GENERATOR
V_{IN}
D.U.T.
V_{OUT}
R_T
C_L
R_L
TC01860S

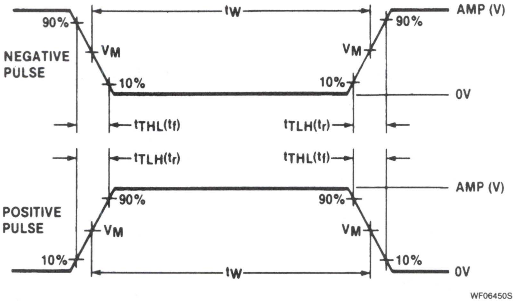
Test Circuit for Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.


NEGATIVE PULSE
POSITIVE PULSE
90%
10%
V_M
t_W
AMP (V)
0V
$t_{THL}(t_f)$
$t_{TLH}(t_r)$
WF06450S

V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F151A
8-Input Multiplexer

Product Specification

FAST Products

FEATURES
- **Multifunction capability**
- **Complementary outputs**
- **See 'F251A for 3-State version**

DESCRIPTION
The 'F151A is a logic implementation of a single-pole, 8-position switch with the switch position controlled by the state of three Select inputs: S_0, S_1, and S_2. True (Y) and complementary (Y) outputs are both provided. The Enable input ($\overline{E}$) is active-Low. When $\overline{E}$ is High, the $\overline{Y}$ output is High and the Y output is Low, regardless of all other inputs. In one package the 'F151A provides the ability to select from eight sources of data or control information. The device can provide any logic function of four variables and its negation with correct manipulation.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F151A	4.5ns	17.0mA

ORDERING INFORMATION

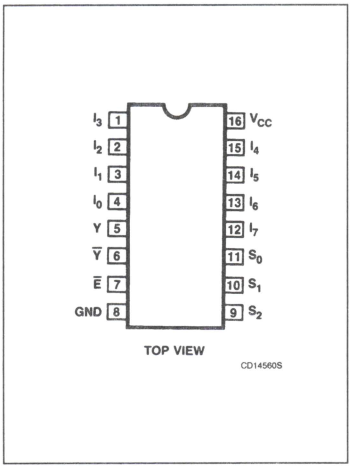
PACKAGE	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$, $T_A = 0°C$ to $+70°C$
16-Pin Plastic DIP	N74F151AN
16-Pin Plastic SO	N74F151AD

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$I_0 - I_7$	Data inputs	1.0/1.0	20μA/0.6mA
$S_0 - S_2$	Select inputs	1.0/1.0	20μA/0.6mA
$\overline{E}$	Enable input (active-Low)	1.0/1.0	20μA/0.6mA
Y, $\overline{Y}$	Data outputs	50/33	1.0mA/20mA

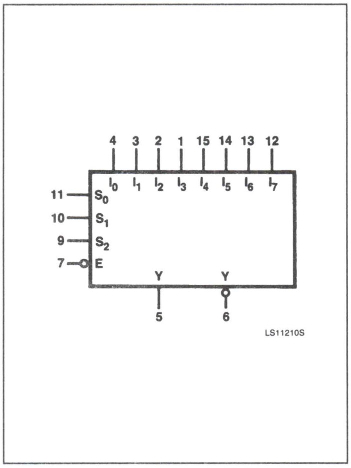
NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



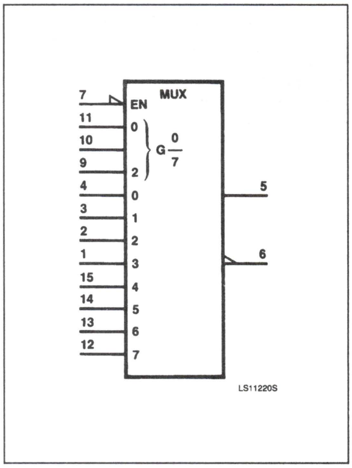
I_3 1
I_2 2
I_1 3
I_0 4
Y 5
$\overline{Y}$ 6
$\overline{E}$ 7
GND 8
16 V_{CC}
15 I_4
14 I_5
13 I_6
12 I_7
11 S_0
10 S_1
9 S_2
TOP VIEW
CD14560S

LOGIC SYMBOL



4 3 2 1 15 14 13 12
I_0 I_1 I_2 I_3 I_4 I_5 I_6 I_7
11 S_0
10 S_1
9 S_2
7 E
Y
Y
5
6
LS11210S

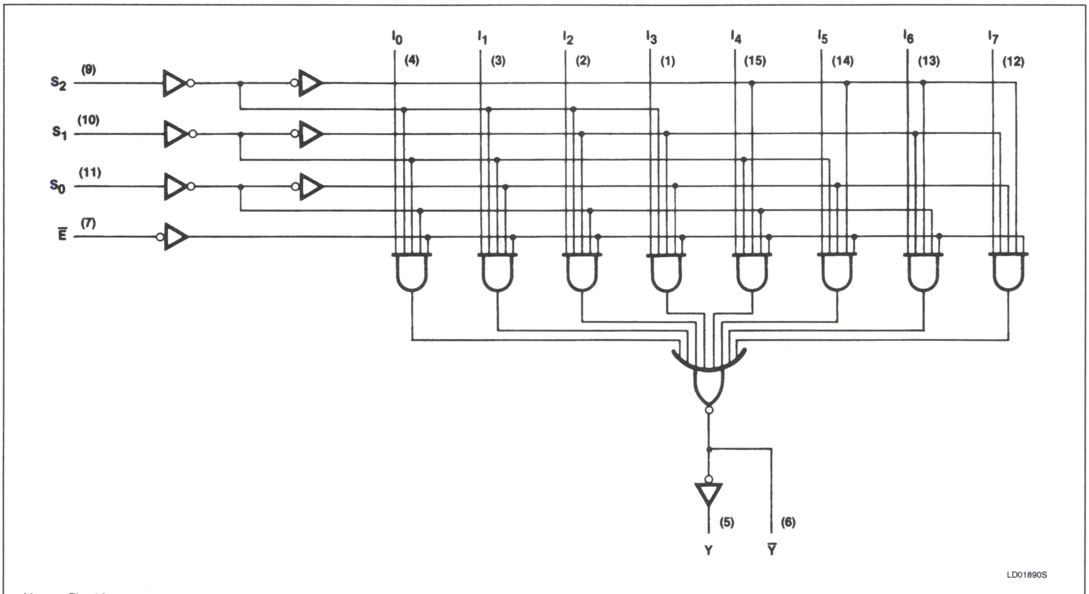
LOGIC SYMBOL (IEEE/IEC)



MUX
7 EN
11 0
10
9 2
G 0/7
4 0
3 1
2 2
1 3
15 4
14 5
13 6
12 7
5
6
LS11220S

8-Input Multiplexer FAST 74F151A

LOGIC DIAGRAM



I_0 (4)
I_1 (3)
I_2 (2)
I_3 (1)
I_4 (15)
I_5 (14)
I_6 (13)
I_7 (12)
S_2 (9)
S_1 (10)
S_0 (11)
$\overline{E}$ (7)
(5) Y
(6) $\overline{Y}$
LD01890S

V_{CC} = Pin 16
GND = Pin 8
( ) = Pin numbers

FUNCTION TABLE

INPUTS				OUTPUTS	
S_2	S_1	S_0	$\overline{E}$	Y	$\overline{Y}$
X	X	X	H	L	H
L	L	L	L	I_0	$\overline{I}_0$
L	L	H	L	I_1	$\overline{I}_1$
L	H	L	L	I_2	$\overline{I}_2$
L	H	H	L	I_3	$\overline{I}_3$
H	L	L	L	I_4	$\overline{I}_4$
H	L	H	L	I_5	$\overline{I}_5$
H	H	L	L	I_6	$\overline{I}_6$
H	H	H	L	I_7	$\overline{I}_7$

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5.0	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN V_{IL} = MAX V_{IH} = MIN	I_{OH} = MAX	±10% V_{CC}	2.5			V
					±5% V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN V_{IL} = MAX V_{IH} = MIN	I_{OL} = MAX	±10% V_{CC}		0.35	0.50	V
					±5% V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$				−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V					100	μA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					−0.6	mA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX			−60		−150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				18	25	mA
		I_{CCL}					17	25	mA

NOTES:

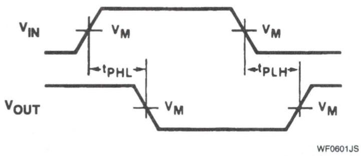
1. For conditions shown as MIN or MAX, use the appropriate value under the recommended operating conditions for the applicable conditions.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of High-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} should be performed last.

8-Input Multiplexer FAST 74F151A

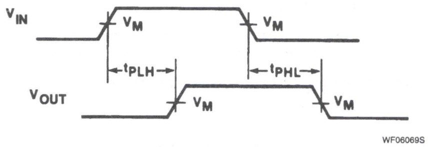
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			$T_A = +25°C$ $V_{CC} = 5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_n to Y	Waveform 2	2.5 2.5	4.5 4.5	7.0 7.0	2.5 2.5	7.5 7.5	ns
t_{PLH} t_{PHL}	Propagation delay I_n to $\overline{Y}$	Waveform 1	2.0 1.0	4.0 2.0	7.0 4.5	2.0 1.0	7.5 5.0	ns
t_{PLH} t_{PHL}	Propagation delay S_n to Y	Waveform 1, 2	4.5 4.0	6.5 6.0	10.0 8.5	4.0 3.5	11.0 9.5	ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{Y}$	Waveform 1, 2	3.0 2.0	5.5 4.5	8.5 7.5	3.0 2.0	9.5 7.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}_n$ to Y	Waveform 1	4.0 3.0	6.5 5.0	9.0 7.0	3.5 3.0	9.5 7.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}_n$ to $\overline{Y}$	Waveform 2	2.5 1.5	4.5 3.5	6.5 5.5	2.5 2.0	7.0 6.0	ns

AC WAVEFORMS



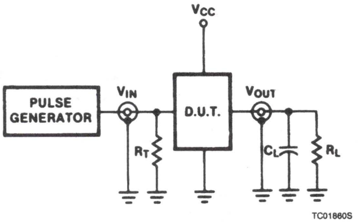
Waveform 1. Inverting



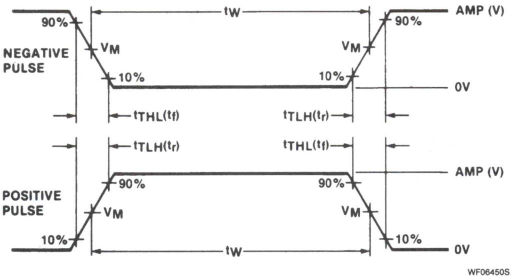
Waveform 2. Non-Inverting

NOTE: $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORMS


V_{CC}
PULSE GENERATOR
V_{IN}
D.U.T.
V_{OUT}
R_T
C_L
R_L
TC01860S

Test Circuit for Totem-Pole Outputs


NEGATIVE PULSE
POSITIVE PULSE
90%
10%
V_M
t_W
AMP (V)
0V
$t_{THL}(t_f)$
$t_{TLH}(t_r)$
WF06450S

$V_M = 1.5V$

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor to GND; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Signetics

FAST 74F153
Multiplexer

Dual 4-Line to 1-Line Multiplexer
Product Specification

FAST Products

TYPE	TYPICAL PROGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F153	7.0ns	12mA

FEATURES

- Non-inverting outputs
- Separate enable for each section
- Common select inputs
- See 'F253 for 3-State version

DESCRIPTION

The 'F153 is a dual 4-input multiplexer that can select 2 bits of data from up to four sources under control of the common Select inputs (S_0, S_1). The two 4-input multiplexer circuits have individual active-Low Enables ($\overline{E}_a$, $\overline{E}_b$) which can be used to strobe the outputs independently. Outputs (Y_a, Y_b) are forced Low when the corresponding Enables ($\overline{E}_a$, $\overline{E}_b$) are High.

The device is the logical implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the two Select inputs. The logic equations for the outputs are shown below.

$$Y_a = \overline{E}_a \cdot (I_{0a} \cdot \overline{S}_1 \cdot \_ \cdot \overline{S}_0 + I_{1a} \cdot \overline{S}_1 \cdot S_0 + I_{2a} \cdot S_1 \cdot \overline{S}_0 + I_{3a} \cdot S_1 \cdot S_0)$$

$$Y_b = \overline{E}_b \cdot (I_{0b} \cdot \overline{S}_1 \cdot \_ \cdot \overline{S}_0 + I_{1b} \cdot \overline{S}_1 \cdot S_0 + I_{2b} \cdot S_1 \cdot \overline{S}_0 + I_{3b} \cdot S_1 \cdot S_0)$$

ORDERING INFORMATION

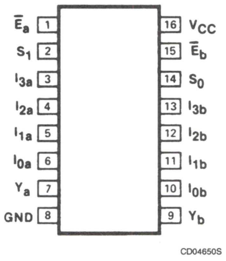
PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
16-Pin Plastic DIP	N74F153N
16-Pin Plastic SO	N74F153D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

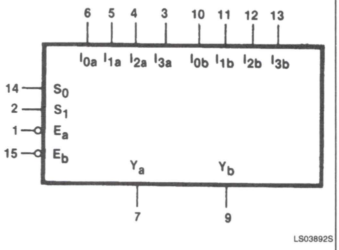
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$I_{0a} - I_{3a}$	Side A data inputs	1.0/1.0	20μA/0.6mA
$I_{0b} - I_{3b}$	Side B data inputs	1.0/1.0	20μA/0.6mA
S_0, S_1	Common select inputs	1.0/1.0	20μA/0.6mA
$\overline{E}_a$	Side A Enable input (active-Low)	1.0/1.0	20μA/0.6mA
$\overline{E}_b$	Side B Enable input (active-Low)	1.0/1.0	20μA/0.6mA
Y_a	Side A output	50/33	1.0mA/20mA
Y_b	Side B output	50/33	1.0mA/20mA

NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

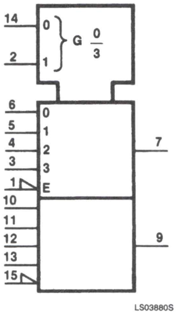
PIN CONFIGURATION


Ēa 1
S1 2
I3a 3
I2a 4
I1a 5
I0a 6
Ya 7
GND 8
16 VCC
15 Ēb
14 S0
13 I3b
12 I2b
11 I1b
10 I0b
9 Yb
CD04650S

LOGIC SYMBOL

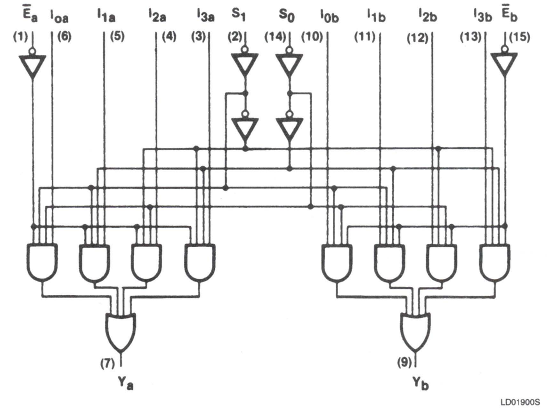

6 5 4 3 10 11 12 13
I0a I1a I2a I3a I0b I1b I2b I3b
14 S0
2 S1
1 Ea
15 Eb
Ya
Yb
7
9
LS03892S

LOGIC SYMBOL (IEEE/IEC)


14
2
0
1
G 0/3
6 0
5 1
4 2
3 3
1 E
10
11
12
13
15
7
9
LS03880S

The '153 can be used to move data to a common output bus from a group of registers. The state of the Select inputs would determine the particular register from which the data came. An alternative application is as a function generator. The device can generate two functions or three variables. This is useful for implementing highly irregular random logic.

LOGIC DIAGRAM


Ē_a
I_0a
I_1a
I_2a
I_3a
S_1
S_0
I_0b
I_1b
I_2b
I_3b
Ē_b
(1)
(6)
(5)
(4)
(3)
(2)
(14)
(10)
(11)
(12)
(13)
(15)
(7)
Y_a
(9)
Y_b
LD01900S

V_{CC} = Pin 16
GND = Pin 8

FUNCTION TABLE

SELECTS INPUTS		INPUTS (a or b)					OUTPUT
S_0	S_1	$\bar{E}$	I_0	I_1	I_2	I_3	Y
X	X	H	X	X	X	X	L
L	L	L	L	X	X	X	L
L	L	L	H	X	X	X	H
H	L	L	X	L	X	X	L
H	L	L	X	H	X	X	H
L	H	L	X	X	L	X	L
L	H	L	X	X	H	X	H
H	H	L	X	X	X	L	L
H	H	L	X	X	X	H	H

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−1	mA
I_{OL}	Low-level output current			20	mA

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX V_{IH} = MIN,	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OL} = MAX V_{IH} = MIN,	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				−0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	$\overline{E}_n$ = GND; $S_n = I_n$ = 4.5V		12	20	mA
		I_{CCL}		$\overline{E}_n = S_n = I_n$ = GND		12	20	mA

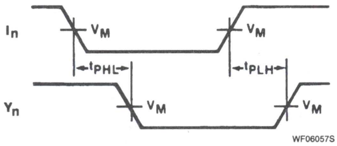
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

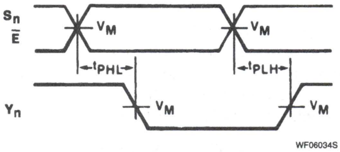
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F153					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_n to Y_n	Waveform 1	3.0 3.0	4.5 5.0	7.0 7.5	2.5 2.5	8.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay S_n to Y_n	Waveform 2	5.0 5.0	8.0 8.0	10.5 10.5	4.5 4.5	12.0 12.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to Y_n	Waveform 2	5.0 4.0	7.5 5.5	9.0 7.0	4.5 3.5	10.5 8.0	ns

AC WAVEFORMS


I_n
V_M
t_{PHL}
t_{PLH}
Y_n
WF06057S

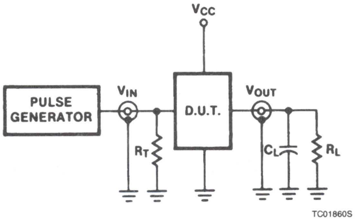
Waveform 1. Propagation Delay Data (I_n) to Output (Y_n)


S_n
$\overline{E}$
V_M
t_{PHL}
t_{PLH}
Y_n
WF06034S

Waveform 2. Propagation Delay Select (S_n) or Enable ($\overline{E}$) to Output (Y_n)

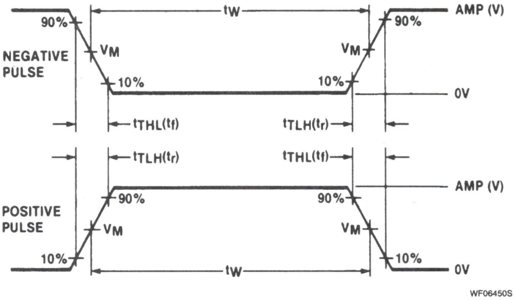
NOTE: For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORMS


V_{CC}
PULSE GENERATOR
V_{IN}
R_T
D.U.T.
V_{OUT}
C_L
R_L
TC01860S

Test Circuit for Totem-Pole Outputs

DEFINITIONS
R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.


NEGATIVE PULSE
90%
V_M
10%
t_W
AMP (V)
0V
$t_{THL}(t_f)$
$t_{TLH}(t_r)$
POSITIVE PULSE
WF06450S

$V_M = 1.5V$

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

FAST 74F157A, 74F158A
Data Selectors/Multiplexers

'157A Quad 2-Input Data Selector/Multiplexer (Non-Inverted)
'158A Quad 2-Input Data Selector/Multiplexer (Inverted)
Product Specification

DESCRIPTION

The 'F157A is a high-speed quad 2-input multiplexer which selects 4 bits of data from two sources under the control of a common Select input (S). The Enable input ($\overline{E}$) is active-Low. When $\overline{E}$ is High, all of the outputs (Y) are forced Low regardless of all other input conditions.

Moving data from two groups of registers to four common output busses is a common use of the 'F157A. The state of the Select input determines the particular register from which the data comes. It can also be used as a function generator. The device is useful for implementing highly irregular logic by generating any four of the 16 different functions of two variables with one variable common.

The device is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. Logic equations for the outputs are shown below:

$$Y_a = \overline{E}\cdot(I_{1a}\cdot S + I_{0a}\cdot\overline{S})$$
$$Y_b = \overline{E}\cdot(I_{1b}\cdot S + I_{0b}\cdot\overline{S})$$
$$Y_c = \overline{E}\cdot(I_{1c}\cdot S + I_{0c}\cdot\overline{S})$$
$$Y_d = \overline{E}\cdot(I_{1d}\cdot S + I_{0d}\cdot\overline{S})$$

The 'F158A is similar but has inverting outputs:

$$\overline{Y}_a = \overline{E}\cdot(I_{1a}\cdot S + I_{0a}\cdot\overline{S})$$
$$\overline{Y}_b = \overline{E}\cdot(I_{1b}\cdot S + I_{0b}\cdot\overline{S})$$
$$\overline{Y}_c = \overline{E}\cdot(I_{1c}\cdot S + I_{0c}\cdot\overline{S})$$
$$\overline{Y}_d = \overline{E}\cdot(I_{1d}\cdot S + I_{0d}\cdot\overline{S})$$

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F157A	4.6ns	15mA
74F158A	3.7ns	10mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
16-Pin Plastic DIP	N74F157AN, N74F158AN
16-Pin Plastic SO	N74F157AD, N74F158AD

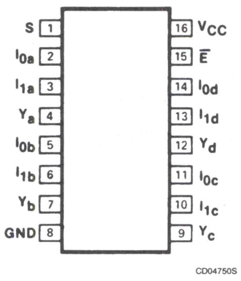
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
All	Inputs	1.0/1.0	20μA/0.6mA
Y_a–Y_d, $\overline{Y}_a$–$\overline{Y}_d$	Outputs	50/33	1.0mA/20mA

NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

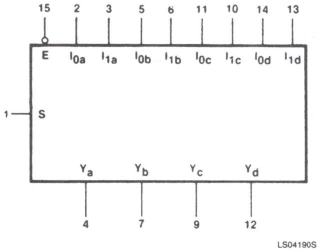
PIN CONFIGURATION

'F157A



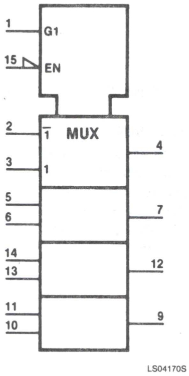
LOGIC SYMBOL

'F157A

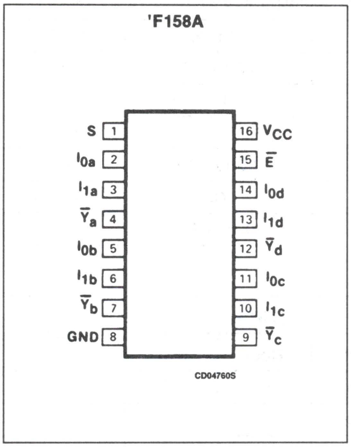


LOGIC SYMBOL (IEEE/IEC)

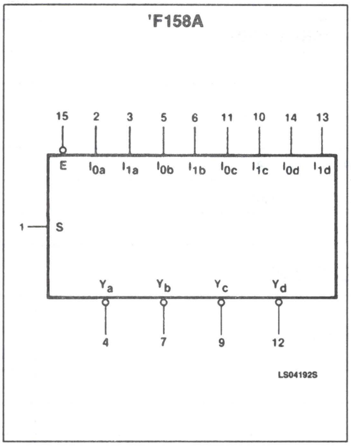
'F157A



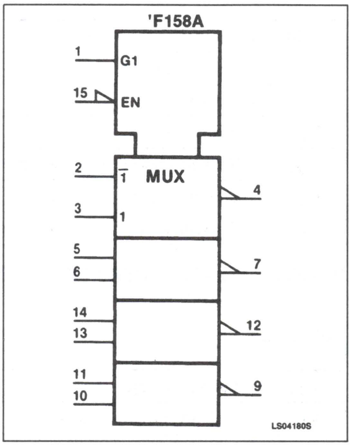
PIN CONFIGURATION


'F158A
S 1
I0a 2
I1a 3
Ȳa 4
I0b 5
I1b 6
Ȳb 7
GND 8
16 VCC
15 Ē
14 I0d
13 I1d
12 Ȳd
11 I0c
10 I1c
9 Ȳc
CD04760S

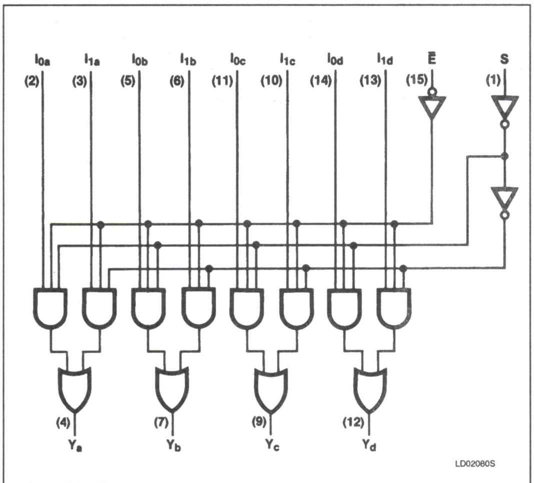
LOGIC SYMBOL


'F158A
15 2 3 5 6 11 10 14 13
E I0a I1a I0b I1b I0c I1c I0d I1d
1 S
Ya Yb Yc Yd
4 7 9 12
LS04192S

LOGIC SYMBOL (IEEE/IEC)

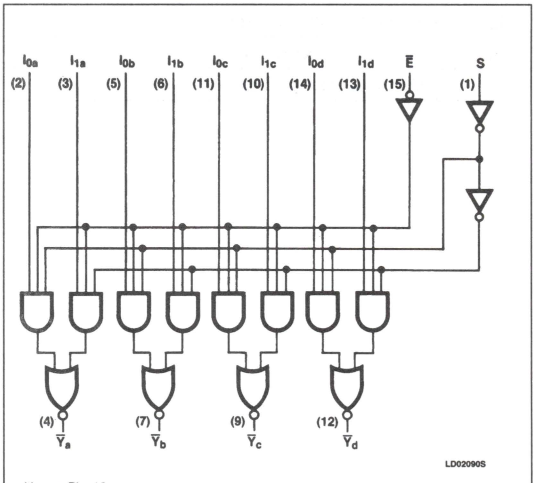

'F158A
1 G1
15 EN
2 1̄ MUX 4
3 1
5 6 7
14 13 12
11 10 9
LS04180S

LOGIC DIAGRAM, '157A


I0a (2)
I1a (3)
I0b (5)
I1b (6)
I0c (11)
I1c (10)
I0d (14)
I1d (13)
Ē (15)
S (1)
(4) Ya
(7) Yb
(9) Yc
(12) Yd
LD02080S

VCC = Pin 16
GND = Pin 8

LOGIC DIAGRAM, '158A


I0a (2)
I1a (3)
I0b (5)
I1b (6)
I0c (11)
I1c (10)
I0d (14)
I1d (13)
Ē (15)
S (1)
(4) Ȳa
(7) Ȳb
(9) Ȳc
(12) Ȳd
LD02090S

VCC = Pin 16
GND = Pin 8

FUNCTION TABLE, '157A

ENABLE	SELECT INPUT	DATA INPUTS		OUTPUT
Ē	S	I_0	I_1	Y
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = High voltage level
L = Low voltage level
X = Don't care

FUNCTION TABLE, '158A

ENABLE	SELECT INPUT	DATA INPUTS		OUTPUT
Ē	S	I_0	I_1	Ȳ
H	X	X	X	H
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		74F157A, 74F158A			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX V_{IH} = MIN,	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OL} = MAX V_{IH} = MIN,	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				−0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current[4] (total)	'F157A	V_{CC} = MAX			15.0	23.0	mA
		'F158A				14.0	19.0	mA

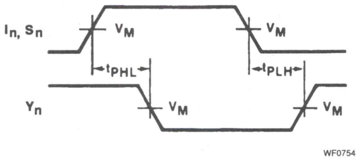
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. I_{CC} is measured with 4.5V applied to all inputs and all outputs open.

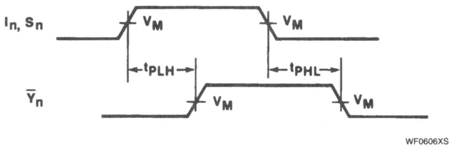
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	'F157A, 'F158A					UNIT
				T_A = +25°C V_{CC} = +5.0V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF R_L = 500Ω		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_n to Y	'F157A	Waveform 2	3.5 2.5	4.5 3.5	6.5 5.0	3.0 1.5	7.0 6.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to Y		Waveform 1	6.0 4.0	7.5 5.0	9.0 6.5	5.5 4.0	10.5 7.0	ns
t_{PLH} t_{PHL}	Propagation delay S to Y		Waveform 2	5.5 4.5	7.5 6.0	10.0 7.5	5.0 4.0	11.0 8.5	ns
t_{PLH} t_{PHL}	Propagation delay I_n to Y	'F158A	Waveform 3	3.0 1.5	4.0 2.5	6.0 4.0	2.5 1.0	7.0 4.5	ns
t_{PLH} t_{PHL}	Propagation delay E to $\overline{Y}$		Waveform 4	4.5 5.0	5.5 6.0	7.0 7.5	4.0 5.0	7.5 8.0	ns
t_{PLH} t_{PHL}	Propagation delay S to $\overline{Y}$		Waveform 3	4.5 4.0	6.5 5.5	8.5 7.5	4.0 3.5	9.5 8.0	ns

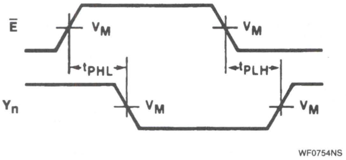
AC WAVEFORMS


In, Sn
VM
VM
tPHL
tPLH
Yn
VM
VM
WF0754MS

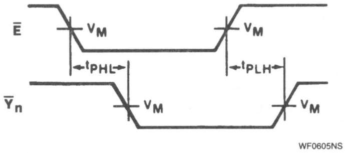
Waveform 1. For Inverting Outputs


In, Sn
VM
VM
tPLH
tPHL
Ȳn
VM
VM
WF0606XS

Waveform 2. For Non-Inverting Outputs


Ē
VM
VM
tPHL
tPLH
Yn
VM
VM
WF0754NS

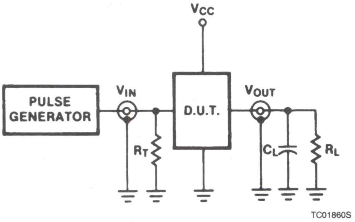
Waveform 3. For Inverting Outputs


Ē
VM
VM
tPHL
tPLH
Ȳn
VM
VM
WF0605NS

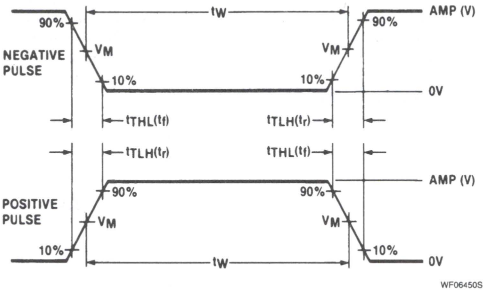
Waveform 4. For Non-Inverting Outputs

NOTE: For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORM


VCC
PULSE GENERATOR
VIN
D.U.T.
VOUT
RT
CL
RL
TC01860S

Test Circuit for Totem-Pole Outputs


tW
90%
90%
AMP (V)
NEGATIVE PULSE
VM
VM
10%
10%
0V
tTHL(tf)
tTLH(tr)
tTLH(tr)
tTHL(tf)
AMP (V)
90%
90%
POSITIVE PULSE
VM
VM
10%
10%
0V
tW
WF06450S

$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST Products

FAST 74F160A, 74F161A, 74F162A, 74F163A
Counters

'F160A, 'F162A BCD Decade Counter
'F161A, 'F163A 4-Bit Binary Counter
Product Specification

FEATURES

- Synchronous counting and loading
- Two Count Enable inputs for n-bit cascading
- Positive edge-triggered Clock
- Asynchronous Reset ('F160A, 'F161A)
- Synchronous Reset ('F162A, 'F163A)
- High-speed synchronous expansion
- Typical count rate of 120MHz

DESCRIPTION

Synchronous presettable decade ('F160A, 'F162A) and 4-bit ('F161A, 'F163A) counters feature an internal carry look-ahead and can be used for high-speed counting. Synchronous operation is provided by having all flip-flops clocked simultaneously on the positive-going edge of the clock. The Clock input is buffered.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F160A	130MHz	46mA
74F161A	130MHz	46mA
74F162A	130MHz	46mA
74F163A	130MHz	46mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
16-Pin Plastic DIP	N74F160AN, N74F161AN N74F162AN, N74F163AN
16-Pin Plastic SO	N74F160AD, N74F161AD N74F162AD, N74F163AD

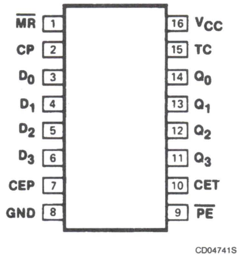
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
CEP	Count Enable Parallel input	1.0/1.0	20μA/0.6mA
CET	Count Enable Trickle input	1.0/2.0	20μA/1.2mA
CP	Clock Pulse input (active rising edge)	1.0/1.0	20μA/0.6mA
$\overline{MR}$	Asynchronous Master Reset input (active-Low)	1.0/1.0	20μA/0.6mA
$\overline{SR}$	Synchronous Reset input (active-Low)	1.0/2.0	20μA/1.2mA
$D_0 - D_3$	Parallel data inputs	1.0/1.0	20μA/0.6mA
$\overline{PE}$	Parallel Enable input (active-Low)	1.0/2.0	20μA/1.2mA
$Q_0 - Q_3$	Flip-flop outputs	50/33	1.0mA/20mA
TC	Terminal Count output	50/33	1.0mA/20mA

NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

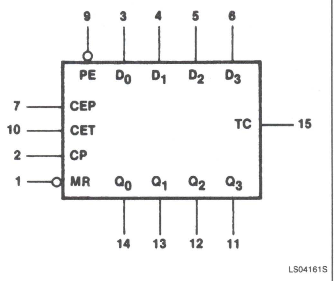
PIN CONFIGURATION

'F160A


MR 1
CP 2
D0 3
D1 4
D2 5
D3 6
CEP 7
GND 8
16 VCC
15 TC
14 Q0
13 Q1
12 Q2
11 Q3
10 CET
9 PE
CD04741S

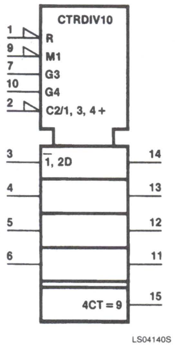
LOGIC SYMBOL

'F160A


9
3
4
5
6
PE
D0
D1
D2
D3
7
CEP
10
CET
2
CP
1
MR
TC
15
Q0
Q1
Q2
Q3
14
13
12
11
LS04161S

LOGIC SYMBOL (IEEE/IEC)

'F160A

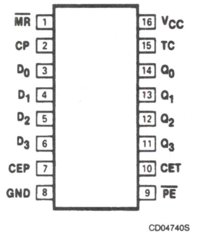

CTRDIV10
1
R
9
M1
7
G3
10
G4
2
C2/1, 3, 4+
3
1, 2D
14
4
13
5
12
6
11
4CT=9
15
LS04140S

Counters

FAST 74F160A, 74F161A, 74F162A, 74F163A

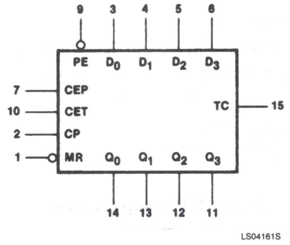
PIN CONFIGURATION

'F161A


MR 1
CP 2
D0 3
D1 4
D2 5
D3 6
CEP 7
GND 8
16 VCC
15 TC
14 Q0
13 Q1
12 Q2
11 Q3
10 CET
9 PE
CD04740S

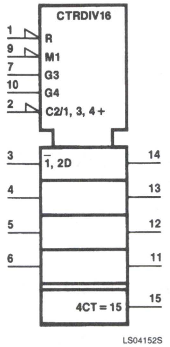
LOGIC SYMBOL

'F161A


9 3 4 5 6
PE D0 D1 D2 D3
7 CEP
10 CET
2 CP
1 MR
TC 15
Q0 Q1 Q2 Q3
14 13 12 11
LS04161S

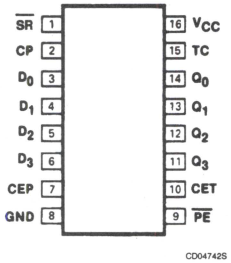
LOGIC SYMBOL

'F161A


CTRDIV16
1 R
9 M1
7 G3
10 G4
2 C2/1, 3, 4+
3 1, 2D 14
4 13
5 12
6 11
4CT=15 15
LS04152S

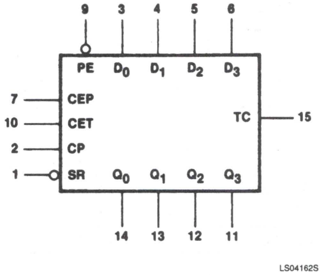
PIN CONFIGURATION

'F162A


SR 1
CP 2
D0 3
D1 4
D2 5
D3 6
CEP 7
GND 8
16 VCC
15 TC
14 Q0
13 Q1
12 Q2
11 Q3
10 CET
9 PE
CD04742S

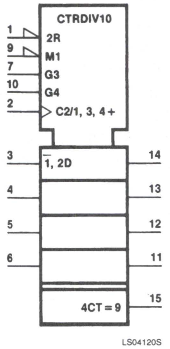
LOGIC SYMBOL

'F162A


9 3 4 5 6
PE D0 D1 D2 D3
7 CEP
10 CET
2 CP
1 SR
TC 15
Q0 Q1 Q2 Q3
14 13 12 11
LS04162S

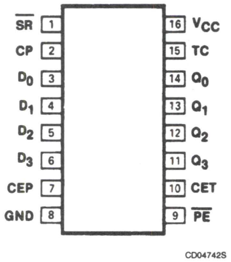
LOGIC SYMBOL

'F162A


CTRDIV10
1 2R
9 M1
7 G3
10 G4
2 C2/1, 3, 4+
3 1, 2D 14
4 13
5 12
6 11
4CT=9 15
LS04120S

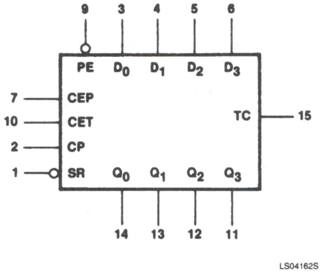
PIN CONFIGURATION

'F163A


SR 1
CP 2
D0 3
D1 4
D2 5
D3 6
CEP 7
GND 8
16 VCC
15 TC
14 Q0
13 Q1
12 Q2
11 Q3
10 CET
9 PE
CD04742S

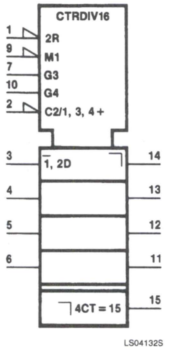
LOGIC SYMBOL

'F163A


9 3 4 5 6
PE D0 D1 D2 D3
7 CEP
10 CET
2 CP
1 SR
TC 15
Q0 Q1 Q2 Q3
14 13 12 11
LS04162S

LOGIC SYMBOL

'F163A


CTRDIV16
1 2R
9 M1
7 G3
10 G4
2 C2/1, 3, 4+
3 1, 2D 14
4 13
5 12
6 11
4CT=15 15
LS04132S

The outputs of the counters may be preset to High or Low level. A Low level at the Parallel Enable ($\overline{PE}$) input disables the counting action and causes the data at the $D_0 - D_3$ inputs to be loaded into the counter on the positive-going edge of the clock (providing that the setup and hold requirements for $\overline{PE}$ are met). Preset takes place regardless of the levels at Count Enable (CEP, CET) inputs.

A Low level at the Master Reset ($\overline{MR}$) input sets all four outputs of the flip-flops ($Q_0 - Q_3$) in 'F160A and 'F161A to Low levels, regardless of the levels at CP, $\overline{PE}$, CET and CEP inputs (thus providing an asynchronous clear function).

For the 'F162A and 'F163A, the clear function is synchronous. A Low level at the Reset ($\overline{SR}$) input sets all four outputs of the flip-flops ($Q_0 - Q_3$) to Low levels after the next positive-going transition on the Clock (CP) input (providing that the setup and hold requirements for $\overline{MR}$ are met). This action occurs regardless of the levels at $\overline{PE}$, CET, and CEP inputs. This synchronous reset feature enables the designer to modify the maximum count with only one external NAND gate (see Figure A).

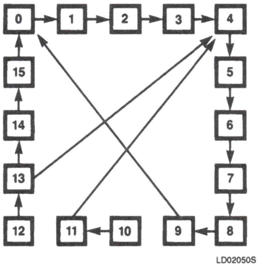
The carry look-ahead simplifies serial cascading of the counters. Both Count Enable inputs (CEP and CET) must be High to count. The CET input is fed forward to enable the TC output. The TC output thus enabled will produce a High output pulse of a duration approximately equal to the High level output of Q_0. This pulse can be used to enable the next cascaded stage (see Figure B).

The TC output is subject to decoding spikes due to internal race conditions. Therefore, it is not recommended for use as clock or asynchronous reset for flip-flops, registers, or counters.

STATE DIAGRAMS

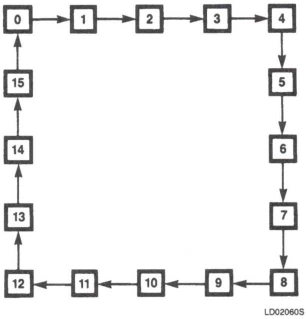
Logic Equations: Count Enable = CEP•CET•PE
TC = $Q_0 \cdot \overline{Q}_1 \cdot Q_2 \cdot Q_3 \cdot$CET

'F160A, 'F162A

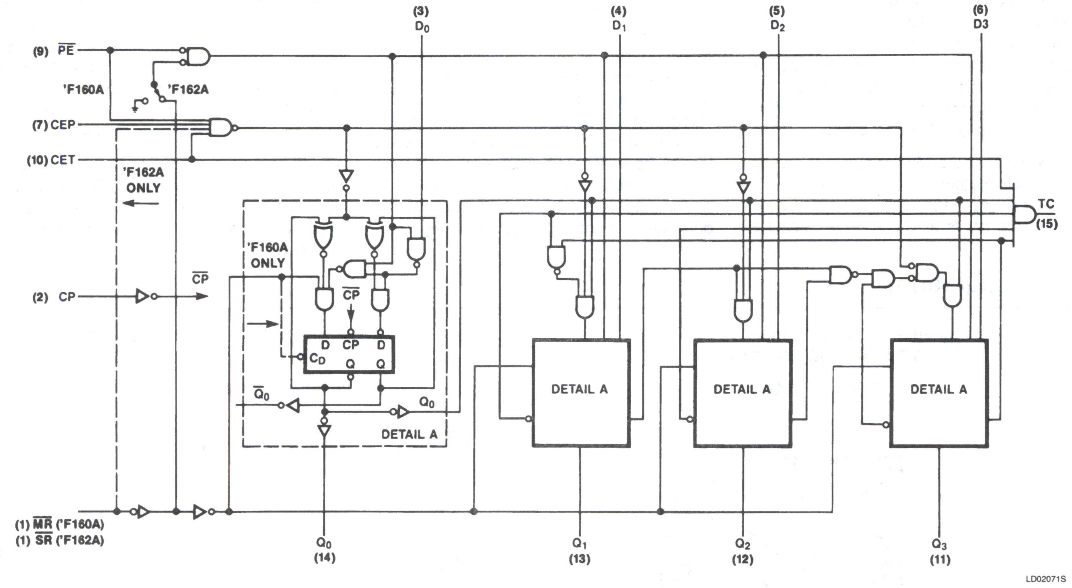


Logic Equations: Count Enable = CEP•CET•PE
TC = $Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot$CET

'F161A, 'F163A

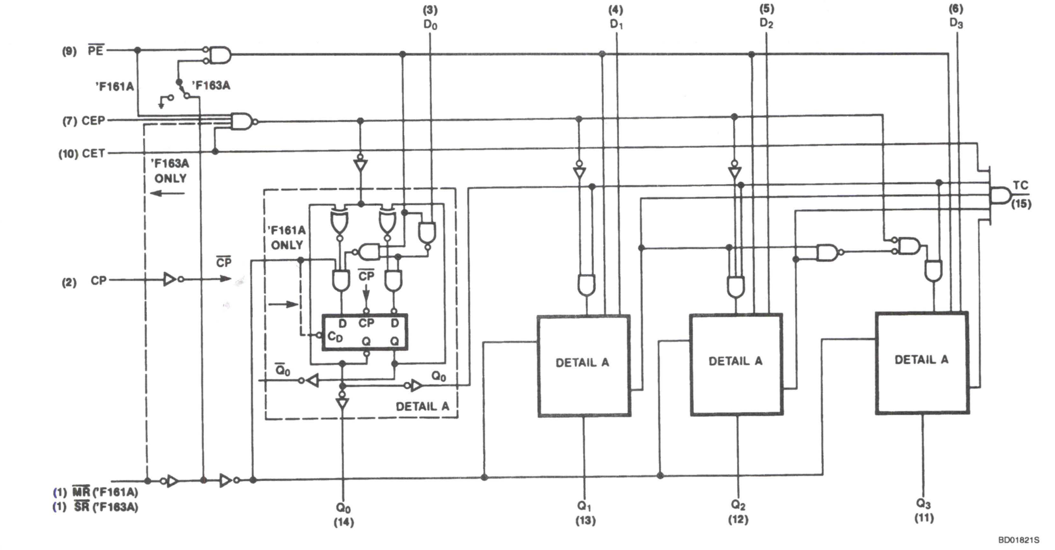


LOGIC DIAGRAM, 'F160A, 'F162A


(3) D0
(4) D1
(5) D2
(6) D3
(9) PE
'F160A
'F162A
(7) CEP
(10) CET
'F162A ONLY
'F160A ONLY
CP
(2) CP
D CP D
CD Q Q
Q0
Q0
DETAIL A
DETAIL A
DETAIL A
DETAIL A
TC
(15)
(1) MR ('F160A)
(1) SR ('F162A)
Q0 (14)
Q1 (13)
Q2 (12)
Q3 (11)
LD02071S

V_{CC} = Pin16
GND = Pin 8
( ) = Pin numbers

LOGIC DIAGRAM, 'F161A, 'F163A


(3) D0
(4) D1
(5) D2
(6) D3
(9) PE
'F161A
'F163A
(7) CEP
(10) CET
'F163A ONLY
'F161A ONLY
CP
(2) CP
CP
D CP D
CD Q Q
Q0
Q0
DETAIL A
DETAIL A
DETAIL A
DETAIL A
TC
(15)
(1) MR ('F161A)
(1) SR ('F163A)
Q0 (14)
Q1 (13)
Q2 (12)
Q3 (11)
BD01821S

V_{CC} = Pin16
GND = Pin 8
( ) = Pin numbers

MODE SELECT — FUNCTION TABLE, 'F160A, 'F161A

OPERATING MODE	INPUTS						OUTPUTS	
	$\overline{MR}$	CP	CEP	CET	$\overline{PE}$	D_n	Q_n	TC
Reset (clear)	L	X	X	X	X	X	L	L
Parallel load	H	↑	X	X	l	l	L	L
	H	↑	X	X	l	h	H	(1)
Count	H	↑	h	h	h	X	count	(1)
Hold (do nothing)	H	X	l	X	h	X	q_n	(1)
	H	X	X	l(2)	h	X	q_n	L

MODE SELECT — FUNCTION TABLE, 'F162A, 'F163A

OPERATING MODE	INPUTS						OUTPUTS	
	$\overline{SR}$	CP	CEP	CET	$\overline{PE}$	D_n	Q_n	TC
Reset (clear)	l	↑	X	X	X	X	L	L
Parallel load	h	↑	X	X	l	l	L	L
	h	↑	X	X	l	h	H	(2)
Count	h	↑	h	h	h	X	count	(2)
Hold (do nothing)	h	X	l	X	h	X	q_n	(2)
	h	X	X	l	h	X	q_n	L

H = High voltage level steady state.
L = Low voltage level steady state.
h = High voltage level one setup time prior to the Low-to-High clock transition.
l = Low voltage level one setup time prior to Low-to-High clock transition.
X = Don't care.
q = Lower case letters indicate the state of the referenced output prior to the Low-to-High clock transition.
↑ = Low-to-High clock transition.

NOTES:

(1) The TC output is High when CET is High and the counter is at Terminal Count (HHHH for 'F161A and HLLH for 'F160A).

(2) The TC output is High when CET is High and the counter is at Terminal Count (HLLH for 'F162A and HHHH for 'F163A).

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.50	5.0	5.50	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX V_{IH} = MIN,	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OL} = MAX V_{IH} = MIN,	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	High-level input current	$\overline{CET}$, $\overline{SR}$, $\overline{PE}$	V_{CC} = MAX, V_I = 2.7V				40	μA
		Other inputs					20	μA
I_{IL}	Low-level input current	$\overline{CET}$, $\overline{SR}$, $\overline{PE}$	V_{CC} = MAX, V_I = 0.5V				−1.2	mA
		Other inputs				−0.4	−0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current[4] (total)	I_{CCH}	V_{CC} = MAX			42	55	mA
		I_{CCL}				49	65	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of High-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. I_{CCH} is measured with $\overline{PE}$ input High, again with $\overline{PE}$ input Low, all other inputs High and outputs open. I_{CCL} is measured with Clock input High, again with Clock input Low all other inputs Low, and outputs open.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	74F160A, 74F162A					UNIT
				$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
				Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency		Waveform 1	100	130		90		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n		Waveform 1 $\overline{PE}$ = High	2.0 4.0	4.5 7.0	7.0 10.0	2.0 4.0	8.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to Q_n		Waveform 1 $\overline{PE}$ = Low	2.0 4.0	4.5 6.0	7.5 8.5	2.0 4.0	8.5 9.5	ns
t_{PLH} t_{PHL}	Propagation delay CP to TC		Waveform 1	4.5 4.5	10 10	10.5 9.5	4.5 4.5	15 15	ns
t_{PLH} t_{PHL}	Propagation delay CET to TC		Waveform 2	1.5 2.5	4.5 4.5	6.5 7.0	1.5 2.5	8.5 8.5	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	'F160A	Waveform 3	6.5	9.0	12	6.5	13	ns
t_{PHL}	Propagation delay $\overline{MR}$ to TC	'F160A	Waveform 3	6.0	8.0	10.0	5.5	11.0	ns

AC SETUP REQUIREMENTS

SYMBOL	PARAMETER		TEST CONDITIONS	74F160A, 74F162A					UNIT
				$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
				Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to CP		Waveform 5	5.0 5.0			5.5 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to CP		Waveform 5	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{PE}$ or $\overline{SR}$ to CP		Waveform 5 or 6	11 7.0			11.0 7.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{PE}$ or $\overline{SR}$ to CP		Waveform 5 or 6	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low CEP or CET to CP		Waveform 4	11.0 6.0			11.0 7.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low CEP or CET to CP		Waveform 4	0 0			0 0		ns
$t_W(H)$ $t_W(L)$	Clock pulse width (load), High or Low		Waveform 1	4.0 5.0			4.0 6.5		ns
$t_W(H)$ $t_W(L)$	Clock pulse width (count), High or Low		Waveform 1	4.0 5.5			4.0 6.0		ns
$t_W(L)$	$\overline{MR}$ pulse width Low	'F160A	Waveform 3	5.0			5.0		ns
t_{rec}	Recovery time, $\overline{MR}$ to CP	'F160A	Waveform 3	5.0			6.0		ns

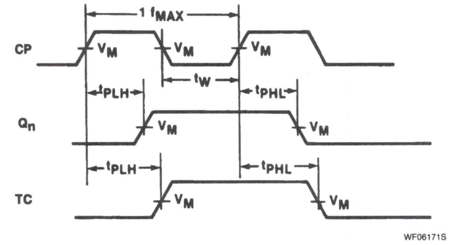
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	74F161A, 74F163A					UNIT
				$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
				Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency		Waveform 1	100	130		90		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n		Waveform 1 $\overline{PE}$ = High	2.0 4.0	4.0 6.5	6.5 10.5	2.0 4.0	7.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to Q_n		Waveform 1 $\overline{PE}$ = Low	2.0 3.5	4.5 5.5	6.5 8.5	2.0 3.5	7.5 9.5	ns
t_{PLH} t_{PHL}	Propagation delay CP to TC		Waveform 1	5.0 4.5	7.5 7.5	10.5 10.5	5.0 4.0	11.5 11.5	ns
t_{PLH} t_{PHL}	Propagation delay CET to TC		Waveform 2	1.5 2.5	3.5 5.0	6.5 7.5	1.5 2.5	7.0 8.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	'F161A	Waveform 3	6.5	8.5	12.5	5.5	13	ns
t_{PHL}	Propagation delay $\overline{MR}$ to TC	'F161A	Waveform 3	6.0	8.5	11.0	5.0	12.0	ns

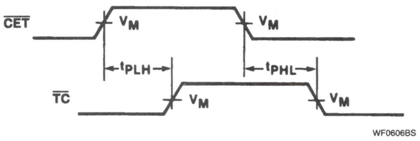
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER		TEST CONDITIONS	74F161A, 74F163A					UNIT
				$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
				Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to CP		Waveform 5	5.0 5.0			5.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to CP		Waveform 5	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{PE}$ or $\overline{SR}$ to CP		Waveform 5 or 6	9.0 6.5			9.5 7.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{PE}$ or $\overline{SR}$ to CP		Waveform 5 or 6	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low CEP or CET to CP		Waveform 4	10.5 7.0			10.5 7.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low CEP or CET to CP		Waveform 4	0 0			0 0		ns
$t_W(H)$ $t_W(L)$	Clock pulse width (load), High or Low		Waveform 1	4.0 5.0			4.0 5.5		ns
$t_W(H)$ $t_W(L)$	Clock pulse width (count), High or Low		Waveform 1	4.0 6.0			4.0 7.0		ns
$t_W(L)$	$\overline{MR}$ pulse width Low	'F161A	Waveform 3	4.5			4.5		ns
t_{rec}	Recovery time, $\overline{MR}$ to CP	'F161A	Waveform 3	6.0			6.5		ns

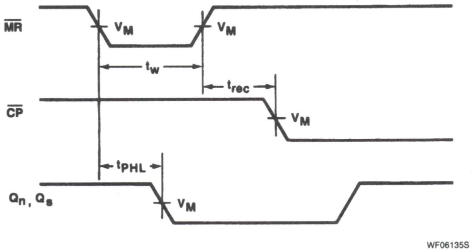
AC WAVEFORMS


1 fMAX
CP
VM
tW
tPLH
tPHL
Qn
TC
WF06171S

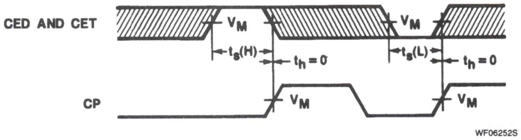
Waveform 1. Clock to Output Delays, Maximum Clock Frequency, and Clock Pulse Width


CET
VM
tPLH
tPHL
TC
WF0606BS

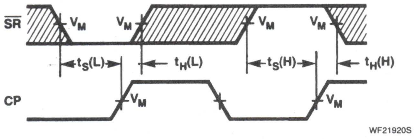
Waveform 2. Propagation Delays CET Input to TC Output

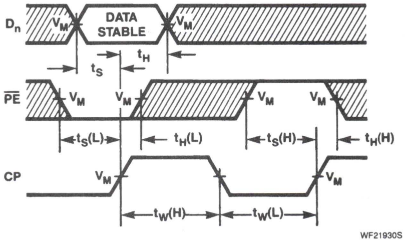

MR
VM
tw
trec
CP
tPHL
Qn, Qs
WF06135S

Waveform 3. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time ('F160A, 'F161A)


CED AND CET
VM
ts(H)
th = 0
ts(L)
CP
WF06252S

Waveform 4. CEP and CET Setup and Hold Times


SR
VM
ts(L)
tH(L)
ts(H)
tH(H)
CP
WF21920S

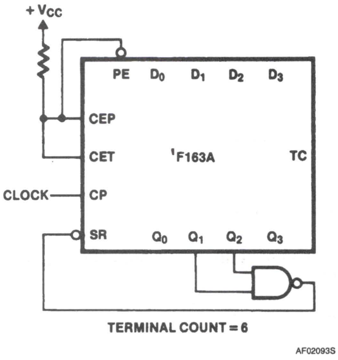

Dn
VM
DATA STABLE
ts
tH
PE
ts(L)
tH(L)
ts(H)
tH(H)
CP
tW(H)
tW(L)
WF21930S

Waveform 5. Synchronous Reset Setup and Hold Times

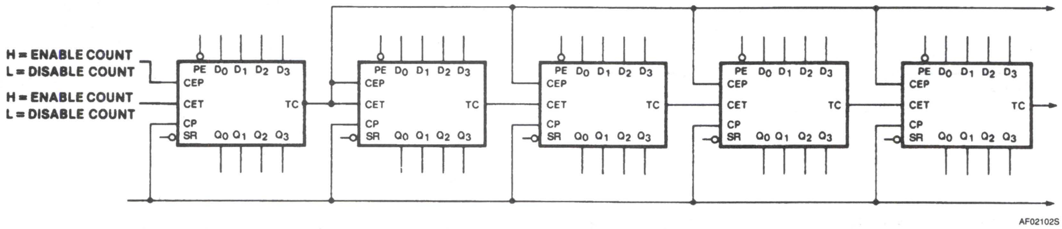
Waveform 6. Parallel Data and Parallel Enable Setup and Hold Times

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

APPLICATION

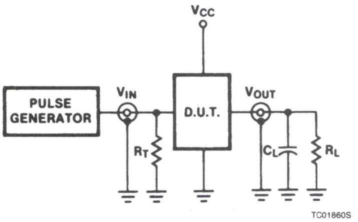

+VCC
PE
D0
D1
D2
D3
CEP
CET
'F163A
TC
CLOCK
CP
SR
Q0
Q1
Q2
Q3
TERMINAL COUNT = 6
AF02093S

a.

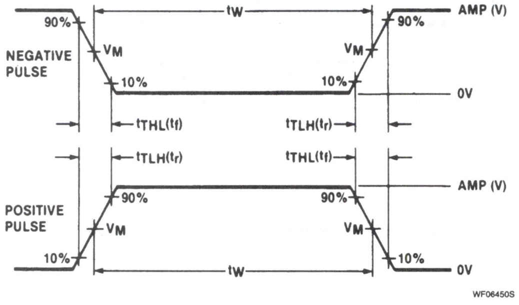

H = ENABLE COUNT
L = DISABLE COUNT
H = ENABLE COUNT
L = DISABLE COUNT
PE D0 D1 D2 D3
CEP
CET
TC
CP
SR
Q0 Q1 Q2 Q3
AF02102S

b. Synchronous Multistage Counting Scheme

TEST CIRCUIT AND WAVEFORMS


VCC
PULSE GENERATOR
VIN
D.U.T.
VOUT
RT
CL
RL
TC01860S

Test Circuit for Totem-Pole Outputs


NEGATIVE PULSE
90%
VM
10%
tW
AMP (V)
0V
tTHL(tf)
tTLH(tr)
POSITIVE PULSE
AMP (V)
0V
WF06450S

$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS

R_L = Load resistor to GND; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F164
Shift Register

8-Bit Serial-In Parallel-Out Shift Register
Preliminary Specification

FAST Products

FEATURES

- **Gated serial data inputs**
- **Typical shift frequency of 100MHz**
- **Asynchronous Master Reset**
- **Fully buffered Clock and Data inputs**
- **Fully synchronous data transfers**

DESCRIPTION

The 'F164 is an 8-bit edge-triggered shift register with serial data entry and an output from each of the eight stages. Data is entered serially through one of two inputs ($D_{sa} \cdot D_{sb}$); either input can be used as an active-High enable for data entry though the other input. Both inputs must be connected together or an unused input must be tied High.

Data shifts one place to the right on each Low-to-High transition of the Clock (CP) input, and enters into Q_0 the logical AND of the two Data inputs ($D_{sa} \cdot D_{sb}$) that existed one setup time before the rising clock edge. A Low level on the Master Reset ($\overline{MR}$) input overrides all other inputs and clears the register asynchronously, forcing all outputs Low.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F164	100MHz	33mA

ORDERING INFORMATION

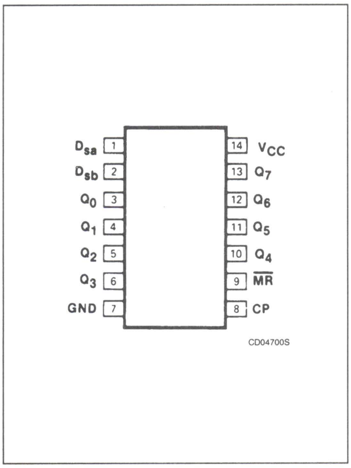
PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
14-Pin Plastic DIP	N74F164N
14-Pin Plastic SO	N74F164D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

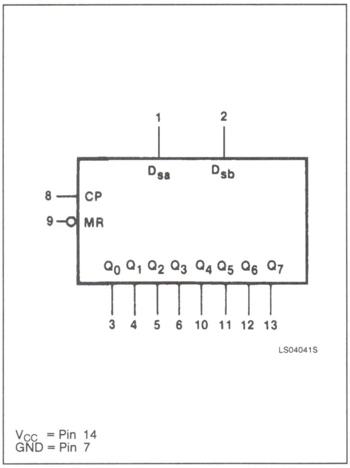
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_{sa}, D_{sb}	Data inputs	1.0/1.0	20µA/0.6mA
CP	Clock Pulse input (active rising edge)	1.0/1.0	20µA/0.6mA
$\overline{MR}$	Master Reset input (active-Low)	1.0/1.0	20µA/0.6mA
$Q_0 - Q_7$	Outputs	50/33	1.0mA/20mA

NOTE:
1. One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION

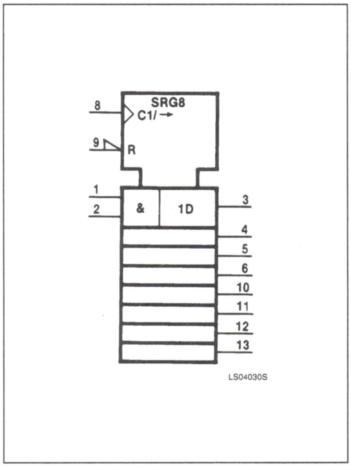


LOGIC SYMBOL



V_{CC} = Pin 14
GND = Pin 7

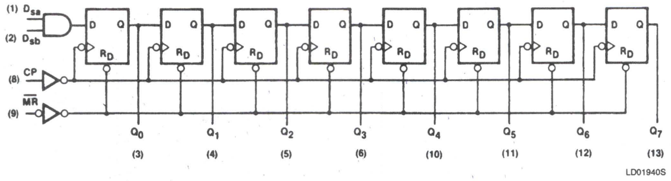
LOGIC SYMBOL (IEEE/IEC)



Shift Register

FAST 74F164

LOGIC DIAGRAM


(1) D_{sa}
(2) D_{sb}
(8) CP
(9) $\overline{MR}$
D
Q
R_D
Q_0
Q_1
Q_2
Q_3
Q_4
Q_5
Q_6
Q_7
(3)
(4)
(5)
(6)
(10)
(11)
(12)
(13)
LD01940S

V_{CC} = Pin 14
GND = Pin 7

MODE SELECT—TRUTH TABLE

OPERATING MODE	INPUTS				OUTPUTS			
	$\overline{MR}$	CP	D_{sa}	D_{sb}	Q_0	Q_1	—	Q_7
Reset (clear)	L	X	X	X	L	L	—	L
Shift	H	↑	l	l	L	q_0	—	q_6
	H	↑	l	h	L	q_0	—	q_6
	H	↑	h	l	L	q_0	—	q_6
	H	↑	h	h	H	q_0	—	q_6

H = High voltage level.
h = High voltage level one set-up time prior to the Low-to-High Clock transition.
L = Low voltage level.
l = Low voltage level one set-up time prior to the Low-to-High Clock transition.
q = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the Low-to-High Clock transition.
X = Don't care.
↑ = Low-to-High Clock transition.

Shift Register FAST 74F164

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

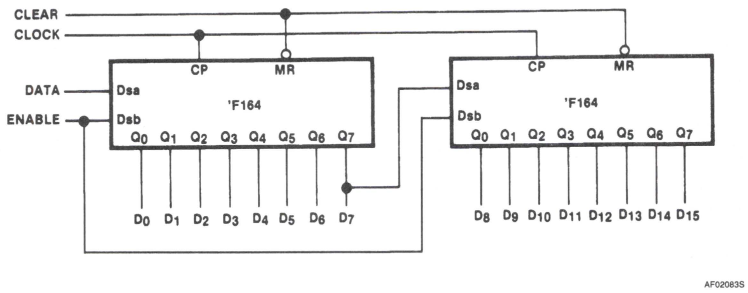
SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX V_{IH} = MIN,	±10%V_{CC}	2.5			V
			±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, I_{OL} = MAX V_{IH} = MIN,	±10%V_{CC}		0.35	0.50	V
			±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, $I_I = I_{IK}$				-1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX			33	55	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Measure I_{CC} with the serial inputs grounded, the clock input at 2.4V, and a momentary ground, then 4.5V applied to Master Reset, and all outputs open.

Shift Register　FAST 74F164

APPLICATION



NOTES:
The 'F164 can be cascaded to form synchronous shift registers of longer length.
Here, two devices are combined to form a 16-bit shift register.

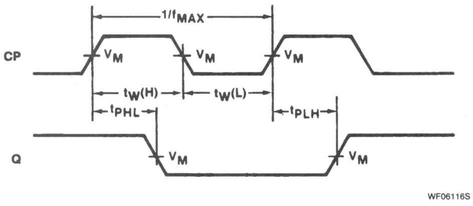
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F164 $T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50pF$, $R_L = 500\Omega$ Min	Typ	Max	74F164 $T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$ Min	Max	UNIT
f_{MAX}	Maximum shift frequency	Waveform 1	80	100		80		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	Waveform 1	3.0 5.0	5.0 7.0	8.0 10	2.5 5.0	9.0 11	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	Waveform 2	4.0	7.5	10.5	4.0	11.5	ns

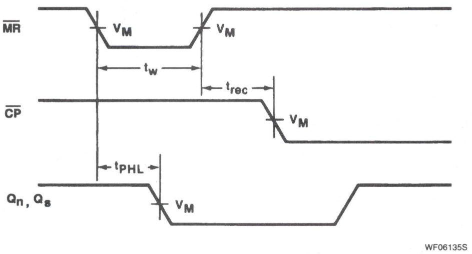
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	74F164 $T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50pF$, $R_L = 500\Omega$ Min	Typ	Max	74F164 $T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$ Min	Max	UNIT
$t_s(H)$ $t_s(L)$	Setup time, High or Low A or B to CP	Waveform 3	7.0 7.0			7.0 7.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low A or B to CP		1.0 1.0			1.0 1.0		ns
$t_w(H)$ $t_w(L)$	CP pulse width, High or Low	Waveform 1	4.0 7.0			4.0 7.0		ns
$t_w(L)$	$\overline{MR}$ pulse width Low	Waveform 2	7.0			7.0		ns
t_{rec}	Recovery time $\overline{MR}$ to CP	Waveform 2	7.0			7.0		ns

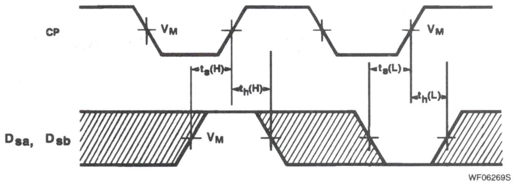
AC WAVEFORMS


1/fMAX
CP
VM
VM
VM
tW(H)
tW(L)
tPHL
tPLH
Q
VM
VM
WF06116S

Waveform 1. Clock to Output Delays And Clock Pulse Width


MR
VM
VM
tw
trec
CP
VM
tPHL
Qn, Qs
VM
WF06135S

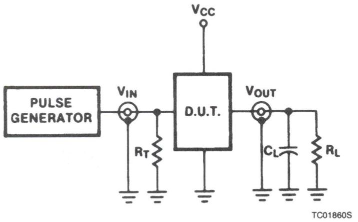
Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time


CP
VM
VM
ts(H)
th(H)
ts(L)
th(L)
Dsa, Dsb
VM
WF06269S

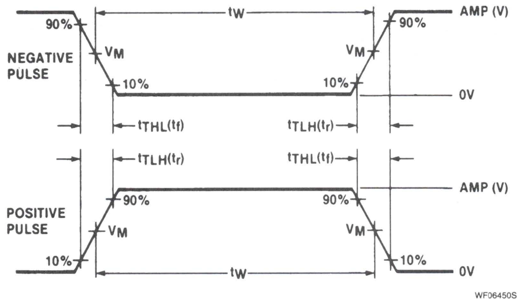
Waveform 3. Data Setup and Hold Times

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORM


VCC
PULSE GENERATOR
VIN
D.U.T.
VOUT
RT
CL
RL
TC01860S

Test Circuit for Totem-Pole Outputs


tW
90%
90%
AMP (V)
NEGATIVE PULSE
VM
VM
10%
10%
0V
tTHL(tf)
tTLH(tr)
tTLH(tr)
tTHL(tf)
AMP (V)
90%
90%
POSITIVE PULSE
VM
VM
10%
10%
tW
0V
WF06450S

$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F166
Shift Register

8-Bit Serial/Parallel-In, Serial Out Shift Register
Product Specification

FAST Products

FEATURES

- **High-impedance NPN base inputs for reduced loading (20µA in High and Low states)**
- **Synchronous parallel to serial applications**
- **Synchronous serial data input for easy expansion**
- **Clock enable for "do nothing" mode**
- **Asynchronous Master Reset**
- **Exandable to 16-bits in 8-bit increments**

DESCRIPTION

The 166 is a high-speed 8-bit shift register that has fully synchronous serial parallel data entry selected by an active-Low Parallel Enable ($\overline{PE}$) input. When the $\overline{PE}$ is Low one setup time before the Low-to-High clock transistion, parallel data is entered into the register. When $\overline{PE}$ is High, data is entered into internal bit position Q_0 from Serial Data Input (D_s), and the remaining bits are shifted one place to the right ($Q_0 - Q_1 - Q_2$, etc.), with each positive-going clock transition.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F166	175MHz	41mA

ORDERING INFORMATION

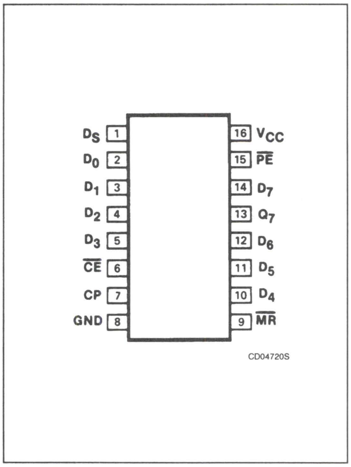
PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
16-Pin Plastic DIP	N74F166N
16-Pin Plastic SO	N74F166D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$\overline{PE}$	Parallel enable input	1/0.033	20µA/20µA
$\overline{CE}$	Clock enable input	1/0.033	20µA/20µA
CP	Clock input (active rising edge)	1/0.033	20µA/20µA
D_s	Serial data input	2/0.066	40µA/40µA
$D_0 - D_7$	Parallel data input	1/0.033	20µA/20µA
$\overline{MR}$	Master Reset input (active-Low)	2/0.066	40µA/40µA
Q_7	Output	50/33	1.0mA/20mA

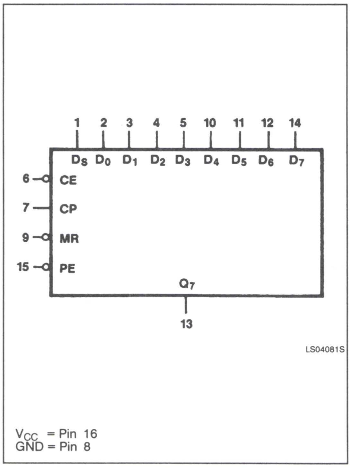
NOTE:
1. One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



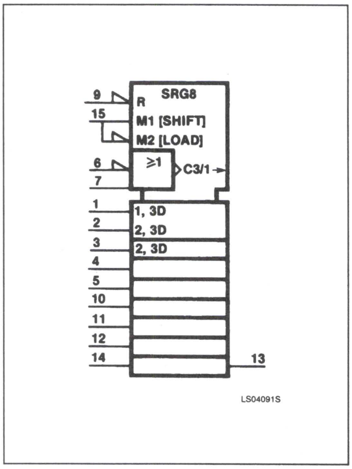
DS 1
D0 2
D1 3
D2 4
D3 5
CE 6
CP 7
GND 8
16 VCC
15 PE
14 D7
13 Q7
12 D6
11 D5
10 D4
9 MR
CD04720S

LOGIC SYMBOL



1 2 3 4 5 10 11 12 14
DS D0 D1 D2 D3 D4 D5 D6 D7
6 CE
7 CP
9 MR
15 PE
Q7
13
LS04081S
VCC = Pin 16
GND = Pin 8

LOGIC SYMBOL (IEEE/IEC)



SRG8
9 R
15 M1 [SHIFT]
M2 [LOAD]
6 ≥1
7
C3/1→
1 1, 3D
2 2, 3D
3 2, 3D
4
5
10
11
12
14
13
LS04091S

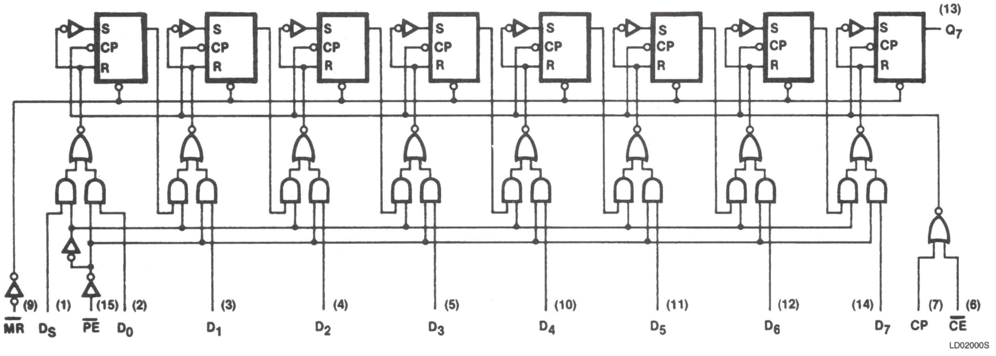
For expansion of the register in parallel to serial converters, the Q_7 output is connected to the D_S input of the succeeding stage. The clock input is a gated OR structure which allows one input to be used as an active-Low Clock Enable ($\overline{CE}$) input. The pin assignment for the CP and $\overline{CE}$ inputs is arbitrary and can be reversed for layout convenience. The Low-to-High transition of $\overline{CE}$ input should only take place while the CP is High for predictable operation. A Low on the Master Reset ($\overline{MR}$) input overrides all other inputs and clears the register asynchronously, forcing all bit positions to a Low state.

MODE SELECT — FUNCTION TABLE

OPERATING MODES	INPUTS					Q_n REGISTER		OUTPUT
	$\overline{PE}$	$\overline{CE}$	CP	D_S	D_0-D_7	Q_0	Q_1-Q_6	Q_7
Parallel load	l l	l l	↑ ↑	X X	l – l h – h	L H	L – L H – H	L H
Serial shift	h h	l l	↑ ↑	l h	X – X X – X	L H	q_0-q_5 q_0-q_5	q_6 q_6
Hold (do nothing)	X	h	X	X	X – X	q_0	q_1-q_6	q_7

H = High voltage level.
h = High voltage level one setup time prior to the Low-to-High Clock transition.
L = Low voltage level.
l = Low voltage level one setup time prior to the Low-to-High Clock transition.
q_n = Lower case letters indicate the state of the referenced input (or output) one setup time prior to the Low-to-High Clock transition.
X = Don't care.
↑ = Low-to-High Clock transition.

LOGIC DIAGRAM



( ) = Pin number
V_{CC} = Pin 16
GND = Pin 8

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.35	0.5	V
				±5%V_{CC}		0.35	0.5	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$			−0.73	−1.2	V
I_I	Input current at maximum input voltage	Others	V_{CC} = 0.0V, V_I = 7.0V				100	μA
		$\overline{CE}$, CP[3]					100	μA
I_{IH}	High-level input current	Others	V_{CC} = MAX, V_I = 2.7V				20	μA
		$\overline{MR}$, D_S					40	μA
I_{IL}	Low-level input current	Others	V_{CC} = MAX, V_I = 0.5V				−20	μA
		$\overline{MR}$, D_S					−40	μA
I_{OS}	Short-circuit output current[4]		V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current[4] (total)		V_{CC} = MAX; $\overline{MR} = D_S$ = 4.5V; $D_n = \overline{PE} = \overline{CE}$ = GND, CP = ↑			41	60	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. When testing CP, $\overline{CE}$ must remain in High state, whereas CP must remain in High state when testing $\overline{CE}$.
4. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

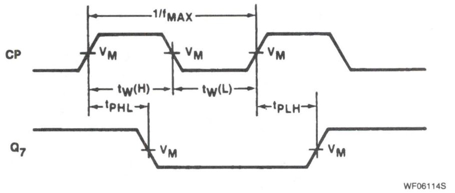
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F166					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum shift frequency	Waveform 1	135	175		110		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_7	Waveform 1	5.0 4.0	7.5 6.0	10.0 8.0	5.0 3.5	14.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{MR}$ to Q_7	Waveform 2	4.0	6.5	8.5	4.0	9.5	ns

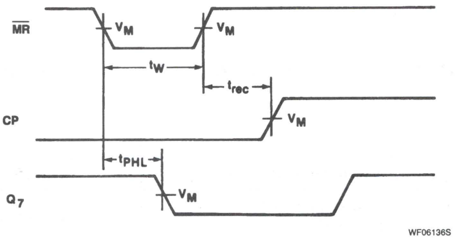
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	74F166					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n, D_s to CP	Waveform 3	2.5 2.5			3.0 3.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n, D_s to CP	Waveform 3	0 0			0 0		ns
$t_s(L)$	Setup time, High or Low $\overline{CE}$ to CP	Waveform 3	5.0			6.0		ns
$t_h(H)$	Hold time, High or Low $\overline{CE}$ to CP	Waveform 3	0			0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{PE}$ to CP	Waveform 3	3.0 3.0			4.0 4.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{PE}$ to CP	Waveform 3	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	CP pulse width, High or Low	Waveform 1	3.5 5.5			3.5 6.5		ns
$t_w(L)$	$\overline{MR}$ pulse width Low	Waveform 2	4.0			4.0		ns
t_{rec}	Recovery time $\overline{MR}$ to CP	Waveform 2	4.0			4.5		ns

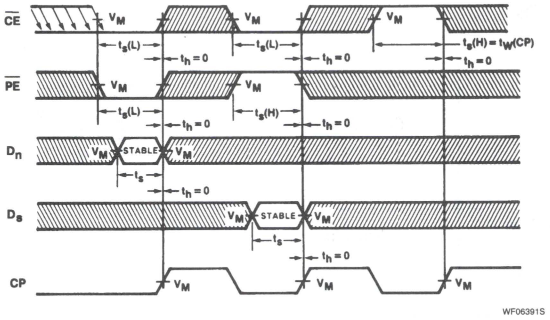
AC WAVEFORMS


CP
Q7
1/fMAX
VM
tW(H)
tW(L)
tPHL
tPLH
WF06114S

Waveform 1. Clock to Output Delays and Clock Pulse Width


MR
CP
Q7
VM
tW
trec
tPHL
WF06136S

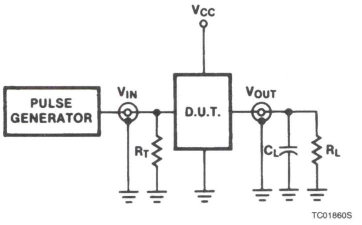
Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time


CE
PE
Dn
Ds
CP
VM
ts(L)
th = 0
ts(H)
ts(H) = tW(CP)
STABLE
ts
WF06391S

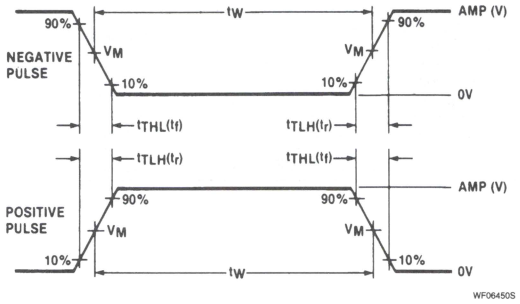
Waveform 3. Setup and Hold Time for PE, D_n, D_s, and $\overline{CE}$ to CP

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable performance.

TEST CIRCUIT AND WAVEFORMS


VCC
PULSE GENERATOR
VIN
D.U.T.
VOUT
RT
CL
RL
TC01860S

Test Circuit for Totem-Pole Outputs


NEGATIVE PULSE
POSITIVE PULSE
90%
10%
VM
tW
tTHL(tf)
tTLH(tr)
AMP (V)
0V
WF06450S

V_M = 1.5V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F168, 74F169

Counters

'F168 — 4-Bit Up/Down BCD Decade Synchronous Counter

Product Specification

FAST Products

FEATURES

- Synchronous counting and loading
- Up/Down counting
- Modulo 16 binary counter — 'F169
- BCD decade counter — 'F168
- Two Count Enable inputs for n-bit cascading
- Positive edge-triggered Clock
- Built-in look-ahead carry capability
- Presettable for programmable operation

DESCRIPTION

The 'F168 is a synchronous, presettable BCD decade up/down counter featuring an internal Carry look-ahead for applications in high-speed counting designs. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the Count Enable inputs and internal gating. This mode of operation eliminates the output spikes which are normally associated with asynchronous (ripple clock) counters. A buffered Clock input triggers the flip-flops on the Low-to-High transition of the clock.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F168	115MHz	35mA
74F169	115MHz	35mA

ORDERING INFORMATION

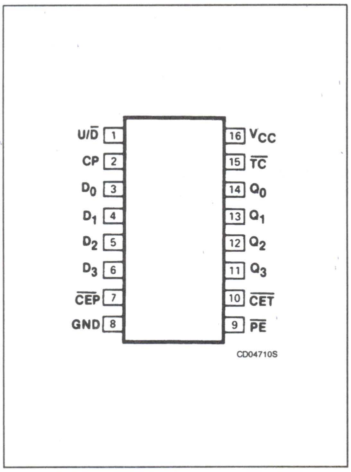
PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
16-Pin Plastic DIP	N74F168N, N74F169N
16-Pin Plastic SO	N74F168D, N74F169D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

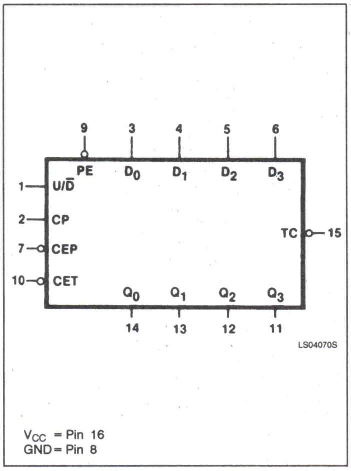
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$\overline{CEP}$	Count enable parallel input (active-Low)	1.0/1.0	20μA/0.6mA
$\overline{CET}$	Count enable trickle input (active-Low)	1.0/2.0	20μA/1.2mA
CP	Clock Pulse input (active rising edge)	1.0/1.0	20μA/0.6mA
$D_0 - D_3$	Parallel data inputs	1.0/1.0	20μA/0.6mA
$\overline{PE}$	Parallel enable input (active-Low)	1.0/1.0	20μA/0.6mA
$U/\overline{D}$	Up/down count control input	1.0/1.0	20μA/0.6mA
$Q_0 - Q_3$	Flip-flop outputs	50/33	1.0mA/20mA
$\overline{TC}$	Terminal count output (active-Low)	50/33	1.0mA/20mA

NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

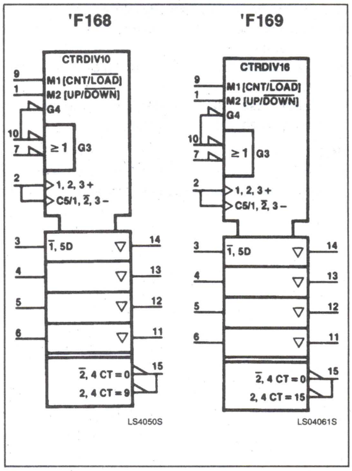
PIN CONFIGRATION


U/D̄ 1
CP 2
D0 3
D1 4
D2 5
D3 6
CEP̄ 7
GND 8
16 VCC
15 TC̄
14 Q0
13 Q1
12 Q2
11 Q3
10 CET̄
9 PĒ
CD04710S

LOGIC SYMBOL


9
3
4
5
6
PE
D0
D1
D2
D3
1 U/D̄
2 CP
7 CEP
10 CET
TC 15
Q0
Q1
Q2
Q3
14
13
12
11
LS04070S
VCC = Pin 16
GND = Pin 8

LOGIC SYMBOL (IEEE/IEC)


'F168
'F169
CTRDIV10
CTRDIV16
M1 [CNT/LOAD̄]
M2 [UP/DOWN̄]
G4
≥1
G3
1, 2, 3 +
C5/1, 2̄, 3 −
1̄, 5D
2̄, 4 CT = 0
2, 4 CT = 9
2, 4 CT = 15
9
1
10
7
2
3
4
5
6
14
13
12
11
15
LS4050S
LS04061S

The counter is fully programmable; that is, the outputs may be preset to either level.

Presetting is synchronous with the clock and takes place regardless of the levels of the Count Enable inputs. A Low level on the Parallel Enable ($\overline{PE}$) input disables the counter and causes the data at the D_n input to be loaded into the counter on the next Low-to-High transition of the clock.

The direction of counting is controlled by the Up/Down ($U/\overline{D}$) input; a High will cause the count to increase, a Low will cause the count to decrease.

The Carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two Count Enable inputs ($\overline{CET}\bullet\overline{CEP}$) and a Terminal Count ($\overline{TC}$) output. Both Count Enable inputs must be Low to count. The $\overline{CET}$ input is fed forward to enable the $\overline{TC}$ output. The $\overline{TC}$ output thus enabled will produce a Low output pulse with a duration approximately equal to the High level portion of the Q_0 output. This Low level $\overline{TC}$ pulse is used to enable successive cascaded stages. See Figure 1 for the fast synchronous multi-stage counting connections.

The 'F169A is identical except that it is a Modulo 16 counter.

FUNCTIONAL DESCRIPTION

The 'F168 and 'F169 use edge-triggered J-K-type flip-flops and have no constraints on changing the control or data input signals in either state of the Clock. The only requirement is that the various inputs attain the desired state at least a setup time before the rising edge of the Clock and remain valid for the recommended hold time thereafter. The parallel load operation takes precedence over the other operations, as indicated in the Mode Select Table. When $\overline{PE}$ is Low, the data on the $D_0 - D_3$ inputs enter the flip-flops on the next rising edge of the Clock. In order for counting to occur, both $\overline{CEP}$ and $\overline{CET}$ must be Low and $\overline{PE}$ must be High; the $U/\overline{D}$ input then determines the direction of counting. The Terminal Count ($\overline{TC}$) output is normally High and goes Low, provided that $\overline{CET}$ is Low, when a counter reaches zero in the Count Down mode or reaches 9 (15 for the 'F169) in the Count Up mode. The $\overline{TC}$ output state is not a function of the Count Enable Parallel ($\overline{CEP}$) input level. The $\overline{TC}$ output of the 'F168 decade counter can also be Low in the illegal states 11, 13 and 15, which can occur when power is turned on or via parallel loading. If an illegal state occurs, the 'F168 will return to the legitimate sequence within two counts. Since the $\overline{TC}$ signal is derived by decoding the flip-flop states, there exists the possibility of decoding spikes on $\overline{TC}$. For this reason the use of $\overline{TC}$ as a clock signal is not recommended (see logic equations below).

1) Count Enable = $\overline{CEP}\cdot\overline{CET}\cdot\overline{PE}$
2) Up: $\overline{TC} = Q_0\cdot Q_3\cdot(U/\overline{D})\cdot\overline{CET}$

3) Down: $\overline{TC} = Q_0\cdot Q_1\cdot Q_2\cdot Q_3\cdot(U/\overline{D})$
$\cdot\overline{CET}$

MODE SELECT TABLE

$\overline{PE}$	$\overline{CEP}$	$\overline{CET}$	$U/\overline{D}$	ACTION ON RISING CLOCK EDGE
L	X	X	X	Load ($D_n \rightarrow Q_n$)
H	L	L	H	Count Up (Increment)
H	L	L	L	Count Down (Decrement)
H	H	X	X	No Change (Hold)
H	X	H	X	No Change (Hold)

H = High Voltage Level
L = Low Voltage Level
X = Don't care

MODE SELECT — FUNCTION TABLE

OPERATING MODE	INPUTS						OUTPUTS	
	CP	$U/\overline{D}$	$\overline{CEP}$	$\overline{CET}$	$\overline{PE}$	D_n	Q_n	$\overline{TC}$
Parallel load	↑	X	X	X	l	l	L	(1)
	↑	X	X	X	l	h	H	(1)
Count up	↑	h	l	l	h	X	Count Up	(1)
Count down	↑	l	l	l	h	X	Count Down	(1)
Hold (do nothing)	↑	X	h	X	h	X	q_n	(1)
	↑	X	X	h	h	X	q_n	H

H = High voltage level steady state
h = High voltage level one setup time prior to the Low-to-High clock transition
L = Low voltage level steady state
l = Low voltage level one setup time prior to the Low-to-High clock transition
X = Don't care
q = Lower case letters indicate the state of the referenced output prior to the Low-to-High clock transition.
↑ = Low-to-High clock transition

NOTE:

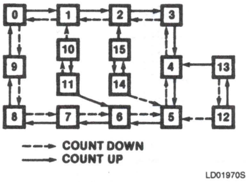
1. The $\overline{TC}$ is Low when $\overline{CET}$ is Low and the counter is at Terminal Count. Terminal Count Up is (HHHH) and Terminal Count Down is (LLLL) for 'F169.
The $\overline{TC}$ is Low when $\overline{CET}$ is Low and the counter is at Terminal Count. Terminal Count Up is (HLLH) and Terminal Count Down is (LLLL) for 'F168.

Counters

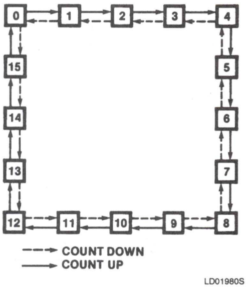
FAST 74F168, 74F169

STATE DIAGRAMS

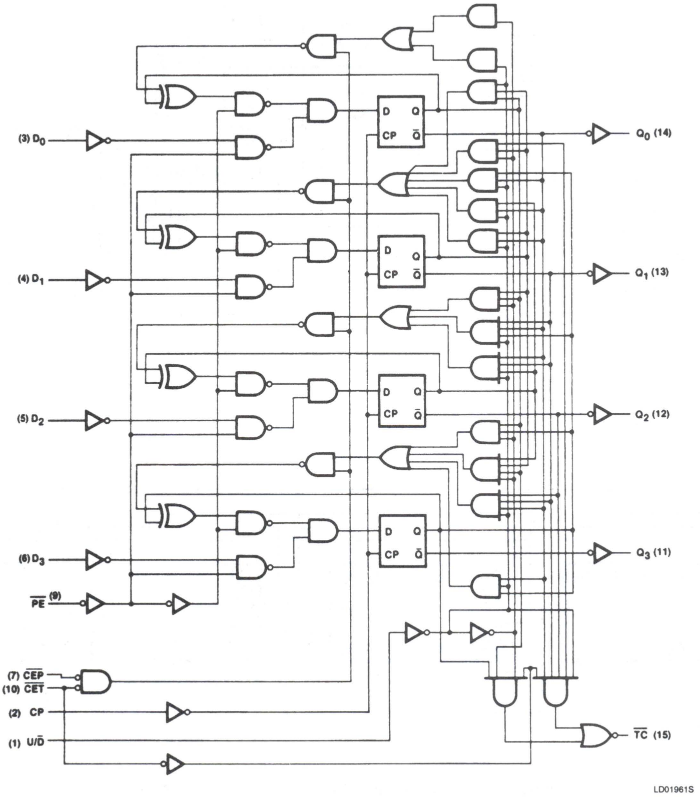
'F168


0
1
2
3
9
10
15
4
13
11
14
8
7
6
5
12
COUNT DOWN
COUNT UP
LD01970S

'F169

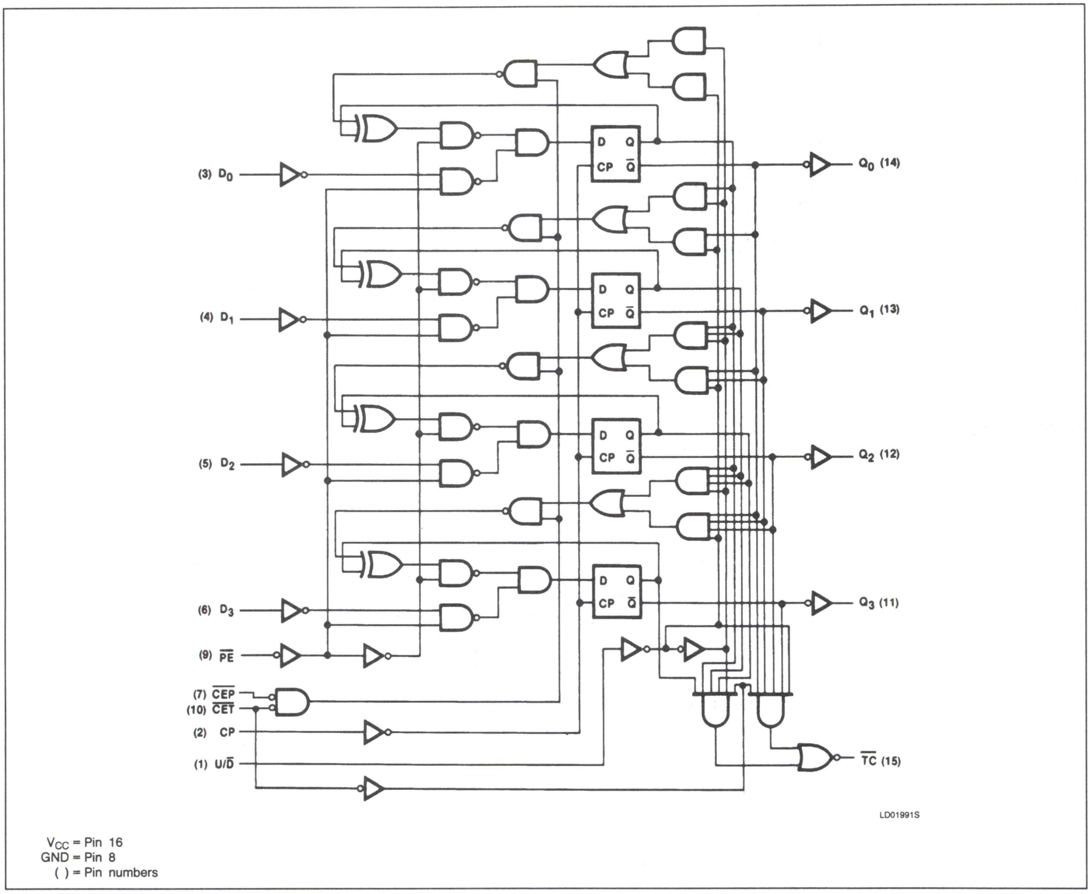

0
1
2
3
4
15
5
14
6
13
7
12
11
10
9
8
COUNT DOWN
COUNT UP
LD01980S

LOGIC DIAGRAM, 'F168


(3) D0
(4) D1
(5) D2
(6) D3
PE (9)
(7) CEP
(10) CET
(2) CP
(1) U/D
D
Q
CP
Q
Q0 (14)
Q1 (13)
Q2 (12)
Q3 (11)
TC (15)
LD01961S

VCC = Pin 16
GND = Pin 8
( ) = Pin numbers

LOGIC DIAGRAM, 'F169


(3) D0
(4) D1
(5) D2
(6) D3
(9) PE
(7) CEP
(10) CET
(2) CP
(1) U/D
D
Q
CP
Q̄
Q0 (14)
Q1 (13)
Q2 (12)
Q3 (11)
TC (15)
LD01991S

VCC = Pin 16
GND = Pin 8
( ) = Pin numbers

APPLICATIONS

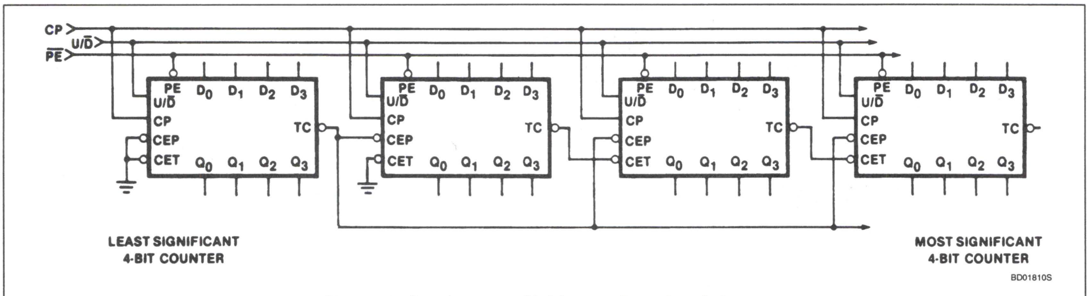

CP
U/D
PE
PE
D0
D1
D2
D3
U/D
CP
CEP
CET
TC
Q0
Q1
Q2
Q3
LEAST SIGNIFICANT 4-BIT COUNTER
MOST SIGNIFICANT 4-BIT COUNTER
BD01810S

Figure 1. Synchronous Multistage Counting Scheme

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS[1]		74F168, 'F169			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX V_{IH} = MIN,	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OL} = MAX V_{IH} = MIN,	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current	$\overline{CET}$ input	V_{CC} = MAX, V_I = 0.5V				−1.2	mA
		Other inputs					−0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current[4] (total)		V_{CC} = MAX			35	52	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. I_{CC} is measured after applying a momentary 4.5V, then ground to the clock input with all other inputs grounded and outputs open.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	74F168, 'F169					UNIT
				$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
				Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency		Waveform 1	100	115		90		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n ($\overline{PE}$, High or Low)		Waveform 1	3.0 4.0	6.5 9.0	8.5 11.5	3.0 4.0	9.5 13.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{TC}$		Waveform 1	5.5 4.0	12.0 8.5	15.5 11.0	5.5 4.0	17.0 12.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CET}$ to $\overline{TC}$		Waveform 2	2.5 2.5	4.5 6.0	6.0 8.0	2.5 2.5	7.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay U/$\overline{D}$ to $\overline{TC}$	'F168	Waveform 3	3.5 4.0	8.5 12.5	11.0 16	3.5 4.0	12.5 17.5	ns
t_{PLH} t_{PHL}	Propagation delay U/$\overline{D}$ to $\overline{TC}$	'F169	Waveform 3	3.5 4.0	8.5 8.0	15.0 10.5	3.5 4.0	15.5 12.0	ns

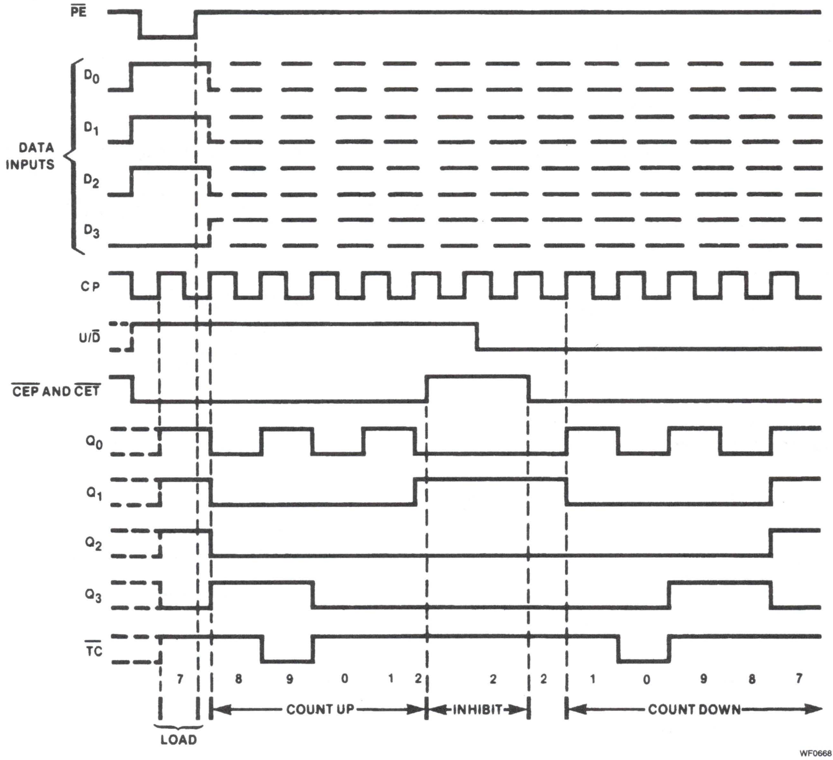
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER		TEST CONDITIONS	74F168, 'F169					UNIT
				$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
				Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to CP		Waveform 4	4.0 4.0			4.5 4.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to CP		Waveform 4	3.0 3.0			3.5 3.5		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{CEP}$ or $\overline{CET}$ to CP		Waveform 5	5.0 5.0			5.5 5.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{CEP}$ or $\overline{CET}$ to CP		Waveform 5	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{PE}$ to CP		Waveform 4	8.0 8.0			9.0 9.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{PE}$ to CP		Waveform 4	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low U/$\overline{D}$ to CP	'F168	Waveform 6	11.0 16.5			12.5 18.0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low U/$\overline{D}$ to CP	'F169	Waveform 6	11.0 7.0			12.5 8.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low U/$\overline{D}$ to CP		Waveform 6	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	CP pulse width, High or Low		Waveform 1	5.0 5.0			5.5 5.5		ns

WAVEFORM (Typical Load, Count, and Inhibit Sequences)

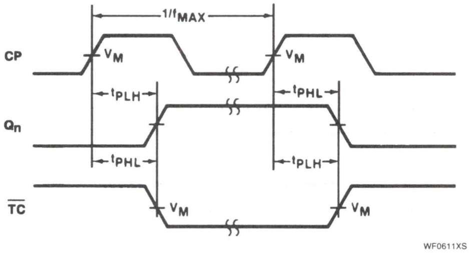
Illustrated below is the following sequence for the 'F168. The operation of the 'F169 is similar.

1. Load (preset) to BCD seven
2. Count up to eight, nine (maximum), zero, one, and two
3. Inhibit
4. Count down to one, zero (minimum), nine, eight, and seven

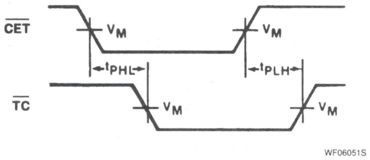

$\overline{PE}$
DATA INPUTS
D_0
D_1
D_2
D_3
CP
$U/\overline{D}$
$\overline{CEP}$ AND $\overline{CET}$
Q_0
Q_1
Q_2
Q_3
$\overline{TC}$
7
8
9
0
1
2
2
2
1
0
9
8
7
COUNT UP
INHIBIT
COUNT DOWN
LOAD

WF06681S

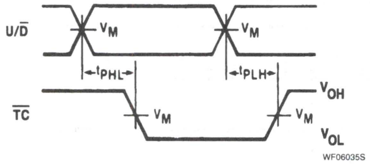
AC WAVEFORMS


1/fMAX
CP
VM
VM
tPLH
tPHL
Qn
tPHL
tPLH
TC
VM
VM
WF0611XS

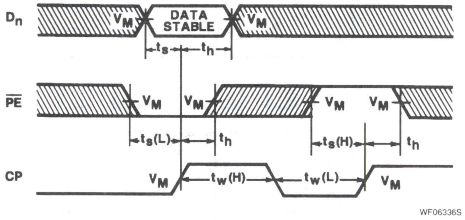
Waveform 1. Clock to Output Delays and Clock Pulse Width


CET
VM
VM
tPHL
tPLH
TC
VM
VM
WF06051S

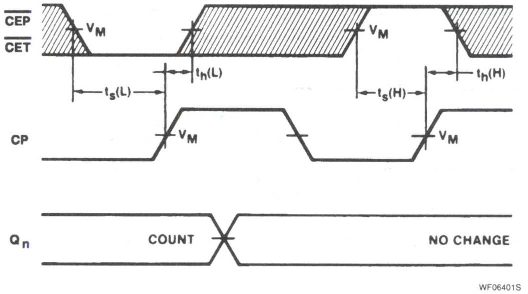
Waveform 2. Propagation Delays CET Input to Terminal Count Output

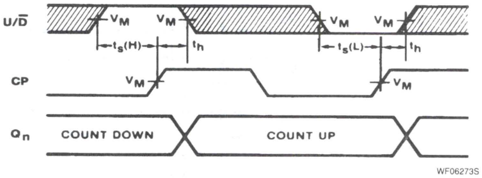

U/D
VM
VM
tPHL
tPLH
VOH
TC
VM
VM
VOL
WF06035S

Waveform 3. Propagation Delays U/D Control to Terminal Count Output


Dn
VM
DATA STABLE
VM
ts
th
PE
VM
VM
VM
VM
ts(L)
th
ts(H)
th
CP
VM
tw(H)
tw(L)
VM
WF06336S

Waveform 4. Parallel Data and Parallel Enable Setup and Hold Times


CEP
CET
VM
VM
th(L)
th(H)
ts(L)
ts(H)
CP
VM
VM
Qn
COUNT
NO CHANGE
WF06401S

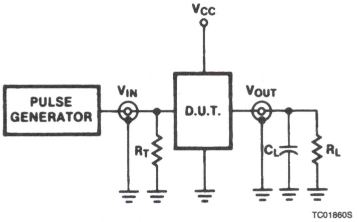

U/D
VM
VM
VM
VM
ts(H)
th
ts(L)
th
CP
VM
VM
Qn
COUNT DOWN
COUNT UP
WF06273S

Waveform 5. Count Enable Setup and Hold Times

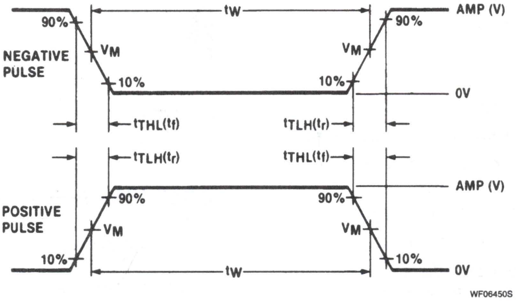
Waveform 6. Up/Down Control Setup and Hold Times

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORM


VCC
PULSE GENERATOR
VIN
D.U.T.
VOUT
RT
CL
RL
TC01860S

Test Circuit for Totem-Pole Outputs


NEGATIVE PULSE
POSITIVE PULSE
90%
10%
VM
tW
AMP (V)
0V
tTHL(tf)
tTLH(tr)
WF06450S

$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F173
Quad D-Type Flip-Flop (3-State)

Product Specification

FAST Products

FEATURES

- Edge-triggered D-type register
- Gated clock enable for hold "do nothing" mode
- 3-State output buffers
- Gated output enable control
- Speed upgrade of N8T10 and current sink upgrade
- Controlled output edges to minimize ground bounce
- 48mA sinking capability

DESCRIPTION

The 'F173 is a High-speed 4-bit parallel load register with clock enable control, 3-state buffered outputs, and Master Reset (MR). When the two clock Enable ($\overline{E}_0$ and $\overline{E}_1$) inputs are Low, the data on the D inputs is loaded into the register simultaneously with Low-to-High Clock (CP) transition. When one or both $\overline{E}$ inputs are High one setup time before the Low-to-High clock transition, the register retains the previous data. Data inputs and clock Enable inputs are fully edge-triggered and must be stable only one setup time before the Low-to-High clock transition.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F173	100MHz	23mA

ORDERING INFORMATION

PACKAGE	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
16-Pin Plastic DIP	74F173N
16-Pin Plastic SOL	74F173D

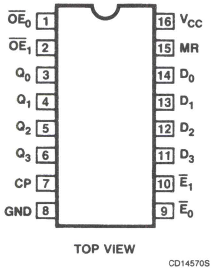
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$D_0 - D_3$	Data inputs	1.0/1.0	20μA/0.6mA
CP	Clock input	1.0/1.0	20μA/0.6mA
$\overline{E}_0$, $\overline{E}_1$	Clock Enable input	1.0/1.0	20μA/0.6mA
MR	Master Reset input	1.0/1.0	20μA/0.6mA
$\overline{OE}_0$, $\overline{OE}_1$	Output Enable input	1.0/1.0	20μA/0.6mA
$Q_0 - Q_4$	Data outputs	750/80	15mA/48mA

NOTE:

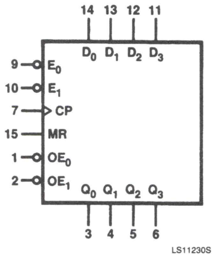
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



$\overline{OE}_0$ 1
$\overline{OE}_1$ 2
Q_0 3
Q_1 4
Q_2 5
Q_3 6
CP 7
GND 8
16 V_{CC}
15 MR
14 D_0
13 D_1
12 D_2
11 D_3
10 $\overline{E}_1$
9 $\overline{E}_0$
TOP VIEW
CD14570S

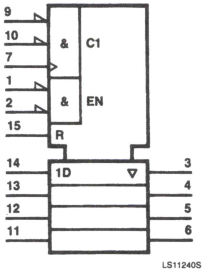
LOGIC SYMBOL



14 13 12 11
D_0 D_1 D_2 D_3
9 E_0
10 E_1
7 CP
15 MR
1 OE_0
2 OE_1
Q_0 Q_1 Q_2 Q_3
3 4 5 6
LS11230S

V_{CC} = Pin 16
GND = Pin 8

LOGIC SYMBOL (IEEE/IEC)



9
10
7
1
2
15
&
C1
&
EN
R
1D
14
13
12
11
3
4
5
6
LS11240S

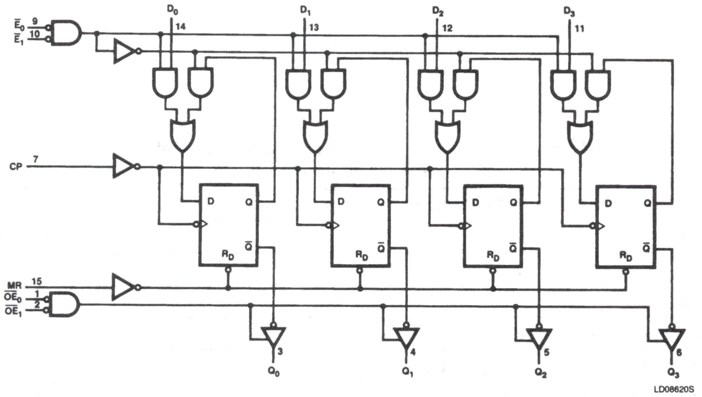
Quad D-Type Flip-Flop (3-State) FAST 74F173

DESCRIPTION (Continued)

The Master Reset (MR) is an active-High asynchronous input. When the MR is High, all four flip-flops are reset (cleared) independently of any other input condition.

The 3-State output buffers are controlled by a 2-input NOR gate. When both Output Enable ($\overline{OE}_0$ and $\overline{OE}_1$) inputs are Low, the data in the register is presented at the Q output. When one or both $\overline{OE}$ inputs are High, the outputs are forced to a High-impedance "OFF" state. The 3-State output buffers are completely independent of the register operation; the $\overline{OE}$ transition does not affect the clock and reset operations.

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
( ) = Pin numbers

FUNCTION TABLE

OPERATING MODE	INPUTS					OUTPUTS
	MR	CP	$\overline{E}_0$	$\overline{E}_1$	D_n	Q_n (Register)
Reset (clear)	H	X	X	X	X	L
Parallel load	L	↑	l	l	l	L
	L	↑	l	l	h	H
Hold (do nothing)	L	X	h	X	X	q_n
	L	X	X	h	X	q_n

H = High voltage level
h = High voltage level one setup time prior to Low-to-High clock transition
L = Low voltage level
l = Low voltage level one setup time prior to Low-to-High clock transition
q_n = Lower case letters indicate the state of the referenced input (or output) on setup time prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition

Quad D-Type Flip-Flop (3-State)

FAST 74F173

FUNCTION TABLE

OPERATING MODE	INPUTS			OUTPUTS
	Q_n (Register)	$\overline{OE}_0$	$\overline{OE}_1$	Q_n
Read	L H	L L	L L	L H
Disabled	X X	H X	X H	Z Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High-impedance "OFF" state

ABSOLUTE MAXIMUM RATINGS

(Operating beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	96	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−15	mA
I_{OL}	Low-level output current			48	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN V_{IL} = MAX V_{IH} = MIN	I_{OH} = −3mA	±10% V_{CC}	2.4			V
					±5% V_{CC}	2.7			V
				I_{OH} = −15mA	±10% V_{CC}	2.0			V
					±5% V_{CC}	2.0			V
V_{OL}	Low-level output voltage		V_{CC} = MIN V_{IL} = MAX V_{IH} = MIN	I_{OL} = MAX	±10% V_{CC}		0.38	0.55	V
					±5% V_{CC}		0.38	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$				−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V					100	μA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					−0.6	mA
I_{OZH}	OFF-state output current, High-level voltage applied		V_{CC} = MAX, V_O = 2.7V					20	μA
I_{OZL}	OFF-state output current, High-level voltage applied		V_{CC}=MAX, V_O = 0.5V					−20	μA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX			−60		−150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				19	26	mA
		I_{CCL}					27	37	mA
		I_{CCZ}					23	32	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value under the recommended operating conditions for the applicable conditions.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of High-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} should be performed last.

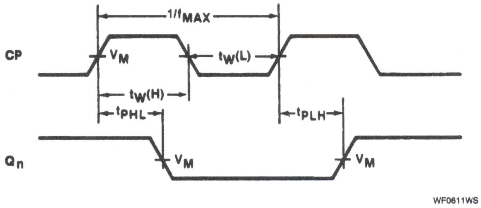
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			$T_A = +25°C$ $V_{CC} = 5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	100	125		90		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	Waveform 1	4.5 6.0	6.5 8.0	9.0 10.5	4.0 5.5	10.0 11.5	ns
t_{PHL}	Propagation delay MR to Q_n	Waveform 2	6.5	8.5	11.5	6.0	12.5	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level	Waveform 4 Waveform 5	3.5 5.5	5.0 7.0	8.0 10.0	2.5 4.5	8.5 11.0	ns ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level	Waveform 4 Waveform 5	1.5 3.0	3.5 5.0	7.0 8.5	1.0 2.5	8.0 9.0	ns
t_{TZL} t_{THZ}	Transition Time 10% to 90%, 90% to 10%	Waveform 4 Waveform 5	4.0 2.0	7.5 5.0	10.0 8.0	4.0 2.0	11.0 8.5	ns

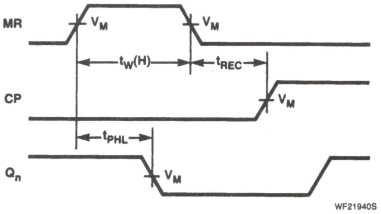
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			$T_A = +25°C$ $V_{CC} = 5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time D_n to CP	Waveform 3	2.5 2.5			3.0 4.0		ns
$t_h(H)$ $t_h(L)$	Hold time D_n to CP	Waveform 3	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time $\overline{E}_n$ to CP	Waveform 3	4.5 7.5			5.0 8.5		ns
$t_h(H)$ $t_h(L)$	Hold time, $\overline{E}_n$ to CP	Waveform 3	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width High or Low	Waveform 1	3.0 6.0			3.0 6.0		ns
$t_w(H)$	MR Pulse width High	Waveform 2	3.5			3.5		ns
t_{rec}	Recovery time, MR to CP	Waveform 2	4.5			5.5		ns

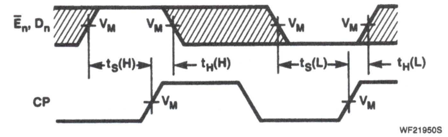
AC WAVEFORMS


CP
Qn
1/fMAX
VM
tW(L)
tW(H)
tPHL
tPLH
VM
VM
WF0611WS

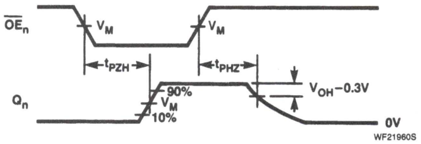
Waveform 1. Propagation Delay, Clock and Enable Inputs to Outputs, Clock and Enable Widths and Maximum Clock Frequency


MR
CP
Qn
VM
VM
tW(H)
tREC
VM
tPHL
VM
WF21940S

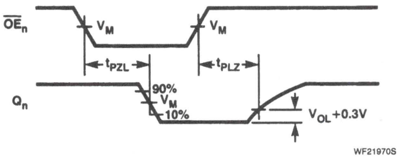
Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time


Ēn, Dn
VM
VM
VM
VM
tS(H)
tH(H)
tS(L)
tH(L)
CP
VM
VM
WF21950S

Waveform 3. Data and Select Setup and Hold Times


OEn
VM
VM
tPZH
tPHZ
Qn
90%
VM
10%
VOH−0.3V
0V
WF21960S

Waveform 4. 3-state Output Enable Time to High Level and Output Disable Time From High Level


OEn
VM
VM
tPZL
tPLZ
Qn
90%
VM
10%
VOL+0.3V
WF21970S

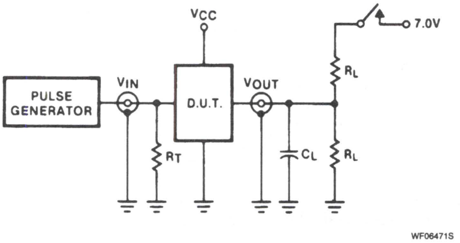
Waveform 5. 3-state Output Enable Time to Low Level and Output Disable Time From Low Level

NOTE: $V_M = 1.5V$.
The Shaded Area Indicates When the Output is Permitted to Change for Predictable Output Performance.

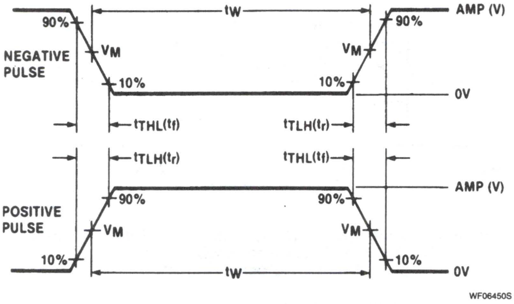
Quad D-Type Flip-Flop (3-State)

FAST 74F173

TEST CIRCUIT AND WAVEFORMS


VCC
7.0V
RL
PULSE GENERATOR
VIN
D.U.T.
VOUT
RT
CL
RL
WF06471S

Test Circuit for 3-State Outputs


90%
tW
90%
AMP (V)
NEGATIVE PULSE
VM
VM
10%
10%
0V
tTHL(tf)
tTLH(tr)
tTLH(tr)
tTHL(tf)
AMP (V)
90%
90%
POSITIVE PULSE
VM
VM
10%
10%
0V
tW
WF06450S

$V_M = 1.5V$

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F174
Flip-Flop

Hex D Flip-Flops
Product Specification

FAST Products

FEATURES

- **Six edge-triggered D-type flip-flops.**
- **Buffered common Clock**
- **Buffered, asynchronous Master Reset**

DESCRIPTION

The 'F174 has six edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one setup time before the Low-to-High clock transition is transferred to the corresponding flip-flop's Q output.

All Q outputs will be forced Low independent of Clock or Data inputs by a Low voltage level on the $\overline{MR}$ input. The device is useful for applications where true outputs only are required, and the Clock and Master Reset are common to all storage elements.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F174	100MHz	35mA

ORDERING INFORMATION

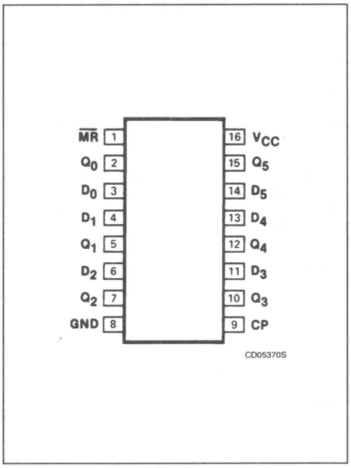
PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
16-Pin Plastic DIP	N74F174N
16-Pin Plastic SO	N74F174D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

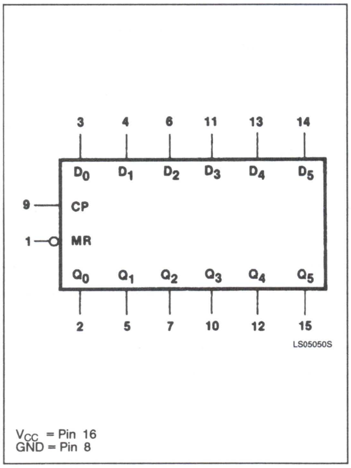
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$D_0 - D_5$	Data inputs	1.0/1.0	20μA/0.6mA
CP	Clock Pulse input (active rising edge)	1.0/1.0	20μA/0.6mA
$\overline{MR}$	Master Reset input (active-Low)	1.0/1.0	20μA/0.6mA
$Q_0 - Q_5$	Data outputs	50/33	1.0mA/20mA

NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION

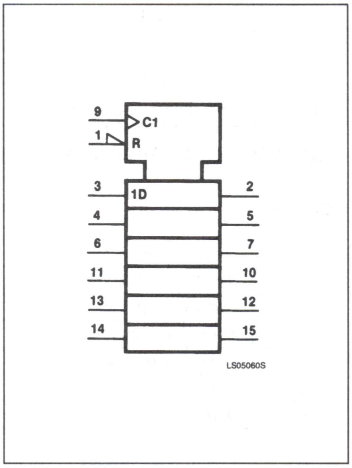

MR 1
Q0 2
D0 3
D1 4
Q1 5
D2 6
Q2 7
GND 8
16 VCC
15 Q5
14 D5
13 D4
12 Q4
11 D3
10 Q3
9 CP
CD05370S

LOGIC SYMBOL

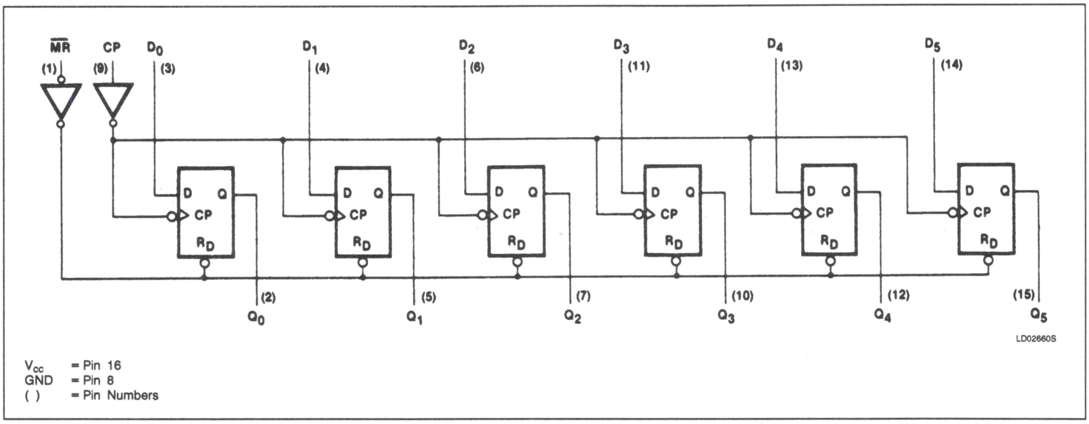

3
4
6
11
13
14
D0
D1
D2
D3
D4
D5
9
CP
1
MR
Q0
Q1
Q2
Q3
Q4
Q5
2
5
7
10
12
15
LS05050S

V_{CC} = Pin 16
GND = Pin 8

LOGIC SYMBOL (IEEE/IEC)


9
C1
1
R
3
1D
2
4
5
6
7
11
10
13
12
14
15
LS05060S

LOGIC DIAGRAM



FUNCTION TABLE

OPERATING MODE	INPUTS			OUTPUTS
	$\overline{MR}$	CP	D_n	Q_n
Reset (clear)	L	X	X	L
Load "1"	H	↑	h	H
Load "0"	H	↑	l	L

H = High voltage level steady state
h = High voltage level one setup time prior to the Low-to-High clock transition
L = Low voltage level steady state
l = Low voltage level one setup time prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

Flip-Flop

FAST 74F174

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		74F174			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX V_{IH} = MIN	±10%V_{CC}	2.5			V
			±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, I_{OL} = MAX V_{IH} = MIN	±10%V_{CC}		0.35	0.50	V
			±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, $I_I = I_{IK}$			−0.73	−1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V				−0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current (total)	V_{CC} = MAX, D_n = $\overline{MR}$ = 4.5V, CP = ↑			35	45	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

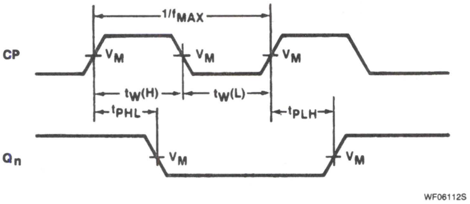
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F174					UNIT
			T_A = +25°C V_{CC} = +5.0V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	80	100		80		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n or $\overline{Q}_n$	Waveform 1	3.5 4.5	5.5 6.0	8.0 10.0	3.5 4.5	9.0 11.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	Waveform 3	5.0	8.5	14.0	5.0	15.0	ns

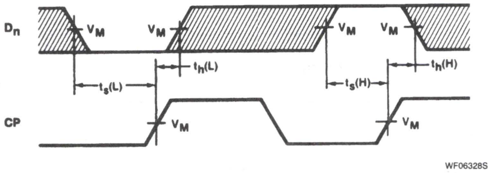
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	74F174					UNIT
			T_A = +25°C V_{CC} = +5.0V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to CP	Waveform 2	4.0 4.0			4.0 4.0		ns ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to CP	Waveform 2	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	CP pulse width, High or Low	Waveform 1	4.0 6.0			4.0 6.0		ns ns
$t_w(L)$	$\overline{MR}$ pulse width Low	Waveform 3	5.0			5.0		ns
t_{rec}	Recovery time $\overline{MR}$ to CP	Waveform 3	5.0			5.0		ns ns

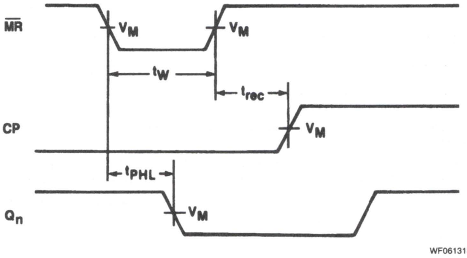
AC WAVEFORMS


CP
Qn
1/fMAX
VM
tW(H)
tW(L)
tPHL
tPLH
WF06112S

Waveform 1. Clock to Output Delays, Clock Pulse Width, and Maximum Clock Frequency


Dn
CP
VM
ts(L)
th(L)
ts(H)
th(H)
WF06328S

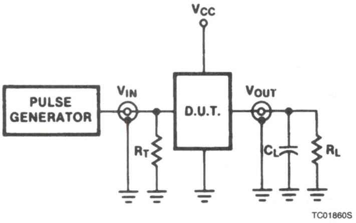
Waveform 2. Data Setup and Hold Times


MR
CP
Qn
VM
tW
trec
tPHL
WF06131S

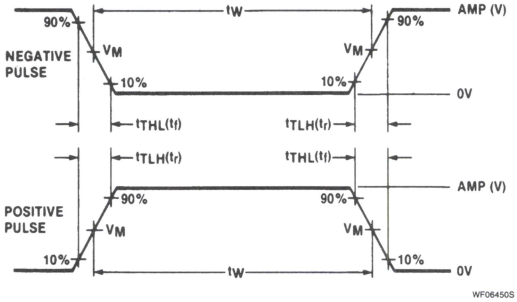
Waveform 3. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORM


VCC
PULSE GENERATOR
VIN
D.U.T.
VOUT
RT
CL
RL
TC01860S

Test Circuit for Totem-Pole Outputs


NEGATIVE PULSE
POSITIVE PULSE
tW
90%
10%
VM
AMP (V)
0V
tTHL(tf)
tTLH(tr)
WF06450S

V_M = 1.5V

Input Pulse Definition

DEFINITIONS
R_L = Load resistor to GND; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F175
Quad D Flip-Flop

Quad D Flip-Flop
Product Specification

FAST Products

FEATURES

- **Four edge-triggered D flip-flops**
- **Buffered common Clock**
- **Buffered, asynchronous Master Reset**
- **True and complementary output**

DESCRIPTION

The 'F175 is a quad, edge-triggered D-type flip-flop with individual D inputs and both Q and $\overline{Q}$ outputs. The common buffered Clock (CP) and Master Reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one setup time before the Low-to-High clock transition, is transferred to the corresponding flip-flop's Q output.

All Q outputs will be forced Low independantly of Clock or Data inputs by a Low voltage level on the $\overline{MR}$ input. The device is useful for applications where both true and complement outputs are required, and the Clock and Master Reset are common to all storage elements.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F175	140MHz	25mA

ORDERING INFORMATION

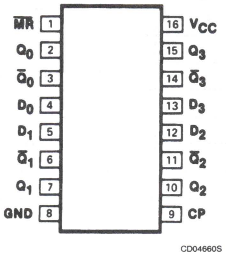
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ± 10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F175N
16-Pin Plastic SO	N74F175D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

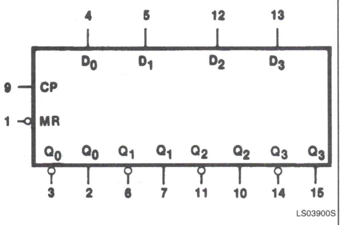
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$D_0 - D_3$	Data inputs	1.0/1.0	20μA/0.6mA
CP	Clock Pulse input (active rising edge)	1.0/1.0	20μA/0.6mA
$\overline{MR}$	Master Reset input (active-Low)	1.0/1.0	20μA/0.6mA
$Q_0 - Q_3$	True outputs	50/33	1.0mA/20mA
$\overline{Q}_0 - \overline{Q}_3$	Complementary outputs	50/33	1.0mA/20mA

NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

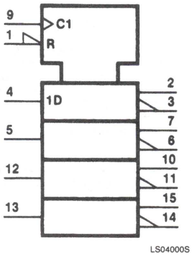
PIN CONFIGURATION


MR 1
Q0 2
Q̄0 3
D0 4
D1 5
Q̄1 6
Q1 7
GND 8
16 VCC
15 Q3
14 Q̄3
13 D3
12 D2
11 Q̄2
10 Q2
9 CP
CD04660S

LOGIC SYMBOL


4
5
12
13
D0
D1
D2
D3
9 CP
1 MR
Q0 Q̄0 Q1 Q̄1 Q2 Q̄2 Q3 Q̄3
3 2 6 7 11 10 14 15
LS03900S

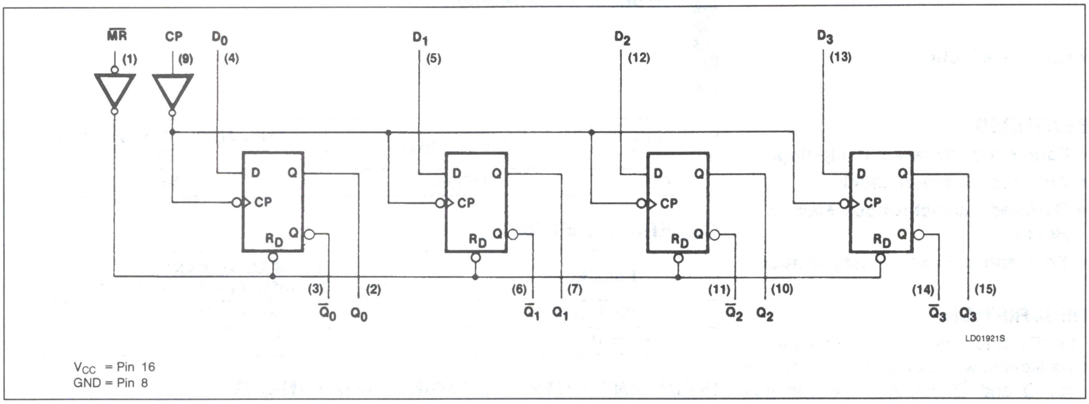
LOGIC SYMBOL (IEEE/IEC)


9
1
C1
R
4
1D
5
12
13
2
3
7
6
10
11
15
14
LS04000S

Quad D Flip-Flop

FAST 74F175

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8

MODE SELECT – FUNCTION TABLE

OPERATING MODE	INPUTS			OUTPUTS	
	$\overline{MR}$	CP	D_n	Q_n	$\overline{Q}_n$
Reset (clear)	L	X	X	L	H
Load "1"	H	↑	h	H	L
Load "0"	H	↑	l	L	H

H = High voltage level steady state
h = High voltage level one setup time prior to the Low-to-High clock transition
L = Low voltage level steady state
l = Low voltage level one setup time prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		74F175			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.5			V
			±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}		0.35	0.50	V
			±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, $I_I = I_{IK}$			-0.73	-1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	V_{CC} = MAX, D_n = $\overline{MR}$ = 4.5V, CP = ↑			25	34	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

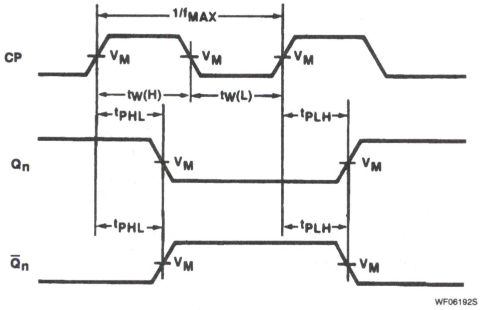
SYMBOL	PARAMETER	TEST CONDITIONS	74F175					UNIT
			T_A = +25°C V_{CC} = +5.0V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{max}	Maximum clock frequency	Waveform 1	100	140		100		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n or $\overline{Q}_n$	Waveform 1	4.0 4.0	5.0 6.5	6.5 8.5	4.0 4.0	7.5 9.5	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	Waveform 3	4.5	9.0	11.5	4.5	13	ns
t_{PLH}	Propagation delay $\overline{MR}$ to $\overline{Q}_n$	Waveform 3	4.0	6.5	8.0	4.0	9.0	ns

Quad D Flip-Flop FAST 74F175

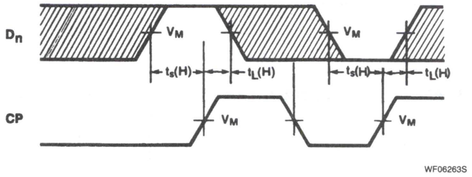
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	74F175					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to CP	Waveform 2	3.0 3.0			3.0 3.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to CP	Waveform 2	1.0 1.0			1.0 1.0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low	Waveform 1	4.0 5.0			4.0 5.0		ns
$t_w(L)$	$\overline{MR}$ Pulse width Low	Waveform 3	5.0			5.0		ns
t_{rec}	Recovery time $\overline{MR}$ to CP	Waveform 3	5.0			5.0		ns

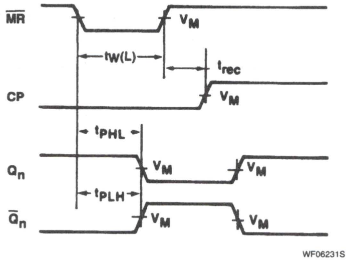
AC WAVEFORMS


1/fMAX
CP
VM
tW(H)
tW(L)
tPHL
tPLH
Qn
Q̄n
WF06192S

Waveform 1. Clock to Output Delays and Clock Pulse Width


Dn
CP
VM
ts(H)
tL(H)
WF06263S

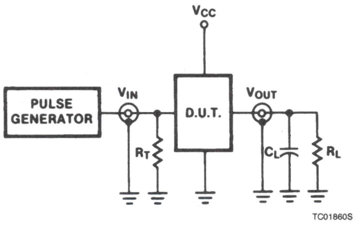
Waveform 2. Data Setup and Hold Times


MR
CP
Qn
Q̄n
VM
tW(L)
trec
tPHL
tPLH
WF06231S

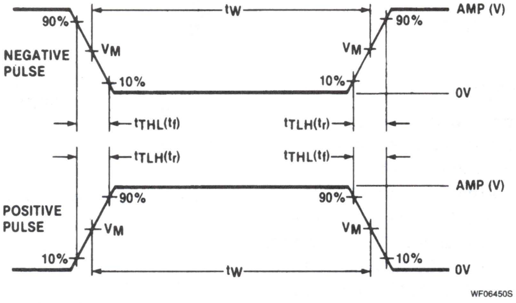
Waveform 3. Master Reset to Output Delay, Master Reset Pulse Width, and Master Reset Recovery Time

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORM


VCC
PULSE GENERATOR
VIN
D.U.T.
VOUT
RT
CL
RL
TC01860S

Test Circuit for Totem-Pole Outputs


NEGATIVE PULSE
POSITIVE PULSE
tW
90%
10%
VM
AMP (V)
0V
tTHL(tf)
tTLH(tr)
WF06450S

$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS

R_L = Load resistor to GND; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F181
Arithmetic Logic Unit

4-Bit Arithmetic Logic Unit
Product Specification

FAST Products

FEATURES
- **Provides 16 arithmetic operations: add, subtract, compare, and double; plus 12 other arithmetic operations**
- **Provides all 16 logic operations of two variables: Exclusive-OR, Compare, AND, NAND, NOR, OR, plus 10 other logic operations**
- **Full look-ahead Carry for High-speed arithmetic operation on long words**
- **40% faster than 'S181 with only 30% 'S181 power consumption**
- **Available in 300mil-wide 24-pin Slim DIP package**

DESCRIPTION
The 'F181 is a 4-bit High-speed parallel Arithmetic Logic Unit (ALU). Controlled by the four Function Select inputs ($S_0 - S_3$) and the Mode Control input (M), it can perform all the 16 possible logic operations or 16 different arithmetic operations on active-High or active-Low operands. The Function Table lists these operations.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F181	7.3ns	43mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
24-Pin Plastic DIP	N74F181N
24-Pin Plastic SOL	N74F181D

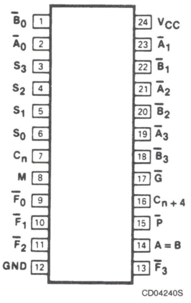
NOTE:
1. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
M	Mode control input	1.0/1.0	20μA/0.6mA
$\overline{A}_0 - \overline{A}_3$, $\overline{B}_0 - \overline{B}_3$	Operand inputs	1.0/3.0	20μA/1.8mA
$S_0 - S_3$	Function select inputs	1.0/4.0	20μA/2.4mA
C_n	Carry input	1.0/5.0	20μA/3.0mA
C_{n+4}	Carry output	50/33	1.0mA/20mA
A = B	Compare output	*OC/33	*OC/20mA
$\overline{F}_0 - \overline{F}_3$	Outputs	50/33	1.0mA/20mA
$\overline{G}$	Carry generate output	50/33	1.0mA/20mA
$\overline{P}$	Carry propagate output	50/33	1.0mA/20mA

NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.
*OC = Open-Collector

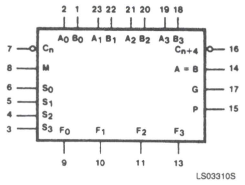
PIN CONFIGURATION



$\overline{B}_0$ 1
$\overline{A}_0$ 2
S_3 3
S_2 4
S_1 5
S_0 6
C_n 7
M 8
$\overline{F}_0$ 9
$\overline{F}_1$ 10
$\overline{F}_2$ 11
GND 12
24 V_{CC}
23 $\overline{A}_1$
22 $\overline{B}_1$
21 $\overline{A}_2$
20 $\overline{B}_2$
19 $\overline{A}_3$
18 $\overline{B}_3$
17 $\overline{G}$
16 C_{n+4}
15 $\overline{P}$
14 A = B
13 $\overline{F}_3$
CD04240S

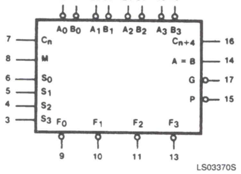
LOGIC SYMBOL

Active-High Operands



2 1 23 22 21 20 19 18
A_0 B_0 A_1 B_1 A_2 B_2 A_3 B_3
7 C_n
8 M
6 S_0
5 S_1
4 S_2
3 S_3
C_{n+4} 16
A = B 14
G 17
P 15
F_0 F_1 F_2 F_3
9 10 11 13
LS03310S

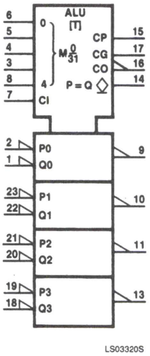
Active-Low Operands



2 1 23 22 21 20 19 18
A_0 B_0 A_1 B_1 A_2 B_2 A_3 B_3
7 C_n
8 M
6 S_0
5 S_1
4 S_2
3 S_3
C_{n+4} 16
A = B 14
G 17
P 15
F_0 F_1 F_2 F_3
9 10 11 13
LS03370S

V_{CC} = Pin 24
GND = Pin 12

LOGIC SYMBOL (IEEE/IEC)



ALU
[T]
6 5 4 3 8 7
0
M $\frac{0}{31}$
4
CI
CP 15
CG 17
CO 16
P=Q 14
2 1 P0 Q0 9
23 22 P1 Q1 10
21 20 P2 Q2 11
19 18 P3 Q3 13
LS03320S

Arithmetic Logic Unit

FAST 74F181

When the Mode Control input (M) is High, all internal carries are inhibited and the device performs logic operations on the individual bits as listed. When the Mode Control input is Low, the carries are enabled and the device performs arithmetic operations on the two 4-bit words. The device incorporates full internal carry look-ahead and provides for either ripple carry between devices using the C_{n+4} output, or for carry look-ahead between packages using the signals $\overline{P}$ (Carry Propagate) and $\overline{G}$ (Carry Generate). $\overline{P}$ and $\overline{G}$ are not affected by carry in. When speed requirements are not stringent, it can be used in a simple ripple carry mode by connecting the Carry output (C_{n+4}) signal to the Carry input (C_n) of the next unit. For High-speed operation the device is used in conjunction with the '182 carry look-ahead circuit. One carry look-ahead package is required for each group of four '181 devices. Carry look-ahead can be provided at various levels and offers High-speed capability over extremely long word lengths.

The A = B output from the device goes High when all four $\overline{F}$ outputs are High and can be used to indicate logic equivalence over 4 bits when the unit is in the subtract mode. The A = B output is open-collector and can be wired – AND with other A = B outputs to give a comparison for more than 4 bits. The A = B signal can also be used with the C_{n+4} signal to indicate A > B and A < B.

The Function Table lists the arithmetic operations that are performed without a carry in. An incoming carry adds a one to each operation. Thus, select code LHHL generates A minus B minus 1 (two's complement notation) without a carry in and generates A minus B when a carry is applied. Because subtraction is actually performed by complementary addition (one's complement), a carry out means borrow; thus, a carry is generated when there is no underflow and no carry is generated when there is underflow.

As indicated, this device can be used with either active-Low inputs producing active-Low outputs or with active-High inputs producing active-High outputs. For either case, the table lists the operations that are performed to the operands labeled inside the logic symbol.

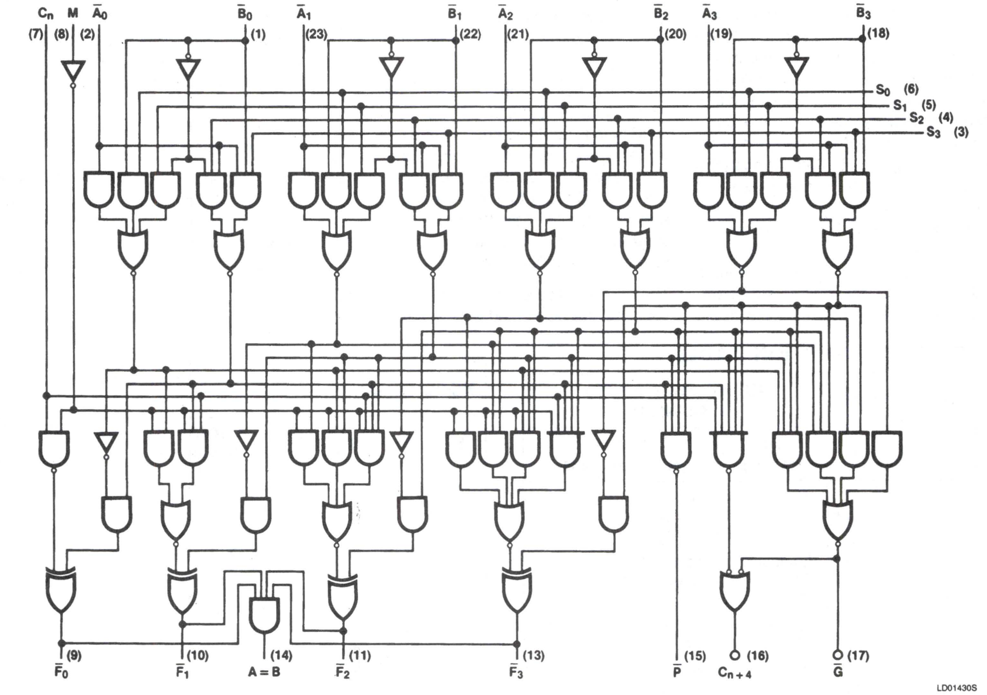
MODE SELECT—FUNCTION TABLE

MODE SELECT INPUTS				ACTIVE HIGH INPUTS & OUTPUTS	
S_3	S_2	S_1	S_0	Logic (M = H)	Arithmetic** (M = L) (C_n = H)
L	L	L	L	$\overline{A}$	A
L	L	L	H	$\overline{A+B}$	A + B
L	L	H	L	$\overline{A}B$	$A+\overline{B}$
L	L	H	H	Logical 0	minus 1
L	H	L	L	$\overline{AB}$	A plus $A\overline{B}$
L	H	L	H	$\overline{B}$	(A + B) plus $A\overline{B}$
L	H	H	L	$A \oplus B$	A minus B minus 1
L	H	H	H	$A\overline{B}$	AB minus 1
H	L	L	L	$\overline{A}+B$	A plus AB
H	L	L	H	$\overline{A \oplus B}$	A plus B
H	L	H	L	B	$(A+\overline{B})$ plus AB
H	L	H	H	AB	AB minus 1
H	H	L	L	Logical 1	A plus A*
H	H	L	H	$A+\overline{B}$	(A + B) plus A
H	H	H	L	A + B	$(A+\overline{B})$ plus A
H	H	H	H	A	A minus 1

MODE SELECT INPUTS				ACTIVE LOW INPUTS & OUTPUTS	
S_3	S_2	S_1	S_0	LOGIC (M = H)	ARITHMETIC** (M = L) (C_n = L)
L	L	L	L	$\overline{A}$	A minus 1
L	L	L	H	$\overline{AB}$	AB minus 1
L	L	H	L	$\overline{A}+B$	$A\overline{B}$ minus 1
L	L	H	H	Logical 1	minus 1
L	H	L	L	$\overline{A+B}$	A plus $(A+\overline{B})$
L	H	L	H	$\overline{B}$	AB plus $(A+\overline{B})$
L	H	H	L	$\overline{A \oplus B}$	A minus B minus 1
L	H	H	H	$A+\overline{B}$	$A+\overline{B}$
H	L	L	L	$\overline{A}B$	A plus (A + B)
H	L	L	H	$A \oplus B$	A plus B
H	L	H	L	B	$A\overline{B}$ plus (A + B)
H	L	H	H	A + B	A + B
H	H	L	L	Logical 0	A plus A*
H	H	L	H	$A\overline{B}$	AB plus A
H	H	H	L	AB	$A\overline{B}$ plus A
H	H	H	H	A	A

L = Low voltage
H = High voltage level
*Each bit is shifted to the next more significant position.
**Arithmetic operations expressed in two's complement notation.

LOGIC DIAGRAM


C_n (7)
M (8)
$\overline{A}_0$ (2)
$\overline{B}_0$ (1)
$\overline{A}_1$ (23)
$\overline{B}_1$ (22)
$\overline{A}_2$ (21)
$\overline{B}_2$ (20)
$\overline{A}_3$ (19)
$\overline{B}_3$ (18)
S_0 (6)
S_1 (5)
S_2 (4)
S_3 (3)
(9) $\overline{F}_0$
(10) $\overline{F}_1$
(14) A = B
(11) $\overline{F}_2$
(13) $\overline{F}_3$
(15) $\overline{P}$
(16) C_{n+4}
(17) $\overline{G}$
LD01430S

V_{CC} = Pin 24
GND = Pin 12
( ) = Pin numbers
Pin 14 is O.C.

SUM MODE TEST TABLE I **FUNCTION INPUTS:** $S_0 = S_3 = 4.5V$, $S_1 = S_2 = M = 0V$

PARAMETER	INPUT UNDER TEST	OTHER INPUT, SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST
		Apply 4.5V	Apply GND	Apply 4.5V	Apply GND	
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{B}_i$	None	$\overline{A}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}
t_{PLH} t_{PHL}	$\overline{B}_i$	None	$\overline{A}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}
t_{PLH} t_{PHL}	C_n	None	None	All $\overline{A}$	All $\overline{B}$	Any $\overline{F}$ or C_{n+4}

DIFF MODE TEST TABLE II **FUNCTION INPUTS:** $S_1 = S_2 = 4.5V$, $S_0 = S_3 = M = 0V$

PARAMETER	INPUT UNDER TEST	OTHER INPUT, SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST
		Apply 4.5V	Apply GND	Apply 4.5V	Apply GND	
t_{PLH} t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{B}_i$	None	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	C_{n+4}
t_{PLH} t_{PHL}	$\overline{B}_i$	None	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	C_{n+4}
t_{PLH} t_{PHL}	C_n	None	None	All $\overline{A}$ and $\overline{B}$	None	Any $\overline{F}$ or C_{n+4}

LOGIC MODE TEST TABLE III

PARAMETER	INPUT UNDER TEST	OTHER INPUT, SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	FUNCTION INPUTS
		Apply 4.5V	Apply GND	Apply 4.5V	Apply GND		
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{F}_i$	$S_1 = S_2 = M = 4.5V$ $S_0 = S_3 = 0V$
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{F}_i$	$S_1 = S_2 = M = 4.5V$ $S_0 = S_3 = 0V$

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +1	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.50	5.0	5.50	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
V_{OH}	High-level output current	A = B			4.5	V
I_{OH}	High-level output current	Any output except A = B			−1	mA
I_{OL}	Low-level output current				20	mA
T_A	Operating free-air temperature		0		70	°C

Arithmetic Logic Unit FAST 74F181

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage	Any output except A = B	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	± 10%V_{CC}	2.5			V
				± 5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	± 10%V_{CC}		0.35	0.50	V
				± 5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current	M	V_{CC} = MAX, V_I = 0.5V				−0.6	mA
		$\overline{A}_0 - \overline{A}_3$ $\overline{B}_0 - \overline{B}_3$					−1.8	mA
		$S_0 - S_3$					−2.4	mA
		C_n					−3.0	mA
I_{OH}	High-level output current	A = B only	V_{CC} = MAX, V_{IH} = MIN, V_{IL} = MAX, V_{OH} = 4.5V				250	μA
I_{OS}	Short-circuit output current[3]	Any output except A = B	V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current[4] (total)	I_{CCH}	V_{CC} = MAX	$S_0 - S_3 = M = \overline{A}_0 - \overline{A}_3$ = 4.5V $\overline{B}_0 - \overline{B}_3 = C_n$ = GND		43	65	mA
		I_{CCL}		$S_0 - S_3 = M$ = 4.5V $\overline{B}_0 - \overline{B}_3 = C_n = \overline{A}_0 - \overline{A}_3$ = GND		43	65	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of High-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Measure I_{CC} with all outputs open.

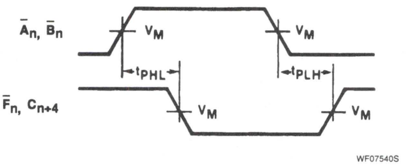
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS				74F181					UNIT
						T_A = +25°C V_{CC} = +5.0V C_L = 50pF R_L = 500Ω			T_A = 0 to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF R_L = 500Ω		
		Mode	Table	Wave form	Conditions	Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay C_n to C_{n+4}	Sum Diff	I II	2	M = 0V	3.0 3.0	6.4 6.1	8.5 8.0	3.0 3.0	9.5 9.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ or $\overline{B}_n$ to C_{n+4}	Sum	I	1	$M = S_1 = S_2 = 0V$, $S_0 = S_3 = 4.5V$	5.0 5.0	10.0 9.4	13 12	5.0 5.0	14.0 13.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ or $\overline{B}_n$ to C_{n+4}	Diff	II	4	$M = S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$	5.0 5.0	10.8 10.0	14 13	5.0 5.0	15.0 14.0	ns
t_{PLH} t_{PHL}	Propagation delay C_n to $\overline{F}_n$	Diff Sum	II I	2	M = 0V	3.0 3.0	6.7 6.5	8.5 8.5	3.0 3.0	9.5 9.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}$ or $\overline{B}_n$ to $\overline{G}$	Sum	I	2	$M = S_1 = S_2 = 0V$, $S_0 = S_3 = 4.5V$	3.0 3.0	5.7 5.8	7.5 7.5	3.0 3.0	8.5 8.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ or $\overline{B}_n$ to $\overline{G}$	Diff	II	3	$M = S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$	3.0 3.0	6.5 7.3	8.5 9.5	3.0 3.0	9.5 10.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ or $\overline{B}_n$ to $\overline{P}$	Sum	I	2	$M = S_1 = S_2 = 0V$, $S_0 = S_3 = 4.5V$	3.0 3.0	5.0 5.5	7.0 7.5	3.0 3.0	8.0 8.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ or $\overline{B}_n$ to $\overline{P}$	Diff	II	3	$M = S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$	4.0 4.0	5.8 6.5	7.5 8.5	4.0 4.0	8.5 9.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_i$ or $\overline{B}_i$ to $\overline{F}_i$	Sum	I	2	$M = S_1 = S_2 = 0V$, $S_0 = S_3 = 4.5V$	3.0 3.0	7.0 7.2	9.0 10.0	3.0 3.0	10.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_i$ or $\overline{B}_i$ to $\overline{F}_i$	Diff	II	3	$M = S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$	3.0 3.0	8.2 8.0	11.0 11.0	3.0 3.0	12.0 12.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ or $\overline{B}_n$ to $\overline{F}_n$	Sum		1, 2		4.0 4.0	8.0 7.8	10.5 10.0	4.0 4.0	11.5 11.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ or $\overline{B}_n$ to $\overline{F}_n$	Diff		1, 2		4.5 4.5	9.4 9.4	12.0 12.0	4.5 4.5	13.0 13.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_i$ or $\overline{B}_i$ to $\overline{F}_i$	Logic	III	3	M = 4.5V	4.0 4.0	6.0 6.0	9.0 10.0	4.0 4.0	10.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ or $\overline{B}_n$ to A = B	Diff	II	3	$M = S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$	11.0 7.0	18.5 9.8	27.0 12.5	11.0 7.0	29.0 13.5	ns

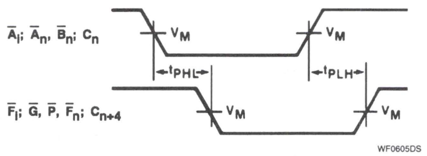
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS					UNIT
				$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
		Mode	Waveform	Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay S_i to $\overline{F}_i$ (Inv)		1	3.0 4.0	7.0 6.0	9.0 9.0	3.0 3.0	10.0 10.5	ns
t_{PLH} t_{PHL}	Propagation delay S_i to $\overline{F}_i$ (Non-Inv)		2	3.0 3.0	7.5 7.5	10.0 10.0	3.0 3.0	11.0 12.0	ns
t_{PLH} t_{PHL}	Propagation delay S_i to A = B (Inv)		1	5.0 10.0	7.5 14.0	11.5 18.0	5.0 10.0	12.5 20.0	ns
t_{PLH} t_{PHL}	Propagation delay S_i to A = B (Non-Inv)		2	10.0 6.0	14.0 10.0	17.5 13.5	10.0 6.0	19.5 15.0	ns
t_{PLH} t_{PHL}	Propagation delay S_i to C_{n+4} (Inv)		1	3.0 6.0	6.5 9.0	9.0 12.5	3.0 6.0	9.0 14.0	ns
t_{PLH} t_{PHL}	Propagation delay S_i to $\overline{G}$ (Non-Inv)		2	2.5 2.5	5.0 4.5	7.5 7.5	2.5 2.5	8.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay S_i to $\overline{P}$ (Non-Inv)		2	2.5 2.5	5.0 5.5	6.5 7.5	2.5 2.5	7.0 8.5	ns
t_{PLH} t_{PHL}	Propagation delay M to $\overline{F}_i$ (Inv)	Sum	1	3.5 3.5	5.5 5.5	8.5 8.5	3.5 3.5	9.0 9.5	ns
t_{PLH} t_{PHL}	Propagation delay M to $\overline{F}_i$ (Non-Inv)	Sum	2	4.0 4.0	6.0 6.5	9.5 10.0	4.0 4.0	10.5 10.5	ns
t_{PLH} t_{PHL}	Propagation delay M to $\overline{F}_i$ (Inv)	Diff	1	3.5 3.5	5.5 5.5	8.5 8.5	3.5 3.5	9.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay M to $\overline{F}_i$ (Non-Inv)	Diff	2	4.0 4.0	6.0 6.5	9.5 10.0	4.0 4.0	10.5 11.0	ns
t_{PLH} t_{PHL}	Propagation delay M to A = B (Inv)	Sum	1	5.0 10.0	8.0 13.0	10.5 16.5	5.0 10.0	11.0 18.5	ns
t_{PLH} t_{PHL}	Propagation delay M to A = B (Non-Inv)	Sum	2	10.0 7.0	14.0 9.5	17.0 12.5	10.0 7.0	18.5 13.5	ns
t_{PLH} t_{PHL}	Propagation delay M to A = B (Inv)	Diff	1	5.0 10.0	7.5 13.0	10.5 16.5	5.0 10.0	11.0 19.0	ns
t_{PLH} t_{PHL}	Propagation delay M to A = B (Non-Inv)	Diff	2	10.0 6.0	13.0 9.5	16.5 12.5	10.0 6.0	19.0 14.0	ns

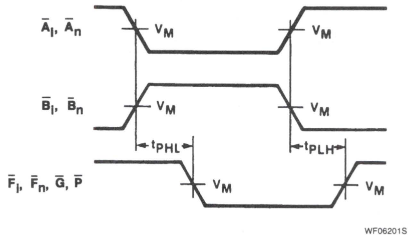
AC WAVEFORMS


$\overline{A}_n$, $\overline{B}_n$
V_M
V_M
t_{PHL}
t_{PLH}
$\overline{F}_n$, C_{n+4}
V_M
V_M
WF07540S

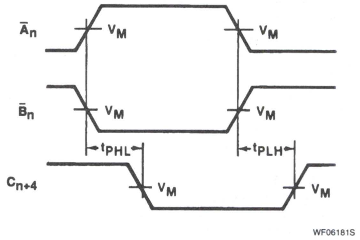
Waveform 1. Propagation Delay for Operands to Carry Output and Outputs


$\overline{A}_i$; $\overline{A}_n$, $\overline{B}_n$; C_n
V_M
V_M
t_{PHL}
t_{PLH}
$\overline{F}_i$; $\overline{G}$, $\overline{P}$, $\overline{F}_n$; C_{n+4}
V_M
V_M
WF0605DS

Waveform 2. Propagation Delays for Carry Input to Carry Output, Carry Input to Outputs, and Operands to Carry Generate Operands to Carry Generate and Carry Propagate Outputs


$\overline{A}_i$, $\overline{A}_n$
V_M
V_M
$\overline{B}_i$, $\overline{B}_n$
V_M
V_M
t_{PHL}
t_{PLH}
$\overline{F}_i$, $\overline{F}_n$, $\overline{G}$, $\overline{P}$
V_M
V_M
WF06201S

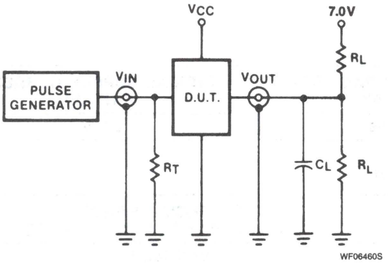
Waveform 3. Propagation Delay for Operands to Carry Generate and Propagate Outputs, Operands to A = B Output, and Outputs


$\overline{A}_n$
V_M
V_M
$\overline{B}_n$
V_M
V_M
t_{PHL}
t_{PLH}
C_{n+4}
V_M
V_M
WF06181S

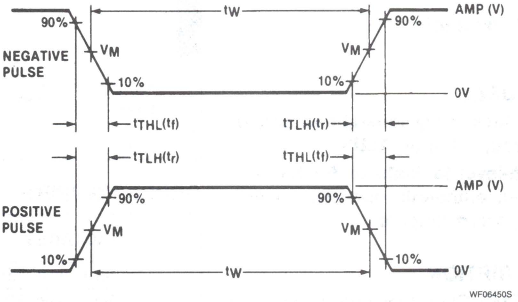
Waveform 4. Propagation Delays for Operands to Carry Output

NOTE: For all waveforms, $V_M = 1.5V$.

TEST CIRCUITS AND WAVEFORMS


VCC
7.0V
RL
PULSE GENERATOR
VIN
D.U.T.
VOUT
RT
CL
RL
WF06460S

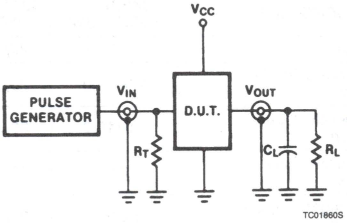
Test Circuit for Open-Collector Outputs


tW
90%
AMP (V)
90%
NEGATIVE PULSE
VM
VM
10%
10%
0V
tTHL(tf)
tTLH(tr)
tTLH(tr)
tTHL(tf)
AMP (V)
90%
90%
POSITIVE PULSE
VM
VM
10%
10%
0V
tW
WF06450S

$V_M = 1.5V$

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns


VCC
PULSE GENERATOR
VIN
D.U.T.
VOUT
RT
CL
RL
TC01860S

Test Circuit for Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Signetics

FAST 74F182
Carry Look-Ahead Generator

Carry Look-Ahead Generator
Product Specification

FAST Products

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F182	5.0ns	21mA

FEATURES

- **Provides carry look-ahead across a group of four ALU's**
- **Multi-level look-ahead for high-speed arithmetic operation over long word lengths**

DESCRIPTION

The 'F182 Carry look-ahead generator accepts up to four pairs of active-Low Carry Propagate ($\overline{P}_0$, $\overline{P}_1$, $\overline{P}_2$, $\overline{P}_3$) and Carry Generate ($\overline{G}_0$, $\overline{G}_1$, $\overline{G}_2$, $\overline{G}_3$) signals and an active-High Carry input (C_n) and provides anticipated active-High carries (C_{n+x}, C_{n+y}, C_{n+z}) across four groups of binary adders. The 'F182 also has active-Low Carry Propagate ($\overline{P}$) and Carry Generate ($\overline{G}$) outputs which may be used for further levels of look-ahead.

The logic equations provided at the outputs are:

$$C_{n+x} = G_0 + P_0C_n$$
$$C_{n+y} = G_1 + P_1G_0 = P_1P_0C_n$$
$$C_{n+z} = G_2 + P_2G_1 + P_2P_2G_0 + P_2P_1P_0C_n$$
$$\overline{G} = \overline{G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0}$$
$$\overline{P} = \overline{P_3P_2P_1P_0}$$

The 'F182 can also be used with binary ALU's in an active-Low or active-High input operand mode. The connections to and from the ALU to the Carry look-ahead generator are identical in both cases.

ORDERING INFORMATION

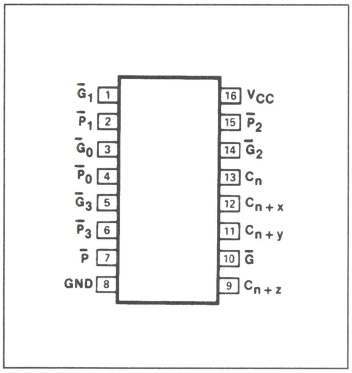
PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
16-Pin Plastic DIP	N74F182N
16-Pin Plastic SO	N74F182D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

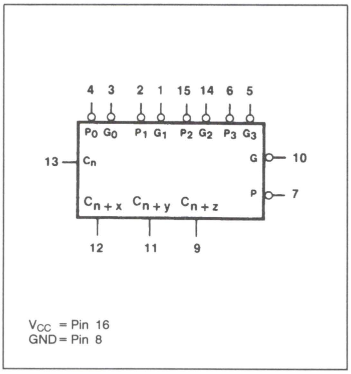
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
C_n	Carry input	1.0/2.0	20μA/1.2mA
$\overline{G}_0$, $\overline{G}_2$	Carry generate inputs (active-Low)	1.0/14.0	20μA/8.4mA
$\overline{G}_1$	Carry generate input (active-Low)	1.0/16.0	20μA/9.6mA
$\overline{G}_3$	Carry generate input (active-Low)	1.0/8.0	20μA/4.8mA
$\overline{P}_0$, $\overline{P}_1$	Carry propagate inputs (active-Low)	1.0/8.0	20μA/4.8mA
$\overline{P}_2$	Carry propagate input (active-Low)	1.0/6.0	20μA/3.6mA
$\overline{P}_3$	Carry propagate input (active-Low)	1.0/4.0	20μA/2.4mA
$C_{n+x} - C_{n+z}$	Carry outputs	50/33	1.0mA/20mA
$\overline{G}$	Carry generate output (active-Low)	50/33	1.0mA/20mA
$\overline{P}$	Carry propagate output (active-Low)	50/33	1.0mA/20mA

NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION

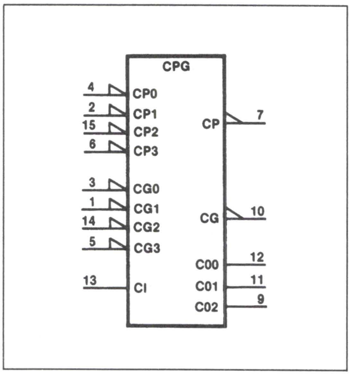

$\overline{G}_1$ 1
$\overline{P}_1$ 2
$\overline{G}_0$ 3
$\overline{P}_0$ 4
$\overline{G}_3$ 5
$\overline{P}_3$ 6
$\overline{P}$ 7
GND 8
16 V_{CC}
15 $\overline{P}_2$
14 $\overline{G}_2$
13 C_n
12 C_{n+x}
11 C_{n+y}
10 $\overline{G}$
9 C_{n+z}

LOGIC SYMBOL


4 3 2 1 15 14 6 5
P_0 G_0 P_1 G_1 P_2 G_2 P_3 G_3
13 C_n
G 10
P 7
C_{n+x} C_{n+y} C_{n+z}
12 11 9

V_{CC} = Pin 16
GND = Pin 8

LOGIC SYMBOL (IEEE/IEC)

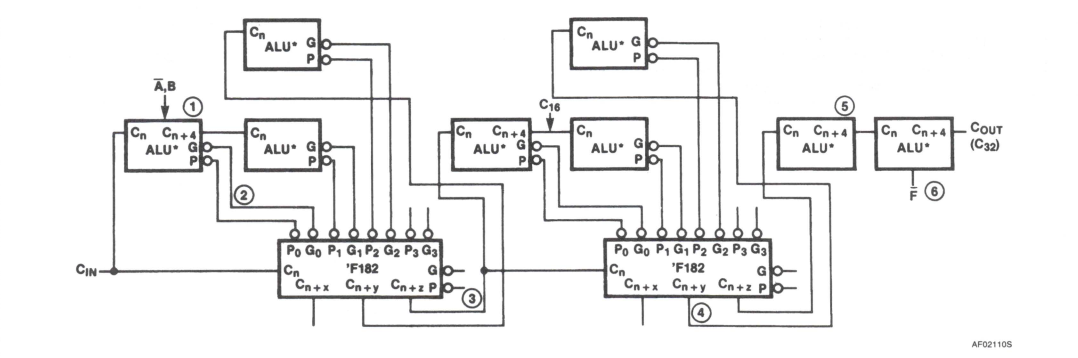

CPG
4 CP0
2 CP1
15 CP2
6 CP3
CP 7
3 CG0
1 CG1
14 CG2
5 CG3
CG 10
13 CI
C00 12
C01 11
C02 9

FUNCTION TABLE

INPUTS									OUTPUTS				
C_n	$\overline{G}_0$	$\overline{P}_0$	$\overline{G}_1$	$\overline{P}_1$	$\overline{G}_2$	$\overline{P}_2$	$\overline{G}_3$	$\overline{P}_3$	C_{n+x}	C_{n+y}	C_{n+z}	$\overline{G}$	$\overline{P}$
X	H	H							L				
L	H	X							L				
X	L	X							H				
H	X	L							H				
X	X	X	H	H						L			
X	H	H	H	X						L			
L	H	X	H	X						L			
X	X	X	L	X						H			
X	L	X	X	L						H			
H	X	L	X	L						H			
X	X	X	X	X	H	H					L		
X	X	X	H	H	H	X					L		
X	H	H	H	X	H	X					L		
L	H	X	H	X	H	X					L		
X	X	X	X	X	L	X					H		
X	X	X	L	X	X	L					H		
X	L	X	X	L	X	L					H		
H	X	L	X	L	X	L					H		
	X		X	X	X	X	H	H				H	
	X		X	X	H	H	H	X				H	
	X		H	H	H	X	H	X				H	
	H		H	X	H	X	H	X				H	
	X		X	X	X	X	L	X				L	
	X		X	X	L	X	X	L				L	
	X		L	X	X	L	X	L				L	
	L		X	L	X	L	X	L				L	
		H		X		X		X					H
		X		H		X		X					H
		X		X		H		X					H
		X		X		X		H					H
		L		L		L		L					L

H = High voltage level
L = Low voltage level
X = Don't care

APPLICATION


Cn
ALU*
G
P
Ā,B
①
Cn Cn+4
ALU*
②
③
④
⑤
⑥
C16
COUT
(C32)
F
P0 G0 P1 G1 P2 G2 P3 G3
Cn
'F182
Cn+x Cn+y Cn+z
CIN
AF02110S

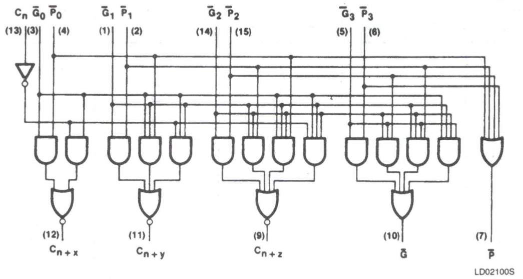
*ALU's may be either 'F181, F381 or 2901A.

32-Bit ALU With Ripple Carry Between 16-Bit Look-Ahead ALUs

Carry Look-Ahead Generator

FAST 74F182

LOGIC DIAGRAM


C_n
$\bar{G}_0$
$\bar{P}_0$
$\bar{G}_1$
$\bar{P}_1$
$\bar{G}_2$
$\bar{P}_2$
$\bar{G}_3$
$\bar{P}_3$
(13)
(3)
(4)
(1)
(2)
(14)
(15)
(5)
(6)
(12)
C_{n+x}
(11)
C_{n+y}
(9)
C_{n+z}
(10)
$\bar{G}$
(7)
$\bar{P}$
LD02100S

V_{CC} = Pin 16
GND = Pin 8
( ) = Pin numbers

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

Carry Look-Ahead Generator FAST 74F182

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		74F182			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX V_{IH} = MIN,	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OL} = MAX V_{IH} = MIN,	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	C_n	V_{CC} = MAX, V_I = 0.5V				-1.2	mA
		$\overline{G}_0$, $\overline{G}_2$					-8.4	mA
		$\overline{G}_1$					-9.6	mA
		$\overline{G}_3$, $\overline{P}_0$, $\overline{P}_1$					-4.8	mA
		$\overline{P}_2$					-3.6	mA
		$\overline{P}_3$					-2.4	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current[4] (total)	I_{CCH}	V_{CC} = MAX			18.0	28	mA
		I_{CCL}				24.0	36	mA

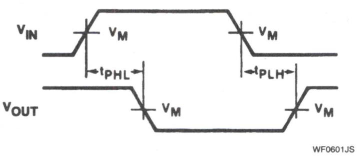
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. I_{CC} is measured with $\overline{G}_0$, $\overline{G}_1$, and $\overline{G}_2$ inputs at 4.5V; all other inputs grounded and all outputs open.

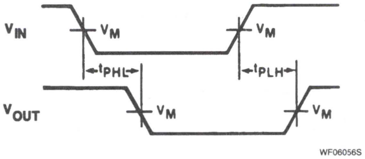
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F182					UNIT
			T_A = +25°C V_{CC} = +5.0V C_L = 50pF R_L = 500Ω			T_A = 0 to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay C_n to C_{n+x}, C_{n+y}, C_{n+z}	Waveform 2	2.5 2.5	5.0 5.0	8.0 7.5	2.5 2.5	8.5 8.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{P}_0$, $\overline{P}_1$ or $\overline{P}_2$, to C_{n+x}, C_{n+y}, C_{n+z}	Waveform 1	2.0 1.5	5.0 3.5	7.0 5.0	1.5 1.5	8.0 6.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{G}_0$, $\overline{G}_1$ or $\overline{G}_2$ to C_{n+x}, C_{n+y}, C_{n+z}	Waveform 1	1.5 1.5	4.0 3.0	7.5 5.0	1.5 1.5	8.5 5.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{P}_1$, $\overline{P}_2$ or $\overline{P}_3$ to $\overline{G}$	Waveform 2	2.0 3.0	7.0 5.0	10.0 7.0	1.5 2.5	11.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{G}_n$ to $\overline{G}$	Waveform 2	1.5 3.0	5.0 5.0	7.0 7.0	1.5 2.5	7.5 8.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{P}_n$ to $\overline{P}$	Waveform 2	1.5 2.5	3.5 4.0	6.0 6.0	1.5 2.5	7.5 6.5	ns

AC WAVEFORMS


V_{IN}
V_M
V_M
t_{PHL}
t_{PLH}
V_{OUT}
V_M
V_M
WF0601JS

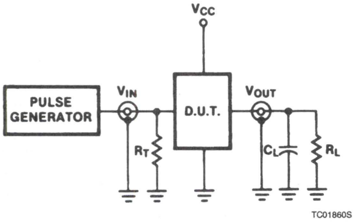
Waveform 1. For Inverting Outputs


V_{IN}
V_M
V_M
t_{PHL}
t_{PLH}
V_{OUT}
V_M
V_M
WF06056S

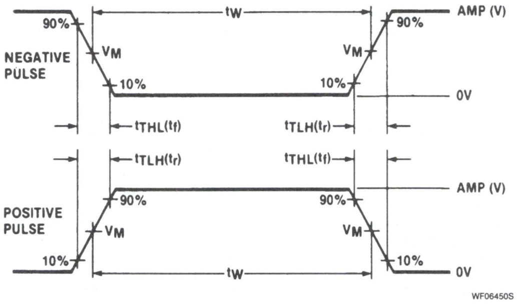
Waveform 2. For Non-Inverting Outputs

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORM


V_{CC}
PULSE GENERATOR
V_{IN}
D.U.T.
V_{OUT}
R_T
C_L
R_L
TC01860S

Test Circuit for Totem-Pole Outputs


tw
90%
AMP (V)
NEGATIVE PULSE
V_M
V_M
10%
10%
0V
$t_{THL}(t_f)$
$t_{TLH}(t_r)$
$t_{TLH}(t_r)$
$t_{THL}(t_f)$
AMP (V)
90%
90%
POSITIVE PULSE
V_M
V_M
10%
10%
0V
tw
WF06450S

V_M = 1.5V

Input Pulse Definition

DEFINITIONS
R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F189A
64-Bit TTL Bipolar RAM

Objective Specification

FAST Products

DESCRIPTION

The 74F189 is a high-speed, 64-bit RAM organized as a 16-word by 4-bit array. Address inputs are buffered to minimize loading and are fully decoded on-chip. The outputs are 3-State and are in the High-impedance state whenever the Chip Select ($\overline{CE}$) input is High. The outputs are active only in the Read mode and the output data is the complement of the stored data.

Ordering information can be found on the following page.

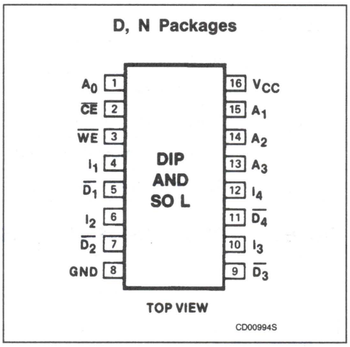
FEATURES

- **Address access time: 15ns max**
- **Power dissipation: 4.3mW/bit typ**
- **Schottky clamped TTL**
- **One chip enable input**
- **I/O**
  - **Inputs: PNP Buffered**
  - **Outputs: 3-State**

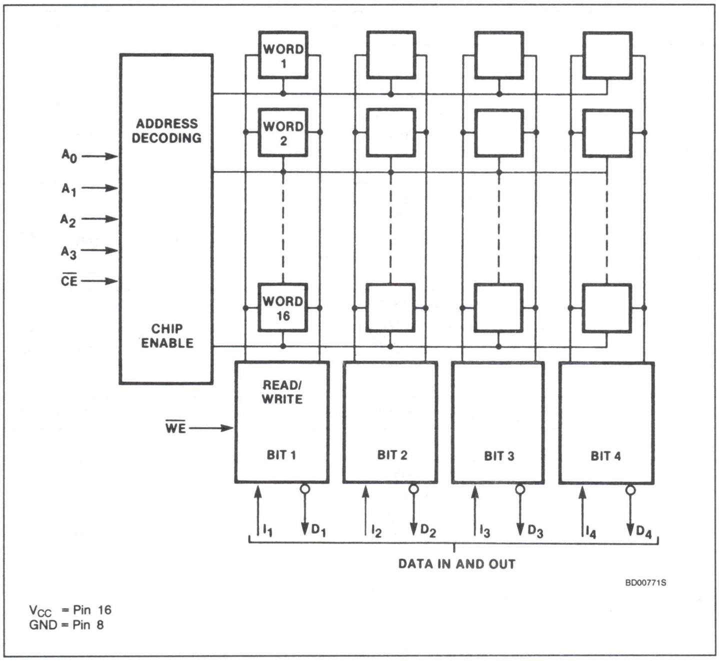
APPLICATIONS

- **Scratch pad memory**
- **Buffer memory**
- **Push down stacks**
- **Control store**

PIN CONFIGURATION


D, N Packages
A0 1
CE 2
WE 3
I1 4
D1 5
I2 6
D2 7
GND 8
16 VCC
15 A1
14 A2
13 A3
12 I4
11 D4
10 I3
9 D3
DIP AND SO L
TOP VIEW
CD00994S

BLOCK DIAGRAM


ADDRESS DECODING
CHIP ENABLE
A0
A1
A2
A3
CE
WORD 1
WORD 2
WORD 16
READ/ WRITE
WE
BIT 1
BIT 2
BIT 3
BIT 4
I1
D1
I2
D2
I3
D3
I4
D4
DATA IN AND OUT
BD00771S
VCC = Pin 16
GND = Pin 8

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16-Pin Plastic Dual-In-Line 300mil-wide	N74F189N
16-Pin Plastic Small Outline 300mil-wide	N74F189D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V_{DC}
V_{IN}	Input voltage	−0.5 to +7.0	V_{DC}
V_{OH}	Output voltage High	−0.5 to +5.5	V_{DC}
T_A	Operating temperature range	0 to +75	°C
T_{STG}	Storage temperature range	−65 to +150	°C

DC ELECTRICAL CHARACTERISTICS $0°C \leqslant T_A \leqslant +75°C$, $4.75V \leqslant V_{CC} \leqslant 5.25V$.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ[3]	Max	
Input voltage[2]						
V_{IC}[7]	Clamp	$V_{CC} = 5.25V$, $I_I = -18mA$			−1.2	V
Output voltage						
V_{OH} V_{OL}[2,3]	High Low	$V_{CC} = 4.75V$, $V_{IH} = 2.0V$, $V_{IL} = 0.8V$ $I_{OH} = -3.0mA$ $I_{OL} = 20mA$	2.4	0.35	0.5	V
Input current						
I_{IH} I_{IL}	High Low	$V_{CC} = 5.25V$ $V_{IN} = 5.5V$ $V_{IN} = 0.5V$			40 0.6	μA
Output current						
I_{OZ} I_{OS}	Off-state Short circuit	$V_{CC} = 5.25V$ $V_{IH} = 2.0V$, $2.4V \geqslant V_{OUT} \geqslant 0.5V$ $V_{CC} = 5.25V$	−60		±50 −150	μA mA
Supply current[6]						
I_{CC}		$V_{CC} = 5.25V$, $\overline{WE}$, $\overline{CE}$ = GND			70	mA
Capacitance						
C_{IN} C_{OUT}	Input Output	$V_{CC} = 5.0V$ $V_{IN} = 2.0V$ $V_{OUT} = 2.0V$		5 8		pF

TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	D_{IN}	DATA OUT
Read	0	1	X	Stored $\overline{\text{Data}}$
Write "0"	0	0	0	Hi-Z
Write "1"	0	0	1	Hi-Z
Disable	1	X	X	Hi-Z

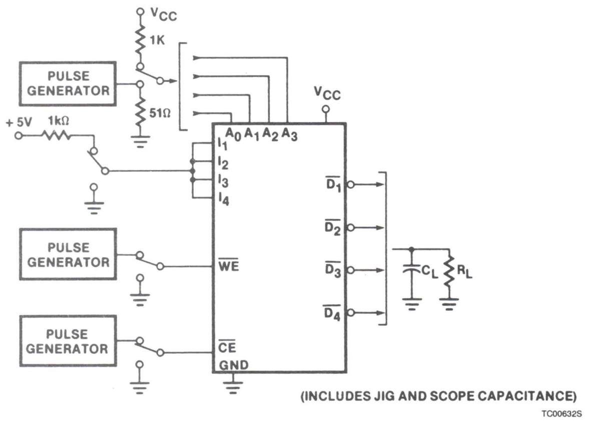
X = Don't care

AC ELECTRICAL CHARACTERISTICS $R_L = 500\Omega$, $C_L = 30pF$, $0°C \leqslant T_A \leqslant +75°C$, $4.75V \leqslant V_{CC} \leqslant 5.25V$

SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ	Max	
Access time							
t_{AA} t_{CE}	Address Chip enable					15 13	ns
Disable time[8]							
t_{CD}		Output	Chip enable			9	ns
Response time[8]							
t_{WD}		Output	Write enable			9	ns
Write recovery time							
t_{WR}		Output	Write enable			13	ns
Setup and hold time							
t_{WSA}[9] t_{WHA}	Setup time Hold time	Write enable	Address	3 2			ns
t_{WSD} t_{WHD}	Setup time Hold time	Write enable	Data in	13 2			
t_{WSC} t_{WHC}	Setup time Hold time	Write enable	$\overline{CE}$	3 2			
Pulse width							
t_{WP}[1]0	Write enable			10			ns

NOTES:
1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. Output sink current is supplied through a resistor to V_{CC}.
3. All sense outputs in Low state.
4. To guarantee a Write into the slowest bit.
5. Positive current is defined as into the terminal referenced.
6. I_{CC} is measured with the Write enable and memory enable inputs grounded, all other inputs at 0.45V, and the output open.
7. Test each input one at a time.
8. Measured at a delta of 0.5V from the logic level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5pF$.
9. Measured with minimum t_{WP}.
10. Measured with minimum t_{WSA}.

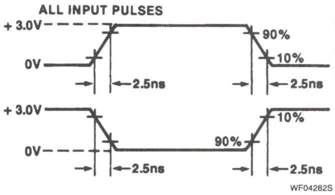
TEST LOAD CIRCUIT


VCC
1K
PULSE GENERATOR
51Ω
+5V 1kΩ
A0 A1 A2 A3
I1
I2
I3
I4
VCC
D1
D2
D3
D4
CL
RL
PULSE GENERATOR
WE
PULSE GENERATOR
CE
GND
TC00632S

(INCLUDES JIG AND SCOPE CAPACITANCE)

Loading Conditions

VOLTAGE WAVEFORM

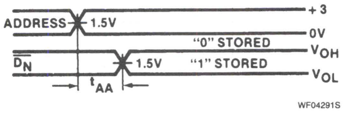

ALL INPUT PULSES
+3.0V
0V
90%
10%
2.5ns
2.5ns
+3.0V
0V
10%
90%
2.5ns
2.5ns
WF04282S

MEASUREMENTS:
All circuit delays are measured at the +1.5V level of inputs and output.

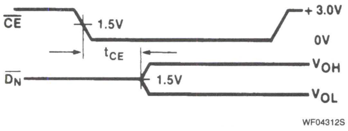
Input Pulses

TIMING DIAGRAMS

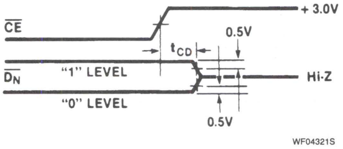
Read Cycle


ADDRESS
1.5V
+3
0V
"0" STORED
VOH
DN
1.5V
"1" STORED
VOL
tAA
WF04291S

Address Access Time

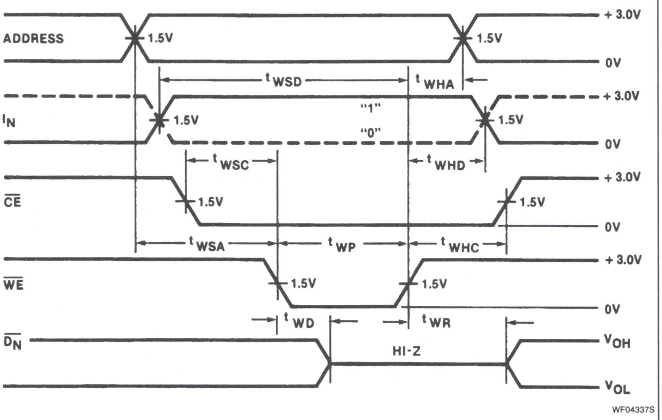

CE
1.5V
+3.0V
0V
tCE
DN
1.5V
VOH
VOL
WF04312S

Chip Enable


CE
+3.0V
0.5V
tCD
DN
"1" LEVEL
"0" LEVEL
Hi-Z
0.5V
WF04321S

Chip Disable

Write Cycle


ADDRESS
1.5V
1.5V
+3.0V
0V
tWSD
tWHA
IN
1.5V
"1"
"0"
1.5V
+3.0V
0V
tWSC
tWHD
CE
1.5V
1.5V
+3.0V
0V
tWSA
tWP
tWHC
WE
1.5V
1.5V
+3.0V
0V
tWD
tWR
DN
HI-Z
VOH
VOL
WF04337S

All AC parameters are measured at 1.5V unless otherwise specified.

Signetics

FAST 74F190, 74F191
Counters

'F190 Asynchronous Presettable BCD/Decade Up/Down Counter
'F191 Asynchronous Presettable 4-Bit Binary Up/Down Counter
Product Specification

FAST Products

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F190	125MHz	40mA
74F191	125MHz	40mA

FEATURES
- High-speed — 125MHz typical f_{MAX}
- Synchronous, reversible counting
- BCD/decade — 'F190
4-bit binary — 'F191
- Asynchronous Parallel Load capability
- Cascadable without external logic
- Single up/down control input

DESCRIPTION
The 'F190 is an asynchronously presettable up/down BCD decade counter. It contains four master/slave flip-flops with internal gating and steering logic to provide asynchronous preset and synchronous count-up and count-down operation. The 'F191 is similar, but is a 4-bit binary counter.

Asynchronous Parallel Load capability permits the counter to be preset to any desired number. Information present on the parallel Data inputs ($D_0 - D_3$) is loaded into the counter and appears on the outputs when the Parallel Load ($\overline{PL}$) input is Low. As indicated in the Mode Select Table, this operation overrides the counting function.

ORDERING INFORMATION

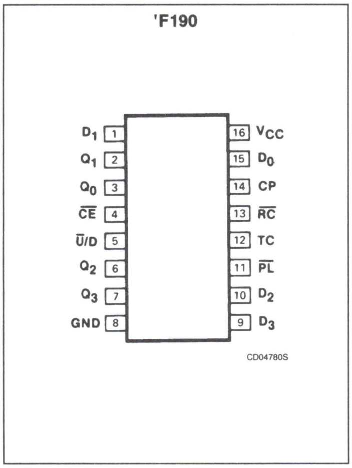
PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
16-Pin Plastic DIP	N74F190N, N74F191N
16-Pin Plastic SO	N74F190D, N74F191D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

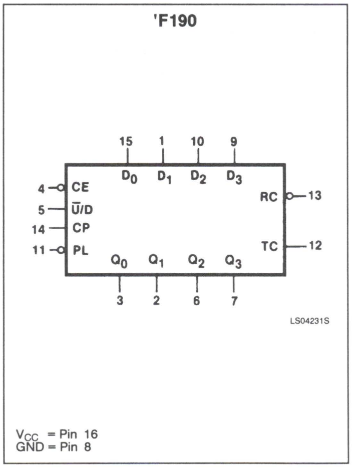
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$D_0 - D_3$	Parallel data inputs	1.0/1.0	20μA/0.6mA
$\overline{CE}$	Count enable input (active-Low)	1.0/3.0	20μA/1.8mA
CP	Clock pulse input (active rising edge)	1.0/1.0	20μA/0.6mA
$\overline{PL}$	Asynchronous Parallel Load input (active-Low)	1.0/1.0	20μA/0.6mA
$\overline{U}/D$	Up/down count control input	1.0/1.0	20μA/0.6mA
$Q_0 - Q_3$	Flip-flop outputs	50/33	1.0mA/20mA
$\overline{RC}$	Ripple clock output (active-Low)	50/33	1.0mA/20mA
TC	Terminal count output (active-High)	50/33	1.0mA/20mA

NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

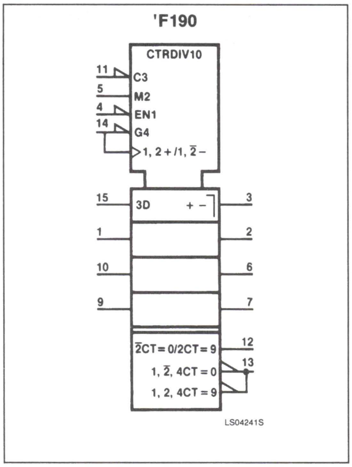
PIN CONFIGURATION


'F190
D1 1
Q1 2
Q0 3
CE 4
U/D 5
Q2 6
Q3 7
GND 8
16 VCC
15 D0
14 CP
13 RC
12 TC
11 PL
10 D2
9 D3
CD04780S

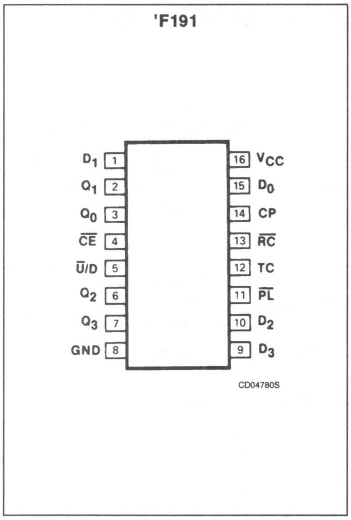
LOGIC SYMBOL


'F190
15
1
10
9
D0
D1
D2
D3
4 CE
5 U/D
14 CP
11 PL
RC 13
TC 12
Q0
Q1
Q2
Q3
3
2
6
7
LS04231S
VCC = Pin 16
GND = Pin 8

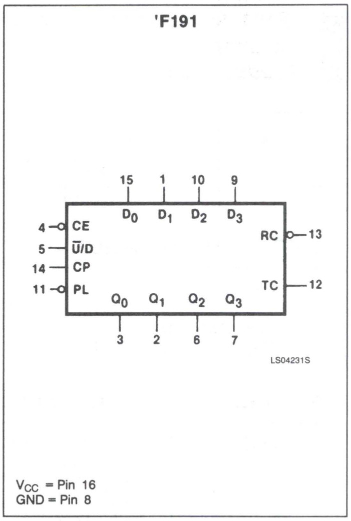
LOGIC SYMBOL (IEEE/IEC)


'F190
CTRDIV10
11 C3
5 M2
4 EN1
14 G4
1, 2 + /1, 2 −
15 3D + −
3
1
2
10
6
9
7
2CT = 0/2CT = 9 12
1, 2, 4CT = 0 13
1, 2, 4CT = 9
LS04241S

PIN CONFIGURATION

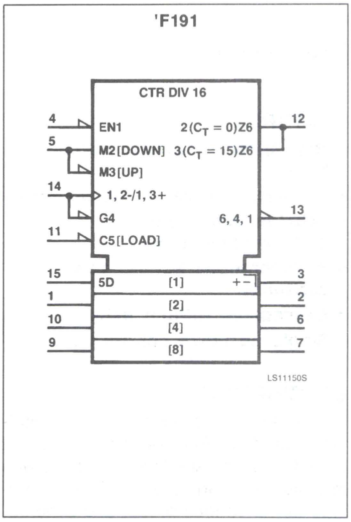


LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

LOGIC SYMBOL (IEEE/IEC)



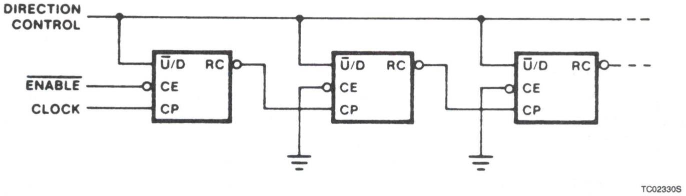
Counting is inhibited by a High level on the Count Enable ($\overline{\text{CE}}$) input. When $\overline{\text{CE}}$ is Low, internal state changes are initiated.

Overflow/underflow indications are provided by two types of outputs, the Terminal Count (TC) and Ripple Clock ($\overline{\text{RC}}$). The TC output is normally Low and goes High when: 1) the count reaches zero in the count-down mode or 2) reaches "9" for 'F190 or "15" for 'F191 in the count-up mode. The TC output will remain High until a state change occurs, either by counting or presetting, or until $\overline{\text{U}}$/D is changed. TC output should not be used as a clock signal because it is subject to decoding spikes. The TC signal is used internally to enable the $\overline{\text{RC}}$ output. When TC is High and $\overline{\text{CE}}$ is Low, the RC follows the Clock Pulse. The $\overline{\text{RC}}$ output essentially duplicates the Low clock pulse width, although delayed in time by two gate delays. The 'F190/'F191 simplifies the design of multistage counters, as indicated in Figures 1a and 1b.

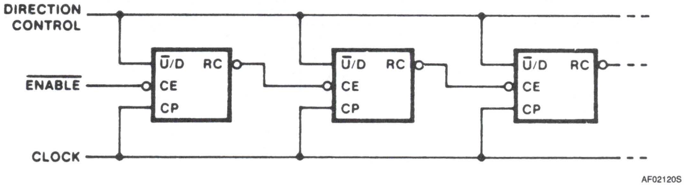
In Figure 1a, each $\overline{\text{RC}}$ output is used as the Clock input for the next higher stage. When the Clock input source has limited drive capability this configuration is particularly advantageous, since the clock source drives only the first stage. It is only necessary to inhibit the first stage to prevent counting in all stages, since a High signal on $\overline{\text{CE}}$ inhibits the $\overline{\text{RC}}$ output pulse as indicated in the Mode Select Table. The timing skew between state changes in the first and last stages is represented by the cumulative delay of the clock as it ripples through the preceding stages. This is a disadvantage of the configuration in some applications.

Figure 1b shows a method of causing state changes to occur simultaneously in all stages. The $\overline{\text{RC}}$ outputs propagate the carry/borrow signals in ripple fashion and all Clock inputs are driven in parallel. The Low state duration of the clock in this configuration must be long enough to allow the negative-going edge of the carry/borrow signal to ripple through to the last stage before the clock goes High. Since the $\overline{\text{RC}}$ output of any package goes High shortly after its CP input goes High, there is no such restriction on the High state duration of the clock.

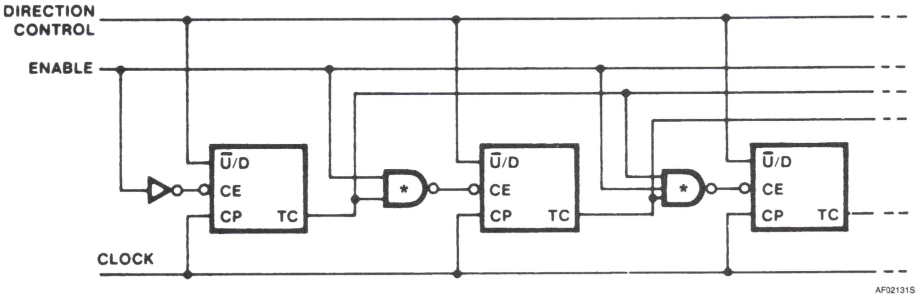
In Figure 1c, the configuration shown avoids ripple delays and their associated restrictions. Combining the TC signals from all the preceding stages forms the $\overline{\text{CE}}$ input signal for a given stage. An enable signal must be included in each carry gate in order to inhibit counting. The TC output of a given stage is not affected by its own $\overline{\text{CE}}$, therefore, the simple inhibit scheme of Figure 1a and 1b does not apply.


DIRECTION CONTROL
ENABLE
CLOCK
U/D
RC
CE
CP
TC02330S

a. N-Stage Counter Using Ripple Clock


DIRECTION CONTROL
ENABLE
CLOCK
U/D
RC
CE
CP
AF02120S

b. Synchronous N-Stage Counter With Common Clock Using Ripple Clock


DIRECTION CONTROL
ENABLE
CLOCK
U/D
CE
CP
TC
*
AF02131S

* Carry Gate

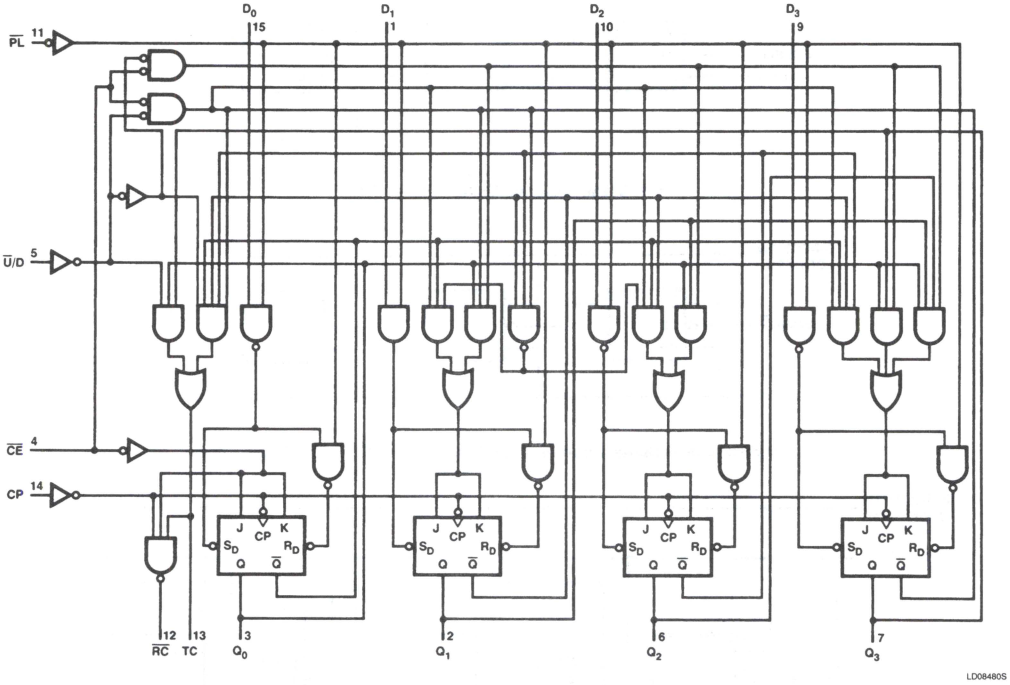
c. Synchronous N-Stage Counter With Common Clock and Parallel Gated Terminal Count

Figure 1

Counters

FAST 74F190, 74F191

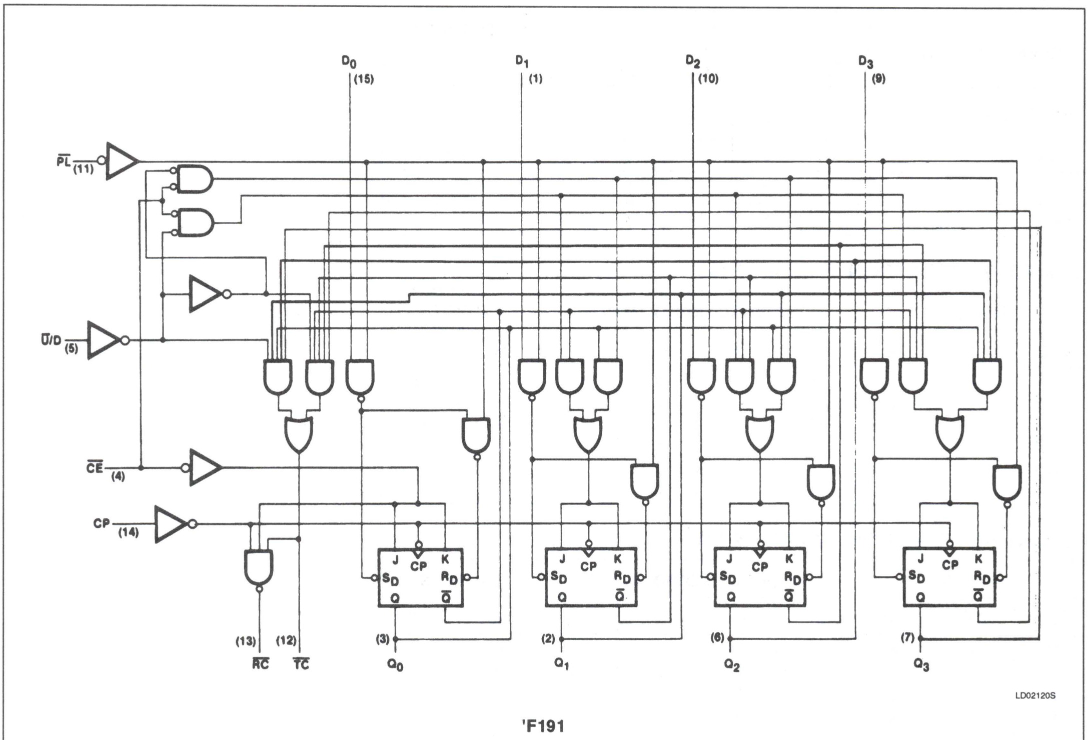
LOGIC DIAGRAM


D0
15
D1
1
D2
10
D3
9
PL
11
U/D
5
CE
4
CP
14
J
CP
K
SD
RD
Q
Q̄
12
RC
13
TC
3
Q0
2
Q1
6
Q2
7
Q3
LD08480S

'F190

VCC = Pin 16
GND = Pin 8

LOGIC DIAGRAM


D0
(15)
D1
(1)
D2
(10)
D3
(9)
PL (11)
U/D (5)
CE (4)
CP (14)
J
CP
K
SD
RD
Q
Q̄
(13)
(12)
RC
TC
(3)
Q0
(2)
Q1
(6)
Q2
(7)
Q3
LD02120S

'F191

VCC = Pin 16
GND = Pin 8
( ) = Pin numbers

MODE SELECT — FUNCTION TABLE, 'F190, 'F191

OPERATING MODE	INPUTS					OUTPUTS
	$\overline{PL}$	$\overline{U}/D$	$\overline{CE}$	CP	D_n	Q_n
Parallel load	L	X	X	X	L	L
	L	X	X	X	H	H
Count up	H	L	l	↑	X	count up
Count down	H	H	l	↑	X	count down
Hold "do nothing"	H	X	H	X	X	no change

TC AND $\overline{RC}$ FUNCTION TABLE, 'F190

INPUTS			TERMINAL COUNT STATE				OUTPUTS	
$\overline{U}/D$	$\overline{CE}$	CP	Q_0	Q_1	Q_2	Q_3	TC	$\overline{RC}$
H	H	X	H	X	X	H	L	H
L	H	X	H	X	X	H	H	H
L	L	⊔	H	X	X	H	↓	⊔
L	H	X	L	L	L	L	L	H
H	H	X	L	L	L	L	H	H
H	L	⊔	L	L	L	L	↓	⊔

TC AND $\overline{RC}$ FUNCTION TABLE, 'F191

INPUTS			TERMINAL COUNT STATE				OUTPUTS	
$\overline{U}/D$	$\overline{CE}$	CP	Q_0	Q_1	Q_2	Q_3	TC	$\overline{RC}$
H	H	X	H	H	H	H	L	H
L	H	X	H	H	H	H	H	H
L	L	⊔	H	H	H	H	↓	⊔
L	H	X	L	L	L	L	L	H
H	H	X	L	L	L	L	H	H
H	L	⊔	L	L	L	L	↓	⊔

H = High voltage level steady state.
L = Low voltage level steady state.
l = Low voltage level one setup time prior to the Low-to-High clock transition.
X = Don't care.
↑ = Low-to-High clock transition.
⊔ = Low pulse.

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		74F190, 191			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX V_{IH} = MIN,	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OL} = MAX V_{IH} = MIN,	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0				0.1	mA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current	$\overline{CE}$ input	V_{CC} = MAX, V_I = 0.5V				−1.8	mA
		Other inputs					−0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current[4] (total)		V_{CC} = MAX			40	55	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Measure I_{CC} with all inputs grounded and all outputs open.

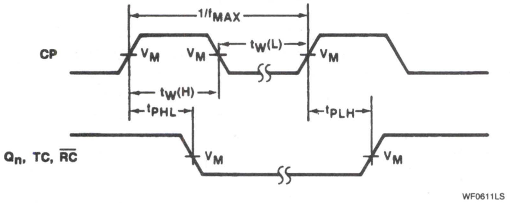
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	74F190, 74F191					UNIT
				$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
				Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	D_n to Q_n	Waveform 1	100	125		90		MHz
		D_n to $\overline{RC}$		85	95		75		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n		Waveform 1	2.5 5.0	4.5 7.5	8.0 11.5	2.0 5.0	8.5 12.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to TC		Waveform 1	6.5 6.0	9.0 8.0	12.5 11.0	6.0 6.0	13.0 12.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{RC}$		Waveform 2	2.5 3.0	4.5 5.0	7.5 7.5	2.0 2.5	8.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CE}$ to $\overline{RC}$		Waveform 2	2.0 3.0	4.0 5.0	7.0 7.5	2.0 3.0	7.5 8.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{U}/D$ to $\overline{RC}$		Waveform 2	8.0 4.5	11.0 7.5	16.0 10.5	8.0 4.0	17.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{U}/D$ to TC		Waveform 4	4.0 3.0	6.5 6.0	9.5 9.5	3.0 3.0	10.5 10.0	ns
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n		Waveform 3	2.0 6.5	4.0 9.0	7.0 12.0	1.5 6.5	7.5 13.0	ns
t_{PLH} t_{PHL}	Propagation delay D_n to TC		Waveform 3 Waveform 4	5.5 6.5	9.5 9.5	13.0 13.0	5.0 6.0	14.0 14.0	ns
t_{PLH} t_{PHL}	Propagation delay D_n to $\overline{RC}$		Waveform 3 Waveform 4	6.0 6.0	14.0 11.0	18.0 13.5	6.0 6.0	19.5 15.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to Q_n		Waveform 5	4.5 5.5	6.5 8.0	9.5 11.5	4.0 5.0	10.5 12.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to TC		Waveform 5	5.5 6.0	8.5 10.5	12.0 13.5	5.5 6.0	13.0 14.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to $\overline{RC}$		Waveform 5	8.5 7.5	16.0 10.0	18.5 13.0	8.5 7.0	21.0 13.5	ns

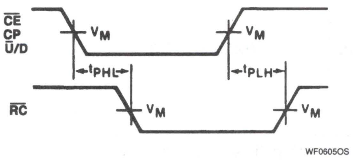
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	74F190, 74F191					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to $\overline{PL}$	Waveform 6	4.5 4.5			5.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to $\overline{PL}$	Waveform 6	2.0 2.0			2.0 2.0		ns
$t_s(L)$	Setup time, High or Low $\overline{CE}$ to CP	Waveform 6	10.0			10.0		ns
$t_h(L)$	Hold time, High or Low $\overline{CE}$ to CP	Waveform 6	0			0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{U}/D$ to CP	Waveform 6	12.0 12.0			12.0 12.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{U}/D$ to CP	Waveform 6	0 0			0 0		ns
$t_w(L)$	$\overline{PL}$ pulse width, Low	Waveform 5	6.0			6.0		ns
$t_w(H)$ $t_w(L)$	CP pulse width High or Low	Waveform 1	3.5 6.0			3.5 6.0		ns
t_{rec}	Recovery time, $\overline{PL}$ to CP	Waveform 5	6.0			6.0		ns

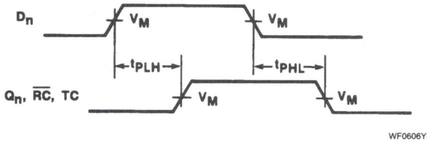
AC WAVEFORMS


1/fMAX
CP
VM
VM
tW(L)
VM
tW(H)
tPHL
tPLH
Qn, TC, RC
VM
VM
WF0611LS

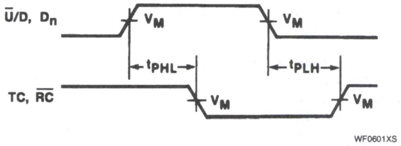
Waveform 1. Propagation Delay, Clock Input to Output, Clock Widths, and Maximum Clock Frequency


CE
CP
U/D
VM
VM
tPHL
tPLH
RC
VM
VM
WF0605OS

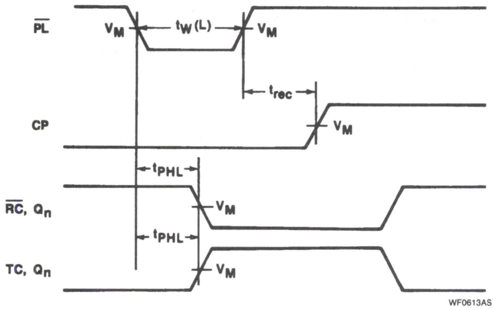
Waveform 2. Propagation Delay, Clock or Clock Enable to Ripple Clock Output


Dn
VM
VM
tPLH
tPHL
Qn, RC, TC
VM
VM
WF0606YS

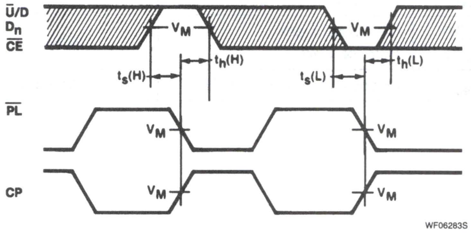
Waveform 3. Propagation Delay, Non-inverting Path


U/D, Dn
VM
VM
tPHL
tPLH
TC, RC
VM
VM
WF0601XS

Waveform 4. Propagation Delay, Inverting Path


PL
VM
tW (L)
VM
trec
CP
VM
tPHL
RC, Qn
VM
tPHL
TC, Qn
VM
WF0613AS

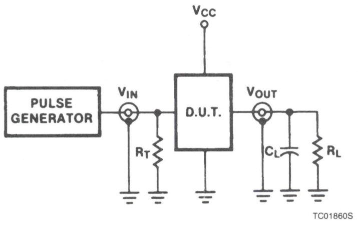
Waveform 5. Parallel Load Pulse Width, Parallel Load to Output Delay and Parallel Load to Clock Recovery Time


U/D
Dn
CE
VM
VM
ts(H)
th(H)
ts(L)
th(L)
PL
VM
VM
CP
VM
VM
WF06283S

Waveform 6. Setup Time and Hold Time for D_n to $\overline{\text{PL}}$, $\overline{\text{U}}$/D to CP and $\overline{\text{CE}}$ to CP

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS


VCC
PULSE GENERATOR
VIN
D.U.T.
VOUT
RT
CL
RL
TC01860S

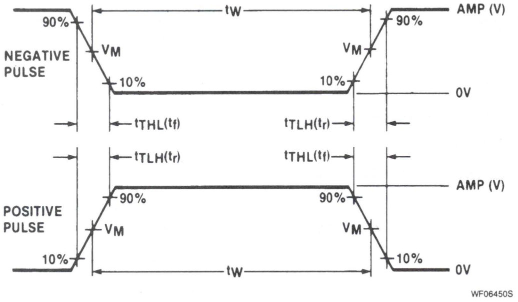
Test Circuit for Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.


tW
90%
AMP (V)
NEGATIVE PULSE
VM
10%
0V
tTHL(tf)
tTLH(tr)
tTLH(tr)
tTHL(tf)
POSITIVE PULSE
90%
VM
10%
AMP (V)
0V
tW
WF06450S

V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F192, 74F193
Counters

'F192 — Synchronous Presettable BCD Decade Up/Down Counter
'F193 — Synchronous Presettable 4-Bit Binary Down Counter
Product Specification

FAST Products

FEATURES

- **Synchronous reversible 4-bit binary counting**
- **Asynchronous parallel load**
- **Asynchronous reset (clear)**
- **Cascadable without external logic**

DESCRIPTION

The 'F192 and 'F193 are 4-bit synchronous up/down counters — the 'F192 counts in BCD mode and the 'F193 counts in the binary mode. Separate up/down clocks, CP_U and CP_D respectively, simplify operation. The outputs change state synchronously with the Low-to-High transition of either Clock input. If the CP_U clock is pulsed while CP_D is held High, the device will count up . . . if CP_D is pulsed while CP_U is held High, the device will count down. Only one Clock input can be held High at any time, or erroneous operation will result. The device can be cleared at any time by the asynchronous reset pin — it may also be loaded in parallel by activating the asynchronous parallel load pin.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F192	125MHz	32mA
74F193	125MHz	32mA

ORDERING INFORMATION

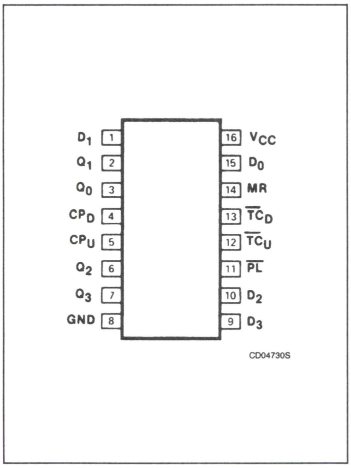
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ± 10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F192N, N74F193N
16-Pin Plastic SO	N74F192D, N74F193D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

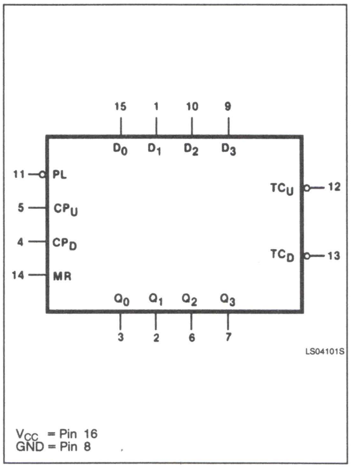
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$D_0 - D_3$	Data inputs	1.0/1.0	20μA/0.6mA
CP_U	Count up clock input (active rising edge)	1.0/3.0	20μA/1.8mA
CP_D	Count down clock input (active rising edge)	1.0/3.0	20μA/1.8mA
$\overline{PL}$	Asynchronous Parallel Load control input (active-Low)	1.0/1.0	20μA/0.6mA
MR	Asynchronous Master Reset input (active-High)	1.0/1.0	20μA/0.6mA
$Q_0 - Q_3$	Flip-flop outputs	50/33	1.0mA/20mA
$\overline{TC}_U$	Terminal count up (carry) output (active-Low)	50/33	1.0mA/20mA
$\overline{TC}_D$	Terminal count down (borrow) output (active-Low)	50/33	1.0mA/20mA

NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION

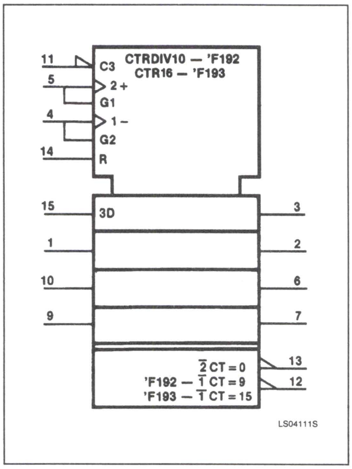

D1 1
Q1 2
Q0 3
CPD 4
CPU 5
Q2 6
Q3 7
GND 8
16 VCC
15 D0
14 MR
13 TCD
12 TCU
11 PL
10 D2
9 D3
CD04730S

LOGIC SYMBOL


15 1 10 9
D0 D1 D2 D3
11 PL
5 CPU
4 CPD
14 MR
TCU 12
TCD 13
Q0 Q1 Q2 Q3
3 2 6 7
LS04101S

V_{CC} = Pin 16
GND = Pin 8

LOGIC SYMBOL (IEEE/IEC)


11 C3
CTRDIV10 — 'F192
CTR16 — 'F193
5 2+
G1
4 1−
G2
14 R
15 3D 3
1 2
10 6
9 7
2CT=0 13
'F192 — 1CT=9 12
'F193 — 1CT=15
LS04111S

Counters

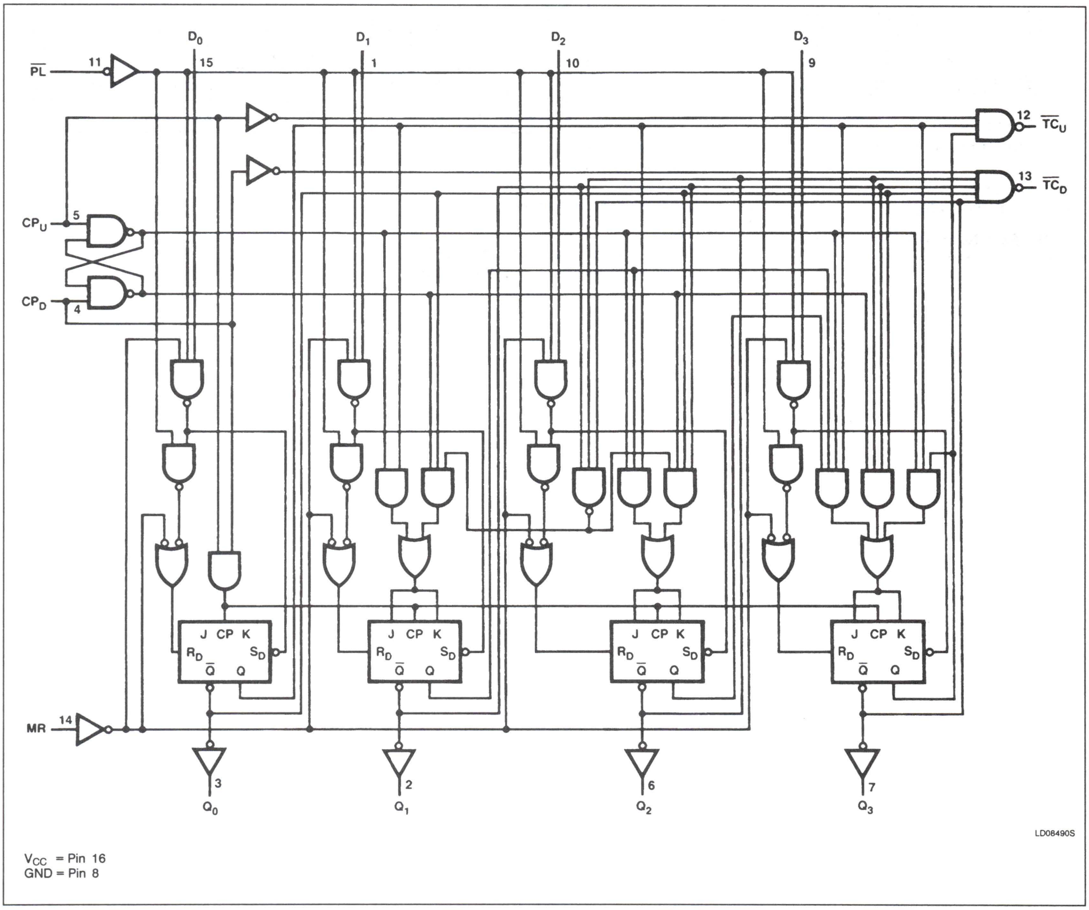
FAST 74F192, 74F193

Inside the device are four master-slave JK flip-flops with the necessary steering logic to provide the asynchronous reset, preset load, and synchronous count up and count down functions.

Each flip-flop contains JK feedback from slave to master such that a Low-to-High transition on the CP_D input will decrease the count by one, while a similar transition on the CP_U input will advance the count by one.

One clock should be held High while counting with the other, because the circuit will either count by two's or not at all depending on the state of the first flip-flop, which cannot toggle as long as either clock input is Low. Applications requiring reversible operation must make the reversing decision while the activating clock is High to avoid erroneous counts.

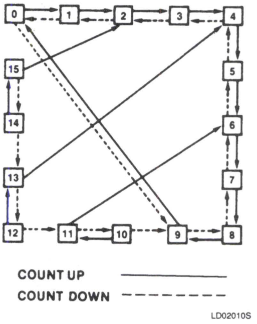
LOGIC DIAGRAM, 'F192



D_0
15
D_1
1
D_2
10
D_3
9
$\overline{PL}$
11
12
$\overline{TC}_U$
13
$\overline{TC}_D$
CP_U
5
CP_D
4
J CP K
R_D
S_D
$\overline{Q}$
Q
MR
14
3
Q_0
2
Q_1
6
Q_2
7
Q_3
LD08490S

V_{CC} = Pin 16
GND = Pin 8

STATE DIAGRAM, 'F192



$\overline{TC}_U = Q_0 \bullet Q_3 \bullet \overline{CP}_U$
$\overline{TC}_D = Q_0 \bullet Q_1 \bullet \overline{CP}_2 \bullet \overline{Q}_3 \bullet \overline{CP}_D$

Logic Equations for Terminal Count

MODE SELECT — FUNCTION TABLE, 'F192

OPERATING MODE	INPUTS								OUTPUTS					
	MR	$\overline{PL}$	CP_U	CP_D	D_0	D_1	D_2	D_3	Q_0	Q_1	Q_2	Q_3	$\overline{TC}_U$	$\overline{TC}_D$
Reset (clear)	H	X	X	L	X	X	X	X	L	L	L	L	H	L
	H	X	X	H	X	X	X	X	L	L	L	L	H	H
Parallel load	L	L	X	L	L	L	L	L	L	L	L	L	H	L
	L	L	X	H	L	L	L	L	L	L	L	L	H	H
	L	L	L	X	H	X	X	H	$Q_n = D_n$				L	H
	L	L	H	X	H	X	X	H	$Q_n = D_n$				H	H
Count up	L	H	↑	H	X	X	X	X	Count up				H[(1)]	H
Count down	L	H	H	↑	X	X	X	X	Count down				H	H[(2)]

H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-to-High clock transition

NOTES:

1. $\overline{TC}_U = CP_U$ at terminal count up (HLLH).
2. $\overline{TC}_D = CP_D$ at terminal count down (LLLL).

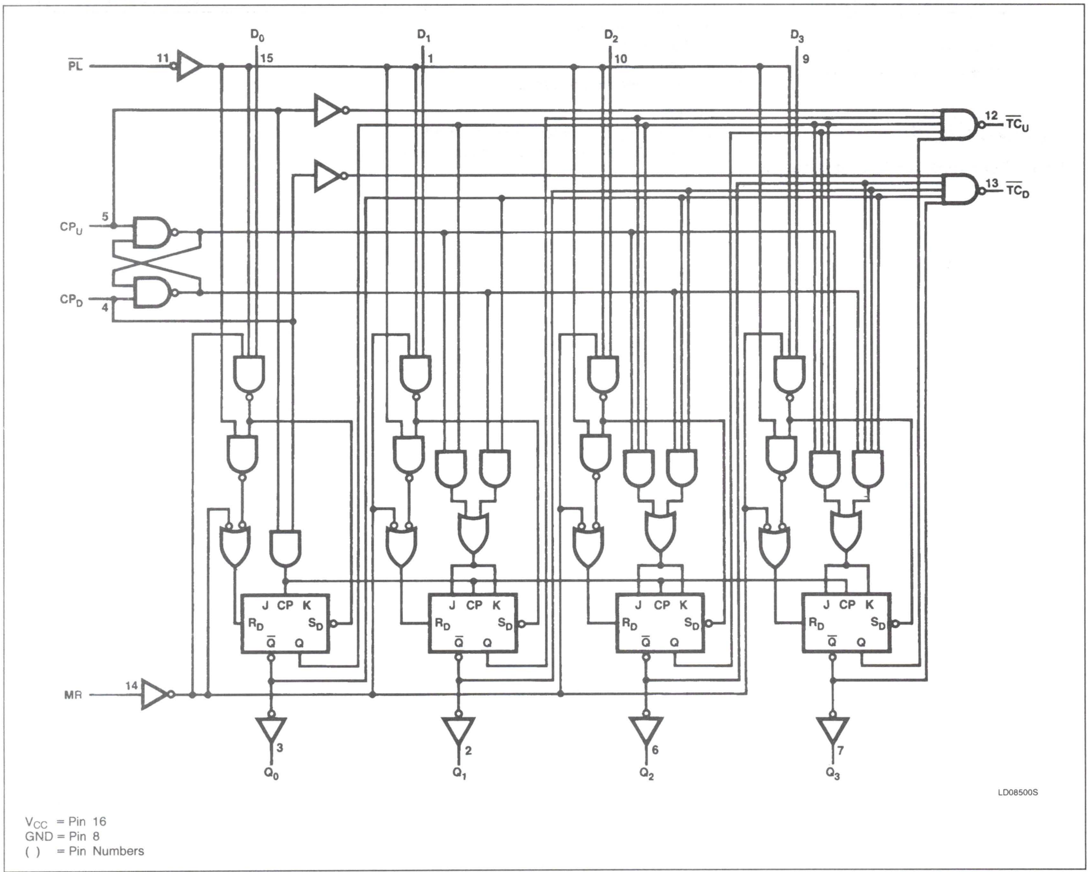
Counters

FAST 74F192, 74F193

The Terminal Count Up ($\overline{TC}_U$) and Terminal Count Down ($\overline{TC}_D$) outputs are normally High. When the circuit has reached the maximum count state of 9 (for the 'F192 and 15 for the 'F193), the next High-to-Low transition of CP_U will cause $\overline{TC}_U$ to go Low. $\overline{TC}_U$ will stay Low until CP_U goes High again, duplicating the count up clock, although delayed by two gate delays. Likewise, the $\overline{TC}_D$ output will go Low when the circuit is in the zero state and the CP_D goes Low. The $\overline{TC}$ outputs can be used as the Clock input signals to the next higher order circuit in a multistage counter, since they duplicate the clock waveforms. Multistage counters will not be fully synchronous, since there is a two-gate delay time difference added for each stage that is added.

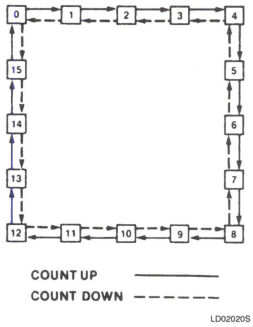
The counter may be preset by the asynchronous parallel load capability of the circuit. Information present on the parallel Data inputs ($D_0 - D_3$) is loaded into the counter and appears on the outputs regardless of the conditions of the Clock inputs when the Parallel Load ($\overline{PL}$) input is Low. A High level on the Master Reset (MR) input will disable the parallel load gates, override both Clock inputs, and set all Q outputs Low. If one of the Clock inputs is Low during and after a reset or load operation, the next Low-to-High transition of that clock will be interpreted as a legitimate signal and will be counted.

LOGIC DIAGRAM 'F193



VCC = Pin 16
GND = Pin 8
( ) = Pin Numbers

STATE DIAGRAM, 'F193



$\overline{TC}_U = Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3 \bullet \overline{CP}_U$
$\overline{TC}_D = Q_0 \bullet Q_1 \bullet \overline{CP}_2 \bullet \overline{Q}_3 \bullet \overline{CP}_D$

Logic Equations for Terminal Count

MODE SELECT — FUNCTION TABLE, 'F193

OPERATING MODE	INPUTS								OUTPUTS					
	MR	$\overline{PL}$	CP_U	CP_D	D_0	D_1	D_2	D_3	Q_0	Q_1	Q_2	Q_3	$\overline{TC}_U$	$\overline{TC}_D$
Reset (clear)	H	X	X	L	X	X	X	X	L	L	L	L	H	L
	H	X	X	H	X	X	X	X	L	L	L	L	H	H
Parallel load	L	L	X	L	L	L	L	L	L	L	L	L	H	L
	L	L	X	H	L	L	L	L	L	L	L	L	H	H
	L	L	L	X	H	H	H	H	H	H	H	L	H	H
	L	L	H	X	H	H	H	H	H	H	H	H	H	H
Count up	L	H	↑	H	X	X	X	X	Count up				H(1)	H
Count down	L	H	H	↑	X	X	X	X	Count down				H	H(2)

H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-to-High clock transition

NOTES:

1. $TC_U = CP_U$ at terminal count up (HHHH).
2. $TC_D = CP_D$ at terminal count down (LLLL).

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		74F192, 'F193			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX V_{IH} = MIN,	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OL} = MAX V_{IH} = MIN,	±10%V_{CC}		0.35	0.5	V
				±5%V_{CC}		0.35	0.5	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	Low-level input current	CP_U, CP_D	V_{CC} = MAX, V_I = 0.5V				−1.8	mA
		Other inputs					−0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current[4] (total)		V_{CC} = MAX			32	50	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Measure I_{CC} with parallel load and Master Reset inputs grounded, all other inputs at 4.5V, and all outputs open.

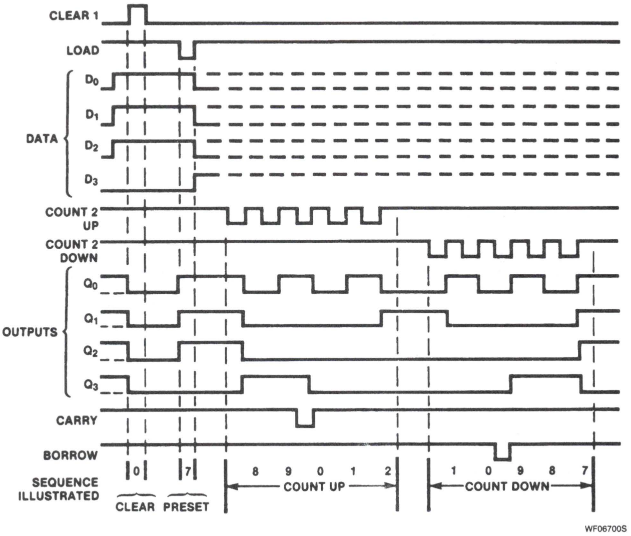
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F192, 'F193					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	100	125		90		MHz
t_{PLH} t_{PHL}	Propagation delay CP_U or CP_D to $\overline{TC}_U$ or $\overline{TC}_D$	Waveform 1, 2	2.5 3.0	5.5 5.0	8.5 8.0	2.5 3.0	9.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay CP_U or CP_D to Q_n	Waveform 1	2.5 5.0	5.5 8.5	8.5 12.0	2.5 5.0	9.0 13.0	ns
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	Waveform 4	2.0 6.0	4.0 9.5	7.0 13.5	1.5 6.0	8.0 15.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to Q_n	Waveform 3	4.5 5.5	6.5 8.5	10.0 12.0	4.0 5.0	11.0 13.0	ns
t_{PHL}	Propagation delay MR to Q_n	Waveform 5	5.0	7.5	11.0	5.0	12.0	ns
t_{PLH}	Propagation delay MR to $\overline{TC}_U$	Waveform 5	6.0	8.5	12.0	5.5	13.0	ns
t_{PHL}	Propagation delay MR to $\overline{TC}_D$	Waveform 5	5.0	7.5	11.0	5.0	12.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to $\overline{TC}_U$ or $\overline{TC}_D$	Waveform 3	6.0 6.0	9.5 9.0	13.5 12.0	6.0 6.0	15.0 13.0	ns
t_{PLH} t_{PHL}	Propagation delay D_n to $\overline{TC}_U$ or $\overline{TC}_D$	Waveform 4	5.5 4.5	9.0 8.5	13.0 12.5	5.0 4.5	14.0 13.5	ns

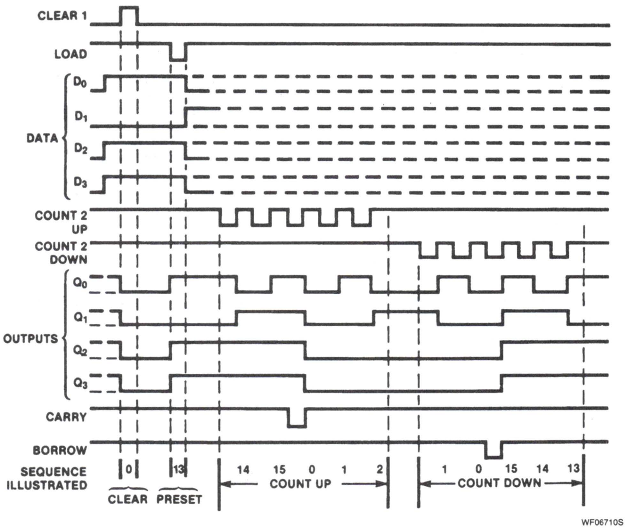
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	74F192, 'F193					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to $\overline{PL}$	Waveform 6	4.5 4.5			5.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to $\overline{PL}$	Waveform 6	2.0 2.0			2.0 2.0		ns
$t_w(L)$	$\overline{PL}$ pulse width Low	Waveform 3	6.0			6.0		ns
$t_w(H)$ $t_w(L)$	CP_U or CP_D pulse width High or Low	Waveform 1	3.5 5.0			3.5 5.0		ns
$t_w(L)$	CP_U or CP_D pulse width Low (change of direction)	Waveform 1	10.0			10.0		ns
$t_w(H)$	MR pulse width High	Waveform 5	6.0			6.0		ns
t_{rec}	Recovery time $\overline{PL}$ to CP_U or CP_D	Waveform 3	6.0			6.0		ns
t_{rec}	Recovery time MR to CP_U or CP_D	Waveform 5	4.0			4.0		ns

FUNCTIONAL WAVEFORMS (Typical clear, load, and count sequences)


CLEAR 1
LOAD
DATA
D0
D1
D2
D3
COUNT 2 UP
COUNT 2 DOWN
OUTPUTS
Q0
Q1
Q2
Q3
CARRY
BORROW
SEQUENCE ILLUSTRATED
0
7
CLEAR
PRESET
8 9 0 1 2
COUNT UP
1 0 9 8 7
COUNT DOWN
WF06700S

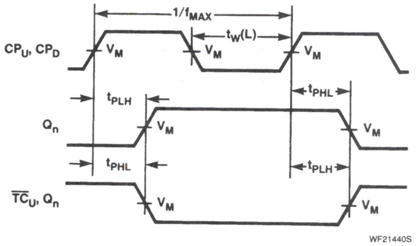
a. 'F192 Decade Counter


CLEAR 1
LOAD
DATA
D0
D1
D2
D3
COUNT 2 UP
COUNT 2 DOWN
OUTPUTS
Q0
Q1
Q2
Q3
CARRY
BORROW
SEQUENCE ILLUSTRATED
0
13
CLEAR
PRESET
14 15 0 1 2
COUNT UP
1 0 15 14 13
COUNT DOWN
WF06710S

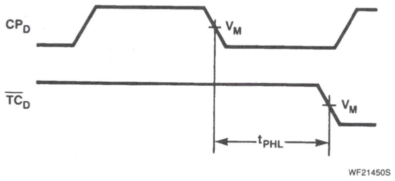
b. 'F193 Binary Counter

NOTES:
1. Clear overrides load data and count inputs.
2. When counting up, count-down input must be High; when counting down, count-up input must be High.

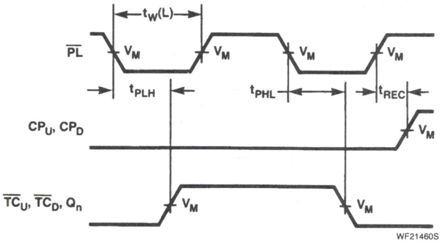
AC WAVEFORMS


$1/f_{MAX}$
$t_W(L)$
CP_U, CP_D
V_M
V_M
V_M
t_{PLH}
t_{PHL}
Q_n
V_M
V_M
t_{PHL}
t_{PLH}
$\overline{TC}_U$, Q_n
V_M
V_M
WF21440S

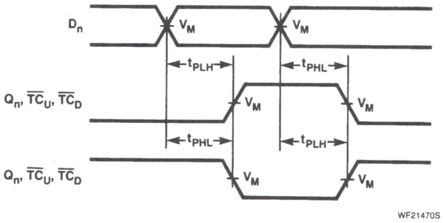
Waveform 1. Propagation Delay, Clock Input to Output, Clock Width and Maximum Clock Frequency


CP_D
V_M
$\overline{TC}_D$
V_M
t_{PHL}
WF21450S

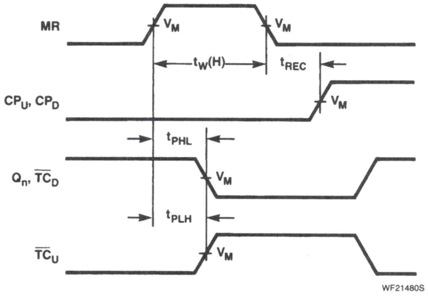
Waveform 2. Propagation Delay, Clock Pulse Down to Terminal Count


$t_W(L)$
$\overline{PL}$
V_M
V_M
V_M
V_M
t_{PLH}
t_{PHL}
t_{REC}
CP_U, CP_D
V_M
$\overline{TC}_U$, $\overline{TC}_D$, Q_n
V_M
V_M
WF21460S

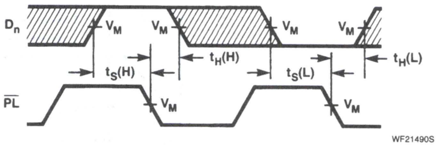
Waveform 3. Parallel Load Pulse Width, Parallel Load to Output Delays, and Parallel Load to Clock Recovery Time


D_n
V_M
V_M
t_{PLH}
t_{PHL}
Q_n, $\overline{TC}_U$, $\overline{TC}_D$
V_M
V_M
t_{PHL}
t_{PLH}
Q_n, $\overline{TC}_U$, $\overline{TC}_D$
V_M
V_M
WF21470S

Waveform 4. Propagation Delay, Data to Flip-Flop Outputs, Terminal Count Up and Down Outputs


MR
V_M
V_M
$t_W(H)$
t_{REC}
CP_U, CP_D
V_M
t_{PHL}
Q_n, $\overline{TC}_D$
V_M
t_{PLH}
$\overline{TC}_U$
V_M
WF21480S

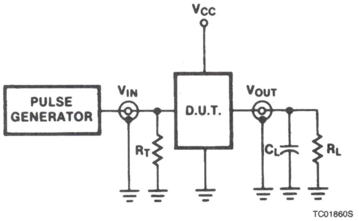
Waveform 5. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery


D_n
V_M
V_M
V_M
V_M
$t_S(H)$
$t_H(H)$
$t_S(L)$
$t_H(L)$
$\overline{PL}$
V_M
V_M
WF21490S

Waveform 6. Setup Time and Hold Time for D_n to $\overline{PL}$

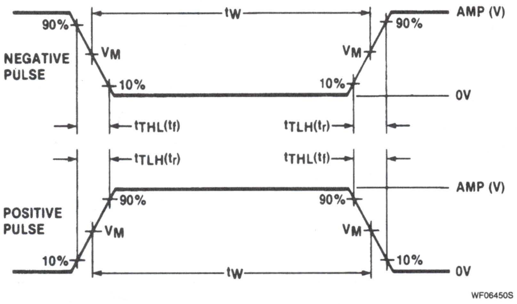
NOTE: $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORMS


VCC
PULSE GENERATOR
VIN
RT
D.U.T.
VOUT
CL
RL
TC01860S

Test Circuit for Totem-Pole Outputs

DEFINITIONS
R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.


tW
AMP (V)
90%
90%
NEGATIVE PULSE
VM
VM
10%
10%
0V
tTHL(tf)
tTLH(tr)
tTLH(tr)
tTHL(tf)
AMP (V)
POSITIVE PULSE
90%
90%
VM
VM
10%
10%
tW
0V
WF06450S

V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F194
Shift Register

4-Bit Bidirectional Universal Shift Register
Product Specification

FAST Products

FEATURES

- Shift left and shift right capability
- Synchronous Parallel and Serial data transfers
- Easily expanded for both Serial and Parallel operation
- Asynchronous Master Reset
- Hold (do nothing) mode

DESCRIPTION

The functional characteristics of the 'F194 4-Bit Bidirectional Shift Register are indicated in the Logic Diagram and Function Table. The register is fully synchronous, with all operations taking place in less than 9ns (typical) for 74F, making the device especially useful for implementing very high-speed CPUs, or for memory buffer registers.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F194	150MHz	33mA

ORDERING INFORMATION

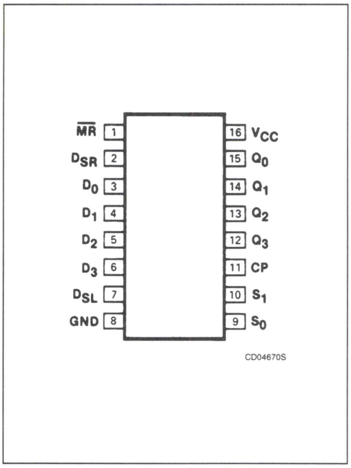
PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
16-Pin Plastic DIP	N74F194N
16-Pin Plastic SO	N74F194D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

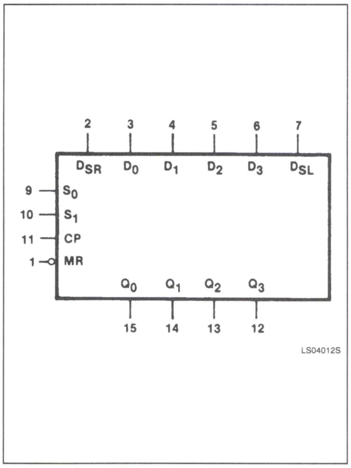
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$D_0 - D_3$	Parallel data inputs	1.0/1.0	20µA/0.6mA
S_0, S_1	Mode control inputs	1.0/1.0	20µA/0.6mA
D_{SR}	Serial data input (shift right)	1.0/1.0	20µA/0.6mA
D_{SL}	Serial data input (shift left)	1.0/1.0	20µA/0.6mA
C_P	Clock pulse input (active rising edge)	1.0/1.0	20µA/0.6mA
$\overline{MR}$	Asynchronous Master Reset (active-Low)	1.0/1.0	20µA/0.6mA
$Q_0 - Q_3$	Parallel outputs	50/33	1.0mA/20mA

NOTE:
1. One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

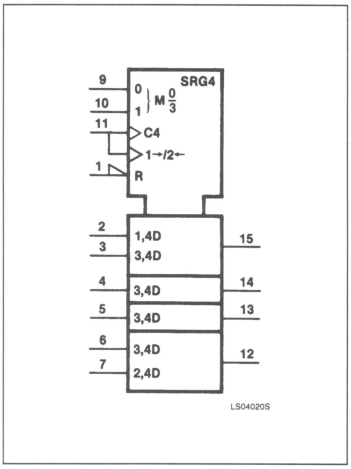
PIN CONFIGURATION


$\overline{MR}$ 1
D_{SR} 2
D_0 3
D_1 4
D_2 5
D_3 6
D_{SL} 7
GND 8
16 V_{CC}
15 Q_0
14 Q_1
13 Q_2
12 Q_3
11 CP
10 S_1
9 S_0
CD04670S

LOGIC SYMBOL


2 3 4 5 6 7
D_{SR} D_0 D_1 D_2 D_3 D_{SL}
9 S_0
10 S_1
11 CP
1 MR
Q_0 Q_1 Q_2 Q_3
15 14 13 12
LS04012S

LOGIC SYMBOL (IEEE/IEC)


SRG4
9
10
11
1
0
1
M 0/3
C4
1→/2←
R
2
3
1,4D
3,4D
15
4
3,4D
14
5
3,4D
13
6
7
3,4D
2,4D
12
LS04020S

Shift Register

FAST 74F194

The 'F194 design has special logic features which increase the range of application. The synchronous operation of the device is determined by two Mode Select inputs, S_0 and S_1. As shown in the Mode Select Table, data can be entered and shifted from left to right (shift right, $Q_0 \rightarrow Q_1$, etc.), or right to left (shift left, $Q_3 \rightarrow Q_2$, etc.), or parallel data can be entered, loading all 4 bits of the register simultaneously. When both S_0 and S_1 are Low, existing data is retained in a hold (do nothing) mode. The first and last stages provide D-type Serial Data inputs (D_{SR}, D_{SL}) to allow multistage shift right or shift left data transfers without interfering with parallel load operation.

Mode Select and Data inputs on the 'F194 are edge-triggered, responding only to the Low-to-High transition of the Clock (CP). Therefore, the only timing restriction is that the Mode Control and selected Data inputs must be stable one setup time prior to the positive transition of the clock pulse. Signals on the Select, Parallel Data ($D_0 - D_3$) and Serial Data (D_{SR}, D_{SL}) inputs can change when the clock is in either state, provided only the recommended setup and hold times, with respect to the clock rising edge, are observed.

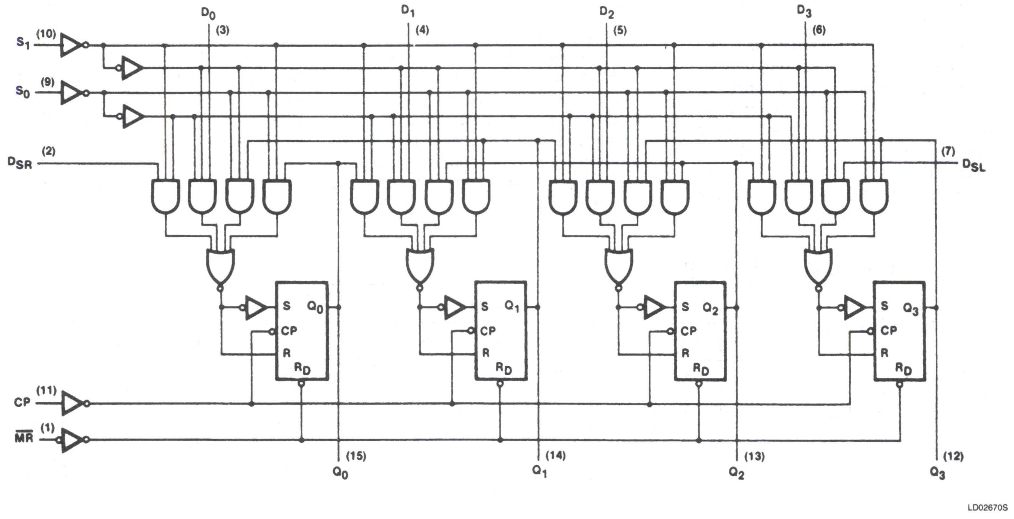
The four Parallel Data inputs ($D_0 - D_3$) are D-type inputs. Data appearing on $D_0 - D_3$ inputs when S_0 and S_1 are High is transferred to the $Q_0 - Q_3$ outputs respectively, following the next Low-to-High transition of the clock. When Low, the asynchronous Master Reset ($\overline{MR}$) overrides all other input conditions and forces the Q outputs Low.

MODE SELECT — FUNCTION TABLE

OPERATING MODE	INPUTS							OUTPUTS			
	CP	$\overline{MR}$	S_1	S_0	D_{SR}	D_{SL}	D_n	Q_0	Q_1	Q_2	Q_3
Reset (clear)	X	L	X	X	X	X	X	L	L	L	L
Hold (do nothing)	X	H	l	l	X	X	X	q_0	q_1	q_2	q_3
Shift left	↑ ↑	H H	h h	l l	X X	l h	X X	q_1 q_1	q_2 q_2	q_3 q_3	L H
Shift right	↑ ↑	H H	l l	h h	l h	X X	X X	L H	q_0 q_0	q_1 q_1	q_2 q_2
Parallel load	↑	H	h	h	X	X	d_n	d_0	d_1	d_2	d_3

H = High voltage level.
h = High voltage level one setup time prior to the Low-to-High clock transition.
L = Low voltage level.
l = Low voltage level one setup time prior to the Low-to-High clock transition.
$d_n(q_n)$ = Lower case letters indicate the state of the referenced input (or output) one setup time prior to the Low-to-High clock transition.
X = Don't care.
↑ = Low-to-High clock transition.

LOGIC DIAGRAM


D0
(3)
D1
(4)
D2
(5)
D3
(6)
S1 (10)
S0 (9)
DSR (2)
(7) DSL
S Q0
CP
R
RD
S Q1
CP
R
RD
S Q2
CP
R
RD
S Q3
CP
R
RD
CP (11)
MR (1)
(15) Q0
(14) Q1
(13) Q2
(12) Q3
LD02670S

V_{CC} = Pin 16
GND = Pin 8

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	–0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			–18	mA
I_{OH}	High-level output current			–1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS[1]		74F194			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage[3]	V_{CC} = MIN, V_{IL} = MAX, V_{OH} = MAX V_{IH} = MIN	±10%V_{CC}	2.5			V
			±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OL} = MAX	±10%V_{CC}		0.35	0.5	V
			±5%V_{CC}		0.35	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, $I_I = I_{IK}$			−0.73	−1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V				−0.6	mA
I_{OS}	Short-circuit output current[4]	V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current[5] (total)	V_{CC} = MAX			33	46	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Output High state will change to Low state if an external voltage of less than 0.0V is applied.
4. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
5. With all outputs open, D_I inputs grounded and 4.5V applied to S_0, S_1, MR and the serial inputs, I_{CC} is tested with a momentary ground, then 4.5V applied to CP.

Shift Register FAST 74F194

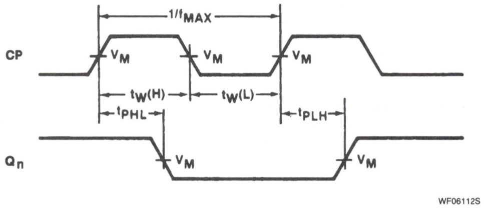
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F194					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	105	150		90		MHz
t_{PLH}	Propagation delay CP to Q_n	Waveform 1	3.5	5.2	7.0	3.5	8.0	ns
t_{PHL}			3.5	5.5	7.0	3.5	8.0	
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	Waveform 2	4.5	8.6	12	4.5	14	ns

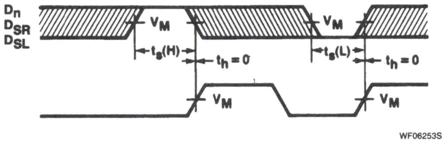
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	74F194					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_w(H)$	Clock pulse width, High	Waveform 1	5.0			5.5		ns
$t_w(L)$	MR pulse width, Low	Waveform 3	5.0			5.0		ns
$t_s(H)$	Setup time, $D_0 - D_3$, D_{SR}, D_{SL} to CP	Waveform 2	4.0			4.0		ns
$t_s(L)$			4.0			4.0		
$t_h(H)$	Hold time, High or Low, $D_0 - D_3$, DSR, DSL to CP		0			1.0		ns
$t_h(L)$			0			1.0		
$t_s(H)$	Setup time, High or Low, S_n to CP	Waveform 4	8.0			9.0		ns
$t_s(L)$			8.0			8.0		
$t_h(H)$	Hold time, High or Low, S_n to CP		0			0		ns
$t_h(L)$			0			0		
t_{rec}	Recovery time, $\overline{MR}$ to CP	Waveform 3	7.0			8.0		ns

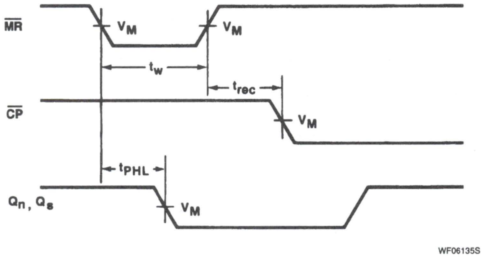
AC WAVEFORMS


1/fMAX
CP
VM
VM
VM
tW(H)
tW(L)
tPHL
tPLH
Qn
VM
VM
WF06112S

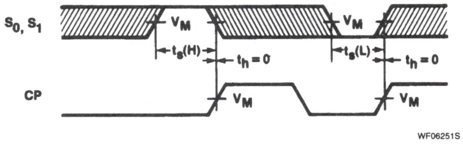
Waveform 1. Clock to Output Delays and Clock Pulse Width


Dn
DSR
DSL
VM
VM
ts(H)
th = 0
ts(L)
th = 0
VM
VM
WF06253S

Waveform 2. Data Setup and Hold Times


MR
VM
VM
tw
trec
CP
VM
tPHL
Qn, Qs
VM
WF06135S

Waveform 3. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time

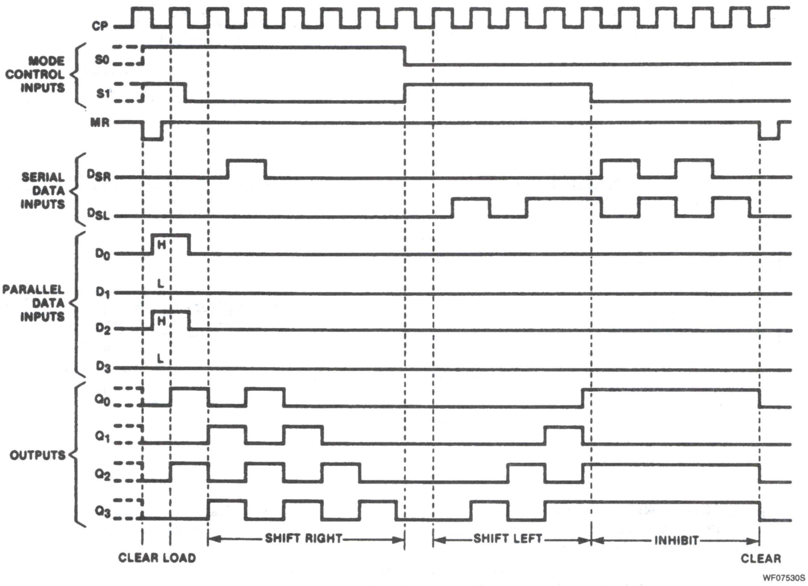

S0, S1
VM
VM
ts(H)
th = 0
ts(L)
th = 0
CP
VM
VM
WF06251S

Waveform 4. Setup and Hold Times for S_0 and S_1 Inputs

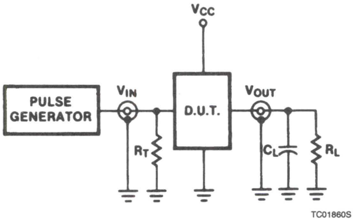
NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change predictable output performance.

TIMING DIAGRAM

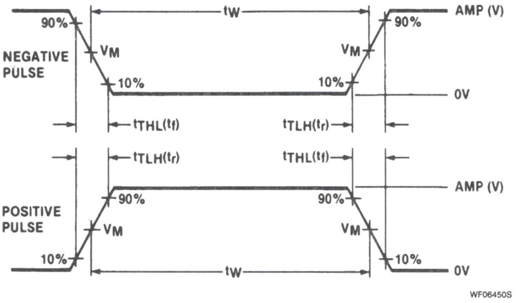
(Typical Clear, Load, Right-Shift, Left-Shift, Inhibit and Clear Sequences)


CP
MODE CONTROL INPUTS
S0
S1
MR
SERIAL DATA INPUTS
DSR
DSL
PARALLEL DATA INPUTS
D0
H
D1
L
D2
H
D3
L
OUTPUTS
Q0
Q1
Q2
Q3
SHIFT RIGHT
SHIFT LEFT
INHIBIT
CLEAR LOAD
CLEAR
WF07530S

TEST CIRCUIT AND WAVEFORMS


VCC
PULSE GENERATOR
VIN
D.U.T.
VOUT
RT
CL
RL
TC01860S

Test Circuit for Totem-Pole Outputs


tW
AMP (V)
90%
90%
NEGATIVE PULSE
VM
VM
10%
10%
0V
tTHL(tf)
tTLH(tr)
tTLH(tr)
tTHL(tf)
AMP (V)
90%
90%
POSITIVE PULSE
VM
VM
10%
10%
0V
tW
WF06450S

$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS

R_L = Load resistor to GND; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_r	t_f
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F195
Shift Register

4-Bit Parallel Access Shift Register
Product Specification

FAST Products

FEATURES

- **High-impedance NPN base inputs for reduced loading (20μA in Low and High states)**
- **Shift right and parallel load capability**
- **J – $\overline{K}$ (D) inputs to first stage**
- **Complement output from last stage**
- **Asynchronous Master Reset**

DESCRIPTION

The functional characteristics of the 'F195 4-Bit Parallel Access Shift Register are indicated in the Logic Diagram and Function Table. The device is useful in a wide variety of shifting, counting and storage applications. It performs serial, parallel, serial-to-parallel, or parallel-to-serial data transfers at very high speeds.

The 'F195 operates on two primary modes: shift right ($Q_0 - Q_1$) and parallel load, which are controlled by the state of the Parallel Enable ($\overline{PE}$) input. Serial data enters the first flip-flop (Q_0) via the J and $\overline{K}$ inputs when the $\overline{PE}$ input is High, and is shifted 1 bit in the direction $Q_0 \rightarrow Q_1 \rightarrow Q_2 \rightarrow Q_3$ following each Low-to-High clock transition.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F195	115MHz	45mA

ORDERING INFORMATION

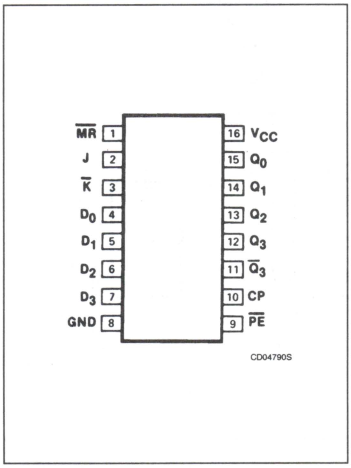
PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
16-Pin Plastic DIP	N74F195N
16-Pin Plastic SO	N74F195D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
CP	Clock Pulse input (active rising edge)	1.0/0.033	20μA/20μA
$D_0 - D_3$	Parallel data inputs	1.0/0.033	20μA/20μA
$\overline{PE}$	Parallel Enable input	1.0/0.033	20μA/20μA
$\overline{MR}$	Asynchronous Master Reset	2.0/0.066	40μA/40μA
J, $\overline{K}$	J – $\overline{K}$ or D type serial inputs	1.0/0.033	20μA/20μA
$Q_0 - Q_3$, $\overline{Q}_3$	Outputs	50/33	1.0mA/20mA

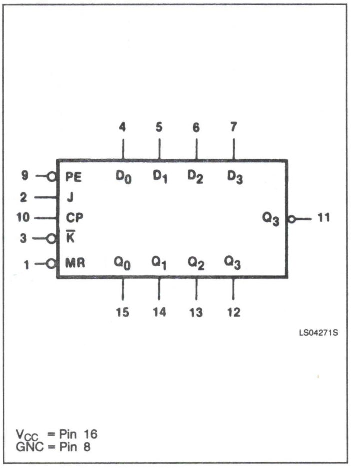
NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



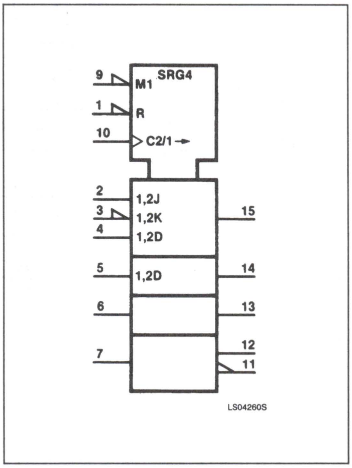
$\overline{MR}$ 1
J 2
$\overline{K}$ 3
D_0 4
D_1 5
D_2 6
D_3 7
GND 8
16 V_{CC}
15 Q_0
14 Q_1
13 Q_2
12 Q_3
11 $\overline{Q}_3$
10 CP
9 $\overline{PE}$
CD04790S

LOGIC SYMBOL



4 5 6 7
9 PE
2 J
10 CP
3 K
1 MR
D_0 D_1 D_2 D_3
Q_0 Q_1 Q_2 Q_3
$\overline{Q}_3$ 11
15 14 13 12
LS04271S
V_{CC} = Pin 16
GNC = Pin 8

LOGIC SYMBOL (IEEE/IEC)



SRG4
9 M1
1 R
10 C2/1→
2 1,2J
3 1,2K
4 1,2D
5 1,2D
6
7
15
14
13
12
11
LS04260S

Shift Register　FAST 74F195

The J and $\overline{K}$ inputs provide the flexibility of the JK type input for special applications and by tying the two pins together, the simple D type input for general applications. The device appears as four common clocked D flip-flops when the $\overline{PE}$ input is Low. After the Low-to-High clock transition, data on the parallel inputs ($D_0 - D_3$) is transferred to the respective $Q_0 - Q_3$ outputs. Shift left operation ($Q_3 - Q_2$) can be achieved by tying the Q_n outputs to the D_{n-1} inputs and holding the $\overline{PE}$ input low.

All parallel and serial data transfers are synchronous, occuring after each Low-to-High clock transition. The 'F195 utilizes edge-triggering, therefore, there is no restriction on the activity of the J, $\overline{K}$, D_n, and $\overline{PE}$ inputs for logic operation, other than the setup and release time requirements.

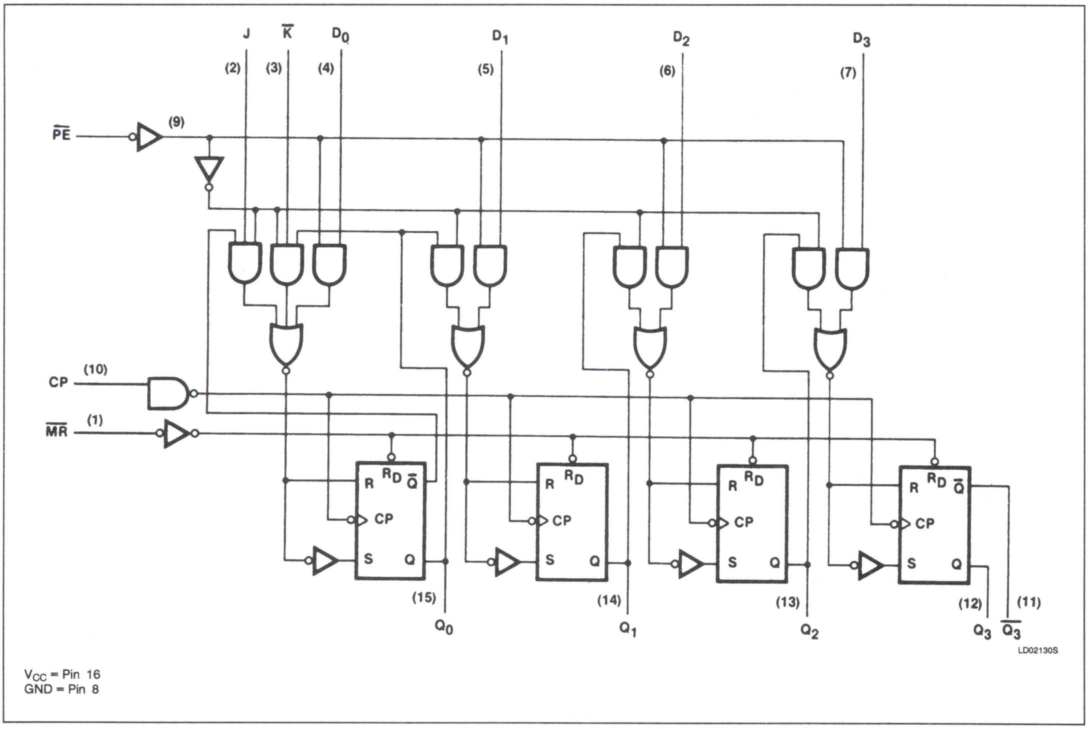
A Low on the asynchronous Master Reset ($\overline{MR}$) input sets all Q outputs Low, independent of any other input condition.

MODE SELECT – FUNCTION TABLE

OPERATING MODES	INPUTS						OUTPUTS				
	$\overline{MR}$	CP	$\overline{PE}$	J	$\overline{K}$	D_n	Q_0	Q_1	Q_2	Q_3	$\overline{Q_3}$
Asynchronous reset	L	X	X	X	X	X	L	L	L	L	H
Shift, set first stage	H	↑	h	h	h	X	H	q_0	q_1	q_2	$\overline{q_2}$
Shift, reset first stage	H	↑	h	l	l	X	L	q_0	q_1	q_2	$\overline{q_2}$
Shift, toggle first stage	H	↑	h	h	l	X	$\overline{q_0}$	q_0	q_1	q_2	$\overline{q_2}$
Shift, retain first stage	H	↑	h	l	h	X	q_0	q_0	q_1	q_2	$\overline{q_2}$
Parallel load	H	↑	l	X	X	d_n	d_0	d_1	d_2	d_3	$\overline{d_3}$

H = High voltage level
L = Low voltage level
X = Don't care
l = Low voltage level one setup time prior to the Low-to-High clock transition
h = High voltage level one setup time prior to the Low-to-High clock transition
d_n (q_n) = Lower case letters indicate the state of the referenced input (or output) one setup time prior to the Low-to-High clock transition
↑ = Low-to-High clock transition

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8

Shift Register FAST 74F195

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX, V_{IH} = MIN	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OL} = MAX, V_{IH} = MIN	±10%V_{CC}		0.35	0.5	V
				±5%V_{CC}		0.35	0.5	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	High-level input current	Others	V_{CC} = MAX, V_I = 2.7V				20	μA
		$\overline{MR}$					40	μA
I_{IL}	Low-level input current	Others	V_{CC} = MAX, V_I = 0.5V				−20	μA
		$\overline{MR}$					−40	μA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current[4] (total)		V_{CC} = MAX			45	58	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. With all outputs open, $\overline{PE}$ grounded, and 4.5V applied to the J, $\overline{K}$, and Data inputs, I_{CC} is measured by applying a momentary ground, followed by 4.5V to $\overline{MR}$, and then a momentary ground followed by 4.5V to clock.

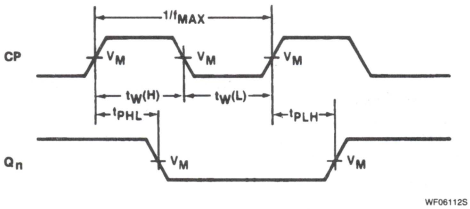
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	74F195					UNIT
				$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0$ to $70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
				Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	$\overline{PE}$ mode	Waveform 1	120	130		110		MHz
		Toggle mode		100	115		90		
t_{PLH} t_{PHL}	Propagation delay CP to Q_n		Waveform 1	4.0 4.0	6.5 6.5	9.5 9.0	4.0 4.0	10.0 8.5	ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{Q}_3$		Waveform 1	7.0 4.5	10.0 7.0	13.0 9.0	7.0 4.0	13.5 9.5	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n		Waveform 2	5.0	7.5	10.5	5.0	11.0	ns
t_{PLH}	Propagation delay $\overline{MR}$ to $\overline{Q}_3$		Waveform 2	7.0	10.0	13.5	7.0	14.0	ns

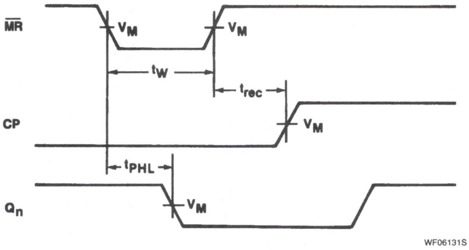
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	74F195					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0$ to $70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low J, $\overline{K}$ and D_n to CP	Waveform 3	4 4			4 4		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low J, $\overline{K}$ and D_n to CP	Waveform 3	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{PE}$ to CP	Waveform 4	3 4			3 5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{PE}$ to CP	Waveform 4	0 0			0 0		ns
$t_w(H)$	CP pulse width, High	Waveform 1	6			6		ns
$t_w(L)$	$\overline{MR}$ pulse width, Low	Waveform 2	5			5		ns
t_{rec}	Recovery time $\overline{MR}$ to CP	Waveform 2	6			6		ns

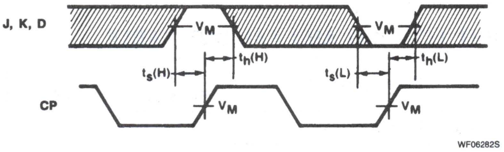
AC WAVEFORMS


CP
Qn
1/fMAX
VM
tW(H)
tW(L)
tPHL
tPLH
WF06112S

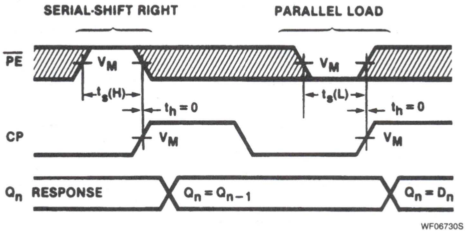
Waveform 1. Clock to Output Delays and Clock Pulse Width


MR
CP
Qn
VM
tW
trec
tPHL
WF06131S

Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay & Master Reset to Clock Recovery Time


J, K, D
CP
VM
ts(H)
th(H)
ts(L)
th(L)
WF06282S

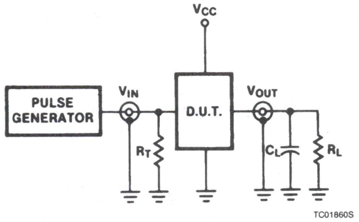
Waveform 3. Data Setup and Hold Times


SERIAL-SHIFT RIGHT
PARALLEL LOAD
PE
CP
Qn RESPONSE
VM
ts(H)
th = 0
ts(L)
th = 0
Qn = Qn−1
Qn = Dn
WF06730S

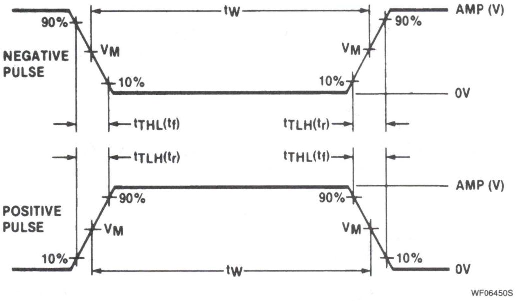
Waveform 4. Setup and Hold Times Parallel Enable to Clock

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORM


VCC
PULSE GENERATOR
VIN
D.U.T.
VOUT
RT
CL
RL
TC01860S

Test Circuit for Totem-Pole Outputs


NEGATIVE PULSE
POSITIVE PULSE
tW
90%
10%
VM
AMP (V)
0V
tTHL(tf)
tTLH(tr)
WF06450S

$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS
R_L = Load resistor to GND; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F198

Shift Register

8-Bit Bidirectional Universal Shift Register
Preliminary Specification

FAST Products

DESCRIPTION

The 'F198 bidirectional register is designed to incorporate virtually all of the features a system designer may want in a shift register. This circuit contains 87 equivalent gates and features parallel inputs, parallel outputs, right-shift and left-shift serial inputs, operating mode control inputs, and a direct overriding clear line. The register has four distinct modes of operation:

- Parallel (broadside) Load
- Shift Right (in the direction Q_A toward Q_H)
- Shift Left (in the direction Q_H toward Q_A)
- Inhibit Clock (do nothing)

Synchronous parallel loading is accomplished by applying the 8 bits of data and taking both mode control inputs, S_0 and S_1, High. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the Clock input. During loading, serial data flow is inhibited.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F198	110MHz	40mA

ORDERING INFORMATION

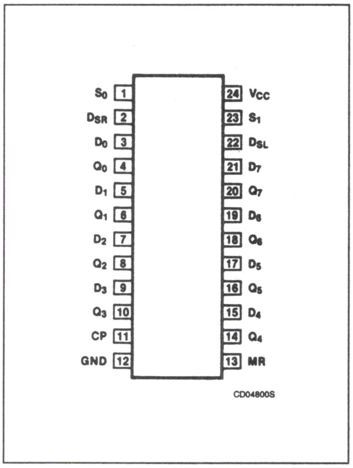
PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
24-Pin Plastic Slim DIP (300mil)	N74F198N
24-Pin Plastic SOL	N74F198D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

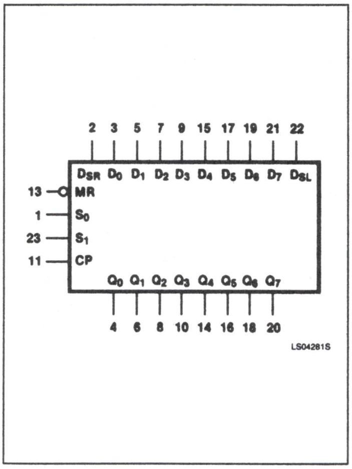
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$D_0 - D_7$	Parallel data inputs	1.0/1.0	20μA/0.6mA
$S_0 - S_1$	Mode control inputs	1.0/1.0	20μA/0.6mA
D_{SR}	Serial data input (shift right)	1.0/1.0	20μA/0.6mA
D_{SL}	Serial data input (shift left)	1.0/1.0	20μA/0.6mA
CP	Clock Pulse input (active rising edge)	1.0/1.0	20μA/0.6mA
$\overline{MR}$	Asynchronous Master Reset (active-Low)	1.0/1.0	20μA/0.6mA
$Q_0 - Q_7$	Parallel outputs	50/33	1.0mA/20mA

NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

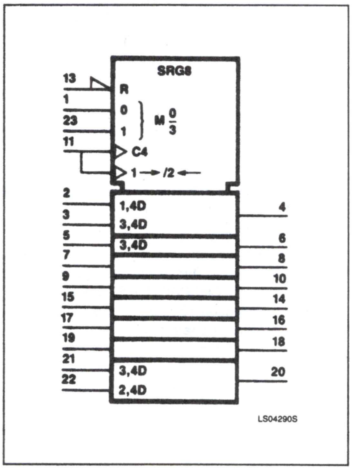
PIN CONFIGURATION


S0 1
DSR 2
D0 3
Q0 4
D1 5
Q1 6
D2 7
Q2 8
D3 9
Q3 10
CP 11
GND 12
24 VCC
23 S1
22 DSL
21 D7
20 Q7
19 D6
18 Q6
17 D5
16 Q5
15 D4
14 Q4
13 MR
CD04800S

LOGIC SYMBOL


2 3 5 7 9 15 17 19 21 22
DSR D0 D1 D2 D3 D4 D5 D6 D7 DSL
13 MR
1 S0
23 S1
11 CP
Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
4 6 8 10 14 16 18 20
LS04281S

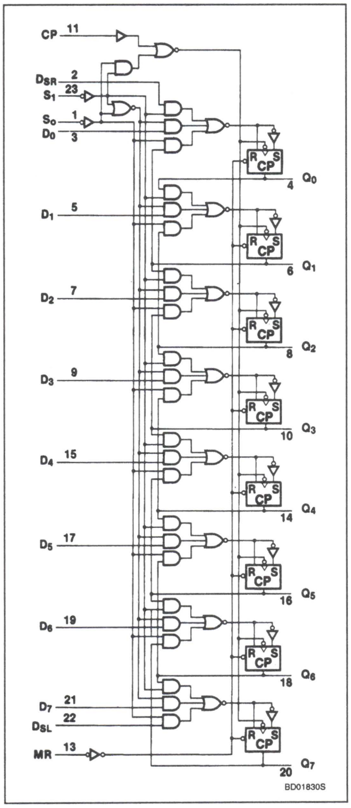
LOGIC SYMBOL (IEEE/IEC)


SRG8
13
R
1
0
23
1
M 0/3
11
C4
1→/2←
2
1,4D
3
3,4D
5
3,4D
7
9
15
17
19
21
3,4D
22
2,4D
4
6
8
10
14
16
18
20
LS04290S

Shift right is accomplished synchronously with the rising edge of the clock pulse when S_0 is High and S_1 is Low. Serial data for this mode is entered at the shift-right data input. When S_0 is Low and S_1 is High, data shifts left synchronously and new data is entered at the shift-left serial input.

Clocking of the flip-flop is inhibited when both mode control inputs are Low. The mode controls should be changed only while the Clock input is High.

BLOCK DIAGRAM



FUNCTION TABLE

INPUTS							OUTPUTS				
$\overline{MR}$	Mode		CP	Serial		Parallel	Q_A	Q_B	...	Q_G	Q_H
	S_1	S_0		Left	Right	A...H					
L	X	X	X	X	X	X	L	L		L	L
H	X	X	L	X	X	X	Q_{A0}	Q_{B0}		Q_{G0}	Q_{H0}
H	H	H	↑	X	X	a...h	a	b		g	h
H	L	H	↑	X	H	X	H	Q_{An}		Q_{Fn}	Q_{Gn}
H	L	H	↑	X	L	X	L	Q_{An}		Q_{Fn}	Q_{Gn}
H	H	L	↑	H	X	X	Q_{Bn}	Q_{Cn}		Q_{Hn}	H
H	H	L	↑	L	X	X	Q_{Bn}	Q_{Cn}		Q_{Hn}	L
H	L	L	X	X	X	X	Q_{A0}	Q_{B0}		Q_{G0}	Q_{H0}

H = High level (steady state)
L = Low level (steady state)
X = Irrelevant (any input, including transition)
↑ = Transition from Low-to-High level
a...h = The level of steady-state input at inputs A through H, respectively.
Q_{A0}, Q_{B0}, Q_{G0}, Q_{H0} = The level of Q_A, Q_B, Q_G or Q_H, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Bn}, etc. = The level of Q_A, Q_B, etc., respectively, before the most recent ↑ transition of the clock.

ABSOLUTE MAXIMUM RATINGS

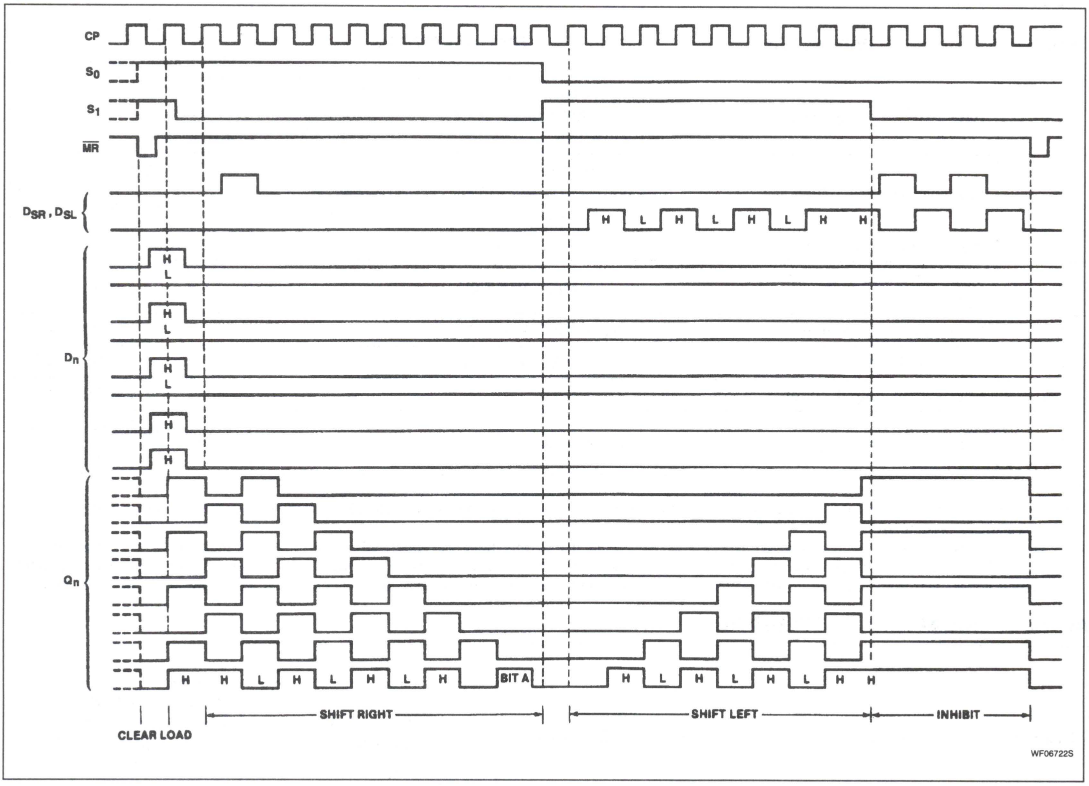
(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature range	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

TIMING DIAGRAM


CP
S0
S1
MR
DSR, DSL
H L H L H L H H
Dn
H
L
H
L
H
L
H
H
Qn
H H L H L H L H BIT A
H L H L H L H H
SHIFT RIGHT
SHIFT LEFT
INHIBIT
CLEAR LOAD
WF06722S

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		74F198			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX V_{IH} = MIN,	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OL} = MAX V_{IH} = MIN,	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				−0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			40	95	mA
		I_{CCL}				40	95	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

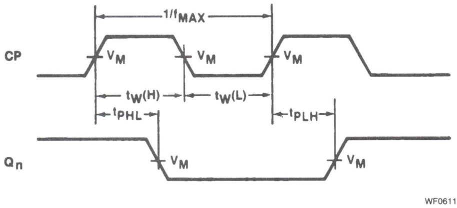
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F198					UNIT
			T_A = +25°C V_{CC} = +5.0V C_L = 50pF R_L = 500Ω			T_A = 0 to +70°C V_{CC} = +5.0V± 10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{max}	Maximum clock frequency	Waveform 1	90	110		80		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n or $\overline{Q}_n$	Waveform 1	3.5 3.5		7.0 7.0	3.5 3.5	8.0 8.0	ns
t_{PHL}	Propagation delay, MR to Q_n	Waveform 3	4.5		12	4.5	14	ns

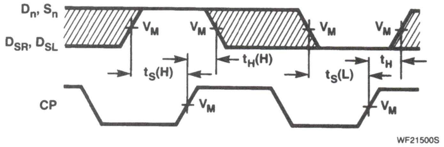
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	74F198					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_s(H) t_s(L)	Setup time, High or Low D_n to CP	Waveform 2	4.0 4.0			6.0 6.0		ns
t_h(H) t_h(L)	Hold time, High or Low, D_n to CP	Waveform 2	0 0			1.0 1.0		ns
t_s(H) t_s(L)	Setup time, High or Low D_{SR}, D_{SL} to CP	Waveform 2	4.0 4.0			6.0 6.0		ns
t_h(H) t_h(L)	Hold time, High or Low, D_{SR}, D_{SL} to CP	Waveform 2	0 0			1.0 1.0		ns
t_s(H) t_s(L)	Setup time, High or Low S_n to CP	Waveform 2	8.0 8.0			9.0 8.0		ns
t_h(H) t_h(L)	Hold time, High or Low S_n to CP	Waveform 2	0 0			0 0		ns
t_w(H)	CP pulse width	Waveform 1	6.0			6.0		ns
t_w(L)	$\overline{MR}$ pulse width	Waveform 3	5.0			5.0		ns
t_{rec}	Recovery time, $\overline{MR}$ to CP	Waveform 3	6.0			6.0		ns

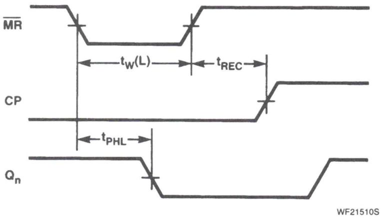
AC WAVEFORMS


1/fMAX
CP
VM
VM
VM
tW(H)
tW(L)
tPHL
tPLH
Qn
VM
VM
WF06112S

Waveform 1. Propagation Delay, Clock Input to Output, Clock Widths, and Maximum Clock Frequency


Dn, Sn
DSR, DSL
VM
VM
VM
VM
tS(H)
tH(H)
tS(L)
tH
CP
VM
VM
WF21500S

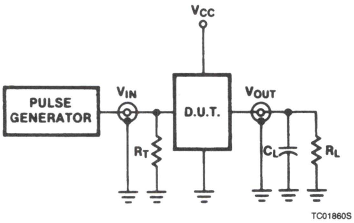
Waveform 2. Setup Time and Hold Time


MR
tW(L)
tREC
CP
tPHL
Qn
WF21510S

Waveform 3. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time

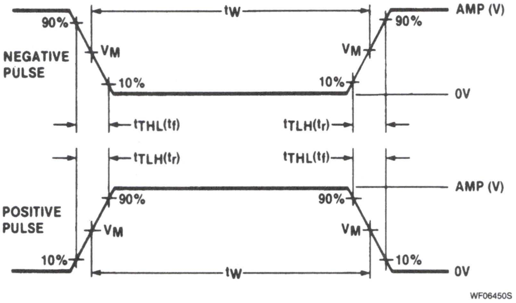
NOTE: $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS


VCC
PULSE GENERATOR
VIN
D.U.T.
VOUT
RT
CL
RL
TC01860S

Test Circuit for Totem-Pole Outputs

DEFINITIONS
R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.


NEGATIVE PULSE
90%
VM
10%
tW
AMP (V)
0V
tTHL(tf)
tTLH(tr)
POSITIVE PULSE
90%
VM
10%
tW
AMP (V)
0V
WF06450S

V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F199
Shift Register

8-Bit Parallel-Access Shift Register
Preliminary Specification

FAST Products

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F199	110MHz	40mA

FEATURES
- **Buffered clock and control inputs**
- **Shift right and parallel load capability**
- **Fully synchronous data transfers**
- **J – $\overline{K}$(D) Inputs to first stage**
- **Clock enable for hold (do nothing) mode**
- **Asynchronous Master Reset**

DESCRIPTION
The 'F199 is an 8-bit Parallel Access Shift Register and its functional characteristics are indicated in the Logic Diagram and Function Table. The device is useful in a variety of shifting, counting and storage applications. It performs serial, parallel, serial to parallel, or parallel to serial data transfers at very high speeds.

The 'F199 operates in two primary modes: shift right ($Q_0 \rightarrow Q_1$) and parallel load, which are controlled by the state of the Parallel Enable ($\overline{PE}$) input. Serial data enters the first flip-flop (Q_0) via the J and $\overline{K}$ inputs when the $\overline{PE}$ input is High, and is shifted one bit in the direction $Q_0 \rightarrow Q_1 \rightarrow Q_2$ following each Low-to-High clock transition.

ORDERING INFORMATION

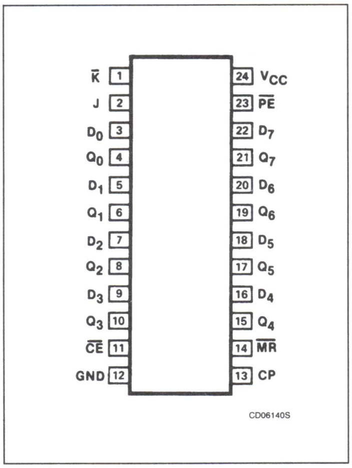
PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
24-Pin Plastic Slim DIP (300mil)	N74F199N
24-Pin Plastic SOL	N74F199D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

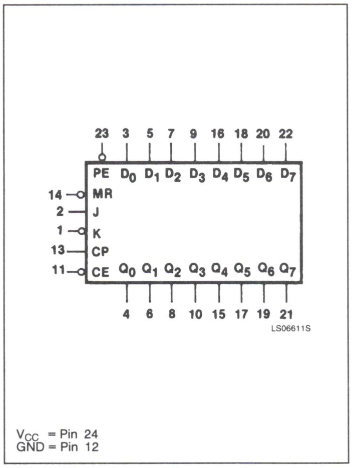
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$D_0 - D_7$	Parallel data inputs	1.0/1.0	20μA/0.6mA
J, $\overline{K}$	J and K inputs	1.0/1.0	20μA/0.6mA
$\overline{PE}$	Parallel Enable input	1.0/1.0	20μA/0.6mA
$\overline{CE}$	Clock Enable input	1.0/1.0	20μA/0.6mA
CP	Clock Pulse input (active rising edge)	1.0/1.0	20μA/0.6mA
$\overline{MR}$	Master Reset input (active-Low)	1.0/1.0	20μA/0.6mA
$Q_0 - Q_7$	Parallel outputs	50/33	1.0mA/20mA

NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION

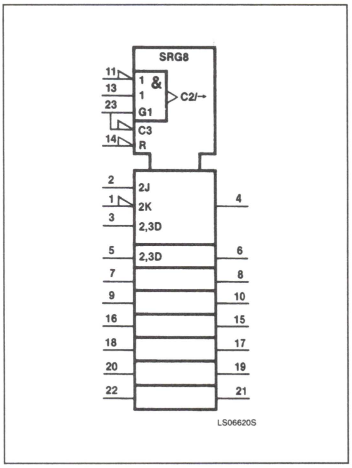

K̅ 1
J 2
D0 3
Q0 4
D1 5
Q1 6
D2 7
Q2 8
D3 9
Q3 10
C̅E̅ 11
GND 12
24 VCC
23 P̅E̅
22 D7
21 Q7
20 D6
19 Q6
18 D5
17 Q5
16 D4
15 Q4
14 M̅R̅
13 CP
CD06140S

LOGIC SYMBOL


23 3 5 7 9 16 18 20 22
PE D0 D1 D2 D3 D4 D5 D6 D7
14 MR
2 J
1 K
13 CP
11 CE
Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
4 6 8 10 15 17 19 21
LS06611S

V_{CC} = Pin 24
GND = Pin 12

LOGIC SYMBOL (IEEE/IEC)


SRG8
11
13
23
14
1 &
1
G1
C3
R
C2/→
2
1
3
2J
2K
2,3D
4
5
2,3D
6
7
8
9
10
16
15
18
17
20
19
22
21
LS06620S

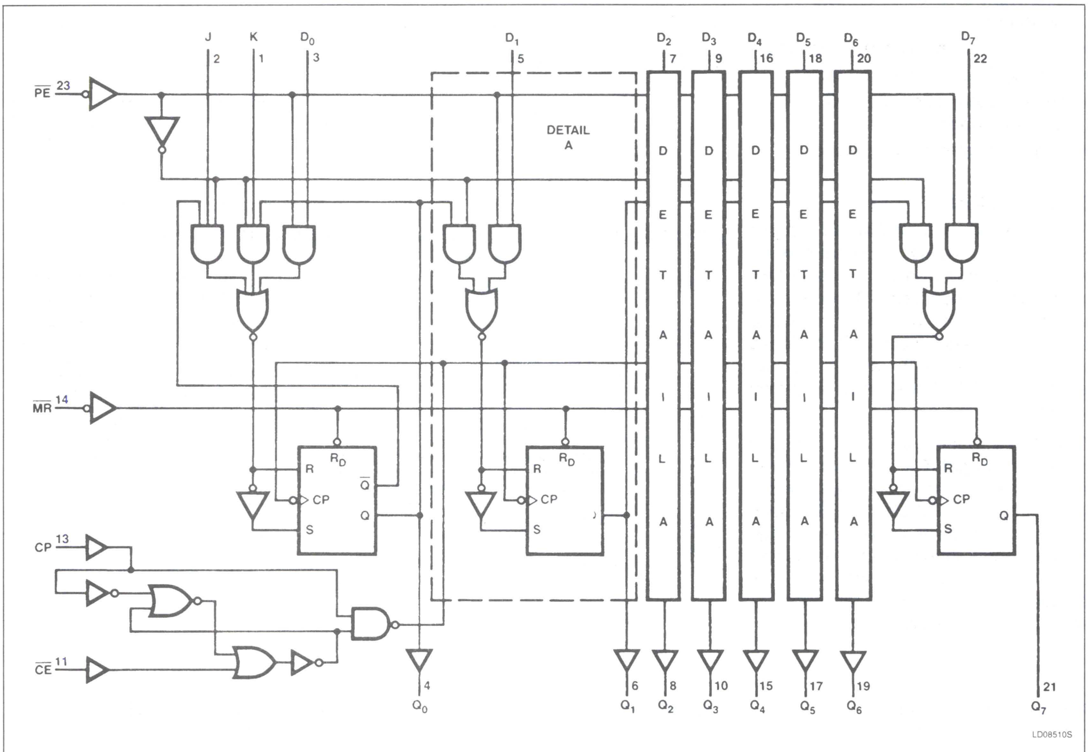
The J and $\overline{K}$ inputs provide the flexibility of the J – $\overline{K}$ type input for special applications and, by tying the two pins together, the simple D-type input for general applications.

The device appears as eight common clocked D flip-flops when the $\overline{PE}$ input is Low. After the Low-to-High clock transition, data on the parallel inputs ($D_0 - D_7$) is transferred to the respective $Q_0 - Q_7$ outputs.

All parallel and serial data transfers are synchronous, occurring after each Low-to-High clock transition. The 'F199 utilizes edge-triggered, therefore, there is no restriction on the activity of the J, $\overline{K}$, D_n, and $\overline{PE}$ inputs for logic operation, other than the setup and release time requirements.

A Low on the Master Reset ($\overline{MR}$) input overrides all other inputs and clears the register asynchronously forcing all bit positions to a Low state.

LOGIC DIAGRAM



J
2
K
1
D0
3
D1
5
D2
7
D3
9
D4
16
D5
18
D6
20
D7
22
PE 23
DETAIL A
D E T A I L A
MR 14
CP 13
CE 11
R
RD
CP
S
Q̄
Q
4
Q0
6
Q1
8
Q2
10
Q3
15
Q4
17
Q5
19
Q6
21
Q7
LD08510S

V_{CC} = Pin 24
GND= Pin 12
( ) = Pin Number

MODE SELECT—FUNCTION TABLE

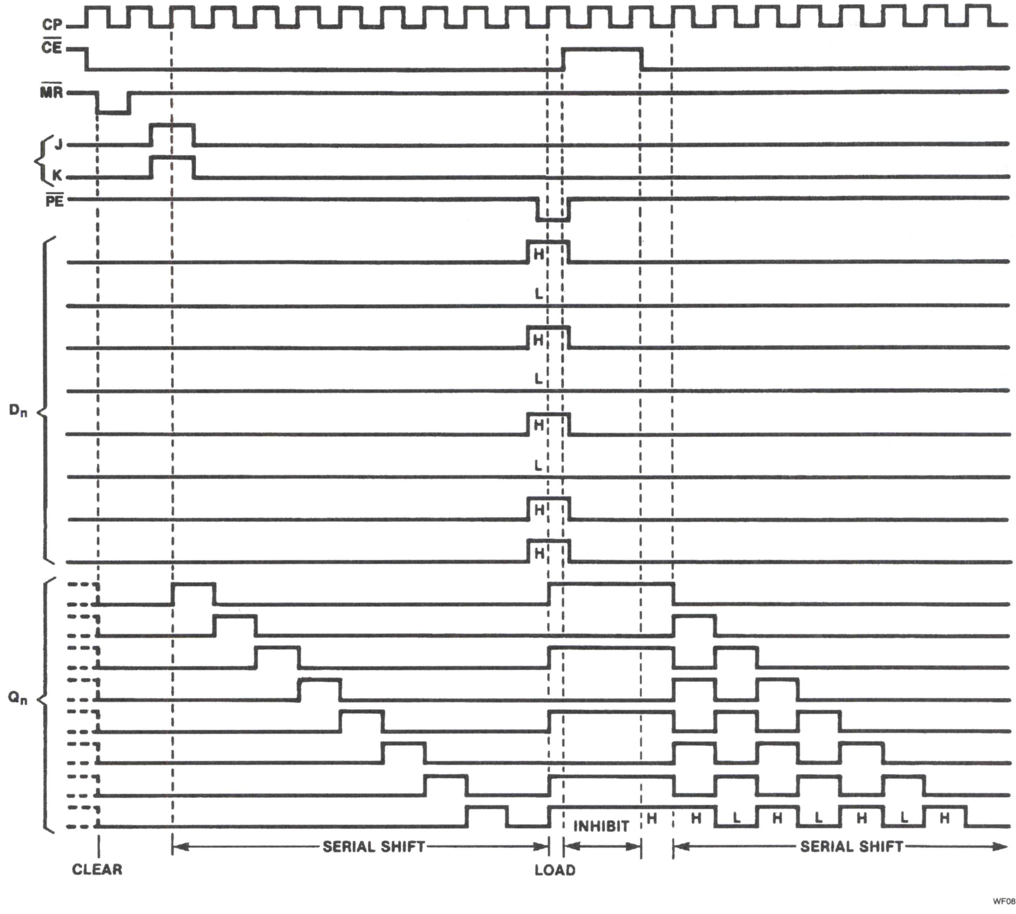
OPERATING MODES	INPUTS							OUTPUTS
	$\overline{MS}$	CP	$\overline{CE}$	$\overline{PE}$	J	$\overline{K}$	D_n	Q_0 Q_1 ... Q_6 Q_7
Reset (clear)	L	X	X	X	X	X	X	L L ... L L
Shift, Set First Stage	H	↑	l	h	h	h	X	H q_0 ... q_5 q_6
Shift, Reset First Stage	H	↑	l	h	l	l	X	L q_0 ... q_5 q_6
Shift, Toggle First Stage	H	↑	l	h	h	l	X	$\overline{q}_0$ q_0 ... q_5 q_6
Shift, Retain First Stage	H	↑	l	h	l	h	X	q_0 q_0 ... q_5 q_6
Parallel Load	H	↑	l	l	X	X	d_n	d_0 d_1 ... d_6 d_7
Hold (do nothing)	H	↑	h$^{(1)}$	X	X	X	X	q_0 q_1 ... q_6 q_7

H = High voltage level steady state.
h = High voltage level one setup time prior to the Low-to-High clock transition.
L = Low voltage level steady state.
l = Low voltage level one setup time prior to the Low-to-High clock transition.
X = Don't care.
d_n(q_n) = Lower case letters indicate the state of the referenced input (or output) one setup time prior to the Low-to-High clock transition.
↑ = Low-to-High clock transition.

NOTE:

1. The Low-to-High transition of $\overline{CE}$ should only occur while CP is High for conventional operation.

TIMING DIAGRAM


CP
CE
MR
J
K
PE
Dn
H
L
H
L
H
L
H
H
Qn
INHIBIT
H
H
L
H
L
H
L
H
SERIAL SHIFT
SERIAL SHIFT
CLEAR
LOAD
WF08781S

Typical Clear, Load, Right-Shift, Left-Shift, Inhibit and Clear Sequences

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS Min	LIMITS Nom	LIMITS Max	UNIT
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS Min	LIMITS Typ[2]	LIMITS Max	UNIT
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX V_{IH} = MIN,	±10%V_{CC}	2.5			V
			±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, I_{OL} = MAX V_{IH} = MIN,	±10%V_{CC}		0.35	0.50	V
			±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, $I_I = I_{IK}$			−0.73	−1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V				−0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current (total)	V_{CC} = MAX, $J = \overline{K} = D_n$ = 4.5V, $CP = \overline{CE} = \overline{MR} = \overline{PE}$ = GND			40	95	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

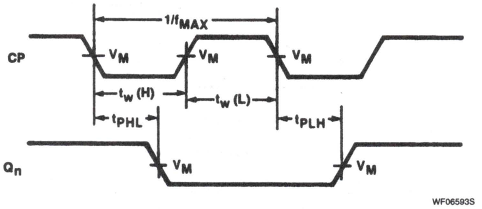
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F199					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	Waveform 1	105	114		90		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	Waveform 1	3.5 3.5		7.0 7.0	3.5 3.5	8.0 8.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	Waveform 2	4.5		12	4.5	14	ns

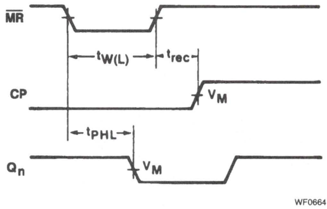
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	74F199					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to CP	Waveform 3	4.0 4.0			6.0 6.0		ns ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to CP	Waveform 3	0 0			1.0 1.0		ns ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low J, $\overline{K}$ to CP	Waveform 3	4.0 4.0			6.0 6.0		ns ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low J, $\overline{K}$ to CP	Waveform 3	0 0			1.0 1.0		ns ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{CE}$ to CP	Waveform 3	8.0 8.0			9.0 8.0		ns ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{CE}$ to CP	Waveform 3	0 0			0 0		ns ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{PE}$ to CP	Waveform 3	8.0 8.0			9.0 8.0		ns ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{PE}$ to CP	Waveform 3	0 0			0 0		ns ns
$t_w(H)$	CP Pulse Width,	Waveform 1	5.0			5.5		ns
$t_w(L)$	$\overline{MR}$ Pulse Width Low	Waveform 2	5.0			5.0		ns
t_{rec}	Recovery time $\overline{MR}$ to CP	Waveform 2	7.0			8.0		ns

AC WAVEFORMS

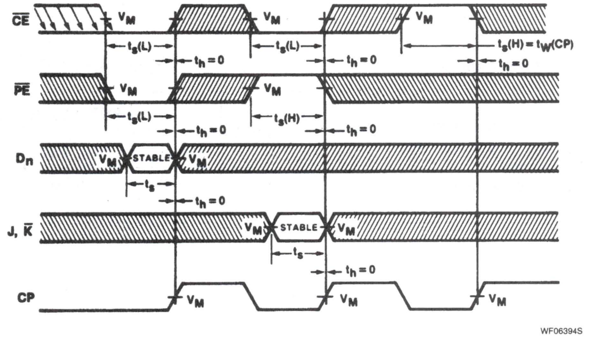

1/fMAX
CP
VM
VM
VM
tw (H)
tw (L)
tPHL
tPLH
Qn
VM
VM
WF06593S

Waveform 1. Clock to Output Delays, Clock Pulse Width, and Maximum Clock Frequency


MR
tW(L)
trec
CP
VM
tPHL
Qn
VM
WF06641S

Condition: MR = High

Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time

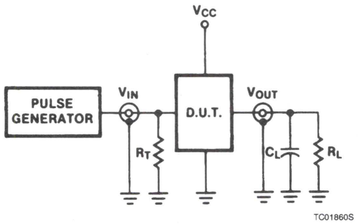

CE
VM
VM
VM
ts(L)
th = 0
ts(L)
th = 0
ts(H) = tW(CP)
th = 0
PE
VM
VM
ts(L)
th = 0
ts(H)
th = 0
Dn
VM
STABLE
VM
ts
th = 0
J, K
VM
STABLE
VM
ts
th = 0
CP
VM
VM
VM
WF06394S

NOTE:
1. The number of clock pulses required between the t_{PLH} and t_{PHL} measurements can be determined from the appropriate Truth Table.
2. The shaded areas indicate when the input is permitted to change for predictable performance.
3. The changing output assumes internal Q_6 opposite state from Q_7.

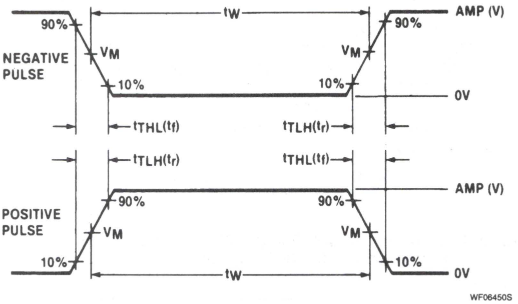
Waveform 3. Setup and Hold Time for $\overline{PE}$, D_n, D_s, and $\overline{CE}$ to CP

NOTE: For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORMS


V_{CC}
PULSE GENERATOR
V_{IN}
D.U.T.
V_{OUT}
R_T
C_L
R_L
TC01860S

Test Circuit for Totem-Pole Outputs


NEGATIVE PULSE
POSITIVE PULSE
90%
10%
VM
tW
AMP (V)
0V
tTHL(tf)
tTLH(tr)
WF06450S

$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS

R_L = Load resistor to GND; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F240, 74F241
Buffers

'F240 Octal Inverter Buffer (3-State)
'F241 Octal Buffer (3-State)
Product Specification

FAST Products

FEATURES

- **Octal bus interface**
- **3-State buffer outputs sink 64mA**
- **15mA source current**

DESCRIPTION

The 'F240 and 'F241 are octal buffers that are ideal for driving bus lines or buffer memory address registers. The outputs are all capable of sinking 64mA and sourcing up to 15mA, producing very good capacitive drive characteristics. The device features two Output Enables, $\overline{OE}$, each controlling four of the 3-State outputs.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F240	4.3ns	37mA
74F241	5.0ns	53mA

ORDERING INFORMATION

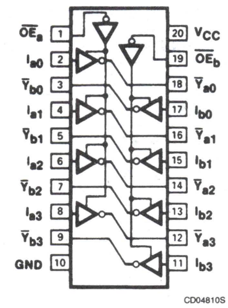
PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
20-Pin Plastic DIP	N74F240N, N74F241N
20-Pin SOL	N74F240D, N74F241D

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$\overline{OE}_a$, $\overline{OE}_b$	3-State output enable input (active-High)	1.0/1.67	20μA/1.0mA
OE_b	3-State output enable input (active-Low)	1.0/1.67	20μA/1.0mA
$I_{a0} - I_{a3}$, $I_{b0} - I_{b3}$	Data inputs ('F240)	1.0/1.67	20μA/1.0mA
$I_{a0} - I_{a3}$, $I_{b0} - I_{b3}$	Data inputs ('F241)	1.0/2.67	20μA/1.6mA
$\overline{Y}_a$, $\overline{Y}_b$ ('F240) Y_a, Y_b ('F241)	Data outputs	750/106.7	15mA/64mA

NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

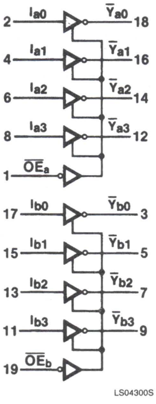
PIN CONFIGURATION

'F240


$\overline{OE}_a$ 1
I_{a0} 2
$\overline{Y}_{b0}$ 3
I_{a1} 4
$\overline{Y}_{b1}$ 5
I_{a2} 6
$\overline{Y}_{b2}$ 7
I_{a3} 8
$\overline{Y}_{b3}$ 9
GND 10
20 V_{CC}
19 $\overline{OE}_b$
18 $\overline{Y}_{a0}$
17 I_{b0}
16 $\overline{Y}_{a1}$
15 I_{b1}
14 $\overline{Y}_{a2}$
13 I_{b2}
12 $\overline{Y}_{a3}$
11 I_{b3}
CD04810S

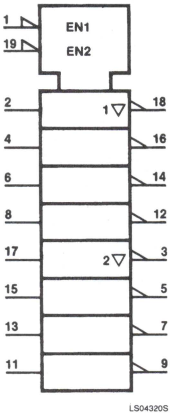
LOGIC SYMBOL

'F240

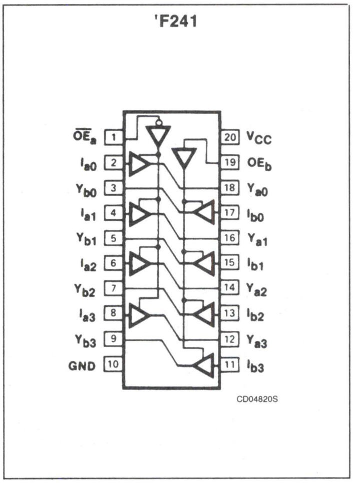

2 I_{a0} $\overline{Y}_{a0}$ 18
4 I_{a1} $\overline{Y}_{a1}$ 16
6 I_{a2} $\overline{Y}_{a2}$ 14
8 I_{a3} $\overline{Y}_{a3}$ 12
1 $\overline{OE}_a$
17 I_{b0} $\overline{Y}_{b0}$ 3
15 I_{b1} $\overline{Y}_{b1}$ 5
13 I_{b2} $\overline{Y}_{b2}$ 7
11 I_{b3} $\overline{Y}_{b3}$ 9
19 $\overline{OE}_b$
LS04300S

LOGIC SYMBOL (IEEE/IEC)

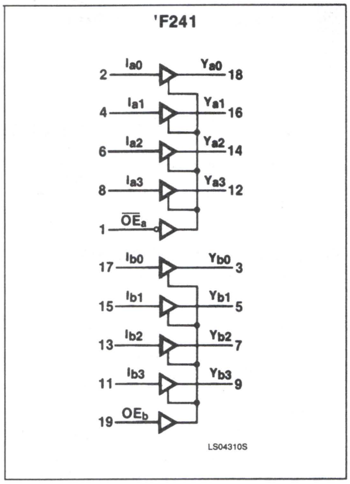
'F240


1
19
EN1
EN2
2
1▽
18
4
16
6
14
8
12
17
2▽
3
15
5
13
7
11
9
LS04320S

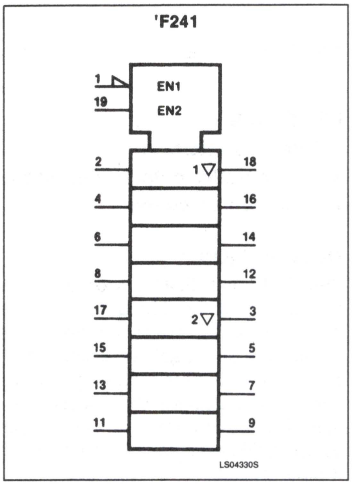
PIN CONFIGURATION


'F241
$\overline{OE}_a$ 1
I_{a0} 2
Y_{b0} 3
I_{a1} 4
Y_{b1} 5
I_{a2} 6
Y_{b2} 7
I_{a3} 8
Y_{b3} 9
GND 10
20 V_{CC}
19 OE_b
18 Y_{a0}
17 I_{b0}
16 Y_{a1}
15 I_{b1}
14 Y_{a2}
13 I_{b2}
12 Y_{a3}
11 I_{b3}
CD04820S

LOGIC SYMBOL


'F241
2 I_{a0} Y_{a0} 18
4 I_{a1} Y_{a1} 16
6 I_{a2} Y_{a2} 14
8 I_{a3} Y_{a3} 12
1 $\overline{OE}_a$
17 I_{b0} Y_{b0} 3
15 I_{b1} Y_{b1} 5
13 I_{b2} Y_{b2} 7
11 I_{b3} Y_{b3} 9
19 OE_b
LS04310S

LOGIC SYMBOL (IEEE/IEC)


'F241
1
19
EN1
EN2
2 1▽ 18
4 16
6 14
8 12
17 2▽ 3
15 5
13 7
11 9
LS04330S

FUNCTION TABLE, 'F240

INPUTS				OUTPUTS	
$\overline{OE}_a$	I_a	$\overline{OE}_b$	I_b	$\overline{Y}_a$	$\overline{Y}_b$
L	L	L	L	H	H
L	H	L	H	L	L
H	X	H	X	Z	Z

FUNCTION TABLE, 'F241

INPUTS				OUTPUTS	
$\overline{OE}_a$	I_a	OE_b	I_b	Y_a	Y_b
L	L	H	L	L	L
L	H	H	H	H	H
H	X	L	X	Z	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High-impedance (OFF) state

ABSOLUTE MAXIMUM RATINGS Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	128	mA
T_A	Operating free-air temperature range	0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−15	mA
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]			74F240, 241			UNIT
							Min	Typ[2]	Max	
V_{OH}	High-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = −3mA	±10%V_{CC}	2.4			V
						±5%V_{CC}	2.7	3.4		V
					I_{OH} = −15mA	±10%V_{CC}	2.0			V
						±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 48mA	±10%V_{CC}		0.35	0.50	V
					I_{OL} = 64mA	±5%V_{CC}		0.40	0.55	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, I_I = I_{IK}				−0.73	−1.2	V
I_I	Input current at maximum input voltage			V_{CC} = MAX, V_I = 7.0V					100	μA
I_{IH}	High-level input current			V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	Low-level input current	'F240 All inputs		V_{CC} = MAX, V_I = 0.5V					−1.0	mA
		'F241 $\overline{OE}_a$, OE_b							−1.0	mA
		'F241 $I_{a0} - I_{a3}$, $I_{b0} - I_{b3}$							−1.6	mA
I_{OZH}	Off-state output current, High-level voltage applied			V_{CC} = MAX, V_{OUT} = 2.7V					50	μA
I_{OZL}	Off-state output current, Low-level voltage applied			V_{CC} = MAX, V_{OUT} = 0.5V					−50	μA
I_{OS}	Short-circuit output current[3]			V_{CC} = MAX			−100		−225	mA
I_{CC}	Supply current[4] (total)	'F240	I_{CCH}	V_{CC} = MAX				12	18	mA
			I_{CCL}					50	70	mA
			I_{CCZ}					35	45	mA
		'F241	I_{CCH}					40	60	mA
			I_{CCL}					60	90	mA
			I_{CCZ}					65	90	mA

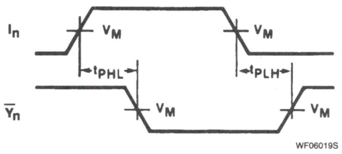
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. I_{CC} is measured with outputs open.

AC ELECTRICAL CHARACTERISTICS

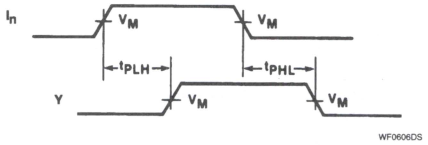
SYMBOL	PARAMETER		TEST CONDITIONS	74F240, 241					UNIT
				$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay Data to output	'F240	Waveform 1	3.0 2.0	4.5 3.0	6.5 4.5	3.0 2.0	7.5 5.0	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level		Waveform 2 Waveform 3	3.0 4.5	5.0 6.5	7.5 8.5	3.0 4.0	9.0 10.0	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level		Waveform 2 Waveform 3	3.0 3.0	5.5 5.0	7.0 7.0	3.0 3.0	7.5 7.5	ns
t_{PLH} t_{PHL}	Propagation delay Data to output	'F241	Waveform 2	2.5 2.5	4.0 4.0	5.2 5.2	2.5 2.5	6.2 6.5	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level		Waveform 2 Waveform 3	2.0 2.0	4.0 5.0	5.7 7.0	2.0 2.0	6.7 8.0	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level		Waveform 2 Waveform 3	2.0 2.0	4.0 4.0	6.0 6.0	2.0 2.0	7.0 7.0	ns

AC WAVEFORMS



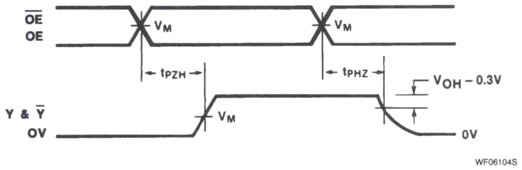
I_n
V_M
V_M
t_{PHL}
t_{PLH}
$\overline{Y}_n$
V_M
V_M
WF06019S

Waveform 1. For Inverting Outputs



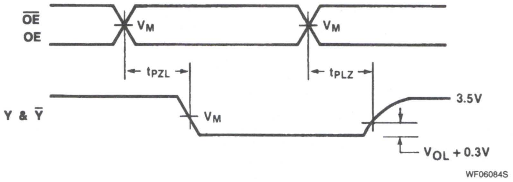
I_n
V_M
V_M
t_{PLH}
t_{PHL}
Y
V_M
V_M
WF0606DS

Waveform 2. For Non-Inverting Outputs



$\overline{OE}$
OE
V_M
V_M
t_{PZH}
t_{PHZ}
$V_{OH} - 0.3V$
Y & $\overline{Y}$
OV
V_M
0V
WF06104S

Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time From High Level

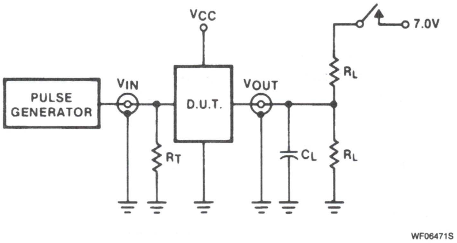


$\overline{OE}$
OE
V_M
V_M
t_{PZL}
t_{PLZ}
Y & $\overline{Y}$
V_M
3.5V
$V_{OL} + 0.3V$
WF06084S

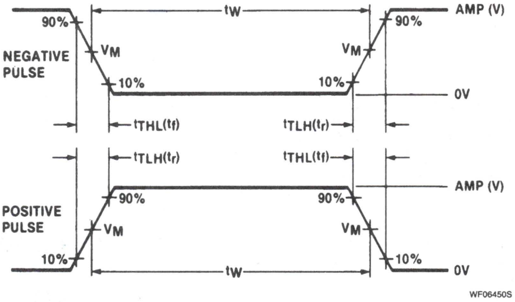
Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORM


VCC
7.0V
RL
PULSE GENERATOR
VIN
D.U.T.
VOUT
RT
CL
RL
WF06471S

Test Circuit for 3-State Outputs


90%
tW
90%
AMP (V)
NEGATIVE PULSE
VM
VM
10%
10%
0V
tTHL(tf)
tTLH(tr)
tTLH(tr)
tTHL(tf)
AMP (V)
90%
90%
POSITIVE PULSE
VM
VM
10%
10%
0V
tW
WF06450S

$V_M = 1.5V$

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST Products

FAST 74F242, 74F243
Transceivers

'F242 Quad Transceiver, Inverting (3-State)
'F243 Quad Transceiver (3-State)
Product Specification

FUNCTION TABLE, 'F242

INPUTS		INPUT/OUTPUT	
$\overline{OE}_A$	OE_B	A_n	B_n
L	L	INPUT	$B = \overline{A}$
H	L	Z	Z
L	H	a	a
H	H	$A = \overline{B}$	INPUT

FUNCTION TABLE, 'F243

INPUTS		INPUT/OUTPUT	
$\overline{OE}_A$	OE_B	A_n	B_n
L	L	INPUT	B = A
H	L	Z	Z
L	H	a	a
H	H	A = B	INPUT

H = High voltage level
L = Low voltage level
Z = High-impedance (OFF) state
a = This condition is not allowed due to excessive currents.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F242	4.3ns	31.2mA
74F243	4.0ns	66mA

ORDERING INFORMATION

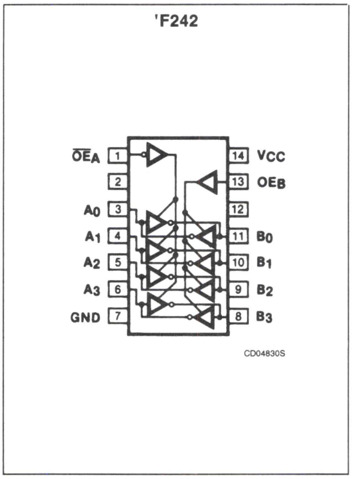
PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
14-Pin Plastic DIP	N74F242N, N74F243N
14-Pin Plastic SO	N74F242D, N74F243D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

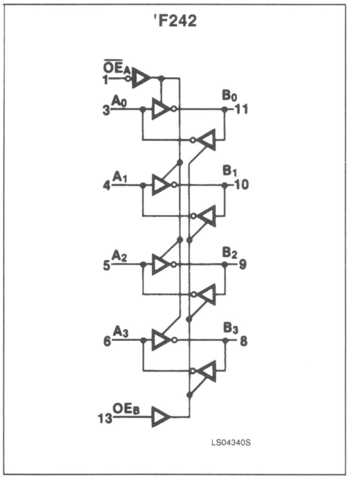
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$\overline{OE}_A$	Enable input (active-Low)	1.0/1.67	20µA/1mA
OE_B	Enable input (active-High)	1.0/1.67	20µA/1mA
A_n, B_n	Inputs ('F242)	3.5/1.67	70µA/1mA
A_n, B_n	Inputs ('F243)	3.5/2.67	70µA/1.6mA
A_n, B_n	Outputs	750/106.7	15mA/64mA

NOTE:
1. One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

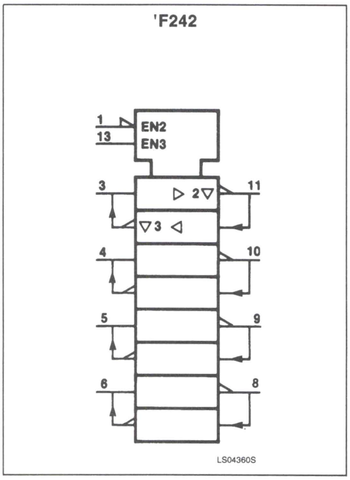
PIN CONFIGURATION


'F242
$\overline{OE}_A$ 1
2
A0 3
A1 4
A2 5
A3 6
GND 7
14 VCC
13 OEB
12
11 B0
10 B1
9 B2
8 B3
CD04830S

LOGIC SYMBOL

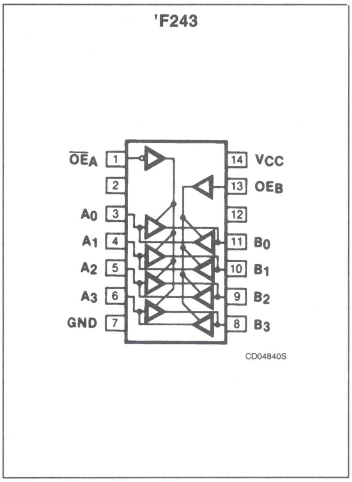

'F242
$\overline{OE}_A$ 1
A0 3
A1 4
A2 5
A3 6
OEB 13
B0 11
B1 10
B2 9
B3 8
LS04340S

LOGIC SYMBOL (IEEE/IEC)

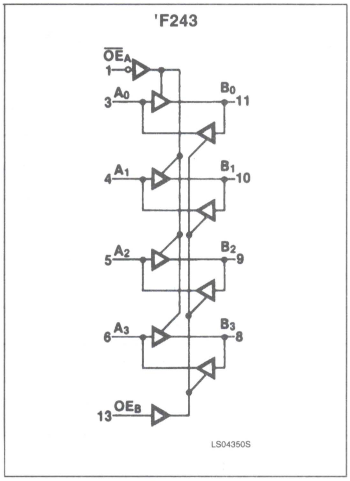

'F242
1
13
EN2
EN3
3
11
▷ 2▽
▽3 ◁
4
10
5
9
6
8
LS04360S

Transceivers FAST 74F242, 74F243

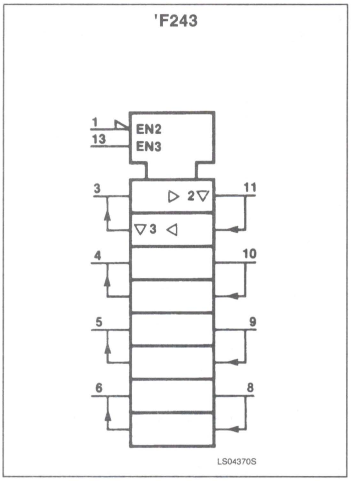
PIN CONFIGURATION


'F243
$\overline{OE}_A$ 1
2
A0 3
A1 4
A2 5
A3 6
GND 7
14 VCC
13 OEB
12
11 B0
10 B1
9 B2
8 B3
CD04840S

LOGIC SYMBOL


'F243
$\overline{OE}_A$ 1
3 A0
B0 11
4 A1
B1 10
5 A2
B2 9
6 A3
B3 8
13 OEB
LS04350S

LOGIC SYMBOL (IEEE/IEC)


'F243
1
13
EN2
EN3
3
▷ 2▽
▽3 ◁
11
4
10
5
9
6
8
LS04370S

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	128	mA
T_A	Operating free-air temperature range	0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−15	mA
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]			74F242, 74F243			UNIT
							Min	Typ[2]	Max	
V_{OH}	High-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = −3mA	±10%V_{CC}	2.4	3.4		V
						±5%V_{CC}	2.7	3.4		V
					I_{OH} = −15mA	±10%V_{CC}	2.0	3.0		V
						±5%V_{CC}	2.0	3.0		V
V_{OL}	Low-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 48mA	±10%V_{CC}		0.40	0.50	V
					I_{OL} = 64mA	±5%V_{CC}		0.40	0.55	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, I_I = I_{IK}				−0.73	−1.2	V
I_I	Input current at maximum input voltage	$A_0 - A_3$, $B_0 - B_3$		V_{CC} = 5.5V, V_I = 5.5V					100	μA
		$\overline{OE}_A$, OE_B		V_{CC} = MAX, V_I = 7.0V					100	μA
I_{IH}	High-level input current for $\overline{OE}_A$ and OE_B inputs only			V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	Low-level input current for $\overline{OE}_A$ and OE_B inputs only			V_{CC} = MAX, V_I = 0.5V					−1	mA
I_{OZH} + I_{IH}	Off-state output current High-level voltage applied			V_{CC} = MAX, V_O = 2.7V					70	μA
I_{OZL} + I_{IL}	Off-state output current, Low-level voltage applied	'F242		V_{CC} = MAX, V_O = 0.5V					−1.0	mA
		'F243							−1.6	mA
I_{OS}	Short-circuit output current[3]			V_{CC} = MAX			−100		−225	mA
I_{CC}	Supply current (total)	'F242	I_{CCH}	V_{CC} = MAX				22	35	mA
			I_{CCL}					40	55	mA
			I_{CCZ}					32	45	mA
		'F243	I_{CCH}					64	80	mA
			I_{CCL}					64	90	mA
			I_{CCZ}					71	90	mA

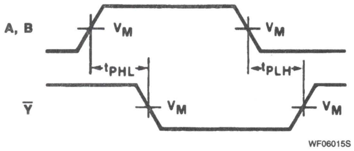
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. I_{CC} is measured with outputs open and transceivers enabled in one direction only, or with all transceivers disabled.

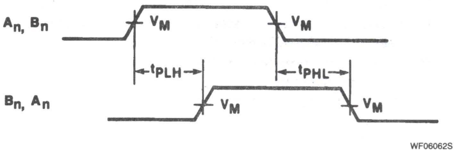
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	74F242, 'F243					UNIT
				$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n, B_n to B_n, A_n	'F242	Waveform 1	3.0 2.0	4.5 3.0	6.5 4.5	3.0 2.0	7.5 4.5	
t_{PZH} t_{PZL}	Output enable time to High or Low level		Waveform 3	3.5 3.5	6.0 6.5	7.5 9.0	3.5 3.5	8.5 10.5	ns
t_{PHZ} t_{PLZ}	Output disable time from High or Low level		Waveform 3	4.0 3.5	7.0 6.0	9.0 9.5	4.0 3.5	9.5 11.0	ns
t_{PLH} t_{PHL}	Propagation delay A_n, B_n to B_n, A_n	'F243	Waveform 2	2.5 2.5	4.0 4.0	5.2 5.2	2.0 2.0	6.2 6.5	ns
t_{PZH} t_{PZL}	Output enable time to High or Low level		Waveform 4	2.0 2.0	4.5 5.0	5.7 7.5	2.0 2.0	6.7 8.5	ns
t_{PHZ} t_{PLZ}	Output disable time from High or Low level		Waveform 4	2.0 2.0	4.0 4.5	6.0 6.0	2.0 2.0	7.0 7.0	ns

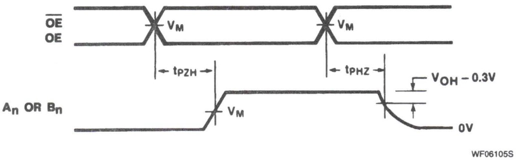
AC WAVEFORMS


A, B
VM
VM
tPHL
tPLH
Ȳ
VM
VM
WF06015S

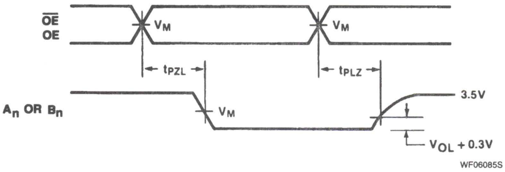
Waveform 1. Waveform for Inverting Outputs


An, Bn
VM
VM
tPLH
tPHL
Bn, An
VM
VM
WF06062S

Waveform 2. Waveform for Non-Inverting Outputs


OE
OE
VM
VM
tPZH
tPHZ
VOH − 0.3V
An OR Bn
VM
0V
WF06105S

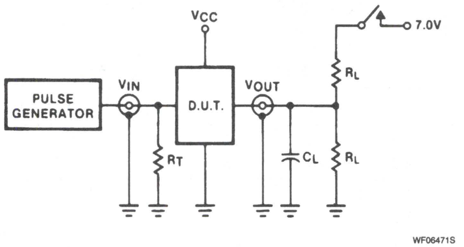
Waveform 3. 3-State Enable Time to High Level and Disable Time from High Level


OE
OE
VM
VM
tPZL
tPLZ
3.5V
An OR Bn
VM
VOL + 0.3V
WF06085S

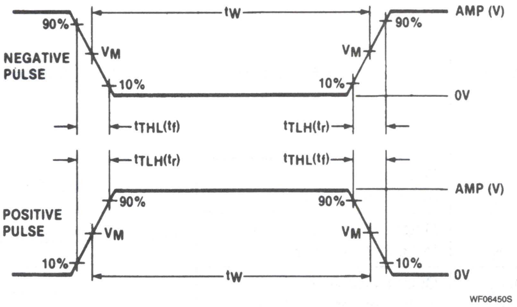
Waveform 4. 3-State Enable Time to Low Level and Disable Time from Low Level

NOTE: For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORM


VCC
7.0V
RL
PULSE GENERATOR
VIN
D.U.T.
VOUT
RT
CL
RL
WF06471S

Test Circuit for 3-State Outputs


tW
AMP (V)
90%
90%
NEGATIVE PULSE
VM
VM
10%
10%
0V
tTHL(tf)
tTLH(tr)
tTLH(tr)
tTHL(tf)
AMP (V)
90%
90%
POSITIVE PULSE
VM
VM
10%
10%
0V
tW
WF06450S

$V_M = 1.5V$.

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F244
Buffer

Octal Buffer (3-State)
Product Specification

FAST Products

FEATURES
- Octal bus interface
- 3-State buffer outputs sink 64mA
- 15mA source current

DESCRIPTION
The 'F244 is an octal buffer that is ideal for driving bus lines or buffer memory address registers. The outputs are all capable of sinking 64mA and sourcing up to 15mA, producing very good capacitive drive characteristics. The device features two Output Enables, $\overline{OE}$, each controlling four of the 3-State outputs.

FUNCTION TABLE

INPUTS				OUTPUTS	
$\overline{OE}_a$	I_a	$\overline{OE}_b$	I_b	Y_a	Y_b
L	L	L	L	L	L
L	H	L	H	H	H
H	X	H	X	Z	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High-impedance (OFF) state

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F244	4.0ns	53mA

ORDERING INFORMATION

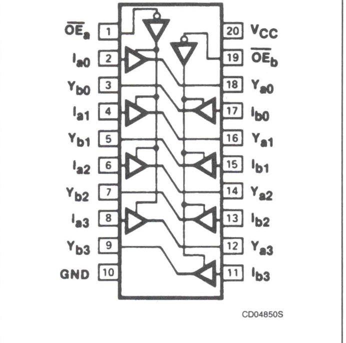
PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
20-Pin Plastic DIP	N74F244N
20-Pin Plastic SOL	N74F244D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$\overline{OE}_a$	3-State output enable input (active-Low)	1.0/1.67	20μA/1.0mA
$\overline{OE}_b$	3-State output enable input (active-Low)	1.0/1.67	20μA/1.0mA
$I_{a0} - I_{a3}$, $I_{b0} - I_{b3}$	Data inputs	1.0/2.67	20μA/1.6mA
$Y_{a0} - Y_{a3}$, $Y_{b0} - Y_{b3}$	Data outputs	750/106.7	15mA/64mA

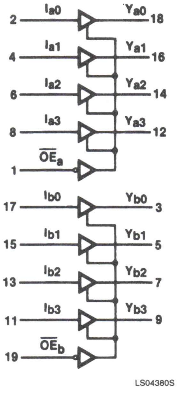
NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



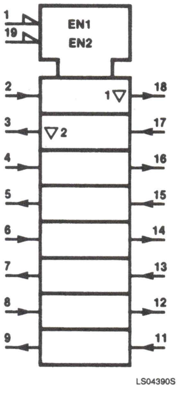
$\overline{OE}_a$ 1
I_{a0} 2
Y_{b0} 3
I_{a1} 4
Y_{b1} 5
I_{a2} 6
Y_{b2} 7
I_{a3} 8
Y_{b3} 9
GND 10
20 V_{CC}
19 $\overline{OE}_b$
18 Y_{a0}
17 I_{b0}
16 Y_{a1}
15 I_{b1}
14 Y_{a2}
13 I_{b2}
12 Y_{a3}
11 I_{b3}
CD04850S

LOGIC SYMBOL



2 I_{a0} Y_{a0} 18
4 I_{a1} Y_{a1} 16
6 I_{a2} Y_{a2} 14
8 I_{a3} Y_{a3} 12
1 $\overline{OE}_a$
17 I_{b0} Y_{b0} 3
15 I_{b1} Y_{b1} 5
13 I_{b2} Y_{b2} 7
11 I_{b3} Y_{b3} 9
19 $\overline{OE}_b$
LS04380S

LOGIC SYMBOL (IEEE/IEC)



1
19
EN1
EN2
2
18
1▽
3
17
▽2
4
16
5
15
6
14
7
13
8
12
9
11
LS04390S

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High-output state	−0.5 to +5.5	V
I_{OUT}	Current applied to output in Low-output state	128	mA
T_A	Operating free-air temperature range	0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−15	mA
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			74F244			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = −3mA	+10%V_{CC}	2.4			V
					+5%V_{CC}	2.7	3.4		V
				I_{OH} = −15mA	+10%V_{CC}	2.0			V
					+5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 48mA	+10%V_{CC}		0.35	0.50	V
				I_{OL} = 64mA	+5%V_{CC}		0.40	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$				−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V					100	μA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					−1.0	mA
								−1.6	mA
I_{OZH}	Off-state output current, High-level voltage applied		V_{CC} = MAX, V_{OUT} = 2.7V					50	μA
I_{OZL}	Off-state output current, Low-level voltage applied		V_{CC} = MAX, V_{OUT} = 0.5V					−50	μA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX			−100		−225	mA
I_{CC}	Supply Current[4] (total)	I_{CCH}	V_{CC} = MAX				40	60	mA
		I_{CCL}					60	90	mA
		I_{CCZ}					60	90	mA

NOTES:

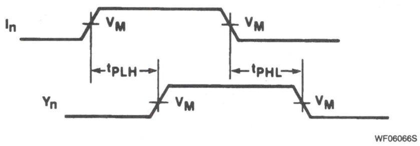
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. I_{CC} is measured with outputs open.

AC ELECTRICAL CHARACTERISTICS

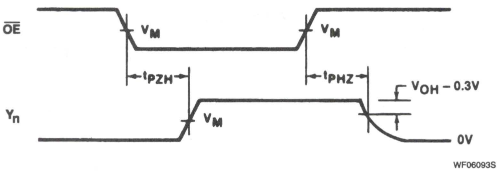
SYMBOL	PARAMETER	TEST CONDITIONS	74F244					UNIT
			T_A = +25°C V_{CC} = +5.0V C_L = 50pF R_L = 500Ω			T_A = 0 to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_n to Y_n	Waveform 1	2.5 2.5	4.0 4.0	5.2 5.2	2.5 2.5	6.2 6.5	ns ns
t_{PZH} t_{PZL}	Output Enable Time to High and Low level	Waveform 2 Waveform 3	2.0 2.0	4.3 5.0	5.7 7.0	2.0 2.0	6.7 8.0	ns ns
t_{PHZ} t_{PLZ}	Output Disable Time from High and Low level	Waveform 2 Waveform 3	2.0 2.0	3.5 4.0	6.0 6.0	2.0 2.0	7.0 7.0	ns ns

Buffer FAST 74F244

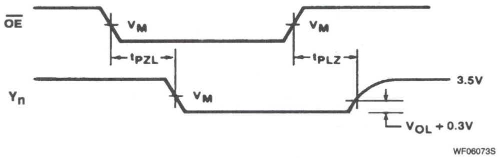
AC WAVEFORMS


In
VM
VM
tPLH
tPHL
Yn
VM
VM
WF06066S

Waveform 1. For Non-Inverting Outputs


OE
VM
VM
tPZH
tPHZ
VOH – 0.3V
Yn
VM
0V
WF06093S

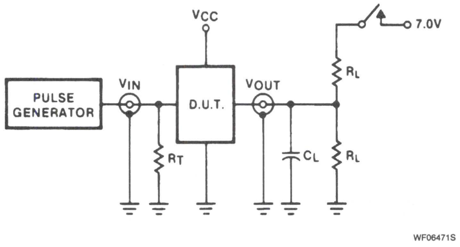
Waveform 2. 3-State Output Enable Time to High Level and Output Disable Time from High Level


OE
VM
VM
tPZL
tPLZ
3.5V
Yn
VM
VOL + 0.3V
WF06073S

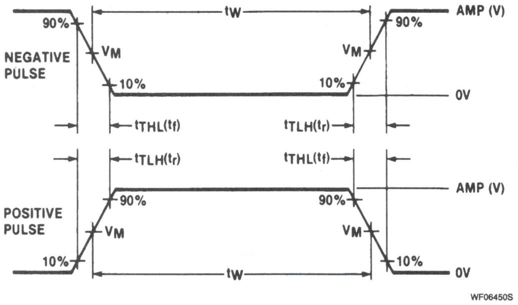
Waveform 3. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

NOTE: For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORM


VCC
7.0V
RL
PULSE GENERATOR
VIN
D.U.T.
VOUT
RT
CL
RL
WF06471S

Test Circuit for 3-State Outputs


90%
tW
90%
AMP (V)
NEGATIVE PULSE
VM
VM
10%
10%
0V
tTHL(tf)
tTLH(tr)
tTLH(tr)
tTHL(tf)
AMP (V)
90%
90%
POSITIVE PULSE
VM
VM
10%
10%
tW
0V
WF06450S

$V_M = 1.5V$

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F245
Transceiver

Octal Transceiver (3-State)
Product Specification

FAST Products

FEATURES
- **Octal bidirectional bus interface**
- **3-State buffer outputs sink 64mA**
- **15mA source current**
- **Outputs are placed in Hi-Z state during power-off conditions**

DESCRIPTION
The 'F245 is an octal transceiver featuring noninverting 3-State bus compatible outputs in both send and receive directions. The B side outputs are all capable of sinking 64mA and sourcing up to 15mA, producing very good capacitive drive characteristics. The device features an Output Enable ($\overline{OE}$) input for easy cascading and a Send/Receive (T/$\overline{R}$) input for direction control. The 3-State outputs, $B_0 - B_7$, have been designed to prevent output bus loading if the power is removed from the device.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F245	4.0ns	100mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%; T_A = 0°C$ to $+70°C$
20-Pin Plastic DIP	N74F245N
20-Pin Plastic SOL[1]	N74F245D

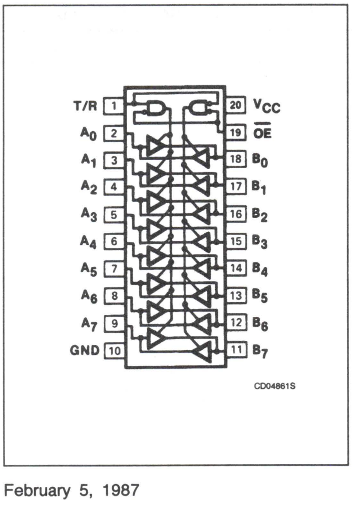
NOTE:
1. Thermal mounting techniques are recommended. See App Note AN SMD-100 for a discussion of thermal considerations for surface-mounted device.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

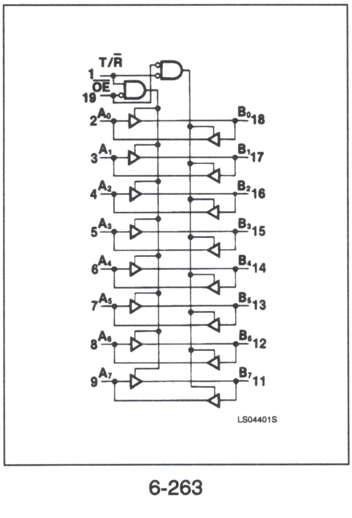
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$A_0 - A_7$	A Port data inputs	3.5/1.0	70µA/0.6mA
$B_0 - B_7$	B Port data inputs	3.5/1.0	70µA/0.6mA
$\overline{OE}$	Output enable input (active-Low)	2.0/2.0	40µA/1.2mA
T/$\overline{R}$	Transmit/Receive input	2.0/2.0	40µA/1.2mA
$A_0 - A_7$	A Port data outputs	150/40	3.0mA/24mA
$B_0 - B_7$	B Port data outputs	750/106.7	15mA/64mA

NOTE:
1. One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

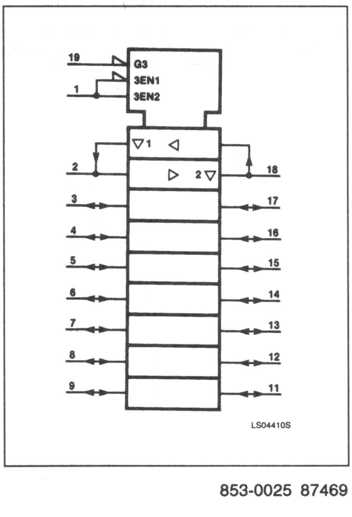
PIN CONFIGURATION


T/R 1
A0 2
A1 3
A2 4
A3 5
A4 6
A5 7
A6 8
A7 9
GND 10
20 VCC
19 OE
18 B0
17 B1
16 B2
15 B3
14 B4
13 B5
12 B6
11 B7
CD04861S

LOGIC SYMBOL


T/R̄
1
OE
19
2 A0
3 A1
4 A2
5 A3
6 A4
7 A5
8 A6
9 A7
B0 18
B1 17
B2 16
B3 15
B4 14
B5 13
B6 12
B7 11
LS04401S

LOGIC SYMBOL (IEEE/IEC)


19
1
G3
3EN1
3EN2
▽1 ◁
▷ 2▽
2
3
4
5
6
7
8
9
18
17
16
15
14
13
12
11
LS04410S

FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS	
$\overline{OE}$	S/$\overline{R}$	A_n	B_n
L	L	A = B	INPUTS
L	H	INPUT	B = A
H	X	Z	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High-impedance (OFF) state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		−0.5 to +7.0	V
V_{IN}	Input voltage		−0.5 to +7.0	V
I_{IN}	Input current		−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		−0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	$A_0 - A_7$	48	mA
		$B_0 - B_7$	128	mA
T_A	Operating free-air temperature range		0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	High-level output current	$A_0 - A_7$			−3	mA
		$B_0 - B_7$			−15	mA
I_{OL}	High-level output current	$A_0 - A_7$			24	mA
		$B_0 - B_7$			64	mA
T_A	Operating free-air temperature		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			74F245 Min	74F245 Typ[2]	74F245 Max	UNIT
V_{OH}	High-level output voltage	$A_0 - A_7$	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = −3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.4		V
		$B_0 - B_7$		I_{OH} = −15mA	±10%V_{CC}	2.0			V
					±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage	$A_0 - A_7$	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 24mA	±10%V_{CC}		0.35	0.50	V
				I_{OL} = 48mA	±10%V_{CC}		0.35	0.50	V
		$B_0 - B_7$		I_{OL} = 64mA	±5%V_{CC}		0.40	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$				−0.73	−1.2	V
I_I	Input current at maximum input voltage	$\overline{OE}$, T/$\overline{R}$	V_{CC} = MAX, V_I = 7.0V					100	μA
		$A_0 - A_7$, $B_0 - B_7$	V_{CC} = 5.5V, V_I = 5.5V					1.0	mA
I_{IH}	High-level input current $\overline{OE}$ and T/$\overline{R}$ only		V_{CC} = MAX, V_I = 2.7V					40	μA
I_{IL}	Low-level input current $\overline{OE}$ and T/$\overline{R}$ only		V_{CC} = MAX, V_I = 0.5V					−1.2	mA
I_{OZH} + I_{IH}	Off-state current High-level voltage applied		V_{CC} = MAX, V_O = 2.7V					70	μA
I_{OZL} + I_{IL}	Off-state current Low-level voltage applied		V_{CC} = MAX, V_O = 0.5V					−600	μA
I_{OS}	Short-circuit output current[3]	$A_0 - A_7$	V_{CC} = MAX			−60		−150	mA
		$B_0 - B_7$				−100		−225	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_{IN} = 4.5V			85	114	mA
		I_{CCL}		V_{IN} = GND			100	125	mA
		I_{CCZ}		$V_{IN} = \overline{OE}$ = 4.5V			90	120	mA

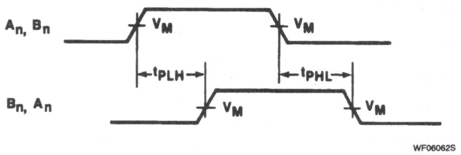
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

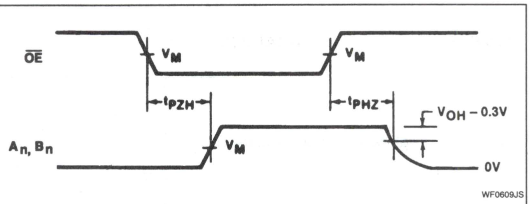
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C V_{CC} = +5.0V C_L = 50pF R_L = 500Ω			T_A = 0 to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH}	Propagation delay	Waveform 1	2.5	3.5	5.5	2.5	6.5	ns
t_{PHL}	A_n to B_n or B_n to A_n		2.5	4.0	6.0	2.5	7.0	
t_{PZH}	Output enable time	Waveform 2	5.0	7.0	8.5	5.0	9.5	ns
t_{PZL}	to High and Low level	Waveform 3	3.5	6.5	8.0	3.5	9.0	
t_{PHZ}	Output disable time	Waveform 2	3.0	4.5	6.5	3.0	7.5	ns
t_{PLZ}	from High and Low level	Waveform 3	2.0	4.0	6.0	2.0	7.0	

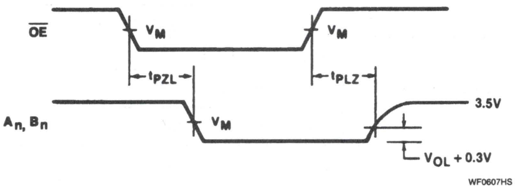
AC WAVEFORMS


An, Bn
VM
VM
tPLH
tPHL
Bn, An
VM
VM
WF06062S

Waveform 1. Propagation Delay Data to Output


OE
VM
VM
tPZH
tPHZ
VOH – 0.3V
An, Bn
VM
0V
WF0609JS

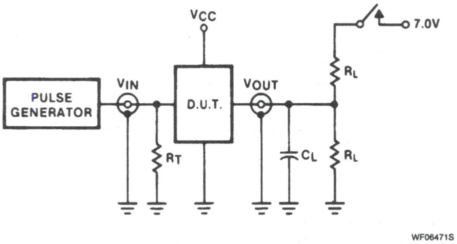
Waveform 2. 3-State Output Enable Time to High Level and Output Disable Time from High Level


OE
VM
VM
tPZL
tPLZ
3.5V
An, Bn
VM
VOL + 0.3V
WF0607HS

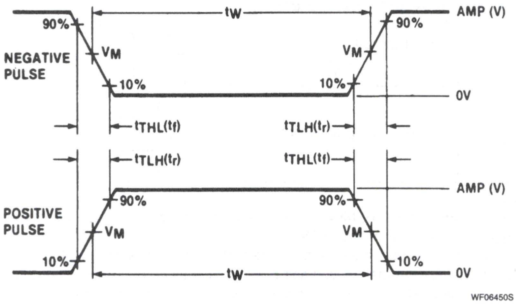
Waveform 3. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

NOTE: For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORM


VCC
7.0V
RL
PULSE GENERATOR
VIN
D.U.T.
VOUT
RT
CL
RL
WF06471S

Test Circuit for 3-State Outputs


NEGATIVE PULSE
90%
VM
10%
tW
VM
90%
10%
AMP (V)
0V
tTHL(tf)
tTLH(tr)
tTLH(tr)
tTHL(tf)
POSITIVE PULSE
90%
VM
10%
90%
VM
10%
tW
AMP (V)
0V
WF06450S

$V_M = 1.5V$
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_r	t_f
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAST 74F251
Multiplexer

8-Input Multiplexer (3-State)
Preliminary Specification

FAST Products

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F251	5.5ns	15mA

FEATURES
- **High-speed 8-to-1 multiplexing**
- **True and complement outputs**
- **Both outputs are 3-State for further multiplexer expansion**

DESCRIPTION
The 'F251 is a logical implementation of a single-pole, 8-position switch with the state of three Select inputs (S_0, S_1, S_2) controlling the switch position. Assertion (Y) and Negation ($\overline{Y}$) outputs are both provided. The Output Enable input ($\overline{OE}$) is active-Low.

Both outputs are in the High-impedance (Hi-Z) state when the output enable is High, allowing multiplexer expansion by tying the outputs of up to 128 devices together. All but one device must be in the High-impedance state to avoid high currents that would exceed the maximum ratings when the outputs of the 3-State devices are tied together. Design of the Output Enable signals must ensure there is no overlap in the active-Low portion of the enable voltages.

ORDERING INFORMATION

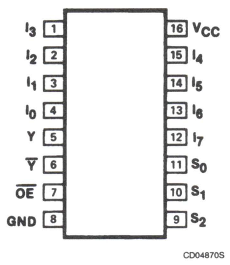
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ± 5%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F251N
16-Pin Plastic SO	N74F251D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$I_0 - I_7$	Data inputs	1.0/1.0	20μA/0.6mA
$S_0 - S_2$	Select inputs	1.0/1.0	20μA/0.6mA
$\overline{OE}$	3-State output enable input (active-Low)	1.0/1.0	20μA/0.6mA
Y, $\overline{Y}$	3-State output 3-State output inverted	150/40	3.0mA/24mA

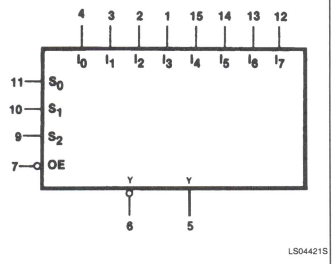
NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



I_3 1
I_2 2
I_1 3
I_0 4
Y 5
$\overline{Y}$ 6
$\overline{OE}$ 7
GND 8
16 V_{CC}
15 I_4
14 I_5
13 I_6
12 I_7
11 S_0
10 S_1
9 S_2
CD04870S

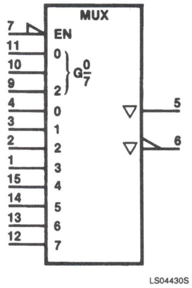
LOGIC SYMBOL



4 3 2 1 15 14 13 12
I_0 I_1 I_2 I_3 I_4 I_5 I_6 I_7
11 S_0
10 S_1
9 S_2
7 OE
$\overline{Y}$ Y
6 5
LS04421S

V_{CC} = Pin 16
GND = Pin 8

LOGIC SYMBOL (IEEE/IEC)

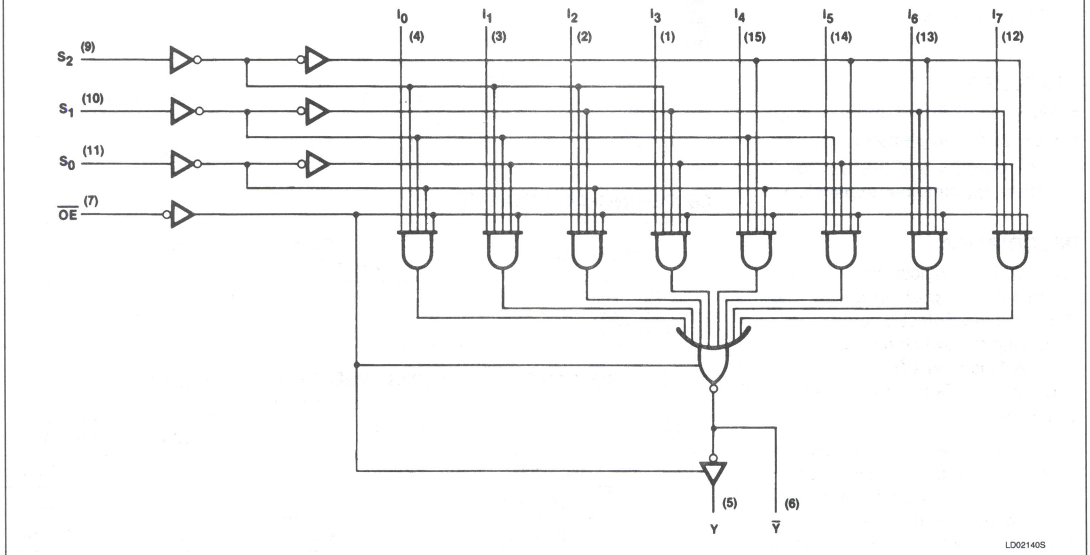


MUX
7 EN
11 0
10
9 2
$G\frac{0}{7}$
4 0
3 1
2 2
1 3
15 4
14 5
13 6
12 7
5
6
LS04430S

Multiplexer

FAST 74F251

LOGIC DIAGRAM


I_0 (4)
I_1 (3)
I_2 (2)
I_3 (1)
I_4 (15)
I_5 (14)
I_6 (13)
I_7 (12)
S_2 (9)
S_1 (10)
S_0 (11)
$\overline{OE}$ (7)
(5)
(6)
Y
$\overline{Y}$
LD02140S

V_{CC} = Pin 16
GND = Pin 8
( ) = Pin numbers

FUNCTION TABLE

INPUTS				OUTPUTS	
S_2	S_1	S_0	$\overline{OE}$	Y	$\overline{Y}$
X	X	X	H	Z	Z
L	L	L	L	I_0	$\overline{I}_0$
L	L	H	L	I_1	$\overline{I}_1$
L	H	L	L	I_2	$\overline{I}_2$
L	H	H	L	I_3	$\overline{I}_3$
H	L	L	L	I_4	$\overline{I}_4$
H	L	H	L	I_5	$\overline{I}_5$
H	H	L	L	I_6	$\overline{I}_6$
H	H	H	L	I_7	$\overline{I}_7$

H = High voltage level
L = Low voltage level
X = Don't care
Z = High-impedance (OFF) state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_A	Operating free-air temperature range	0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−3.0	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			74F251			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = MAX	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.3		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = MAX	±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$				−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V					100	μA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					−0.6	mA
I_{OZH}	OFF-state output current, High-level voltage applied		V_{CC} = MAX, V_O = 2.7V					50	μA
I_{OZL}	OFF-state output current, Low-level voltage applied		V_{CC} = MAX, V_O = 0.5V					−50	μA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX			−60		−150	mA
I_{CC}	Supply current[4] (total)	I_{CCH}	V_{CC} = MAX				14	22	mA
		I_{CCL}					14	22	mA
		I_{CCZ}					16	24	mA

NOTES:

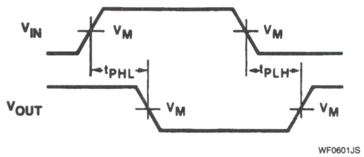
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. I_{CC} is meaured with V_{CC} = MAX, Select and Data inputs at 4.5V, and $\overline{OE}$ ground for output High and Low conditions; V_{CC} = MAX, Data inputs and the $\overline{OE}$ at 4.5V for outputs OFF condition.

Multiplexer FAST 74F251

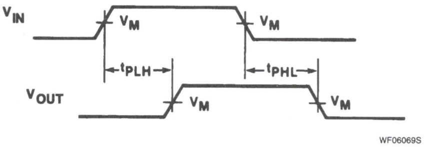
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F251					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_n to Y	Waveform 2	3.0 3.0	4.0 4.5	6.0 6.5	2.5 3.0	7.0 7.0	ns
t_{PLH} t_{PHL}	Propagation delay I_n to $\overline{Y}$	Waveform 1	2.5 1.0	4.0 2.0	6.0 4.0	2.0 1.0	7.0 5.0	ns
t_{PLH} t_{PHL}	Propagation delay S_n to Y	Waveform 1, 2	4.0 4.0	7.0 7.0	9.5 9.0	3.5 4.0	11.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{Y}$	Waveform 1, 2	3.5 1.5	6.0 5.0	9.0 7.5	3.5 1.5	10.0 8.5	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OE}$ to Y	Waveform 3 Waveform 4	4.0 4.0	6.5 5.5	10.0 8.0	4.0 3.5	11.0 9.0	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OE}$ to $\overline{Y}$	Waveform 3 Waveform 4	4.0 4.0	5.5 5.5	8.0 8.0	3.5 3.5	9.0 9.0	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OE}$ to Y	Waveform 3 Waveform 4	2.5 3.0	4.0 4.0	6.5 6.5	2.0 2.5	7.5 7.5	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OE}$ to $\overline{Y}$	Waveform 3 Waveform 4	2.5 2.0	4.0 4.0	6.0 6.5	2.0 2.0	7.0 8.0	ns

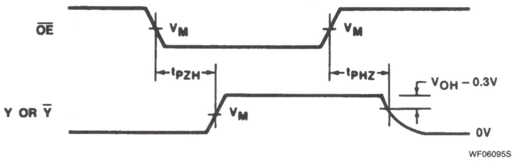
AC WAVEFORMS


V_IN
V_M
V_M
t_PHL
t_PLH
V_OUT
V_M
V_M
WF0601JS

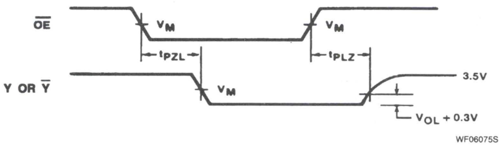
Waveform 1. Inverting


V_IN
V_M
V_M
t_PLH
t_PHL
V_OUT
V_M
V_M
WF06069S

Waveform 2. Non-Inverting


OE
V_M
V_M
t_PZH
t_PHZ
V_OH − 0.3V
Y OR Y
V_M
0V
WF06095S

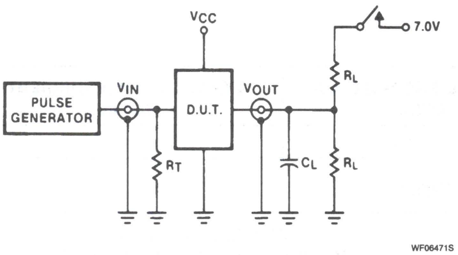
Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time from High Level


OE
V_M
V_M
t_PZL
t_PLZ
3.5V
Y OR Y
V_M
V_OL + 0.3V
WF06075S

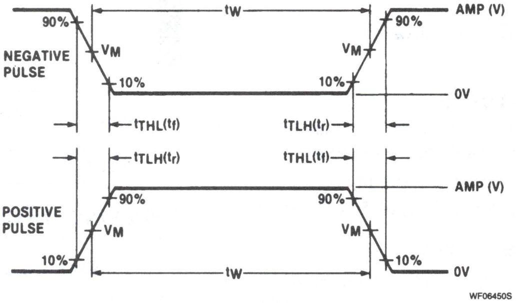
Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

NOTE: $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORMS


VCC
7.0V
RL
VIN
VOUT
PULSE GENERATOR
D.U.T.
RT
CL
RL
WF06471S

Test Circuit for 3-State Outputs


90%
tW
90%
AMP (V)
NEGATIVE PULSE
VM
VM
10%
10%
0V
tTHL(tf)
tTLH(tr)
tTLH(tr)
tTHL(tf)
AMP (V)
90%
90%
POSITIVE PULSE
VM
VM
10%
10%
0V
tW
WF06450S

$V_M = 1.5V$

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F253
Multiplexer

Dual 4-Input Multiplexer (3-State)
Product Specification

FAST Products

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F253	7.0ns	12mA

FEATURES
- **3-State outputs for bus interface and multiplex expansion**
- **Common Select inputs**
- **Separate Output Enable inputs**

DESCRIPTION
The 'F253 has two identical 4-input multiplexers with 3-State outputs which select two bits from four sources selected by common Select inputs (S_0, S_1). When the individual Output Enable ($\overline{E}_{0a}$, $\overline{E}_{0b}$) inputs of the 4-input multiplexers are High, the outputs are forced to a High-impedance (Hi-Z) state.

The 'F253 is the logic implementation of a 2-pole, 4-position switch; the position of the switch being determined by the logic levels supplied to the two Select inputs.

To avoid exceeding maximum current ratings when the outputs of the 3-State devices are tied together, all but one device must be in the High-impedance state. Therefore, only one Output Enable must be active at a time.

ORDERING INFORMATION

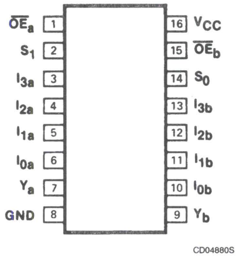
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ± 10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F253N
16-Pin Plastic SO	N74F253D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

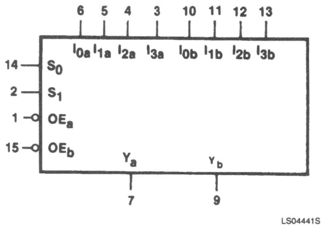
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$I_{0a} - I_{3a}$	Port A data inputs	1.0/1.0	20μA/0.6mA
$I_{0b} - I_{3b}$	Port B data inputs	1.0/1.0	20μA/0.6mA
S_0, S_1	Common select inputs	1.0/1.0	20μA/0.6mA
$\overline{OE}_a$	Port A output enable input (active-Low)	1.0/1.0	20μA/0.6mA
$\overline{OE}_b$	Port B output enable input (active-Low)	1.0/1.0	20μA/0.6mA
Y_a, Y_b	3-State outputs	150/40	3.0mA/24mA

NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION

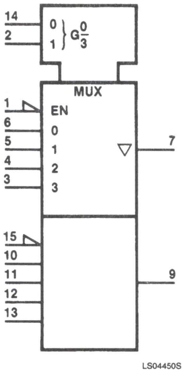

OEa 1
S1 2
I3a 3
I2a 4
I1a 5
I0a 6
Ya 7
GND 8
16 VCC
15 OEb
14 S0
13 I3b
12 I2b
11 I1b
10 I0b
9 Yb
CD04880S

LOGIC SYMBOL


6 5 4 3 10 11 12 13
I0a I1a I2a I3a I0b I1b I2b I3b
14 S0
2 S1
1 OEa
15 OEb
Ya
Yb
7
9
LS04441S

V_{CC} = Pin 16
GND = Pin 8

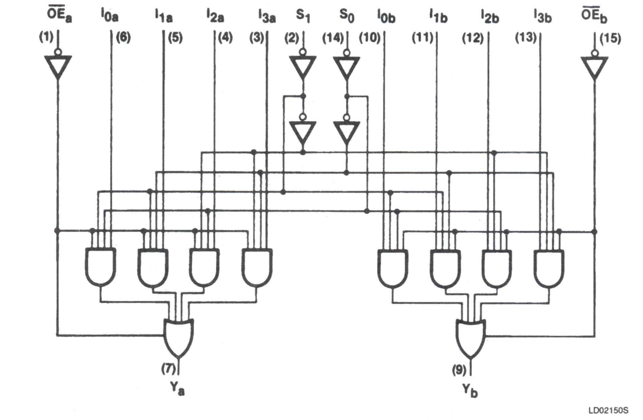
LOGIC SYMBOL (IEEE/IEC)


14
2
0
1
G 0/3
MUX
1
EN
6
0
5
1
4
2
3
3
7
15
10
11
12
13
9
LS04450S

Multiplexer

FAST 74F253

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8

FUNCTION TABLE

INPUTS						OUTPUT	
S_0	S_1	I_0	I_1	I_2	I_3	$\overline{OE}$	Y
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
H	L	X	L	X	X	L	L
H	L	X	H	X	X	L	H
L	H	X	X	L	X	L	L
L	H	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

H = High voltage level
L = Low voltage level
X = Don't care
Z = High-impedence (OFF) state

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_A	Operating free-air temperature range	0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−3	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		74F253			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.4			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				−0.6	mA
I_{OZH}	Off-state output current, High-level voltage applied		V_{CC} = MAX, V_O = 2.7V				50	μA
I_{OZL}	Off-state output current Low-level voltage applied		V_{CC} = MAX, V_O = 0.5V				−50	μA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	$\overline{OE}_n$ = GND; $S_n = I_n$ = 4.5V		10	16	mA
		I_{CCL}		$\overline{OE}_n = S_n = I_n$ = GND		12	23	mA
		I_{CCZ}		$\overline{OE}_n$ = 4.5; $I_n = S_n$ = GND		14	23	mA

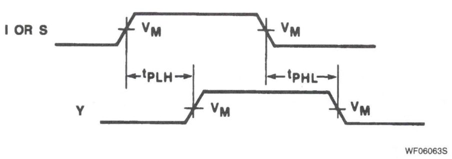
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

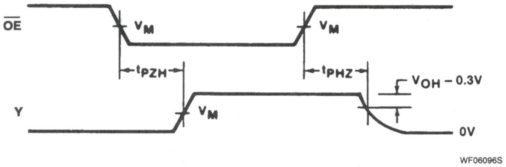
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F253					UNIT
			T_A = +25°C V_{CC} = +5.0V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay Data to output	Waveform 1	3.0 3.0	4.5 5.0	7.0 7.0	3.0 3.0	7.5 8.0	ns
t_{PLH} t_{PHL}	Propagation delay Select to output	Waveform 1	4.5 5.0	7.5 8.5	10.5 11.0	4.5 4.5	11.0 12.0	ns
t_{PZH}	Output enable time to High level	Waveform 2	3.0	6.5	8.0	3.0	9.0	ns
t_{PZL}	Output enable time to Low level	Waveform 3	3.0	6.5	8.0	3.0	9.0	ns
t_{PHZ}	Output disable time from High level	Waveform 2, Waveform 3	2.5	3.5	5.0	2.0	6.0	ns
t_{PLZ}	Output disable time from Low level	Waveform 3, Waveform 4	2.0	3.0	5.0	1.5	6.0	ns

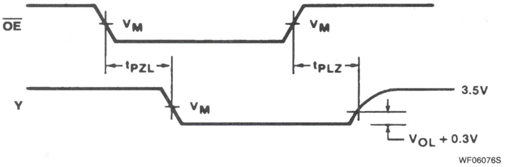
AC WAVEFORMS


I OR S
VM
VM
tPLH
tPHL
Y
VM
VM
WF06063S

Waveform 1. Propagation Delay Data and Select to Output


OE
VM
VM
tPZH
tPHZ
VOH – 0.3V
Y
VM
0V
WF06096S

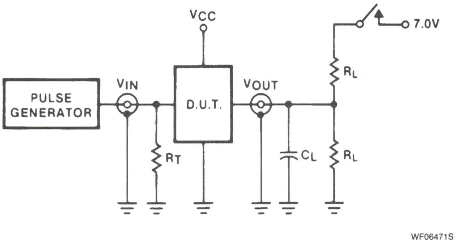
Waveform 2. 3-State Output Enable Time to High Level and Output Disable Time from High Level


OE
VM
VM
tPZL
tPLZ
Y
VM
3.5V
VOL + 0.3V
WF06076S

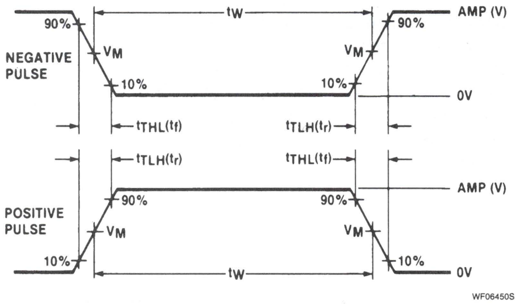
Waveform 3. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

NOTE: For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORM


VCC
7.0V
RL
PULSE GENERATOR
VIN
D.U.T.
VOUT
RT
CL
RL
WF06471S

Test Circuit for 3-State Outputs


tW
AMP (V)
90%
90%
NEGATIVE PULSE
VM
VM
10%
10%
0V
tTHL(tf)
tTLH(tr)
tTLH(tr)
tTHL(tf)
AMP (V)
90%
90%
POSITIVE PULSE
VM
VM
10%
10%
tW
0V
WF06450S

$V_M = 1.5V$

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F256
Latch

Product Specification

FAST Products

FEATURES

- Combines dual demultiplexer and 8-bit latch
- Serial-to-parallel capability
- Output from each storage bit available
- Random (addressable) data entry
- Easily expandable
- Common Clear input
- Useful as dual 1-of-4 active-High decoder

DESCRIPTION

The 'F256 dual addressable latch has four distinct modes of operation which are selectable by controlling the Master Reset and Enable inputs (see Function Table). In the addressable latch mode, data at the Data (D) inputs is written into the addressed latches. The addressed latches will follow the Data input with all unaddressed latches remaining in their previous states. In the memory mode, all latches remain in their previous states and are unaffected by the Data or Address inputs.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F256	7.0ns	28mA

ORDERING INFORMATION

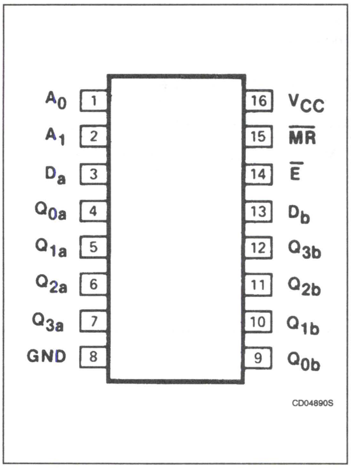
PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
16-Pin Plastic DIP	N74F256N
16-Pin Plastic SO	N74F256D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_a, D_b	Port A, side B data inputs	1.0/1.0	20μA/0.6mA
A_0, A_1	Address inputs	1.0/1.0	20μA/0.6mA
$\overline{E}$, $\overline{MR}$	Enable, Master Reset inputs	1.0/1.0	20μA/0.6mA
$Q_{0a} - Q_{3a}$	Port A outputs	50/33	1mA/20mA
$Q_{0b} - Q_{3b}$	Port B outputs	50/33	1mA/20mA

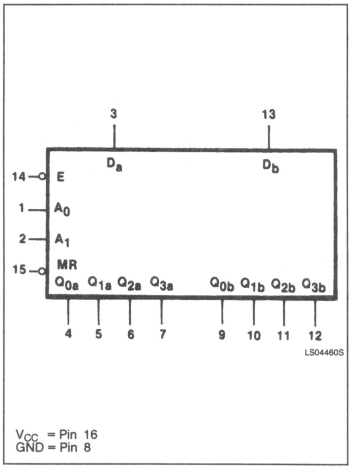
NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



A0 1
A1 2
Da 3
Q0a 4
Q1a 5
Q2a 6
Q3a 7
GND 8
16 VCC
15 MR
14 E
13 Db
12 Q3b
11 Q2b
10 Q1b
9 Q0b
CD04890S

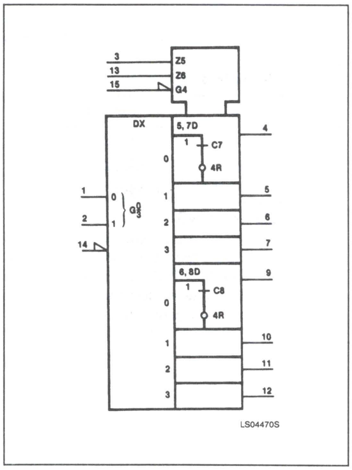
LOGIC SYMBOL



3
13
Da
Db
14 E
1 A0
2 A1
15 MR
Q0a Q1a Q2a Q3a Q0b Q1b Q2b Q3b
4 5 6 7 9 10 11 12
LS04460S

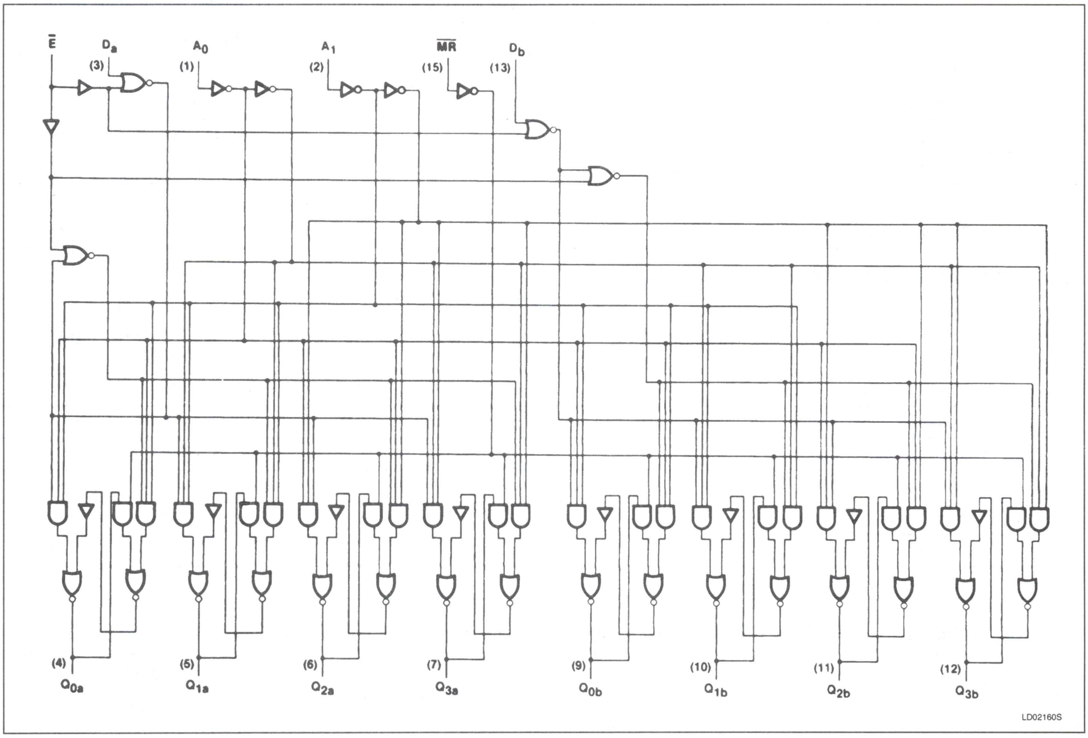
V_{CC} = Pin 16
GND = Pin 8

LOGIC SYMBOL (IEEE/IEC)



3
13
15
Z5
Z6
G4
DX
5, 7D
1
C7
4R
0
1
2
3
1
2
14
G0/3
4
5
6
7
6, 8D
C8
9
10
11
12
LS04470S

LOGIC DIAGRAM



MODE SELECT — FUNCTION TABLE

OPERATING MODE	INPUTS					OUTPUTS			
	$\overline{MR}$	$\overline{E}$	D	A_0	A_1	Q_0	Q_1	Q_2	Q_3
Master reset	L	H	X	X	X	L	L	L	L
Demultiplex (active-High decoder when D = H)	L	L	D	L	L	Q = D	L	L	L
	L	L	d	H	L	L	Q = d	L	L
	L	L	d	L	H	L	L	Q = d	L
	L	L	D	H	H	L	L	L	Q = D
Store (do nothing)	H	H	X	X	X	q_0	q_1	q_2	q_3
Addressable latch	H	L	d	L	L	Q = d	q_1	q_2	q_3
	H	L	d	H	L	q_0	Q = d	q_2	q_3
	H	L	d	L	H	q_0	q_1	Q = d	q_3
	H	L	D	H	H	Q_0	Q_1	Q_2	Q = D

H = High voltage level steady state.
L = Low voltage level steady state.
X = Don't care
d = High or Low data one setup time prior to the Low-to-High Enable transition.
q = Lower case letters indicate the state of the referenced output established during the last cycle in which it was addressed or cleared.

To eliminate the possibility of entering erroneous data in the latches, the enable should be held High (inactive) while the address lines are changing. In the dual 1-of-4 decoding or demultiplexing mode ($\overline{MR}$ = $\overline{E}$ = Low), addressed outputs will follow the level of the D inputs, with all other outputs Low. In the Master Reset mode, all outputs are Low and unaffected by the Address and Data inputs.

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		74F256			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				−0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			21	42	mA
		I_{CCL}				33	60	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequences of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F256					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	Waveform 2	4.0 3.0	7.0 5.0	9.5 7.0	4.0 2.5	10.0 7.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to Q_n	Waveform 1	4.5 3.0	8.0 5.0	10.5 7.0	4.5 3.0	12.0 7.5	ns
t_{PLH} t_{PHL}	Propagation delay A_n to Q_n	Waveform 3	5.0 4.5	10.0 8.5	14.0 9.5	5.0 4.0	14.5 10.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	Waveform 4	5.0	7.0	9.0	4.5	10.0	ns

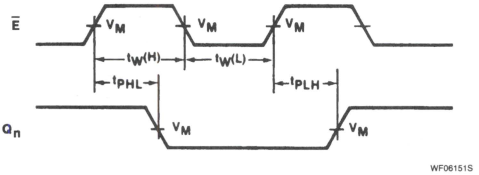
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	74F256					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to $\overline{E}$	Waveform 5	3.0 6.5			3.0 7.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to $\overline{E}$	Waveform 5	0 0			0 0		ns
t_s	Setup time, High or Low A_n to $\overline{E}^1$	Waveform 6	2.0			2.0		ns
t_g	Hold time, High or Low A_n to $\overline{E}^2$	Waveform 6	0			0		ns
t_w	$\overline{E}$ pulse width	Waveform 1	7.5			8.0		ns
t_w	$\overline{MR}$ pulse width	Waveform 4	3.0			3.0		ns

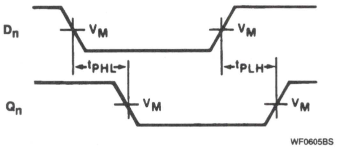
NOTES:

1. The Address to Enable setup time is the time before the High-to-Low Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.
2. The Address to Enable hold time is the time before the Low-to-High Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.

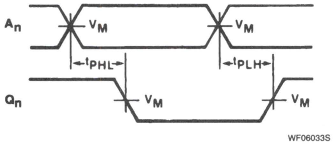
AC WAVEFORMS


Ē
Qn
VM
VM
VM
VM
VM
tW(H)
tW(L)
tPHL
tPLH
WF06151S

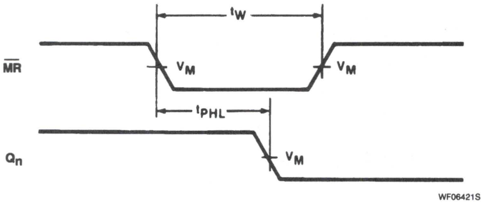
Waveform 1. Propagation Delay Enable to Output and Enable Pulse Width


Dn
Qn
VM
VM
VM
VM
tPHL
tPLH
WF0605BS

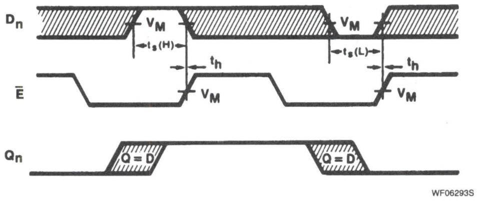
Waveform 2. Propagation Delay Data to Output


An
Qn
VM
VM
VM
VM
tPHL
tPLH
WF06033S

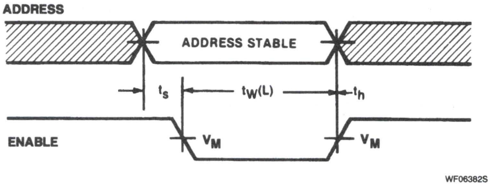
Waveform 3. Propagation Delay Address to Output


MR̄
Qn
tW
VM
VM
tPHL
VM
WF06421S

Waveform 4. Master Reset to Output Delay and Master Reset Pulse Width


Dn
Ē
Qn
VM
VM
ts(H)
ts(L)
th
th
VM
VM
Q = D
Q = D
WF06293S

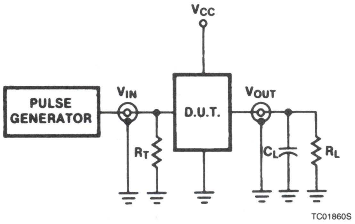
Waveform 5. Data Setup and Hold Times


ADDRESS
ADDRESS STABLE
ts
tW(L)
th
ENABLE
VM
VM
WF06382S

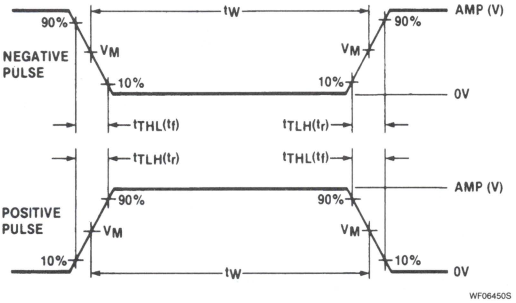
Waveform 6. Address Setup and Hold Times

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORM


VCC
PULSE GENERATOR
VIN
D.U.T.
VOUT
RT
CL
RL
TC01860S

Test Circuit for Totem-Pole Outputs


90%
tW
90%
AMP (V)
NEGATIVE PULSE
VM
VM
10%
10%
0V
tTHL(tf)
tTLH(tr)
tTLH(tr)
tTHL(tf)
AMP (V)
90%
90%
POSITIVE PULSE
VM
VM
10%
tW
10%
0V
WF06450S

$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

FAST 74F257A
Data Selector/Multiplexer

Quad 2-Line To 1-Line Data Selector Multiplexer (3-State)
Product Specification

FEATURES

- **Multifunction capability**
- **Non-inverting data path**
- **3-State outputs**
- **See 'F258A for inverting version**

DESCRIPTION

The 'F257A has four identical 2-input multiplexers with 3-State outputs which select 4 bits of data from two sources under control of a common Data Select input (S). The I_0 inputs are selected when the Select input is Low and the I_1 inputs are selected when the Select input is High. Data appears at the outputs in true (non-inverted) form from the selected outputs.

The 'F257A is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input.

Outputs are forced to a High-impedance "OFF" state when the Output Enable input ($\overline{OE}$) is High. All but one device must be in the High-impedance state to avoid currents exceeding the maximum ratings if outputs are tied together. Design of the output enable signals must ensure that there is no overlap when outputs of 3-State devices are tied together.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F257A	4.3ns	12mA

ORDERING INFORMATION

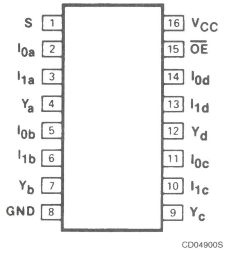
PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
16-Pin Plastic DIP	N74F257N
16-Pin Plastic SO	N74F257D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

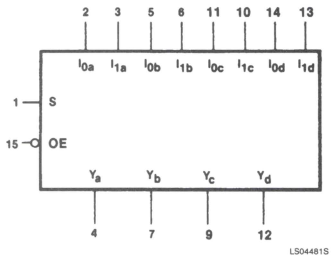
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I_{0n}, I_{1n}	Data inputs	1.0/1.0	20μA/0.6mA
S	Common select input	1.0/1.0	20μA/0.6mA
$\overline{OE}$	Enable input (Active-Low)	1.0/1.0	20μA 0.6mA
$Y_a - Y_d$	Data outputs	50/33	1.0mA/20mA

NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION

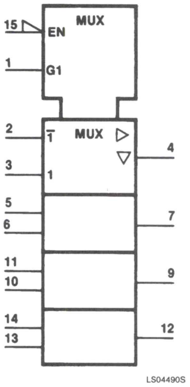

S 1
I0a 2
I1a 3
Ya 4
I0b 5
I1b 6
Yb 7
GND 8
16 VCC
15 OE
14 I0d
13 I1d
12 Yd
11 I0c
10 I1c
9 Yc
CD04900S

LOGIC SYMBOL


2
3
5
6
11
10
14
13
I0a
I1a
I0b
I1b
I0c
I1c
I0d
I1d
1
S
15
OE
Ya
Yb
Yc
Yd
4
7
9
12
LS04481S

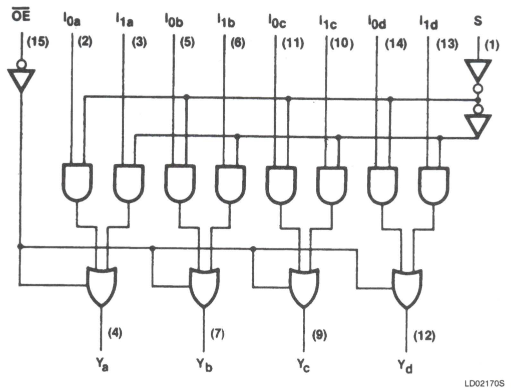
V_{CC} = Pin 16
GND = Pin 8

LOGIC SYMBOL (IEEE/IEC)


15
EN
MUX
1
G1
2
1̄
MUX
4
3
1
5
6
7
11
10
9
14
13
12
LS04490S

Data Selector/Multiplexer FAST 74F257A

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8

FUNCTION TABLE

INPUTS				OUTPUT
$\overline{OE}$	S	I_0	I_1	Y
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = High voltage level
L = Low voltage level
X = Don't care
Z = High-impedance (OFF) state

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_A	Operating free-air temperature range	0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−3.0	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature	0		70	°C

Data Selector/Multiplexer FAST 74F257A

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		74F257A			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX V_{IH} = MIN,	±10%V_{CC}	2.4			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OL} = MAX V_{IH} = MIN,	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				−0.6	mA
I_{OZH}	Off-state output current, High-level voltage applied		V_{CC} = MAX, V_O = 2.7V				50	μA
I_{OZL}	Off-state output current Low-level voltage applied		V_{CC} = MAX, V_O = 0.5V				−50	μA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX,		−60		−150	mA
I_{CC}	Supply current [4] (total)	I_{CCH}	V_{CC} = MAX			9.0	15.0	mA
		I_{CCL}				14.5	22.0	mA
		I_{CCZ}				15.0	23.0	mA

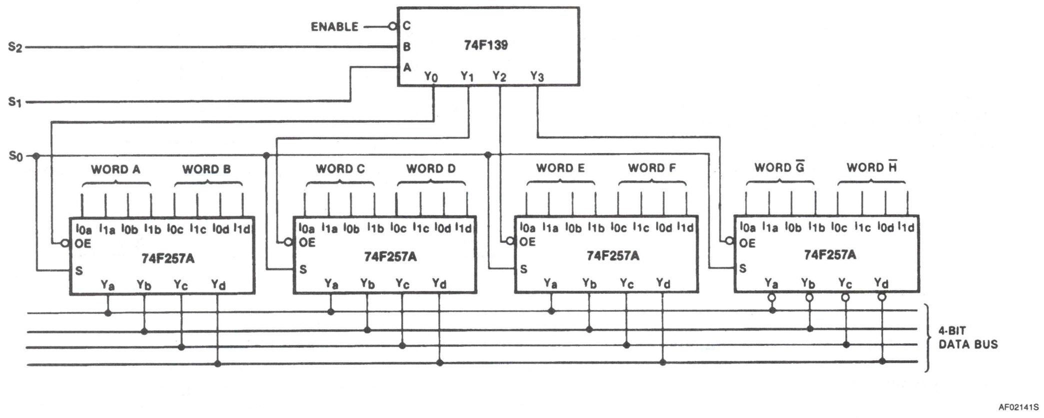
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Measure I_{CC} with all outputs open and inputs grounded.

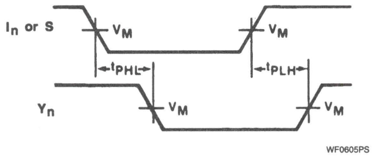
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F257A					UNIT
			T_A = +25°C V_{CC} = +5.0V C_L = 50pF R_L = 500Ω			T_A = 0 to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_{na}, I_{nb} to Y_n	Waveform 1	3.0 2.0	4.5 3.5	6.0 5.0	3.0 2.0	7.0 6.0	ns
t_{PLH} t_{PHL}	Propagation delay S to Y_n	Waveform 1	5.5 4.0	7.5 5.5	9.5 7.0	5.0 4.0	10.5 8.0	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level	Waveform 2 Waveform 3	4.5 4.5	6.5 6.0	7.5 7.5	4.5 4.5	8.5 8.5	ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low	Waveform 2 Waveform 3	2.0 2.0	4.0 3.5	5.5 5.5	2.0 2.0	6.0 6.0	ns

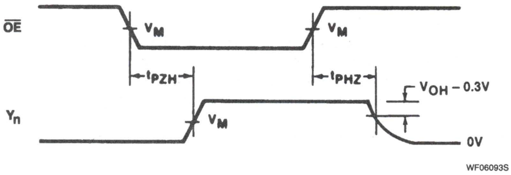
APPLICATIONS


ENABLE
C
B
A
74F139
Y0 Y1 Y2 Y3
S2
S1
S0
WORD A
WORD B
WORD C
WORD D
WORD E
WORD F
WORD G̅
WORD H̅
I0a I1a I0b I1b I0c I1c I0d I1d
OE
S
74F257A
Ya Yb Yc Yd
4-BIT DATA BUS
AF02141S

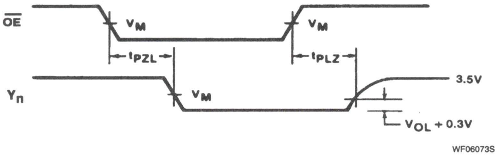
AC WAVEFORMS


In or S
VM
VM
tPHL
tPLH
Yn
VM
VM
WF0605PS

Waveform 1. Propagation Delay Data and Select to Output


OE
VM
VM
tPZH
tPHZ
VOH − 0.3V
Yn
VM
0V
WF06093S

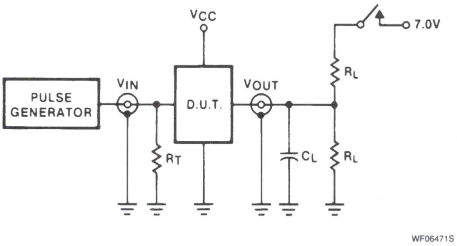
Waveform 2. 3-State Output Enable Time to High Level and Output Disable Time From High Level


OE
VM
VM
tPZL
tPLZ
Yn
VM
3.5V
VOL + 0.3V
WF06073S

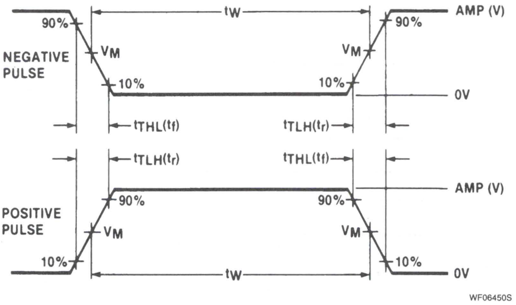
Waveform 3. 3-State Enable Time to Low Level and Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORMS


VCC
7.0V
RL
PULSE GENERATOR
VIN
D.U.T.
VOUT
RT
CL
RL
WF06471S

Test Circuit for 3-State Outputs


tw
AMP (V)
90%
NEGATIVE PULSE
VM
10%
0V
tTHL(tf)
tTLH(tr)
POSITIVE PULSE
90%
VM
10%
AMP (V)
0V
WF06450S

$V_M = 1.5V$

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PZH}	open
t_{PZL}	closed
t_{PHZ}	open
t_{PLZ}	closed

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F258A
Data Selector/Multiplexer

Quad 2-Line To 1-Line Data Selector/Multiplexer (3-State)
Product Specification

FAST Products

FEATURES
- **Multifunction capability**
- **Inverting data path**
- **3-State outputs**
- **See 'F257A for non-inverting version**

DESCRIPTION
The 'F258A has four identical 2-input multiplexers with 3-State outputs which select 4 bits of data from two sources under control of a common Select input (S). The I_{0n} inputs are selected when the Select input is Low and the I_{1n} inputs are selected when the Select input is High. Data appears at the outputs in inverted form from the selected outputs.

The 'F258A is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic level supplied to the Select input. Outputs are forced to a High-impedance "OFF" state when the Output Enable input ($\overline{OE}$) is High. All but one device must be in the High-impedance state to avoid currents exceeding the maximum ratings if outputs are tied together.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F258A	3.5ns	14mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0°C$ to $+70°C$
16-Pin Plastic DIP	N74F258AN
16-Pin Plastic SO	N74F258AD

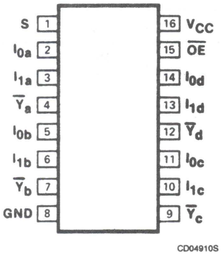
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I_{0n}, I_{1n}	Data inputs	1.0/1.0	20μA/0.6mA
S	Common select input	1.0/1.0	20μA/0.6mA
$\overline{OE}$	Enable input (active-Low)	1.0/1.0	20μA/0.6mA
$\overline{Y}a$-$\overline{Y}d$	Data outputs	50/40	1.0mA/24mA

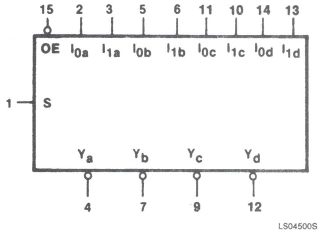
NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

Design of the output signals must ensure that there is no overlap when outputs of 3-State devices are tied together.

PIN CONFIGURATION

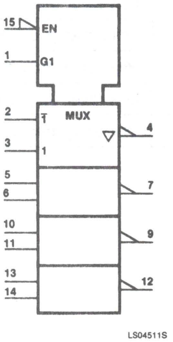

S 1
I0a 2
I1a 3
Ȳa 4
I0b 5
I1b 6
Ȳb 7
GND 8
16 VCC
15 OE
14 I0d
13 I1d
12 Ȳd
11 I0c
10 I1c
9 Ȳc
CD04910S

LOGIC SYMBOL


15
2
3
5
6
11
10
14
13
OE
I0a
I1a
I0b
I1b
I0c
I1c
I0d
I1d
1
S
Ya
Yb
Yc
Yd
4
7
9
12
LS04500S

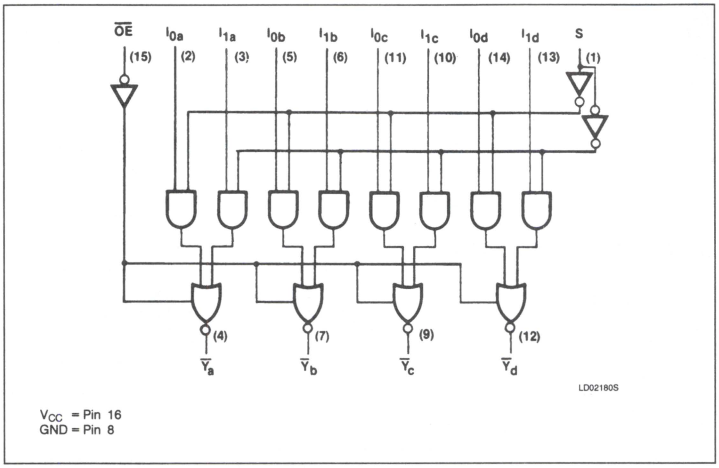
V_{CC} = Pin 16
GND = Pin 8

LOGIC SYMBOL (IEEE/IEC)


15
EN
1
G1
2
MUX
4
3
1
5
7
6
10
9
11
13
12
14
LS04511S

Data Selector/Multiplexer FAST 74F258A

LOGIC DIAGRAM


$\overline{OE}$
I_{0a}
I_{1a}
I_{0b}
I_{1b}
I_{0c}
I_{1c}
I_{0d}
I_{1d}
S
(15)
(2)
(3)
(5)
(6)
(11)
(10)
(14)
(13)
(1)
(4)
(7)
(9)
(12)
$\overline{Y}_a$
$\overline{Y}_b$
$\overline{Y}_c$
$\overline{Y}_d$
LD02180S
V_{CC} = Pin 16
GND = Pin 8

FUNCTION TABLE

OUTPUT ENABLE	SELECT INPUT	DATA INPUTS		OUTPUTS
$\overline{OE}$	S	I_0	I_1	$\overline{Y}$
H	X	X	X	Z
L	H	X	L	H
L	H	X	H	L
L	L	L	X	H
L	L	H	X	L

H = High voltage level
L = Low voltage level
X = Don't care
Z = High-impedance (OFF) state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_A	Operating free-air temperature range	0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−3	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		74F258A			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.4			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.35	0.5	V
				±5%V_{CC}		0.35	0.5	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OZH}	Off-state output current, High-level voltage applied		V_{CC} = MAX, V_O = 2.7V				50	μA
I_{OZL}	Off-state output current, Low-level voltage applied		V_{CC} = MAX, V_O = 0.5V				-50	μA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	I_{1n} = 4.5V, $\overline{OE} = I_{0n}$ = S = GND		8.5	11.5	mA
		I_{CCL}		I_{1n} = S = 4.5V, $\overline{OE} = I_{0n}$ = GND		17.0	23.0	mA
		I_{CCZ}		$I_{1n} = \overline{OE}$ = 4.5V, I_{0n} = S = GND		16.0	22.0	mA

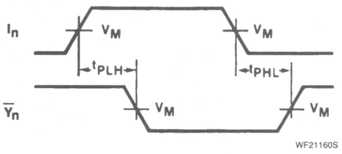
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

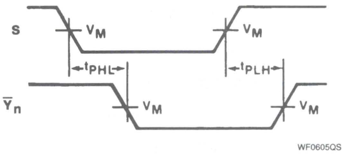
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F258A					UNIT
			T_A = +25°C V_{CC} = +5.0V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH}	Propagation delay	Waveform 1	3.0	4.5	6.0	2.5	7.0	ns
t_{PHL}	I_n to $\overline{Y}_n$		1.0	2.5	4.0	1.0	4.5	
t_{PLH}	Propagation delay	Waveform 1, 2	3.5	6.5	8.0	3.5	9.0	ns
t_{PHL}	S to $\overline{Y}_n$		2.5	6.0	8.0	2.5	9.0	
t_{PZH}	Output enable time	Waveform 3	4.0	6.0	7.5	3.5	8.5	ns
t_{PZL}	to High or Low level	Waveform 4	4.0	5.5	7.5	3.5	8.5	
t_{PHZ}	Output disable time	Waveform 3	2.0	3.5	5.5	2.0	6.5	ns
t_{PLZ}	from High or Low level	Waveform 4	2.0	3.5	5.5	2.0	6.0	

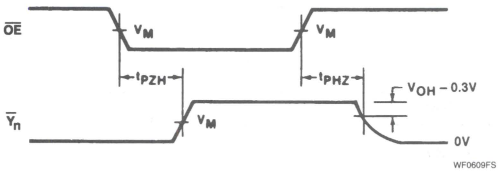
AC WAVEFORMS


In
VM
VM
tPLH
tPHL
Yn
VM
VM
WF21160S

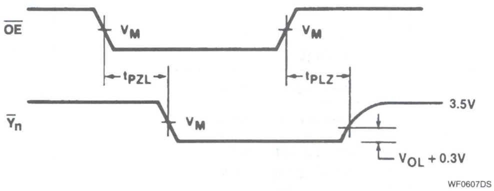
Waveform 1. Propagation Delay Data (I_n) to Output ($\overline{Y}_n$)


S
VM
VM
tPHL
tPLH
Yn
VM
VM
WF0605QS

Waveform 2. Propagation Delay Select (S) to Output ($\overline{Y}_n$)


OE
VM
VM
tPZH
tPHZ
VOH – 0.3V
Yn
VM
0V
WF0609FS

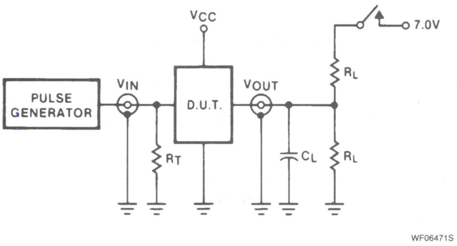
Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time From High Level


OE
VM
VM
tPZL
tPLZ
3.5V
Yn
VM
VOL + 0.3V
WF0607DS

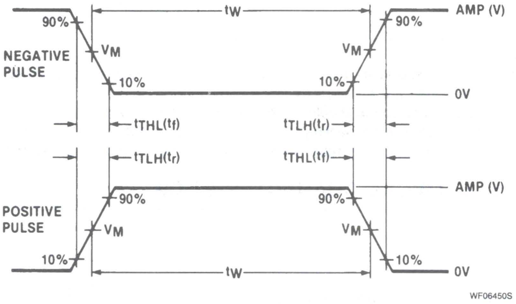
Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORM


VCC
7.0V
RL
PULSE GENERATOR
VIN
D.U.T.
VOUT
RT
CL
RL
WF06471S

Test Circuit for 3-State Outputs


90%
tW
90%
AMP (V)
NEGATIVE PULSE
VM
VM
10%
10%
0V
tTHL(tf)
tTLH(tr)
tTLH(tr)
tTHL(tf)
AMP (V)
90%
90%
POSITIVE PULSE
VM
VM
10%
10%
tW
0V
WF06450S

$V_M = 1.5V$

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F259
Latch

8-Bit Addressable Latch
Product Specification

FAST Products

FEATURES

- **Combines demultiplexer and 8-bit latch**
- **Serial-to-parallel capability**
- **Output from each storage bit available**
- **Random (addressable) data entry**
- **Easily expandable**
- **Common Clear input**
- **Useful as a 1-of-8 active-High decoder**

DESCRIPTION

The 'F259 addressable latch has four distinct modes of operation that are selectable by controlling the Master Reset and Enable inputs (see Function Table). In the addressable latch mode, data at the Data (D) inputs is written into the addressed latches. The addressed latches will follow the Data input with all unaddressed latches remaining in their previous states. In the store mode, all latches remain in their previous states and are unaffected by the Data or Address inputs.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F259	7.5ns	31mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
16-Pin Plastic DIP	N74F259N
16-Pin Plastic SO	N74F259D

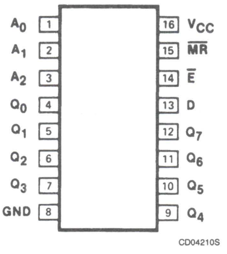
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$\overline{MR}$, $\overline{E}$	Master Reset, Enable inputs	1.0/1.0	20μA/0.6mA
A_0, A_2	Address inputs	1.0/1.0	20μA/0.6mA
D	Data input	1.0/1.0	20μA/0.6mA
$Q_0 - Q_7$	Outputs	50/33	1mA/20mA

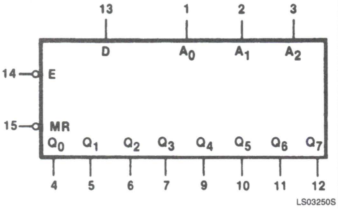
NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

To eliminate the possibility of entering erroneous data in the latches, the enable should be held High (inactive) while the address lines are changing. In the 1-of-8 decoding or demultiplexing mode ($\overline{MR} = \overline{E} =$ Low), addressed outputs will follow the level of the D inputs, with all other outputs Low. In the Master Reset mode, all outputs are Low and unaffected by the Address and Data inputs.

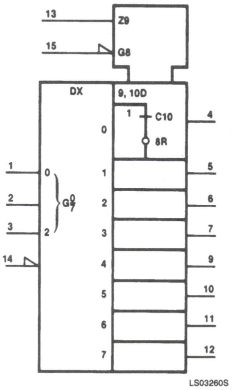
PIN CONFIGURATION


A0 1
A1 2
A2 3
Q0 4
Q1 5
Q2 6
Q3 7
GND 8
16 VCC
15 $\overline{MR}$
14 $\overline{E}$
13 D
12 Q7
11 Q6
10 Q5
9 Q4
CD04210S

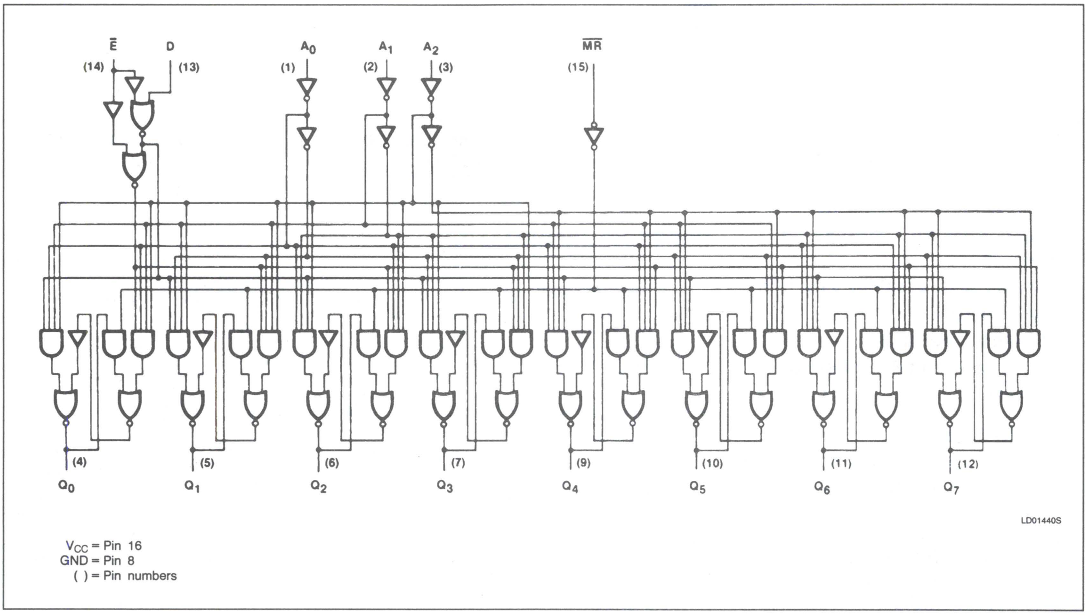
LOGIC SYMBOL


13
1
2
3
D
A0
A1
A2
14 E
15 MR
Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
4 5 6 7 9 10 11 12
LS03250S

LOGIC SYMBOL (IEEE/IEC)


13
15
Z9
G8
DX
9, 10D
1
C10
8R
0
1
2
G0/7
1
2
3
14
0 1 2 3 4 5 6 7
4 5 6 7 9 10 11 12
LS03260S

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
( ) = Pin numbers

MODE SELECT — FUNCTION TABLE

OPERATING MODE	INPUTS						OUTPUTS							
	$\overline{MR}$	$\overline{E}$	D	A_0	A_1	A_2	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7
Master Reset	L	H	X	X	X	X	L	L	L	L	L	L	L	L
Demultiplex (active-High decoder when D = H)	L	L	d	L	L	L	Q = d	L	L	L	L	L	L	L
	L	L	d	H	L	L	L	Q = d	L	L	L	L	L	L
	L	L	d	L	H	L	L	L	Q = d	L	L	L	L	L
	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
	L	L	d	H	H	H	L	L	L	L	L	L	L	Q = d
Store (do nothing)	H	H	X	X	X	X	q_0	q_1	q_2	q_3	q_4	q_5	q_6	q_7
Addressable latch	H	L	d	L	L	L	Q = d	q_1	q_2	q_3	q_4	q_5	q_6	q_7
	H	L	d	H	L	L	q_0	Q = d	q_2	q_3	q_4	q_5	q_6	q_7
	H	L	d	L	H	L	q_0	q_1	Q = d	q_3	q_4	q_5	q_6	q_7
	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
	H	L	d	H	H	H	q_0	q_1	q_2	q_3	q_4	q_5	q_6	Q = d

H = High voltage level steady state.
L = Low voltage level steady state.
X = Don't care.
d = High or Low data one setup time prior to the Low-to-High Enable transition.
q = Lower case letters indicate the state of the referenced output established during the last cycle in which it was addressed or cleared.

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		74F259			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX V_{IH} = MIN,	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OL} = MAX V_{IH} = MIN,	±10%V_{CC}		.35	.50	V
				±5%V_{CC}		.35	.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				−0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			24	46	mA
		I_{CCL}				37	75	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F259					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D to Q_n	Waveform 2	4.0 3.0	7.0 5.0	9.0 7.0	4.0 2.5	10.0 7.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to Q_n	Waveform 1	4.5 3.0	8.0 5.0	10.5 7.0	4.5 3.0	12.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay A_n to Q_n	Waveform 3	5.0 4.0	10.0 8.5	14.0 9.5	5.0 4.0	14.5 10.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	Waveform 4	5.0	7.0	9.0	4.5	10.0	ns

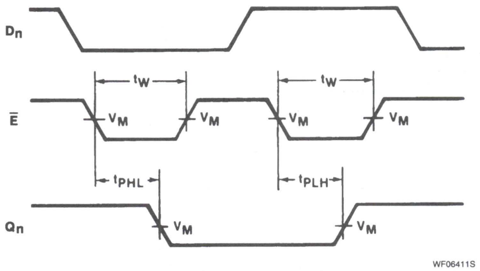
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	74F259					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D to $\overline{E}$	Waveform 5	3.0 6.5			3.0 7.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D to $\overline{E}$	Waveform 5	0 0			0 0		ns
t_s	Setup time, High or Low A_n to $\overline{E}$[1]	Waveform 6	2.0			2.0		ns
t_g	Hold time, High or Low A_n to $\overline{E}$[2]	Waveform 6	0			0		ns
t_w	$\overline{E}$ pulse width	Waveform 1	7.5			8.0		ns
t_w	$\overline{MR}$ pulse width	Waveform 4	3.0			3.0		ns

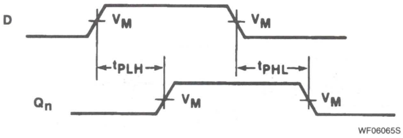
NOTES:

1. The Address to Enable setup time is the time before the High-to-Low Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.
2. The Address to Enable hold time is the time after the Low-to-High Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.

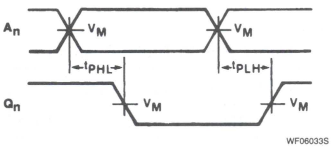
AC WAVEFORMS


Dn
Ē
Qn
tW
tW
VM
tPHL
tPLH
WF06411S

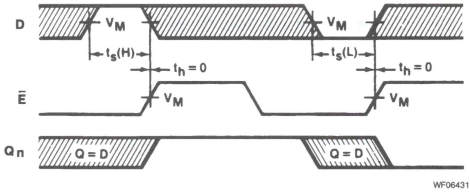
Waveform 1. Propagation Delay Enable to Output and Enable Pulse Width


D
Qn
VM
tPLH
tPHL
WF06065S

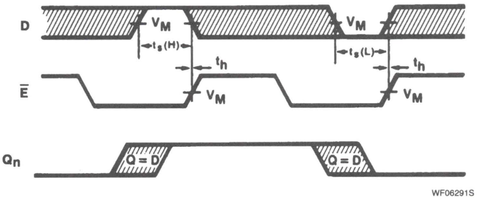
Waveform 2. Propagation Delay Data to Output


An
Qn
VM
tPHL
tPLH
WF06033S

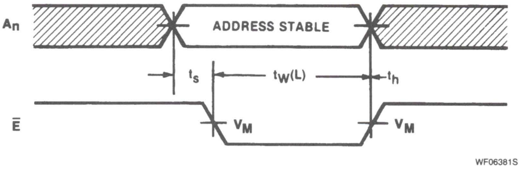
Waveform 3. Propagation Delay Address to Output


D
Ē
Qn
VM
ts(H)
ts(L)
th = 0
th = 0
Q = D
Q = D
WF06431S

Waveform 4. Master Reset to Output Delay and Master Reset Pulse Width


D
Ē
Qn
VM
ts(H)
ts(L)
th
th
Q = D
Q = D
WF06291S

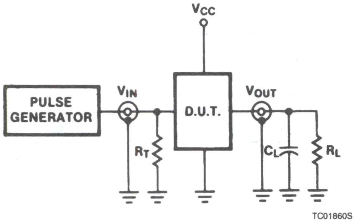
Waveform 5. Data Setup and Hold Times


An
Ē
ADDRESS STABLE
ts
tW(L)
th
VM
WF06381S

Waveform 6. Address Setup and Hold Times

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORM


V_{CC}
PULSE GENERATOR
V_{IN}
D.U.T.
V_{OUT}
R_T
C_L
R_L
TC01860S

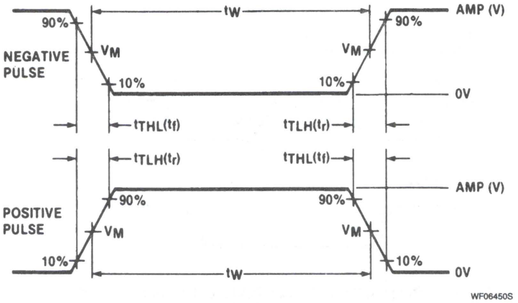
Test Circuit for Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.


tW
90%
AMP (V)
NEGATIVE PULSE
VM
10%
0V
tTHL(tf)
tTLH(tr)
tTLH(tr)
tTHL(tf)
POSITIVE PULSE
90%
VM
10%
tW
WF06450S

V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F260
Gate

Dual 5-Input NOR Gate
Product Specification

FAST Products

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F260	3.5ns	6mA

FUNCTION TABLE

INPUTS					OUTPUT
A	B	C	D	E	$\overline{Y}$
H	X	X	X	X	L
X	H	X	X	X	L
X	X	H	X	X	L
X	X	X	H	X	L
X	X	X	X	H	L
L	L	L	L	L	H

H = High voltage level
L = Low voltage level
X = Don't care

ORDERING INFORMATION

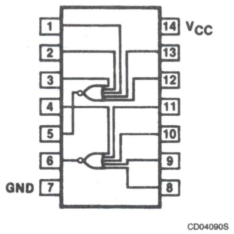
PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
14-Pin Plastic DIP	N74F260N
14-Pin Plastic SO	N74F260D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

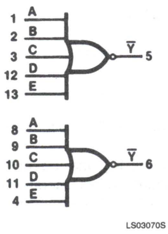
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A – E	Data inputs	1.0/1.0	20μA/0.6mA
$\overline{Y}$	Data outputs	50/33	1mA/20mA

NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

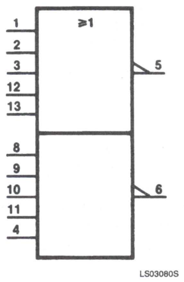
PIN CONFIGURATION


1
2
3
4
5
6
GND 7
14 VCC
13
12
11
10
9
8
CD04090S

LOGIC SYMBOL


1 A
2 B
3 C
12 D
13 E
Y 5
8 A
9 B
10 C
11 D
4 E
Y 6
LS03070S

LOGIC SYMBOL (IEEE/IEC)


≥1
1
2
3
12
13
5
8
9
10
11
4
6
LS03080S

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				−0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_{IN} = GND		4.6	6.5	mA
		I_{CCL}		V_{IN} = 4.5V		7.3	9.5	mA

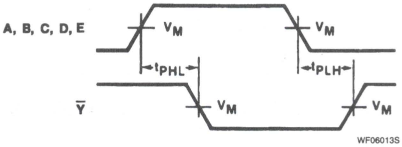
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F260					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A, B, C, D, E to $\overline{Y}$	Waveform 1	2.5 1.5	4.0 2.5	5.5 4.0	2.0 1.0	6.5 4.5	ns

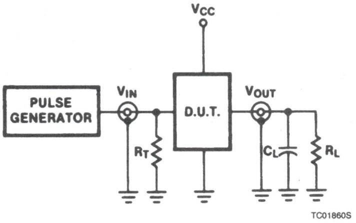
AC WAVEFORM


A, B, C, D, E
V_M
V_M
t_{PHL}
t_{PLH}
$\overline{Y}$
V_M
V_M
WF06013S

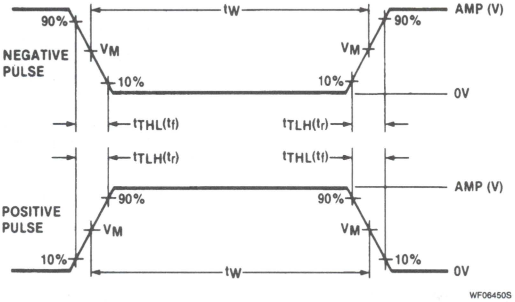
NOTE: For all waveforms, $V_M = 1.5V$.

Waveform 1. Propagation Delay Input to Output

TEST CIRCUIT AND WAVEFORM


V_{CC}
PULSE GENERATOR
V_{IN}
D.U.T.
V_{OUT}
R_T
C_L
R_L
TC01860S

Test Circuit for Totem-Pole Outputs


AMP (V)
90%
90%
t_W
NEGATIVE PULSE
V_M
V_M
10%
10%
0V
$t_{THL}(t_f)$
$t_{TLH}(t_r)$
$t_{TLH}(t_r)$
$t_{THL}(t_f)$
AMP (V)
90%
90%
POSITIVE PULSE
V_M
V_M
10%
10%
t_W
0V
WF06450S

$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS

R_L = Load resistor to GND; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F269
8-Bit Counter

8-Bit Bidirectional Binary Counter
Product Specification

FAST Products

FEATURES

- **Synchronous counting and loading**
- **Built-in look-ahead Carry capability**
- **Count frequency 115MHz typ**
- **Supply current 95mA typ**
- **24-Pin plastic Slim DIP (300mil) package**

DESCRIPTION

The 'F269 is a fully synchronous 8-stage up/down counter featuring a preset capability for programmable operation, Carry look-ahead for easy cascading and a U/$\overline{D}$ input to control the direction of counting. All state changes, whether in counting or parallel loading, are initiated by the rising edge of the clock.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F269	115MHz	95mA

ORDERING INFORMATION

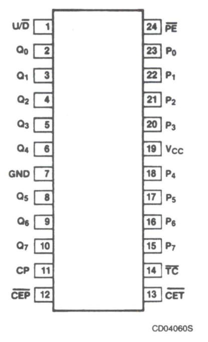
PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
24-Pin Plastic Slim DIP	N74F269N
24-Pin Plastic SOL	N74F269D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

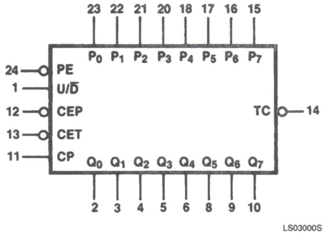
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$P_0 - P_7$	Parallel data inputs	1.0/1.0	20μA/0.6mA
$\overline{PE}$	Parallel enable input (active-Low)	1.0/1.0	20μA/0.6mA
U/$\overline{D}$	Up-Down count control input	1.0/1.0	20μA/0.6mA
$\overline{CEP}$	Count enable parallel input (active-Low)	1.0/1.0	20μA/0.6mA
$\overline{CET}$	Count enable trickle input (active-Low)	1.0/1.0	20μA/0.6mA
CP	Clock input	1.0/1.0	20μA/0.6mA
$\overline{TC}$	Terminal count output (active-Low)	50/33	1mA/20mA
$Q_0 - Q_7$	Flip-flop outputs	50/33	1mA/20mA

NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION

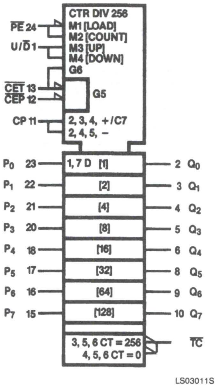

U/D̄ 1
Q0 2
Q1 3
Q2 4
Q3 5
Q4 6
GND 7
Q5 8
Q6 9
Q7 10
CP 11
CEP̄ 12
24 PĒ
23 P0
22 P1
21 P2
20 P3
19 VCC
18 P4
17 P5
16 P6
15 P7
14 TC̄
13 CĒT
CD04060S

LOGIC SYMBOL

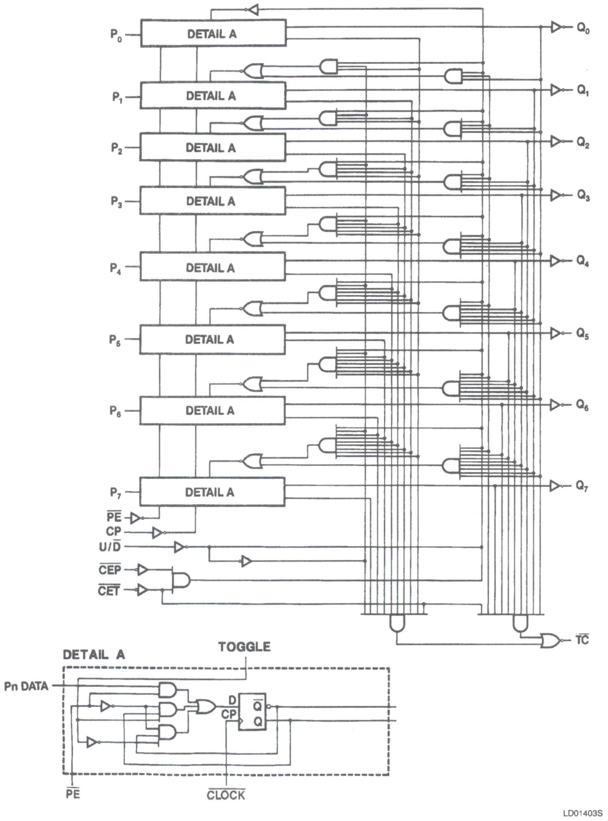

23 22 21 20 18 17 16 15
P0 P1 P2 P3 P4 P5 P6 P7
24 PE
1 U/D̄
12 CEP
13 CET
11 CP
TC 14
Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
2 3 4 5 6 8 9 10
LS03000S

V_{CC} = Pin 19
GND = Pin 7

LOGIC SYMBOL (IEEE/IEC)


CTR DIV 256
M1 [LOAD]
M2 [COUNT]
M3 [UP]
M4 [DOWN]
G6
PĒ 24
U/D̄ 1
CĒT 13
CEP̄ 12
G5
CP 11
2, 3, 4, +/C7
2, 4, 5, −
P0 23
P1 22
P2 21
P3 20
P4 18
P5 17
P6 16
P7 15
1, 7 D [1]
[2]
[4]
[8]
[16]
[32]
[64]
[128]
2 Q0
3 Q1
4 Q2
5 Q3
6 Q4
8 Q5
9 Q6
10 Q7
3, 5, 6 CT = 256
4, 5, 6 CT = 0
TC̄
LS03011S

LOGIC DIAGRAM


P_0
P_1
P_2
P_3
P_4
P_5
P_6
P_7
DETAIL A
Q_0
Q_1
Q_2
Q_3
Q_4
Q_5
Q_6
Q_7
$\overline{PE}$
CP
$U/\overline{D}$
$\overline{CEP}$
$\overline{CET}$
$\overline{TC}$
DETAIL A
TOGGLE
Pn DATA
D
CP
$\overline{Q}$
Q
$\overline{PE}$
$\overline{CLOCK}$
LD01403S

8-Bit Counter

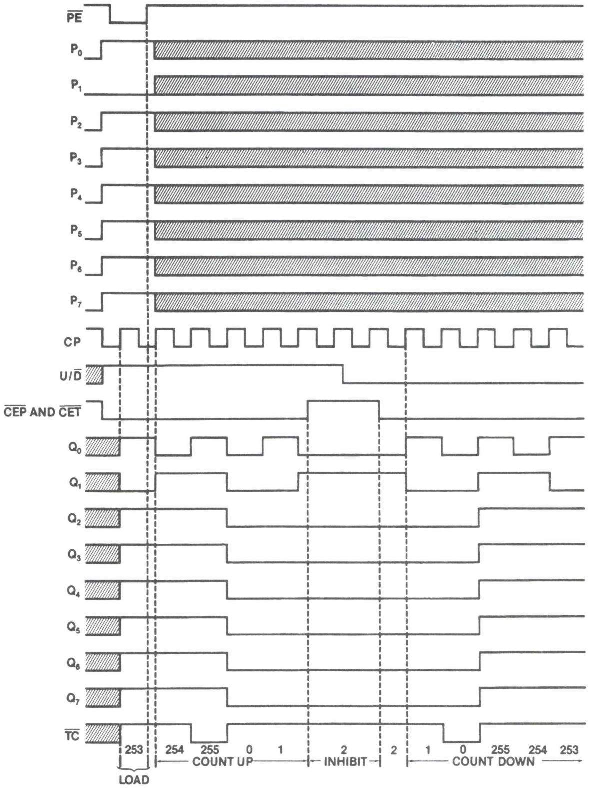
FAST 74F269

FUNCTION TABLE

OPERATING MODE	INPUTS						OUTPUTS	
	CP	U/$\overline{\text{D}}$	$\overline{\text{CEP}}$	$\overline{\text{CET}}$	$\overline{\text{PE}}$	P_n	Q_n	$\overline{\text{TC}}$
Parallel Load	↑ ↑	X X	X X	X X	l l	l h	L H	(a) (a)
Count Up	↑	h	l	l	h	X	Count Up	(a)
Count Down	↑	l	l	l	h	X	Count Down	(a)
Hold (do nothing)	↑ ↑	X X	h X	X h	h h	X X	q_n q_n	(a) H

H = High voltage level steady state
h = High voltage level one setup time prior to the Low-to-High clock transition
L = Low voltage level steady state
l = Low voltage level one setup time prior to the Low-to-High clock transition
X = Don't care
q = Lower case letters indicate the state of the referenced output prior to the Low-to-High clock transition
↑ = Low-to-High clock transition
(a) = The $\overline{\text{TC}}$ is Low when $\overline{\text{CET}}$ is Low and the counter is at Terminal Count. Terminal Count Up is with all Q_n outputs High and Terminal Count Down is with all Q_n outputs Low.

TIMING DIAGRAM


$\overline{\text{PE}}$
P_0
P_1
P_2
P_3
P_4
P_5
P_6
P_7
CP
U/$\overline{\text{D}}$
$\overline{\text{CEP}}$ AND $\overline{\text{CET}}$
Q_0
Q_1
Q_2
Q_3
Q_4
Q_5
Q_6
Q_7
$\overline{\text{TC}}$
253
254
255
0
1
2
2
1
0
255
254
253
COUNT UP
INHIBIT
COUNT DOWN
LOAD
WF06490S

8-Bit Counter FAST 74F269

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.50	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				−0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	$\overline{PE} = \overline{CET} = \overline{CEP} = U/\overline{D}$ = GND, P_n = 4.5V, CP = ↑		93	120	mA
		I_{CCL}		$\overline{PE} = \overline{CET} = \overline{CEP} = U/\overline{D}$ = GND CP = ↑		98	125	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

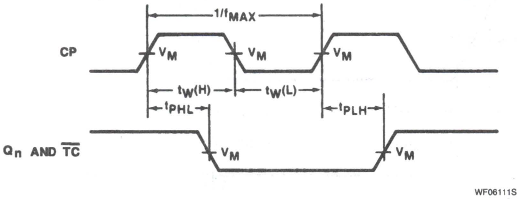
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F269					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	100	115		85		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n (Load)	Waveform 1 $\overline{PE}$ = Low	3.0 4.0	6.0 6.5	9.0 9.0	3.0 4.0	9.5 9.5	ns
t_{PLH} t_{PHL}	Propagation delay CP to Q_n (Count)	Waveform 1 $\overline{PE}$ = High	3.0 4.5	6.0 7.0	9.0 10.0	3.0 4.0	10.0 10.5	ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{TC}$	Waveform 1	4.5 5.0	6.5 6.5	9.5 9.5	4.0 5.0	10.5 10.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CET}$ to $\overline{TC}$	Waveform 2	3.5 3.5	6.0 6.5	9.0 9.0	3.0 3.0	10.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay $U/\overline{D}$ to $\overline{TC}$	Waveform 3	4.5 4.5	7.0 7.0	9.0 9.5	4.0 4.0	10.0 10.0	ns

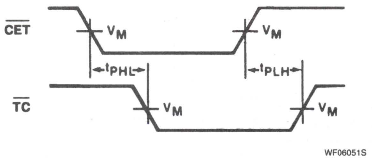
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	74F269					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low P_n to CP	Waveform 4	2.0 2.0			2.5 2.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low P_n to CP	Waveform 4	1.0 1.0			1.0 1.0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{PE}$ to CP	Waveform 4	5.0 5.5			5.5 6.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{PE}$ to CP	Waveform 4	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{CET}$, $\overline{CEP}$ to CP	Waveform 5	4.5 4.5			5.5 5.5		ns
$t_h(H)$ $t_h(L)$	Setup time, High or Low $\overline{CET}$, $\overline{CEP}$ to CP	Waveform 5	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $U/\overline{D}$ to CP	Waveform 6	5.5 5.5			6.5 6.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $U/\overline{D}$ to CP	Waveform 6	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	Clock pulse width High or Low	Waveform 1	4.0 4.5			4.0 5.0		ns

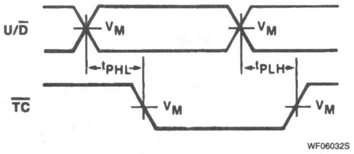
AC WAVEFORMS


1/fMAX
CP
VM
VM
VM
tW(H)
tW(L)
tPHL
tPLH
Qn AND TC
VM
VM
WF06111S

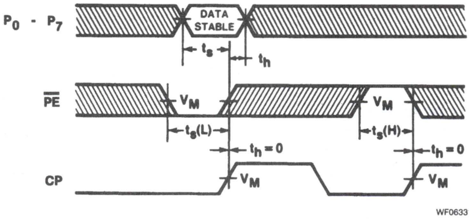
Waveform 1. Clock to Output Delays and Clock Pulse Width


CET
VM
VM
tPHL
tPLH
TC
VM
VM
WF06051S

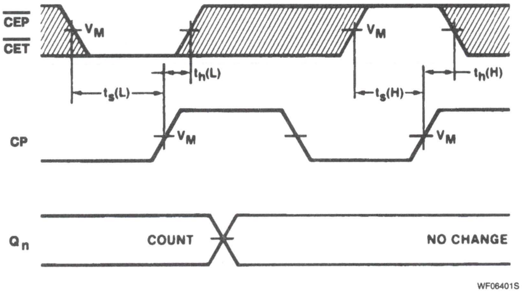
Waveform 2. Propagation Delays CET Input to Terminal Count Output

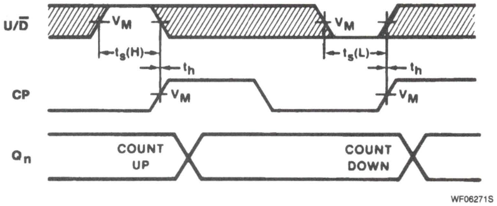

U/D
VM
VM
tPHL
tPLH
TC
VM
VM
WF06032S

Waveform 3. Propagation Delays U/D Control to Terminal Count Output


P0 - P7
DATA STABLE
ts
th
PE
VM
VM
ts(L)
ts(H)
th = 0
th = 0
CP
VM
VM
WF06331S

Waveform 4. Parallel Data and Parallel Enable Setup and Hold Times


CEP
CET
VM
VM
th(L)
th(H)
ts(L)
ts(H)
CP
VM
VM
Qn
COUNT
NO CHANGE
WF06401S

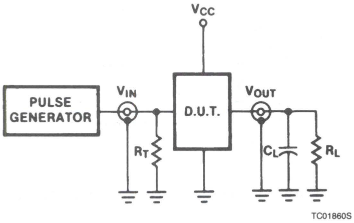

U/D
VM
VM
ts(H)
ts(L)
th
th
CP
VM
VM
Qn
COUNT UP
COUNT DOWN
WF06271S

Waveform 5. Count Enable Setup and Hold Times

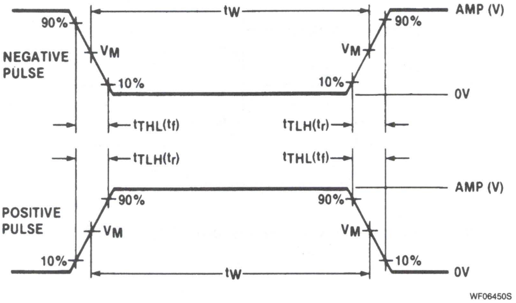
Waveform 6. Up/Down Control Setup and Hold Times

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORM


V_{CC}
PULSE GENERATOR
V_{IN}
D.U.T.
V_{OUT}
R_T
C_L
R_L
TC01860S

Test Circuit for Totem-Pole Outputs


NEGATIVE PULSE
POSITIVE PULSE
90%
10%
V_M
t_W
AMP (V)
0V
t_{THL}(t_f)
t_{TLH}(t_r)
WF06450S

$V_M = 1.5V$

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F273
Flip-Flop

Octal D Flip-Flop
Product Specification

FAST Products

FEATURES
- **High-impedance NPN base inputs for reduced loading (20µA in Low and High states)**
- **Ideal buffer for MOS microprocessor or memory**
- **Eight edge-triggered D-type flip-flops**
- **Buffered common Clock**
- **Buffered, asynchronous Master Reset**
- **See 'F377 for Clock Enable version**
- **See 'F373 for transparent latch version**
- **See 'F374 for 3-State version**

DESCRIPTION
The 'F273 has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F273	145MHz	66mA

ORDERING INFORMATION

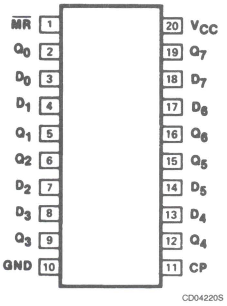
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ± 10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F273N
20-Pin Plastic SOL	N74F273D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$D_0 - D_7$	Data inputs	1.0/0.033	20µA/20µA
$\overline{MR}$	Master Reset (active-Low)	1.0/0.033	20µA/20µA
CP	Clock Pulse input (active rising edge)	1.0/0.033	20µA/20µA
Q_0-Q_7	Data outputs	50/33	1.0mA/20mA

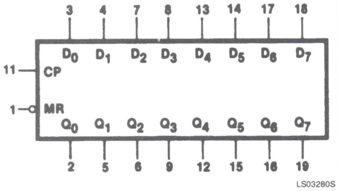
NOTE:
1. One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



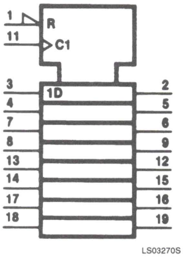
$\overline{MR}$ 1
Q_0 2
D_0 3
D_1 4
Q_1 5
Q_2 6
D_2 7
D_3 8
Q_3 9
GND 10
20 V_{CC}
19 Q_7
18 D_7
17 D_6
16 Q_6
15 Q_5
14 D_5
13 D_4
12 Q_4
11 CP
CD04220S

LOGIC SYMBOL



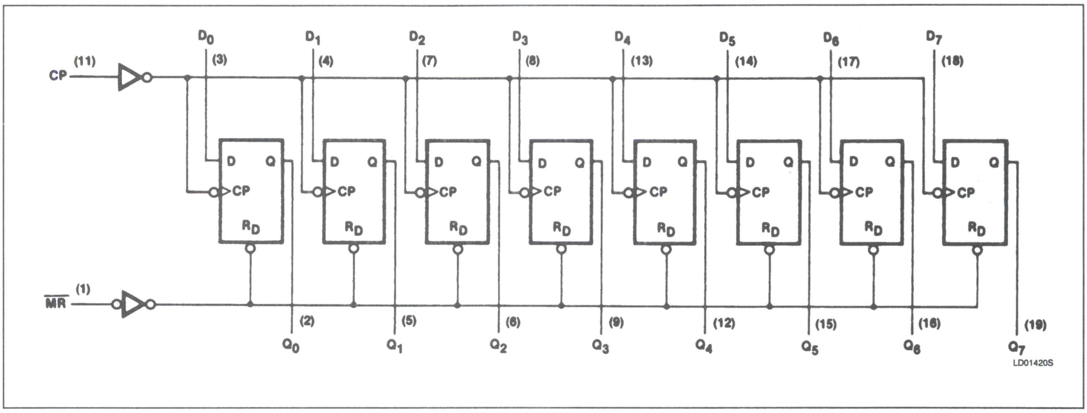
3 4 7 8 13 14 17 18
D_0 D_1 D_2 D_3 D_4 D_5 D_6 D_7
11 CP
1 MR
Q_0 Q_1 Q_2 Q_3 Q_4 Q_5 Q_6 Q_7
2 5 6 9 12 15 16 19
LS03280S

LOGIC SYMBOL (IEEE/IEC)



1 R
11 C1
3 1D 2
4 5
7 6
8 9
13 12
14 15
17 16
18 19
LS03270S

LOGIC DIAGRAM



The register is fully edge-triggered. The state of each D input, one setup time before the Low-to-High clock transition, is transferred to the corresponding flip-flop's Q output.

All outputs will be forced Low independently of Clock or Data inputs by a Low voltage level on the $\overline{MR}$ input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

MODE SELECT — FUNCTION TABLE

OPERATING MODE	INPUTS			OUTPUTS
	$\overline{MR}$	CP	D_n	Q_n
Reset (clear)	L	X	X	L
Load "1"	H	↑	h	H
Load "0"	H	↑	l	L

H = High voltage level steady state.
h = High voltage level one setup time prior to the Low-to-High clock transition.
L = Low voltage level steady state.
l = Low voltage level one setup time prior to the Low-to-High clock transition.
X = Don't care.
↑ = Low-to-High clock transition.

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage	$\overline{MR}$ & CP inputs[3]	V_{CC} = MIN, V_{IL} = 0.0V, V_{IH} = 4.5V, I_{OH} = MAX	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
		Other inputs	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = 0.0V, V_I = 7.0V				100	μA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				−20	μA
I_{OS}	Short-circuit output current[4]		V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current[5] (total)	I_{CCH}	V_{CC} = MAX			65	85	mA
		I_{CCL}				68	88	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. To reduce the effect of external noise durung test.
4. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
5. Measure I_{CC} after a momentary ground, then 4.5V is applied to clock with all outputs open and 4.5V applied to clock with all outputs open and 4.5V applied to the Master Reset input, all data inputs and the Master Reset input.

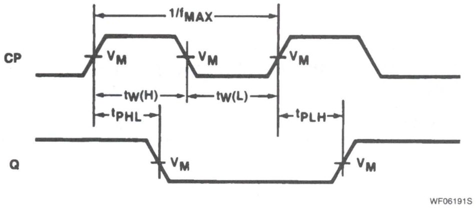
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F273					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	130	145		120		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	Waveform 1	4.0 4.0	7.5 7.5	9.5 9.5	4.0 4.0	10.5 10.5	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	Waveform 2	4.5	7.0	9.5	3.5	10.5	ns

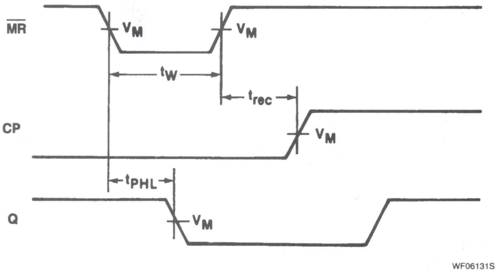
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	74F273					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to CP	Waveform 3	3.0 3.0			3.0 3.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to CP	Waveform 3	0 0			0 0		ns
t_{rec}	Recovery time $\overline{MR}$ to CP	Waveform 2	8.0			8.5		ns
$t_w(H)$ $t_w(L)$	Clock pulse width High or Low	Waveform 1	4.0 5.0			4.0 5.0		ns
$t_w(L)$	Master Reset pulse width	Waveform 2	3.5			4.0		ns

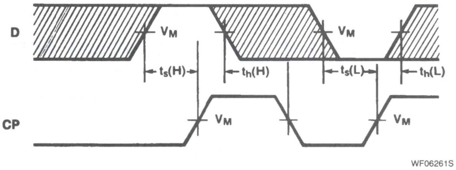
AC WAVEFORMS


1/fMAX
CP
VM
VM
VM
tW(H)
tW(L)
tPHL
tPLH
Q
VM
VM
WF06191S

Waveform 1. Clock to Output Delays and Clock Pulse Width


MR
VM
VM
tW
trec
CP
VM
tPHL
Q
VM
WF06131S

Waveform 2. Master Reset Pulse Width, Master Reset to Output and Master Reset to Clock Recovery Time

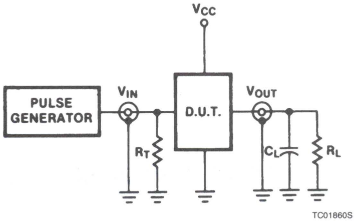

D
VM
VM
ts(H)
th(H)
ts(L)
th(L)
CP
VM
VM
WF06261S

Waveform 3. Data Setup and Hold Times

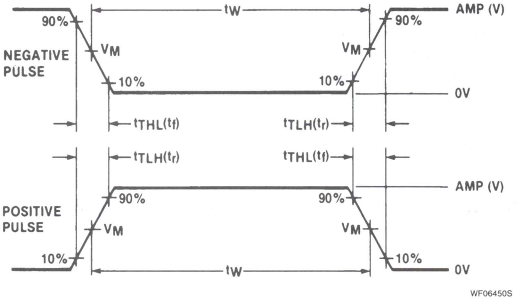
NOTE: For all waveforms, $V_M = 1.5V$.

The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORM


VCC
PULSE GENERATOR
VIN
D.U.T.
VOUT
RT
CL
RL
TC01860S

Test Circuit for Totem-Pole Outputs


tW
AMP (V)
90%
90%
NEGATIVE PULSE
VM
VM
10%
10%
0V
tTHL(tf)
tTLH(tr)
tTLH(tr)
tTHL(tf)
AMP (V)
90%
90%
POSITIVE PULSE
VM
VM
10%
10%
0V
tW
WF06450S

$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST Products

FAST 74F280A
FAST 74F280B
Parity Generator Checker

9-Bit Odd/Even Parity Generator/Checker
Product Specification

FEATURES

- **High-impedance NPN base inputs for reduced loading (20μA in Low and High states)**
- **Buffered inputs — one normalized load**
- **Word length easily expanded by cascading**

DESCRIPTION

The 'F280A is a 9-bit parity generator or checker commonly used to detect errors in high-speed data transmission or data retrieval systems. Both Even and Odd parity outputs are available for generating or checking even or odd parity on up to 9 bits.

The Even parity output (Σ_E) is High when an even number of Data inputs ($I_0 - I_8$) are High. The Odd parity output (Σ_O) is High when an odd number of Data inputs are High.

Expansion to larger word sizes is accomplished by tying the Even outputs (Σ_E) of up to nine parallel devices to the Data inputs of the final stage. This expansion scheme allows an 81-bit data word to be checked in less than 25ns with the 'F280A. 'F280B is a faster version of 'F280A.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F280A	9.0ns	26mA

ORDERING INFORMATION

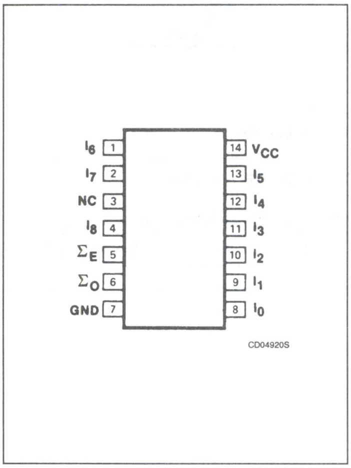
PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
14-Pin Plastic DIP	N74F280AN
14-Pin Plastic SO	N74F280AD

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

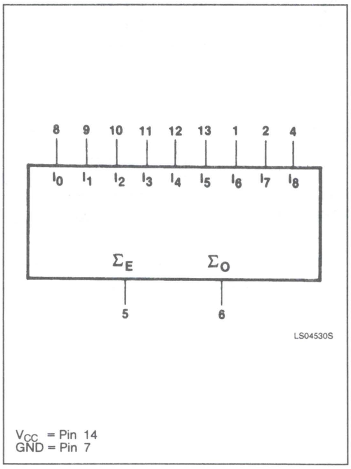
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$I_0 - I_8$	Data inputs	1.0/0.033	20μA/20μA
Σ_E, Σ_O	Parity outputs	50/33	1.0mA/20mA

NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION

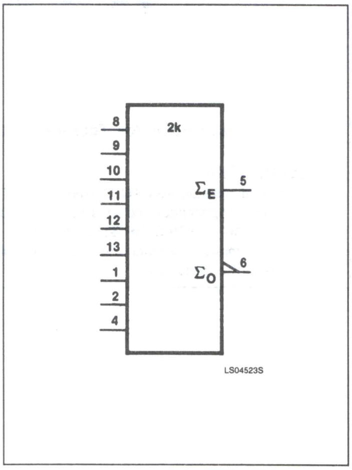

I_6 1
I_7 2
NC 3
I_8 4
Σ_E 5
Σ_O 6
GND 7
14 V_{CC}
13 I_5
12 I_4
11 I_3
10 I_2
9 I_1
8 I_0
CD04920S

LOGIC SYMBOL


8 9 10 11 12 13 1 2 4
I_0 I_1 I_2 I_3 I_4 I_5 I_6 I_7 I_8
Σ_E Σ_O
5 6
LS04530S

V_{CC} = Pin 14
GND = Pin 7

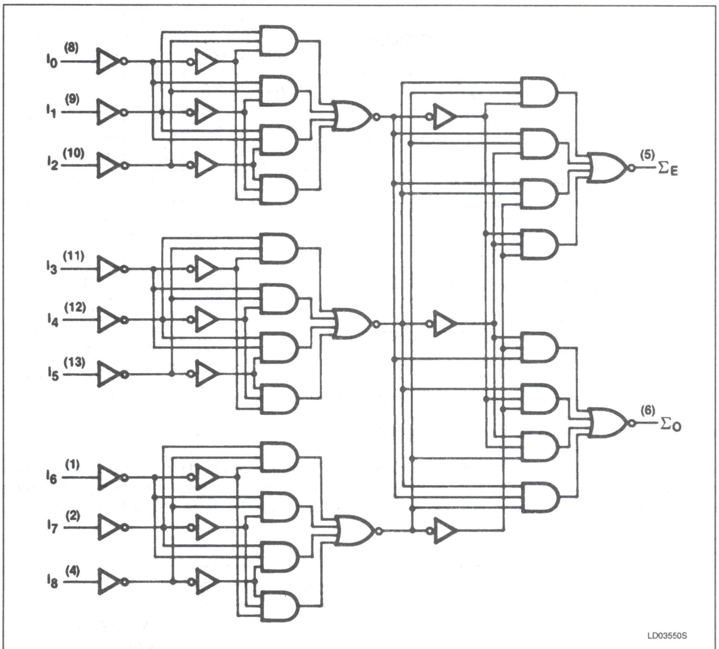
LOGIC SYMBOL (IEEE/IEC)


2k
8
9
10
11
12
13
1
2
4
Σ_E 5
Σ_O 6
LS04523S

Parity Generator Checker

FAST 74F280A, 74F280B

LOGIC DIAGRAM



V_{CC} = Pin 14
GND = Pin 7

FUNCTION TABLE

INPUTS	OUTPUTS	
Number of High Data Inputs ($I_0 - I_8$)	Σ_E	Σ_O
Even — 0, 2, 4, 6, 8	H	L
Odd — 1, 3, 5, 7, 9	L	H

H = High voltage level
L = Low voltage level

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

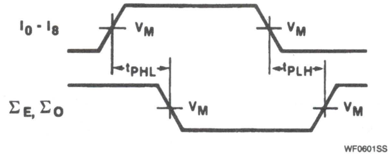
SYMBOL	PARAMETER	TEST CONDITIONS[1]		74F280A			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.5			V
			±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.35	0.50	V
			±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, $I_I = I_{IK}$			−0.73	−1.2	V
I_I	Input current at maximum input voltage	V_{CC} = 0.0V, V_I = 7.0V				100	μA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V				−20	μA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current (total)	V_{CC} = MAX			26	35	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

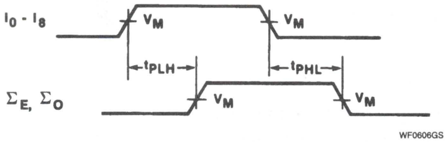
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	74F280A, 74F280B					UNIT
				T_A = +25°C V_{CC} = +5.0V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = +5.0V±10% C_L = 50pF R_L = 500Ω		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay $I_0 - I_8$ to Σ_E	'F280A	Waveform 1, 2	5.0 9.0	7.0 11.1	9.0 13.0	5.0 7.5	10.0 14.5	ns
t_{PLH} t_{PHL}	Propagation delay $I_0 - I_8$ to Σ_C		Waveform 1, 2	6.5 7.0	8.6 9.1	10.5 12.0	6.5 6.0	11.0 13.0	ns
t_{PLH} t_{PHL}	Propagation delay $I_0 - I_8$ to Σ_E	'F280B	Waveform 1, 2	4.0 4.0	6.5 7.0	9.0 10.0	3.5 3.5	10.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay $I_0 - I_8$ to Σ_O		Waveform 1, 2	4.0 4.0	6.5 7.0	9.0 10.0	3.5 3.5	10.0 11.0	ns

AC WAVEFORMS


I0 - I8
VM
VM
tPHL
tPLH
ΣE, ΣO
VM
VM
WF0601SS

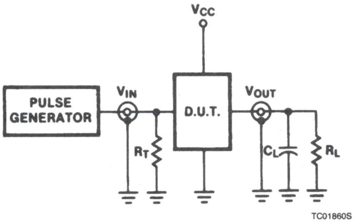
Waveform 1. For Inverting Outputs


I0 - I8
VM
VM
tPLH
tPHL
ΣE, ΣO
VM
VM
WF0606GS

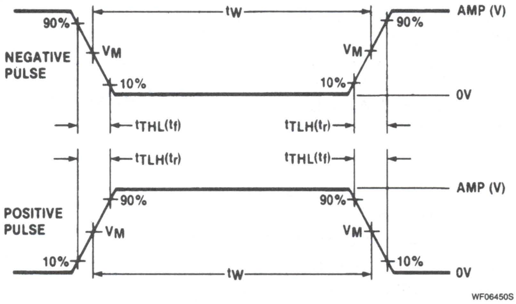
Waveform 2. For Non-Inverting Outputs

NOTE: For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORMS


VCC
PULSE GENERATOR
VIN
D.U.T.
VOUT
RT
CL
RL
TC01860S

Test Circuit for Totem-Pole Outputs


tW
AMP (V)
90%
90%
NEGATIVE PULSE
VM
VM
10%
10%
0V
tTHL(tf)
tTLH(tr)
tTLH(tr)
tTHL(tf)
AMP (V)
90%
90%
POSITIVE PULSE
VM
VM
10%
10%
0V
tW
WF06450S

$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F283
4-Bit Adder

4-Bit Binary Full Adder With Fast Carry
Product Specification

FAST Products

FEATURES

- **High-speed 4-bit binary addition**
- **Cascadable in 4-bit increments**
- **Fast internal Carry look-ahead**

DESCRIPTION

The 'F283 adds two 4-bit binary words (A_n plus B_n) plus the incoming Carry. The binary sum appears on the Sum outputs ($\Sigma_1 - \Sigma_4$) and the outgoing Carry (C_{OUT}) according to the equation:

$$C_{IN} + (A_1 + B_1) + 2(A_2 + B_2)$$
$$= \mathrm{Ip}4(A_3 + B_3) + 8(A_4 + B_4)$$
$$= \Sigma_1 + 2\Sigma_2 + 4\Sigma_3 + 8\Sigma_4 + 16C_{OUT}$$

where (+) = plus.

Due to the symmetry of the binary add function, the 'F283 can be used with either all active-High operands (positive logic) or all active-Low operands (negative logic) — see Function Table. In case of all active-Low operands the results $\Sigma_1 - \Sigma_4$ and C_{OUT} should be interpreted also as active-Low. With active-High inputs, C_{IN} cannot be left open; it must be held Low when no "Carry in" is intended. Interchanging inputs of equal weight does not affect the operation, thus C_{IN}, A_1, B_1 can arbitrarily be assigned to pins 5, 6, 7, etc.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F283	6.5ns	40mA

ORDERING INFORMATION

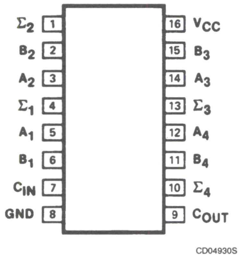
PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
16-Pin Plastic DIP	N74F283N
16-Pin Plastic SO	N74F283D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

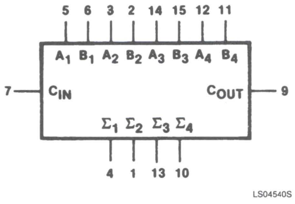
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$A_1 - A_4$	A operand inputs	1.0/2.0	20μA/1.2mA
$B_1 - B_4$	B operand inputs	1.0/2.0	20μA/1.2mA
C_{IN}	Carry input	1.0/1.0	20μA/0.6mA
$\Sigma_1 - \Sigma_4$	Sum outputs	50/33	1.0mA/20mA
C_{OUT}	Carry output	50/33	1.0mA/20mA

NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION

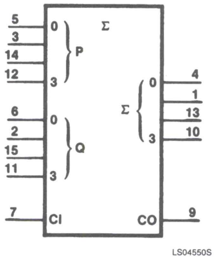

Σ2 1
B2 2
A2 3
Σ1 4
A1 5
B1 6
CIN 7
GND 8
16 VCC
15 B3
14 A3
13 Σ3
12 A4
11 B4
10 Σ4
9 COUT
CD04930S

LOGIC SYMBOL


5 6 3 2 14 15 12 11
A1 B1 A2 B2 A3 B3 A4 B4
7
CIN
COUT
9
Σ1 Σ2 Σ3 Σ4
4 1 13 10
LS04540S

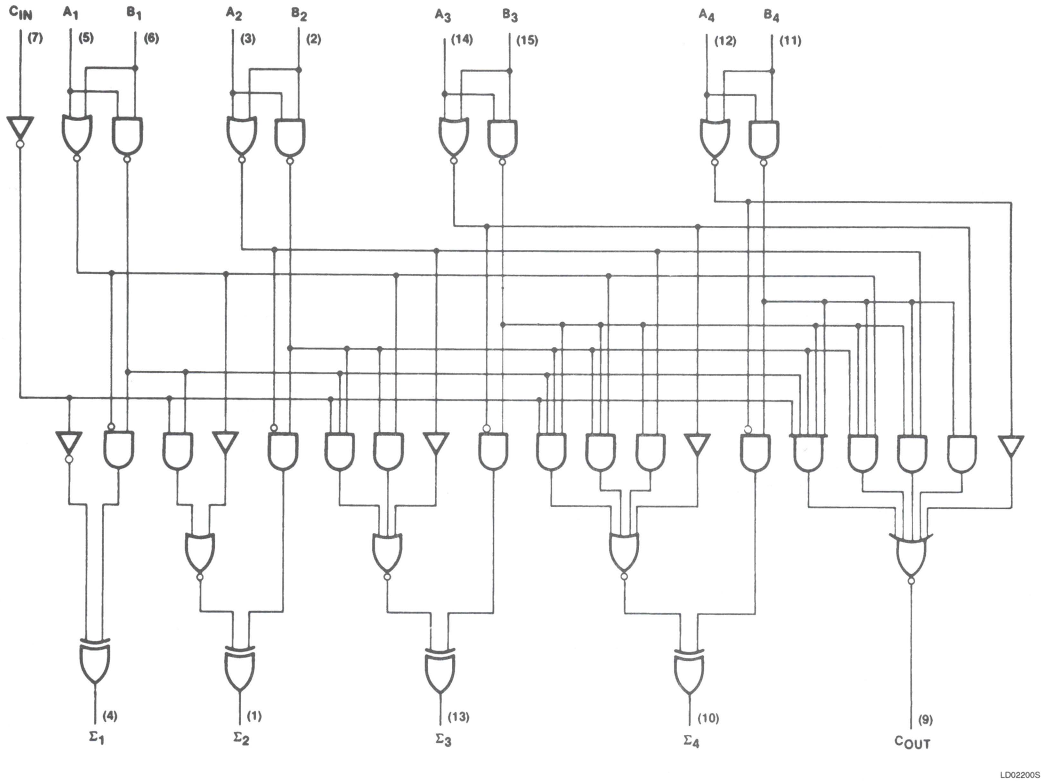
V_{CC} = Pin 16
GND = Pin 8

LOGIC SYMBOL (IEEE/IEC)


5
3
14
12
0
P
3
Σ
6
2
15
11
0
Q
3
Σ
0
3
4
1
13
10
7
CI
CO
9
LS04550S

4-Bit Adder FAST 74F283

LOGIC DIAGRAM



C_{IN} (7)
A_1 (5)
B_1 (6)
A_2 (3)
B_2 (2)
A_3 (14)
B_3 (15)
A_4 (12)
B_4 (11)
(4) Σ_1
(1) Σ_2
(13) Σ_3
(10) Σ_4
(9) C_{OUT}
LD02200S

V_{CC} = Pin 16
GND = Pin 8
( ) = Pin number

FUNCTION TABLE

PINS	C_{IN}	A_1	A_2	A_3	A_4	B_1	B_2	B_3	B_4	Σ_1	Σ_2	Σ_3	Σ_4	C_{OUT}
Logic Levels	L	L	H	L	H	H	L	L	H	H	H	L	L	H
Active-High	0	0	1	0	1	1	0	0	1	1	1	0	0	1
Active-Low	1	1	0	1	0	0	1	1	0	0	0	1	1	0

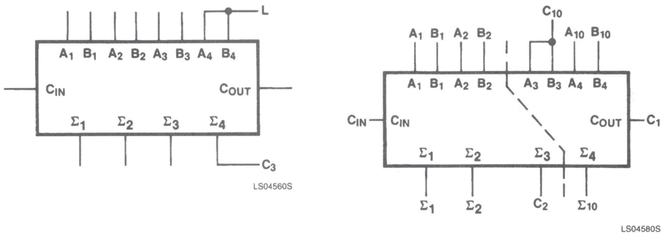
H = High voltage level
L = Low voltage level

Example:
1001
1010
10011
(10 + 9 = 19)
(carry + 5 + 6 = 12)

4-Bit Adder

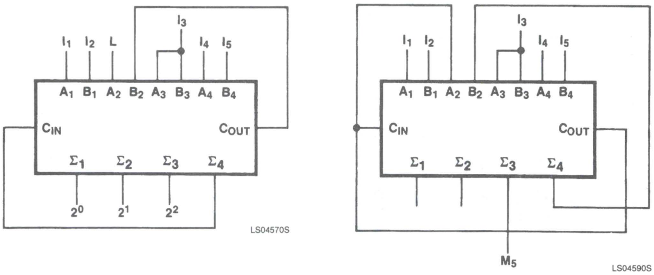
FAST 74F283

Due to pin limitations, the intermediate carries of the 'F283 are not brought out for use as inputs or outputs. However, other means can be used to effectively insert a Carry into, or bring a Carry out from, an intermediate stage. Figure a shows how to make a 3-bit adder. Tying the operand inputs of the fourth adder (A_3, B_3) Low makes S_3 dependent only on, and equal to, the Carry from the third adder. Using somewhat the same principle, Figure b shows a way of dividing the 'F283 into a 2-bit and a 1-bit adder. The third stage adder (A_2, B_2, S_2) is used merely as a means of getting a carry (C_{10}) signal into the fourth stage (via A_2 and B_2) and bringing out the Carry from the second stage on S_2. Note that as long as A_2 and B_2 are the same, whether High or Low, they do not influence S_2. Similarly, when A_2 and B_2 are the same the Carry into the third stage does not influence the Carry out of the third stage. Figure c shows a method of implementing a 5-input encoder, where the inputs are equally weighted. The outputs S_0, S_1 and S_2 present a binary number equal to the number of inputs $I_1 - I_5$ that are true. Figure d shows one method of implementing a 5-input majority gate. When three or more of the inputs $I_1 - I_5$ are true, the output M_5 is true.


L
A1 B1 A2 B2 A3 B3 A4 B4
CIN
COUT
Σ1 Σ2 Σ3 Σ4
C3
LS04560S
C10
A1 B1 A2 B2
A10 B10
A1 B1 A2 B2 A3 B3 A4 B4
CIN
CIN
COUT
C1
Σ1 Σ2 Σ3 Σ4
Σ1 Σ2 C2 Σ10
LS04580S

a. 3-Bit Adder

b. 2-Bit and 1-Bit Adders


I1 I2 L
I3
I4 I5
A1 B1 A2 B2 A3 B3 A4 B4
CIN
COUT
Σ1 Σ2 Σ3 Σ4
2^0 2^1 2^2
LS04570S
I1 I2
I3
I4 I5
A1 B1 A2 B2 A3 B3 A4 B4
CIN
COUT
Σ1 Σ2 Σ3 Σ4
M5
LS04590S

c. 5-Input Encoder

d. 5-Input Majority Gate

Figure 5

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

4-Bit Adder FAST 74F283

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		74F283			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX V_{IH} = MIN,	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OL} = MAX V_{IH} = MIN,	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current	$A_1 - A_4$, $B_1 - B_4$	V_{CC} = MAX, V_I = 0.5V				−1.2	mA
		C_{IN}					−0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current[4] (total)		V_{CC} = MAX			40	55	mA

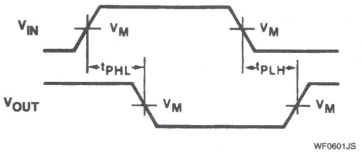
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. I_{CC} should be measured with all outputs open and the following conditions:
   Condition 1: all inputs grounded
   Condition 2: all B inputs Low, other inputs at 4.5V
   Condition 3: all inputs at 4.5V.

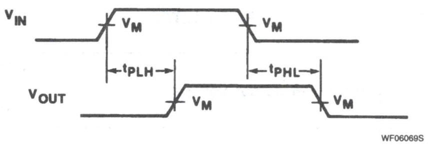
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F283					UNIT
			T_A = +25°C V_{CC} = +5.0V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH}	Propagation delay C_{IN} to Σ_i	Waveforms 1 and 2	3.5	7.0	9.5	3.5	10.5	ns
t_{PHL}			4.0	7.0	9.5	4.0	10.5	
t_{PLH}	Propagation delay A_i or B_i to Σ_i	Waveforms 1 and 2	4.0	7.0	9.5	4.0	10.5	ns
t_{PHL}			3.5	7.0	9.5	3.5	10.5	
t_{PLH}	Propagation delay C_{IN} to C_{OUT}	Waveform 2	3.5	5.7	7.5	3.5	8.5	ns
t_{PHL}			3.0	5.4	7.0	3.0	8.0	
t_{PLH}	Propagation delay A_i or B_i to C_{OUT}	Waveforms 1 and 2	3.5	5.7	7.5	3.5	8.5	ns
t_{PHL}			3.0	5.3	7.0	3.0	8.0	

AC WAVEFORMS


VIN
VM
VM
tPHL
tPLH
VOUT
VM
VM
WF0601JS

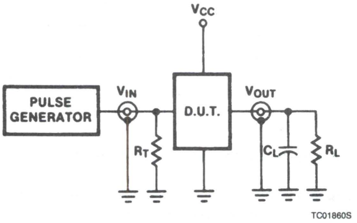
Waveform 1. For Inverting Outputs


VIN
VM
VM
tPLH
tPHL
VOUT
VM
VM
WF06069S

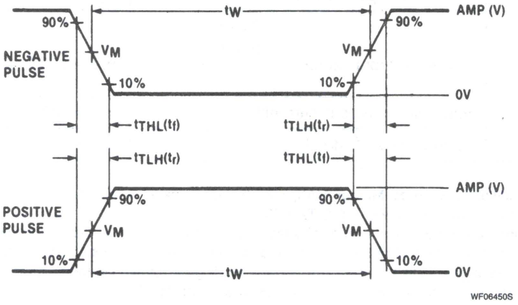
Waveform 2. For Non-Inverting Outputs

NOTE: For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORMS


VCC
PULSE GENERATOR
VIN
D.U.T.
VOUT
RT
CL
RL
TC01860S

Test Circuit for Totem-Pole Outputs


NEGATIVE PULSE
90%
VM
10%
tW
90%
VM
10%
AMP (V)
0V
tTHL(tf)
tTLH(tr)
tTLH(tr)
tTHL(tf)
POSITIVE PULSE
90%
VM
10%
90%
VM
10%
tW
AMP (V)
0V
WF06450S

$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F298
Multiplexer

Quad 2-Input Multiplexer With Storage
Product Specification

FAST Products

FEATURES

- **Fully synchronous operation**
- **Select from two data sources**
- **Buffered, negative edge triggered Clock**
- **Provides the equivalent of function capabilities of two separate MSI functions (74F157 and 74F175)**

DESCRIPTION

The 'F298 is a High-speed Multiplexer with storage. It selects 4 bits of data from two sources (Ports) under the control of a common Select input (S). The selected data is transferred to the 4-bit output register synchronous with the High-to-Low transition of the Clock input ($\overline{CP}$). The 4-bit register is fully edge triggered. The Data inputs (I_0 and I_1) and Select input (S) must be stable only one setup time prior to the High-to-Low transition of the clock for predictable operation.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F298	115MHz	30mA

ORDERING INFORMATION

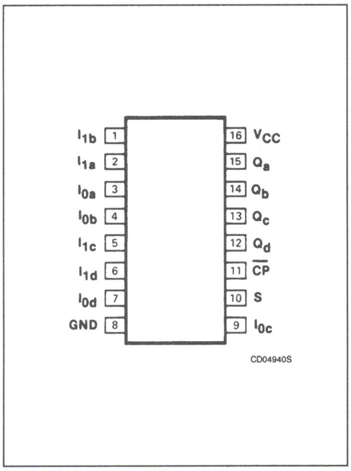
PACKAGE	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
16-Pin Plastic DIP	N74F298N
16-Pin Plastic SOL	N74F298D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

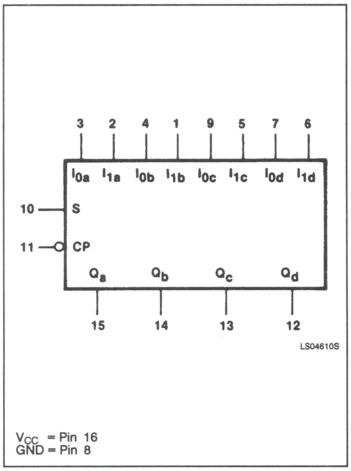
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I_{1a}, I_{1b}, I_{1c}, I_{1d}	Data inputs	1.0/1.0	20μA/0.6mA
I_{0a}, I_{0b}, I_{0c}, I_{0d}	Data inputs	1.0/1.0	20μA/0.6mA
S	Select input	1.0/1.0	20μA/0.6mA
$\overline{CP}$	Clock Pulse input (active falling edge)	1.0/1.0	20μA/0.6mA
Q_a, Q_b, Q_c, Q_d	Outputs	50/33	1.0mA/20mA

NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION

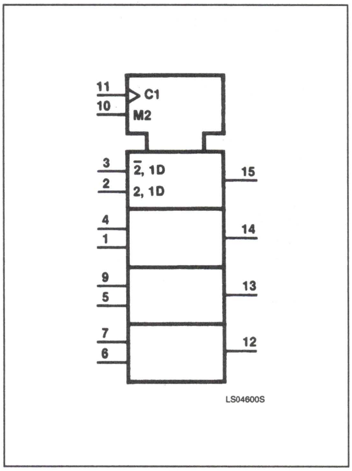

I1b 1
I1a 2
I0a 3
I0b 4
I1c 5
I1d 6
I0d 7
GND 8
16 VCC
15 Qa
14 Qb
13 Qc
12 Qd
11 CP
10 S
9 I0c
CD04940S

LOGIC SYMBOL

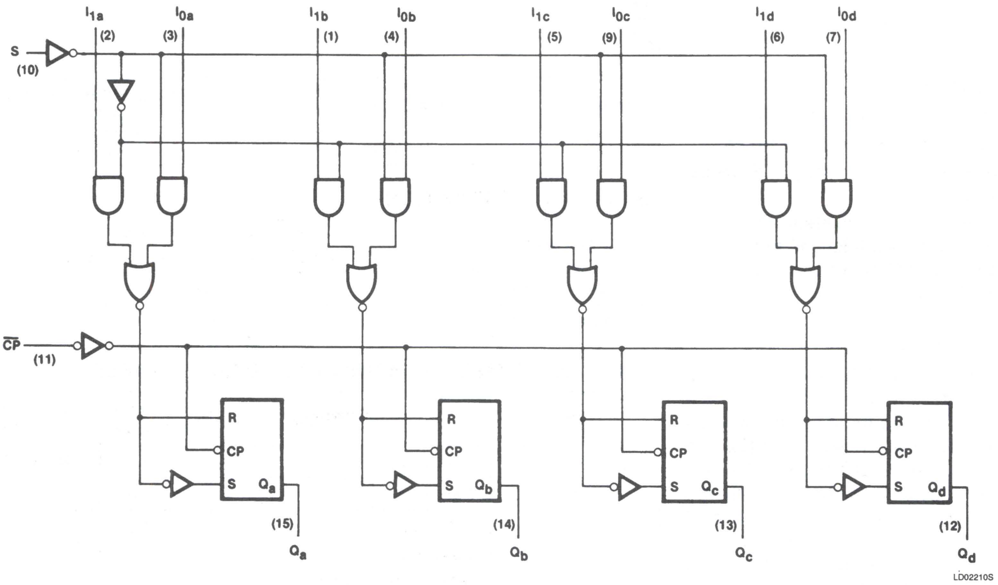

3 2 4 1 9 5 7 6
I0a I1a I0b I1b I0c I1c I0d I1d
10 S
11 CP
Qa Qb Qc Qd
15 14 13 12
LS04610S

V_{CC} = Pin 16
GND = Pin 8

LOGIC SYMBOL (IEEE/IEC)


11 C1
10 M2
3 2̄, 1D
2 2, 1D
15
4
1
14
9
5
13
7
6
12
LS04600S

LOGIC DIAGRAM


I1a (2)
I0a (3)
I1b (1)
I0b (4)
I1c (5)
I0c (9)
I1d (6)
I0d (7)
S (10)
CP (11)
R
CP
S
Qa
Qb
Qc
Qd
(15)
(14)
(13)
(12)
LD02210S

V_{CC} = Pin 16
GND = Pin 8
( ) = Pin Numbers

FUNCTION TABLE

OPERATING MODE	INPUTS				OUTPUTS
	CP	S	I_0	I_1	Q_n
Load Source "0"	↓	l	l	X	L
	↓	l	h	X	H
Load Source "1"	↓	h	X	l	L
	↓	h	X	h	H

H = High voltage level
h = High voltage level one setup time prior to the High-to-Low Clock transition
L = Low voltage level
l = Low voltage level one setup time prior to the High-to-Low Clock transition
X = Don't care
↓ = High-to-Low clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10% V_{CC}	2.5			V
				±5% V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10% V_{CC}		0.35	0.50	V
				±5% V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				−0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			30	40	mA
		I_{CCL}				32	40	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable conditions.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of High-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

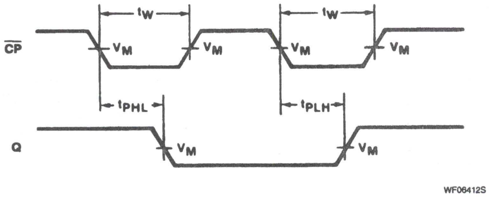
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			$T_A = +25°C$ $V_{CC} = 5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum Clock frequency	Waveform 1	110	115		150		MHz
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}$ to Q_n	Waveform 1	4.0 4.5	5.5 6.5	7.5 8.5	4.0 4.5	9.0 9.5	ns

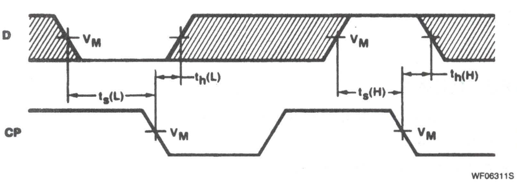
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low I_{0n}, I_{1n} to $\overline{CP}$	Waveform 2	2.0 2.0			2.0 2.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low I_{0n}, I_{1n} to $\overline{CP}$	Waveform 2	1.0 1.0			1.0 1.0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low S to $\overline{CP}$	Waveform 2	6.0 5.0			7.0 6.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low S to $\overline{CP}$	Waveform 2	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	$\overline{CP}$ pulse width, High or Low	Waveform 1	5.0 5.0			5.0 7.0		ns

AC WAVEFORMS


tW
tW
$\overline{CP}$
VM
VM
VM
VM
tPHL
tPLH
Q
VM
VM
WF06412S

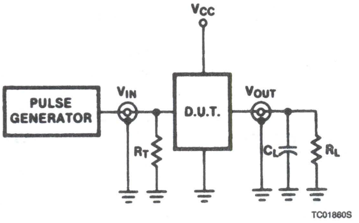
Waveform 1. Clock to Output Delays and Clock Pulse Width


D
VM
VM
th(L)
th(H)
ts(L)
ts(H)
CP
VM
VM
WF06311S

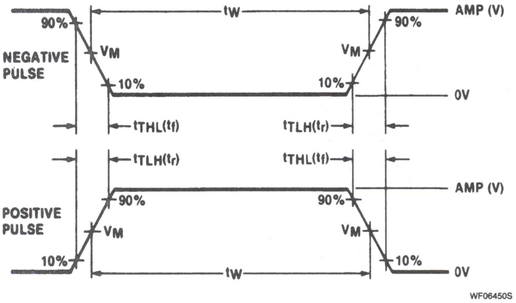
Waveform 2. Data Setup and Hold Times

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS


VCC
PULSE GENERATOR
VIN
D.U.T.
VOUT
RT
CL
RL
TC01880S

Test Circuit for Totem-Pole Outputs


NEGATIVE PULSE
90%
tW
90%
AMP (V)
VM
VM
10%
10%
0V
tTHL(tf)
tTLH(tr)
tTLH(tr)
tTHL(tf)
AMP (V)
POSITIVE PULSE
90%
90%
VM
VM
10%
10%
tW
0V
WF06450S

$V_M = 1.5V$
Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F299
Register

8-Input Universal Shift/Storage Register (3-State)
Product Specification

FAST Products

FEATURES
- **Common parallel I/O for reduced pin count**
- **Additional Serial inputs and outputs for expansion**
- **Four operating modes: Shift Left, Shift Right, Load, and Store**
- **3-State outputs for bus-oriented applications**

DESCRIPTION
The 'F299 is an 8-bit universal shift/storage register with 3-state outputs. Four modes of operation are possible: hold (store), shift left, shift right, and load data. The parallel load inputs and flip-flop outputs are multiplexed to reduce the total number of package pins. Additional outputs are provided for flip-flops Q_0 and Q_7 to allow easy serial cascading. A separate active-Low Master Reset is used to reset the register.

TYPE	TYPICAL	TYPICAL SUPPLY CURRENT (TOTAL)
74F299	115MHz	58mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
20-Pin Plastic DIP	N74F299N
20-Pin Plastic SOL[1]	N74F299D

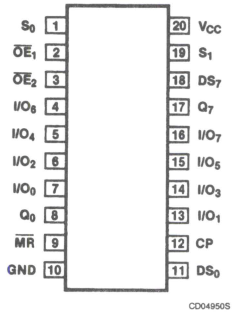
NOTE:
1. Thermal Mounting techniques are recommended. See App Note AN SMD-100 for a discussion of thermal considerations for surface mounted devices.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I/O_n	Parallel data inputs	3.5/1.0	70µA/0.6mA
CP	Clock Pulse input (active rising edge)	1.0/1.0	20µA/0.6mA
DS_0	Serial data input for right shift	1.0/1.0	20µA/0.6mA
DS_7	Serial data input for left shift	1.0/1.0	20µA/0.6mA
S_0, S_1	Mode select inputs	1.0/2.0	20µA/1.2mA
$\overline{MR}$	Asynchronous Master Reset input	1.0/1.0	20µA/0.6mA
$\overline{OE}_0$, $\overline{OE}_1$	Output Enable inputs (active-Low)	1.0/1.0	20µA/0.6mA
I/O_n	3-state parallel outputs	150/40	3.0mA/24mA
Q_0, Q_7	Serial outputs	50/33	1.0mA/20mA

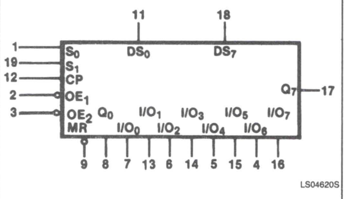
NOTE:
1. One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



S0 1
OE1 2
OE2 3
I/O6 4
I/O4 5
I/O2 6
I/O0 7
Q0 8
MR 9
GND 10
20 VCC
19 S1
18 DS7
17 Q7
16 I/O7
15 I/O5
14 I/O3
13 I/O1
12 CP
11 DS0
CD04950S

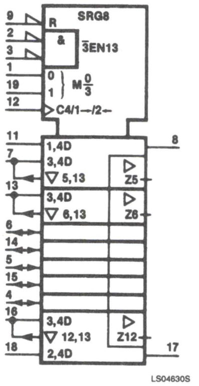
LOGIC SYMBOL



11
18
1
19
12
2
3
S0
S1
CP
OE1
OE2
MR
DS0
DS7
Q7
17
Q0
I/O1
I/O3
I/O5
I/O7
I/O0
I/O2
I/O4
I/O6
9 8 7 13 6 14 5 15 4 16
LS04620S

V_{CC} = Pin 20
GND = Pin 10

LOGIC SYMBOL (IEEE/IEC)



SRG8
R
&
3EN13
M 0/3
C4/1→/2←
1,4D
3,4D
5,13
6,13
12,13
2,4D
Z5
Z6
Z12
9
2
3
1
19
12
11
7
13
6
14
5
15
4
16
18
8
17
LS04630S

Register

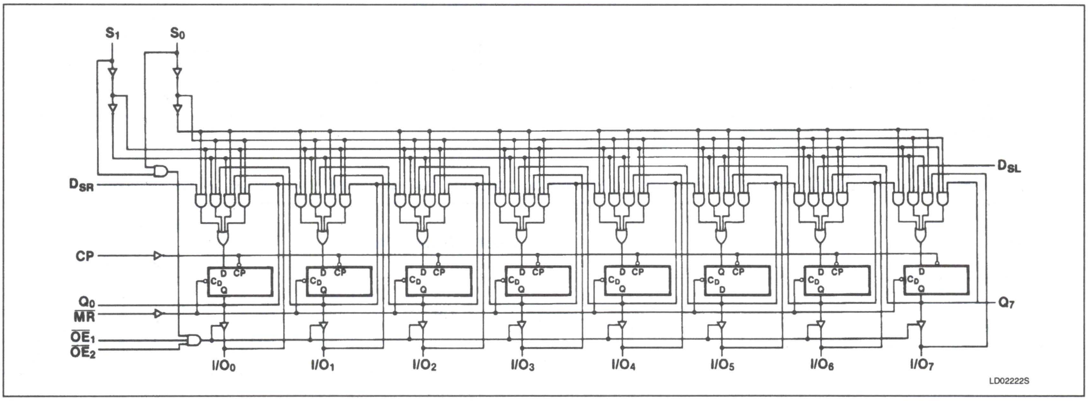
FAST 74F299

The 'F299 contains eight edge-triggered D-type flip-flops and the interstage logic necessary to perform synchronous shift left, shift right, parallel load and hold operations. The type of operation is determined by S_0 and S_1, as shown in the Mode Select Table. All flip-flop outputs are brought out through 3-state buffers to separate I/O pins that also serve as data inputs in the parallel load mode. Q_0 and Q_7 are also brought out on other pins for expansion in serial shifting of longer words.

A Low signal on $\overline{MR}$ overrides the Select and CP inputs and resets the flip-flops. All other state changes are initiated by the rising edge of the clock. Inputs can change when the clock is in either state provided only that the recommended setup and hold times, relative to the rising edge of CP, are observed.

A High signal on either $\overline{OE}_1$ or $\overline{OE}_2$ disables the 3-state buffers and puts the I/O pins in the high-impedance state. In this condition the shift, hold, load and reset operations can still occur. The 3-state buffers are also disabled by High signals on both S_0 and S_1 in preparation for a parallel load operation.

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OPERATING MODE
$\overline{MR}$	S_1	S_0	CP	
L	X	X	X	Asynchronous Reset; $Q_0 - Q_7$ = Low
H	H	H	↑	Parallel Load; $I/O_n \rightarrow Q_n$
H	L	H	↑	Shift Right; $DS_0 \rightarrow Q_0$, $Q_0 \rightarrow Q_1$, etc.
H	H	L	↑	Shift Left; $DS_7 \rightarrow Q_7$, $Q_7 \rightarrow Q_6$, etc.
H	L	L	X	Hold

H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		−0.5 to +7.0	V
V_{IN}	Input voltage		−0.5 to +7.0	V
I_{IN}	Input current		−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		−0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	Q_0, Q_7	40	mA
		I/O_n	48	mA
T_A	Operating free-air temperature range		0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	High-level output current	Q_0, Q_7			−1	mA
		I/O_n			−3	mA
I_{OL}	Low-level output current	Q_0, Q_7			20	mA
		I/O_n			24	mA
T_A	Operating free-air temperature		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage	Q_0, Q_7	$V_{CC} = \text{MIN}$, $V_{IL} = \text{MAX}$, $V_{IH} = \text{MIN}$	$I_{OH} = -1\text{mA}$	$\pm 10\%V_{CC}$	2.5			V
					$\pm 5\%V_{CC}$	2.7	3.4		V
		I/O_n		$I_{OH} = -3\text{mA}$	$\pm 10\%V_{CC}$	2.4			V
					$\pm 5\%V_{CC}$	2.7	3.4		V
V_{OL}	Low-level output voltage		$V_{CC} = \text{MIN}$, $V_{IL} = \text{MAX}$, $V_{IH} = \text{MIN}$	$I_{OL} = \text{MAX}$	$\pm 10\%V_{CC}$		0.35	0.50	V
					$\pm 5\%V_{CC}$		0.35	0.50	V
V_{IK}	Input clamp voltage		$V_{CC} = \text{MIN}$, $I_I = I_{IK}$				−0.73	−1.2	V
I_I	Input current at maximum input voltage	Others	$V_{CC} = 0.0\text{V}$, $V_I = 7.0\text{V}$					100	μA
		I/O_n	$V_{CC} = 5.5\text{V}$, $V_I = 5.5\text{V}$					1.0	mA
I_{IH}	High-level input current		$V_{CC} = \text{MAX}$, $V_I = 2.7\text{V}$					20	μA
I_{IL}	Low-level input current	S_0, S_1	$V_{CC} = \text{MAX}$, $V_I = 0.5\text{V}$					−1.2	mA
		Others						−0.6	mA
$I_{OZH} + I_{IH}$	OFF-state output current, High-level voltage applied	I/O_n only	$V_{CC} = \text{MAX}$, $V_O = 2.7\text{V}$					70	μA
$I_{OZL} + I_{IL}$	OFF-state output current Low-level voltage applied	I/O_n only	$V_{CC} = \text{MAX}$, $V_O = 0.5\text{V}$					−0.6	mA
I_{OS}	Short-circuit output current[3]		$V_{CC} = \text{MAX}$			−60		−150	mA
I_{CC}	Supply current (total)	I_{CCH}	$V_{CC} = \text{MAX}$				50	65	mA
		I_{CCL}					64	85	mA
		I_{CCZ}					60	65	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at $V_{CC} = 5V$, $T_A = 25°C$.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

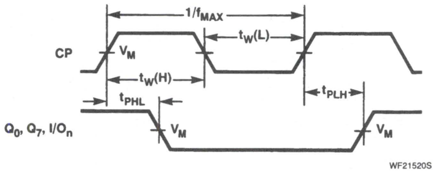
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F299					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency (I/O pins)	Waveform 1	70	100		70		MHz
f_{MAX}	Maximum clock frequency (Q_n pins)	Waveform 1	85	115		85		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_0 or Q_7	Waveform 1	4.0 4.5	5.0 6.0	7.5 8.0	3.5 4.5	8.5 8.5	ns
t_{PLH} t_{PHL}	Propagation delay CP to I/O_n	Waveform 1	4.0 4.0	6.0 6.5	9.0 9.0	4.0 4.0	10.0 10.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_0 or Q_7	Waveform 2	5.5	7.5	9.5	5.5	10.5	ns
t_{PHL}	Propagation delay $\overline{MR}$ to I/O_n	Waveform 2	5.5	7.5	10.0	5.5	10.5	ns
t_{PZH} t_{PZL}	Output enable time S_n, $\overline{OE}$ to I/O_n	Waveform 4 Waveform 5	3.5 4.0	6.0 7.5	8.0 10.0	3.5 4.0	9.0 11.0	ns
t_{PHZ} t_{PLZ}	Output disable time S_n, $\overline{OE}$ to I/O_n	Waveform 4 Waveform 5	2.5 1.5	4.5 2.5	7.0 5.5	2.5 1.5	8.0 6.5	ns

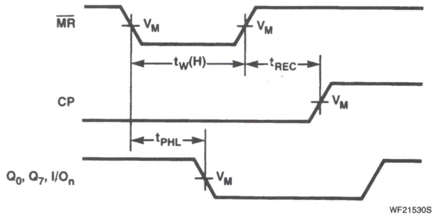
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	74F299					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low S_0 or S_1 to CP	Waveform 3	6.5 6.5			7.5 7.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low S_0 or S_1 to CP	Waveform 3	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low I/O_n, DS_0, DS_7 to CP	Waveform 3	3.5 3.5			4.0 4.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low I/O_n, DS_0, DS_7 to CP	Waveform 3	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	CP pulse width, High or Low	Waveform 1	5.0 4.5			5.0 4.5		ns
$t_w(L)$	$\overline{MR}$ pulse width Low	Waveform 2	4.5			4.5		ns
t_{rec}	Recovery time $\overline{MR}$ to CP	Waveform 2	4.0			4.0		ns

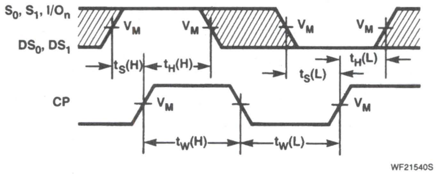
AC WAVEFORMS


1/fMAX
CP
VM
tW(L)
tW(H)
tPHL
tPLH
Q0, Q7, I/On
VM
VM
WF21520S

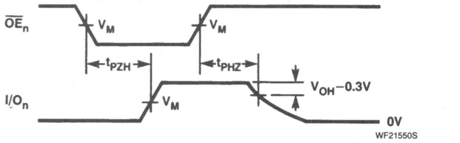
Waveform 1. Propagation Delay, Clock Input to Output, Clock Widths and Maximum Clock Frequency


MR
VM
VM
tW(H)
tREC
CP
VM
tPHL
Q0, Q7, I/On
VM
WF21530S

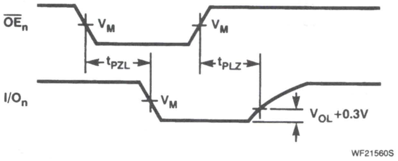
Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time


S0, S1, I/On
DS0, DS1
VM
VM
VM
VM
tS(H)
tH(H)
tS(L)
tH(L)
CP
VM
VM
tW(H)
tW(L)
WF21540S

Waveform 3. Data and Select Setup and Hold Times


OEn
VM
VM
tPZH
tPHZ
VOH−0.3V
I/On
VM
0V
WF21550S

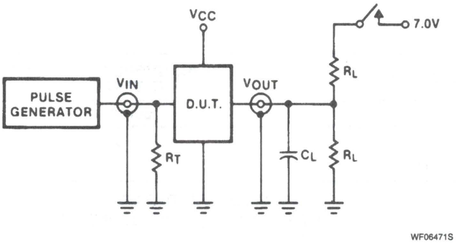
Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time From High Level


OEn
VM
VM
tPZL
tPLZ
I/On
VM
VOL +0.3V
WF21560S

Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time From Low Level

NOTE: $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS


VCC
7.0V
RL
PULSE GENERATOR
VIN
D.U.T.
VOUT
RT
CL
RL
WF06471S

Test Circuit for 3-State Outputs

SWITCH POSITION

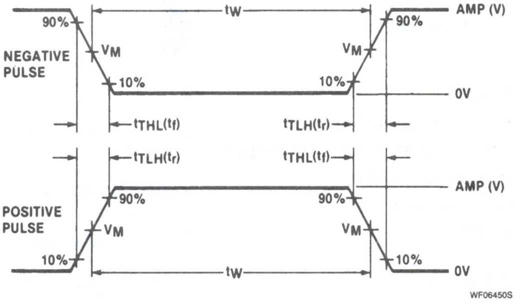
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.


tW
90%
90%
AMP (V)
NEGATIVE PULSE
VM
VM
10%
10%
0V
tTHL(tf)
tTLH(tr)
tTLH(tr)
tTHL(tf)
AMP (V)
90%
90%
POSITIVE PULSE
VM
VM
10%
10%
0V
tW
WF06450S

$V_M = 1.5V$

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F322
Register

8-Bit Serial/Parallel Register With Sign Extend (3-State)
Preliminary Specification

FAST Products

FEATURES
- **Multiplexed parallel I/O ports**
- **Separate Serial input and output**
- **Sign extend function**
- **3-State outputs for bus applications**

DESCRIPTION
The 'F322 is an 8-bit shift register with provision for either serial or parallel loading and with 3-State parallel outputs plus a bi-state Serial output. Parallel Data inputs and outputs are multiplexed to minimize pin count. State changes are initiated by the rising edge of the clock. Four synchronous modes of operation are possible: hold (store), shift right with serial entry, shift right with sign extend, and parallel load. An asynchronous Master Reset ($\overline{MR}$) input overrides clocked operation and clears the register.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F322	90 MHz	60mA

ORDERING INFORMATION

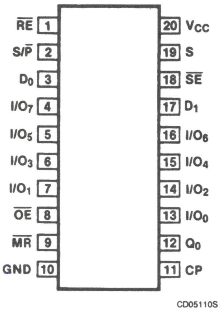
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ± 10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F322N
20-Pin Plastic SOL	N74F322D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0, D_1	Serial data inputs	1.0/1.0	20μA/0.6mA
S	Serial data select input	1.0/2.0	20μA/1.2mA
$\overline{SE}$	Sign Extend input	1.0/3.0	20μA/1.8mA
CP	Clock Pulse input (active rising edge)	1.0/1.0	20μA/0.6mA
S/$\overline{P}$	Serial (High) or Parallel (Low) mode control input	1.0/1.0	20μA/0.6mA
$\overline{RE}$	Register Enable input (active-Low)	1.0/1.0	20μA/0.6mA
$\overline{MR}$	Asynchronous Master Reset input (active-Low)	1.0/1.0	20μA/0.6mA
$\overline{OE}$	Output Enable input (active-Low)	1.0/1.0	20μA/0.6mA
Q_0	Bi-state serial output	50/33	1.0mA/20mA
I/O_n	Multiplexed parallel data inputs or	3.5/1.0	70μA/0.6mA
	3-State parallel outputs	150/40	3.0mA/24mA

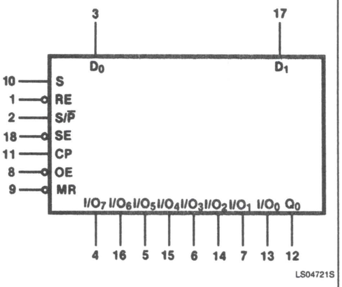
NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



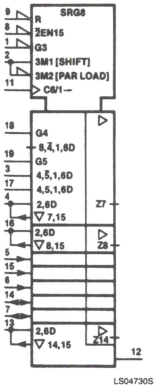
RE 1
S/P 2
D0 3
I/O7 4
I/O5 5
I/O3 6
I/O1 7
OE 8
MR 9
GND 10
20 Vcc
19 S
18 SE
17 D1
16 I/O6
15 I/O4
14 I/O2
13 I/O0
12 Q0
11 CP
CD05110S

LOGIC SYMBOL



3
17
D0
D1
10 S
1 RE
2 S/P
18 SE
11 CP
8 OE
9 MR
I/O7 I/O6 I/O5 I/O4 I/O3 I/O2 I/O1 I/O0 Q0
4 16 5 15 6 14 7 13 12
LS04721S

LOGIC SYMBOL (IEEE/IEC)



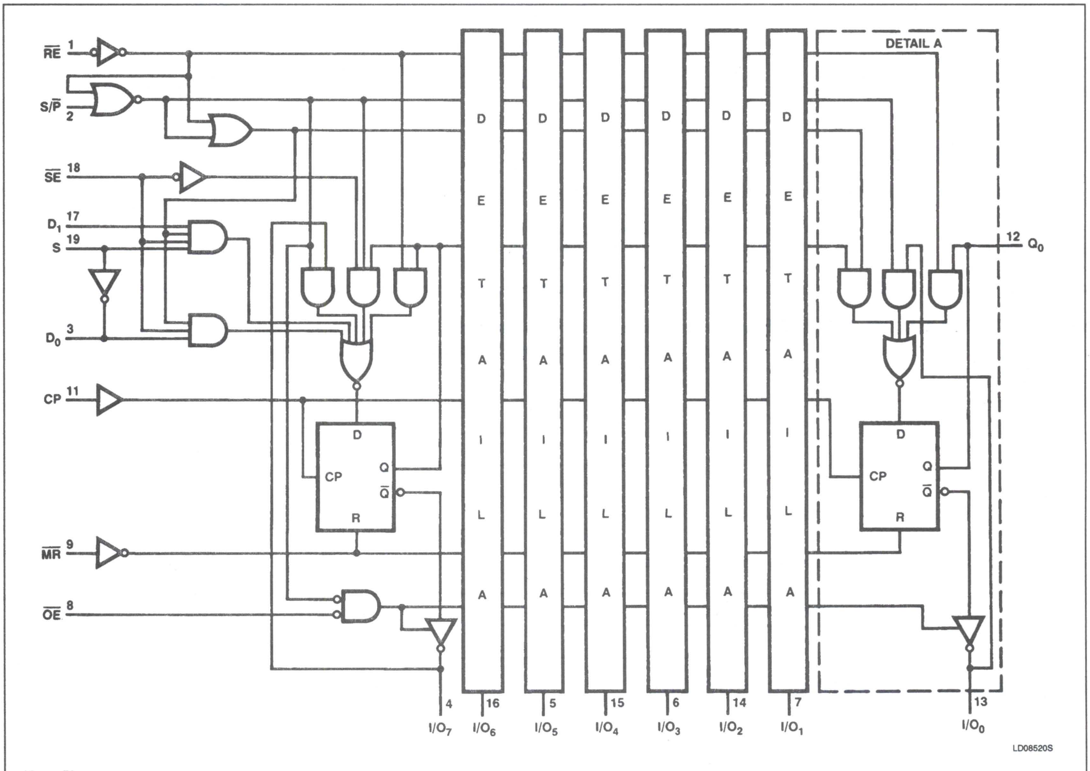
SRG8
9 R
8 Z̄EN15
1 G3
2 3M1 [SHIFT]
3M2 [PAR LOAD]
11 C6/1→
18 G4
8,4̄,1,6D
19 G5
3 4,5̄,1,6D
17 4,5,1,6D
4 2,6D
▽ 7,15
Z7
16 2,6D
▽ 8,15
Z8
5
15
6
14
7
13 2,6D
▽ 14,15
Z14
12
LS04730S

Register

FAST 74F322

The 'F322 contains eight D-type edge-triggered flip-flops and the interstage gating required to perform right shift and the intrastage gating necessary for hold and synchronous parallel load operations. A Low signal on $\overline{RE}$ enables shifting or parallel loading, while a High signal enables the hold mode. A High signal on S/$\overline{P}$ enables shift right, while a Low signal disables the 3-State output buffers and enables parallel loading. In the shift right mode a High signal on $\overline{SE}$ enables serial entry from either D_0 or D_1, as determined by the S input. A Low signal on $\overline{SE}$ enables shift right but Q_7 reloads its contents, thus performing the sign extend function required for the F384 Two's Complement Multiplier. A High signal on $\overline{OE}$ disables the 3-State output buffers, regardless of the other control inputs. In this condition the shifting and loading operations can still be performed.

LOGIC DIAGRAM



V_{CC} = Pin
GND = Pin
( ) = Pin numbers

FUNCTION TABLE

MODE	INPUTS							OUTPUTS								
	$\overline{MR}$	$\overline{RE}$	$S/\overline{P}$	$\overline{SE}$	S	$\overline{OE}^6$	CP	I/O_7	I/O_6	I/O_5	I/O_4	I/O_3	I/O_2	I/O_1	I/O_0	Q_0
Clear	L	X	X	X	X	L	X	L	L	L	L	L	L	L	L	L
	L	X	X	X	X	H	X	Z	Z	Z	Z	Z	Z	Z	Z	L
Parallel Load	H	L	L	X	X	X	↑	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	I_0
Shift Right	H	L	H	H	L	L	↑	D_0	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_1
	H	L	H	H	H	L	↑	D_1	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_1
Sign Extend	H	L	H	L	X	L	↑	O_7	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_1
Hold	H	H	X	X	X	L	↑	NC	NC	NC	NC	NC	NC	NC	NC	NC

H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-to-High clock transition
NC = No change
$I_0 - I_7$ = The level of the steady state input at the respective I/O terminal is loaded into the flip-flop while the flip-flop outputs (except Q_0) are isolated from the I/O terminal.
$D_0 - D_7$ = The level of the steady-state inputs to the serial multiplexer input.
$O_0 - O_7$ = The level of the respective Q_n flip-flop prior to the last clock Low-to-High clock transition.

NOTE:
When the $\overline{OE}$ input is High, all I/O_n terminals are at the High-impedance state, sequential operation or clearing of the register is not affected.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	Q_0	40	mA
		I/O_n	48	mA
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current	Q_0			-1	mA
		I/O_n			-3	mA
I_{OL}	Low-level output current	Q_0			20	mA
		I/O_n			24	mA

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			74F322			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage	Q_0	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = −1mA	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7	3.4		V
		I/O_n		I_{OH} = −3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.3		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OL} = MAX V_{IH} = MIN,		±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$				−0.73	−1.2	V
I_I	Input current at maximum input voltage	Others	V_{CC} = MAX, V_I = 7.0V					100	μA
		I/O_n	V_{CC} = 5.5V, V_I = 5.5V					1.0	mA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	Low-level input current	$\overline{SE}$	V_{CC} = MAX, V_I = 0.5V					−1.8	mA
		S						−1.2	mA
		Others						−0.6	mA
I_{OZH} + I_{IH}	OFF-state output current, High-level voltage applied	I/O_n only	V_{CC} = MAX, V_O = 2.7V					70	μA
I_{OZL} + I_{IL}	OFF-state output current, Low-level voltage applied	I/O_n only	V_{CC} = MAX, V_O = 0.5V					−0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX			−60		−150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX						mA
		I_{CCL}					60		mA
		I_{CCZ}							mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value under the recommended operating conditions for the applicable conditions.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

6

Register

FAST 74F322

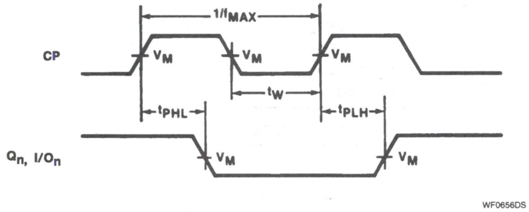
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F322 $T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50pF$, $R_L = 500\Omega$ Min	Typ	Max	74F322 $T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$ Min	Max	UNIT
f_{MAX}	Maximum clock frequency	Waveform 1	70	90		70		MHz
t_{PLH} t_{PHL}	Propagation delay CP to I/O_n	Waveform 1	4 5	7 8.5	9 11	4 5	10 12	ns
t_{PLH} t_{PHL}	Propagation delay CP to Q_0	Waveform 1	3.5 3.5	7 7	9 9	3.5 3.5	10 10	ns
t_{PHL}	Propagation delay $\overline{MR}$ to I/O_n	Waveform 3	6	10	13	6	14	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_0	Waveform 3	5.5	9.5	12.0	5.5	13	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OE}$ to I/O_n	Waveform 4 Waveform 5	3 4	6.5 8.5	9 11	3 4	10 12	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OE}$ to I/O_n	Waveform 4 Waveform 5	2 2	4.5 5	6 7	2 2	7 8	ns
t_{PZH} t_{PZL}	Output enable time $S/\overline{P}$ to I/O_n	Waveform 4 Waveform 5	4.5 5.5	8 10	10.5 14	4.5 5.5	11.5 15	ns
t_{PHZ} t_{PLZ}	Output disable time $S/\overline{P}$ to I/O_n	Waveform 4 Waveform 5	5 6	9 12	11.5 15.5	5 6	12.5 16.5	ns

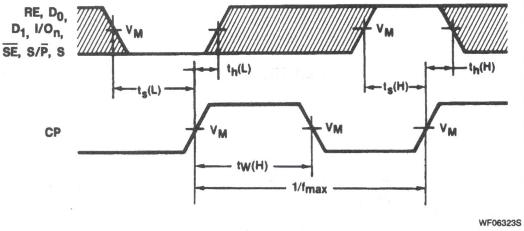
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	74F322					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{RE}$ to CP	Waveform 2	12 12			13 13		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{RE}$ to CP	Waveform 2	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_0, D_1 or I/O_n to CP	Waveform 2	8 8			9 9		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_0, D_1 or I/O_n to CP	Waveform 2	2 2			3 3		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{SE}$ to CP	Waveform 2	7 7			8 8		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{SE}$ to CP	Waveform 2	2 2			2 2		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $S/\overline{P}$ to CP	Waveform 2	12 12			13 13		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low S to CP	Waveform 2	8 8			9 9		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low S or $S/\overline{P}$ to CP	Waveform 2	0 0			0 0		ns
$t_w(H)$	CP pulse width High	Waveform 1	7			7		ns
$t_w(L)$	$\overline{MR}$ pulse width Low	Waveform 3	7			7		ns
t_{rec}	Recovery time, $\overline{MR}$ to CP	Waveform 3	8			8		ns

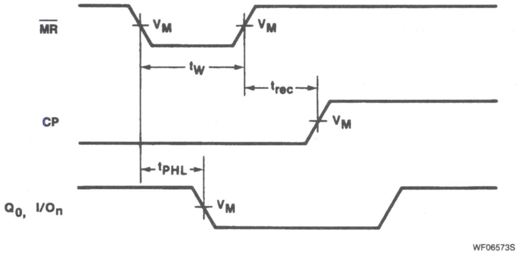
AC WAVEFORMS


CP
1/fMAX
VM
VM
VM
tW
tPHL
tPLH
Qn, I/On
VM
VM
WF0656DS

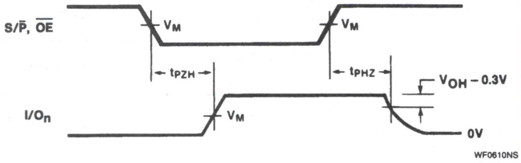
Waveform 1. Clock to Output Delays and Clock Pulse Width


RE, D0, D1, I/On, SE, S/P, S
VM
VM
th(L)
ts(L)
ts(H)
th(H)
CP
VM
VM
VM
tW(H)
1/fmax
WF06323S

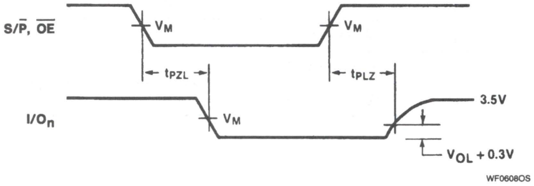
Waveform 2. Data Setup and Hold Times


MR
VM
VM
tW
trec
CP
VM
tPHL
Q0, I/On
VM
WF06573S

Waveform 3. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time


S/P, OE
VM
VM
tPZH
tPHZ
VOH − 0.3V
I/On
VM
0V
WF0610NS

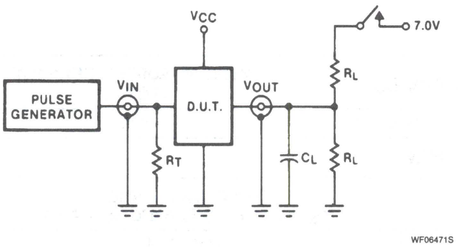
Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time From High Level


S/P, OE
VM
VM
tPZL
tPLZ
3.5V
I/On
VM
VOL + 0.3V
WF0608OS

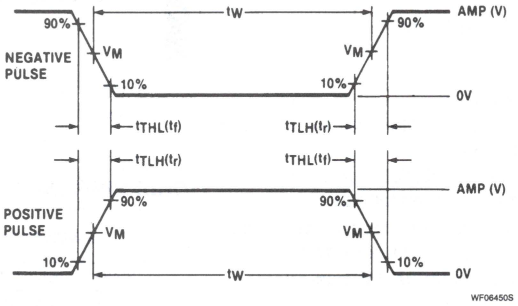
Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS


VCC
7.0V
RL
PULSE GENERATOR
VIN
D.U.T.
VOUT
RT
CL
RL
WF06471S

Test Circuit for 3-State Outputs


NEGATIVE PULSE
90%
VM
10%
tW
VM
10%
90%
AMP (V)
0V
tTHL(tf)
tTLH(tr)
tTLH(tr)
tTHL(tf)
POSITIVE PULSE
90%
VM
10%
90%
VM
10%
AMP (V)
0V
tW
WF06450S

$V_M = 1.5V$

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F323
Register

8-Bit Universal Shift/Storage Register
With Synchronous Reset and Common I/O Pins (3-State)
Product Specification

FAST Products

FEATURES

- **Common parallel I/O for reduced pin count**
- **Additional Serial inputs and outputs for expansion**
- **Four operating modes: shift left, shift right, load, and store**
- **3-State outputs for bus-oriented applications**

DESCRIPTION

The 'F323 is an 8-bit universal shift/storage register with 3-State outputs. Its function is similar to the 'F299 with the exception of Synchronous Reset. Parallel load inputs and flip-flop outputs are multiplexed to minimize pin count. Separate serial inputs and outputs are provided for Q_0 and Q_7 to allow easy cascading. Four operation modes are possible: hold (store), shift left, shift right, and parallel load.

The 'F323 contains eight edge-triggered D-type flip-flops and the interstage logic necessary to perform synchronous reset, shift left, shift right, parallel load and hold operations. The type of operation is determined by S_0 and S_1, as shown in the Mode Select table.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F323	100 MHz	68mA

ORDERING INFORMATION

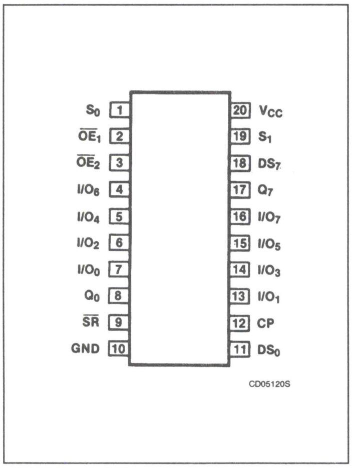
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V± 10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F323N
20-Pin Plastic SOL	N74F323D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I/O_n	Data inputs	3.5/1.0	70μA/0.6mA
DS_0	Serial data input for right shift	1.0/1.0	20μA/0.6mA
DS_7	Serial data input for left shift	1.0/1.0	20μA/0.6mA
CP	Clock pulse input (active rising edge)	1.0/1.0	20μA/0.6mA
S_0, S_1	Mode select inputs	1.0/2.0	20μA/1.2mA
$\overline{SR}$	Synchronous reset input (active-Low)	1.0/1.0	20μA/0.6mA
$\overline{OE}_0$, $\overline{OE}_1$	3-State output enable inputs (active-Low)	1.0/1.0	20μA/0.6mA
I/O_n	3-State parallel data outputs	150/40	3.0mA/24mA
Q_0, Q_7	Serial outputs	50/33	1.0mA/20mA

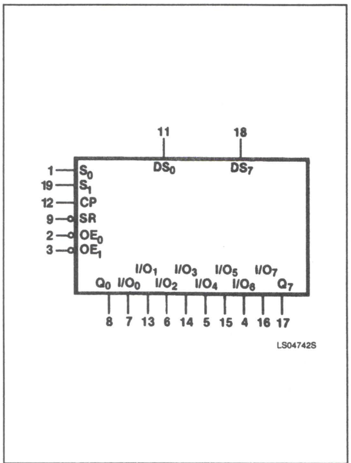
NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



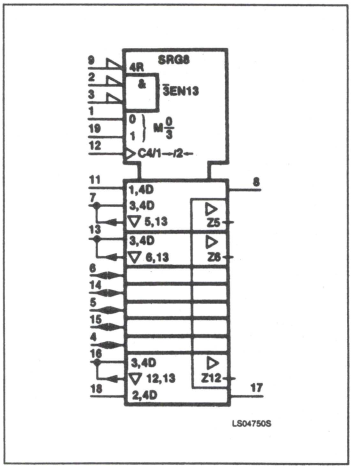
S0 1
OE1 2
OE2 3
I/O6 4
I/O4 5
I/O2 6
I/O0 7
Q0 8
SR 9
GND 10
20 Vcc
19 S1
18 DS7
17 Q7
16 I/O7
15 I/O5
14 I/O3
13 I/O1
12 CP
11 DS0
CD05120S

LOGIC SYMBOL



11
18
DS0
DS7
1 S0
19 S1
12 CP
9 SR
2 OE0
3 OE1
I/O1 I/O3 I/O5 I/O7
Q0 I/O0 I/O2 I/O4 I/O6 Q7
8 7 13 6 14 5 15 4 16 17
LS04742S

LOGIC SYMBOL (IEEE/IEC)



SRG8
9
4R
2
&
3EN13
3
1
0
19
1
M 0/3
12
C4/1→/2←
11
1,4D
8
7
3,4D
▽ 5,13
Z5
13
3,4D
▽ 6,13
Z6
6
14
5
15
4
16
3,4D
▽ 12,13
Z12
18
2,4D
17
LS04750S

All flip-flop outputs are brought out through 3-State buffers to separate I/O pins that also serve as data inputs in the parallel load mode. Q_0 and Q_7 are also brought out on other pins for expansion in serial shifting of longer words.

A Low signal on $\overline{SR}$ overrides the Select inputs and allows the flip-flops to be reset by the next rising edge of CP. All other state changes are also initiated by the Low-to-High CP transition. Inputs can change when the clock is in either state provided only that the recommended setup and hold times, relative to the rising edge of CP, are observed.

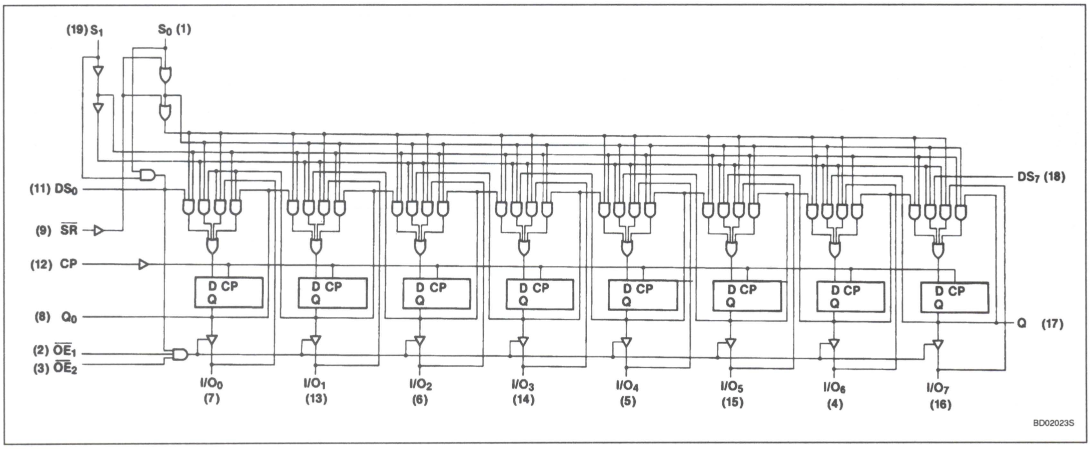
A High signal on either $\overline{OE}_1$ or $\overline{OE}_2$ disables the 3-State buffers and puts the I/O pins in the high impedance state. In this condition the shift, load, hold, and reset operations can still occur. The 3-State buffers are also disabled by High signals on both S_0 and S_1 in preparation for a parallel load operation.

FUNCTION TABLE

INPUTS					OPERATING MODE
$\overline{SR}$	$\overline{OE}_n$	S_1	S_0	CP	
L	L	X	X	X	Synchronous Reset; $Q_0 - Q_7$ = Low
H	L	H	H	↑	Parallel Load; $I/O_n \rightarrow Q_n$
H	L	L	H	↑	Shift Right; $DS_0 \rightarrow Q_0$, $Q_0 \rightarrow Q_1$, etc.
H	L	H	L	↑	Shift Left; $DS_7 \rightarrow Q_7$, $Q_7 \rightarrow Q_6$, etc.
H	L	L	L	X	Hold
X	H	X	X	X	Outputs Disabled

H = High Voltage Level
L = Low Voltage Level
X = Don't care
↑ = Low-to-High Clock Transition

LOGIC DIAGRAM



6

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		−0.5 to +7.0	V
V_{IN}	Input voltage		−0.5 to +7.0	V
I_{IN}	Input current		−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		−0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	Q_0, Q_7	40	mA
		I/O_n	48	mA
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	High-level output current	Q_0, Q_7			−1	mA
		I/O_n			−3	mA
I_{OL}	Low-level output current	Q_0, Q_7			20	mA
		I/O_n			24	mA
T_A	Operating free-air temperature		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			74F323			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage	$Q_0 - Q_7$	$V_{CC} = MIN$, $V_{IL} = MAX$, $I_{OH} = MAX$ $V_{IH} = MIN$,	$I_{OH} = -1mA$	$\pm 10\%V_{CC}$	2.5			V
		I/O_n		$I_{OH} = -3mA$	$\pm 5\%V_{CC}$	2.7	3.4		V
V_{OL}	Low-level output voltage		$V_{CC} = MIN$, $V_{IL} = MAX$, $I_{OL} = MAX$ $V_{IH} = MIN$,		$\pm 10\%V_{CC}$		0.35	0.50	V
					$\pm 5\%V_{CC}$		0.35	0.50	V
V_{IK}	Input clamp voltage		$V_{CC} = MIN$, $I_I = I_{IK}$				-0.73	-1.2	V
I_I	Input current at maximum input voltage	Others	$V_{CC} = MAX$, $V_I = 7.0V$					100	μA
		I/O_n	$V_{CC} = 5.5$, $V_I = 5.5V$					1.0	μA
I_{IH}	High-level input current		$V_{CC} = MAX$, $V_I = 2.7V$					20	μA
I_{IL}	Low-level input current	S_0, S_1	$V_{CC} = MAX$, $V_I = 0.5V$					-1.2	mA
		Others						-0.6	mA
I_{OZH} + I_{IH}	Off-state output current, High-level voltage applied	I/O_n Only	$V_{CC} = MAX$, $V_O = 2.7V$					70	μA
I_{OZL} + I_{IL}	Off-state output current, Low-level voltage applied	I/O_n Only	$V_{CC} = MAX$, $V_O = 0.5V$					-0.6	μA
I_{OS}	Short-circuit output current[3]		$V_{CC} = MAX$			-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	$V_{CC} = MAX$						mA
		I_{CCL}					68	92	mA
		I_{CCZ}							mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at $V_{CC} = 5V$, $T_A = 25°C$.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Register

FAST 74F323

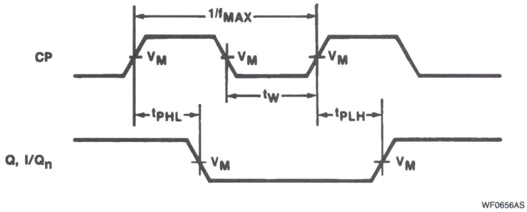
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F323					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum input frequency	Waveform 1	70			70		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_0 or Q_7	Waveform 1	4.0 3.5	7.0 6.5	9.0 8.5	4.0 3.5	10 9.5	ns
t_{PLH} t_{PHL}	Propagation delay CP to I/O_n	Waveform 1	4.0 5.0	7.0 8.5	9.0 11	4.0 5.0	10 12	ns
t_{PZH} t_{PZL}	Output enable time to High or Low level	Waveform 3 Waveform 4	3.5 4.0	6.0 7.0	8.0 10	3.5 4.0	9.0 11	ns
t_{PHZ} t_{PLZ}	Output disable time from High or Low level	Waveform 3 Waveform 4	2.5 2.0	4.5 4.0	6.0 5.5	2.5 2.0	7.0 6.5	ns

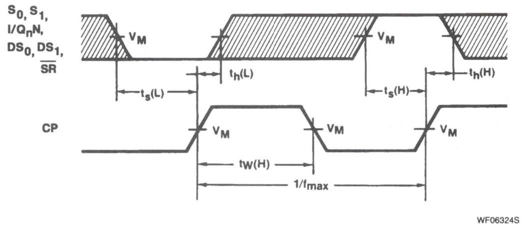
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	74F323					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low S_0 or S_1 to CP	Waveform 2	8.5 8.5					ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low S_0 or S_1 to CP	Waveform 2	0 0					ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low I/O_n, DS_0, DS_7 to CP	Waveform 2	5.0 5.0					ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low I/O_n, DS_0, DS_7 to CP	Waveform 2	2.0 2.0					ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{SR}$ to CP	Waveform 2	10 10					ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{SR}$ to CP	Waveform 2	0 0					ns
$t_w(H)$ $t_w(L)$	CP pulse width, High or Low	Waveform 1	7.0 7.0					ns

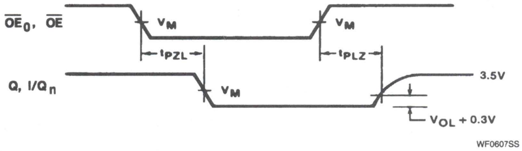
AC WAVEFORMS


1/fMAX
CP
VM
tW
tPHL
tPLH
Q, I/Qn
WF0656AS

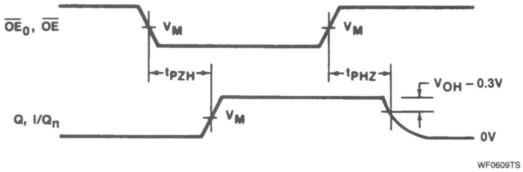
Waveform 1. Clock to Output Delays and Clock Pulse Width


S0, S1, I/QnN, DS0, DS1, SR
VM
th(L)
ts(L)
ts(H)
th(H)
CP
tW(H)
1/fmax
WF06324S

Waveform 2. Data Setup and Hold Times


OE0, OE
VM
tPZL
tPLZ
Q, I/Qn
3.5V
VOL + 0.3V
WF0607SS

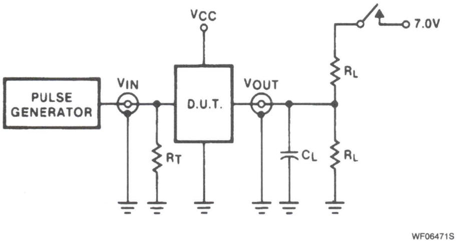
Waveform 3. 3-State Output Enable Time to Low Level and Output Disable Time From Low Level


OE0, OE
VM
tPZH
tPHZ
VOH − 0.3V
Q, I/Qn
0V
WF0609TS

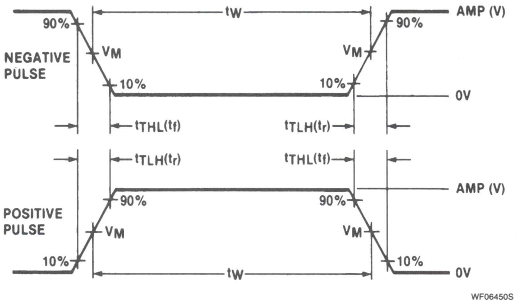
Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time From High Level

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORM


VCC
7.0V
RL
PULSE GENERATOR
VIN
D.U.T.
VOUT
RT
CL
RL
WF06471S

Test Circuit for 3-State Outputs


tW
AMP (V)
90%
NEGATIVE PULSE
VM
10%
0V
tTHL(tf)
tTLH(tr)
POSITIVE PULSE
WF06450S

$V_M = 1.5V$

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS
R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F350
Shifter

4-Bit Shifter (3-State)
Product Specification

FAST Products

FEATURES

- **Shifts 4 bits of data to 0, 1, 2, 3 places under control of two select lines**
- **3-State outputs for bus organized systems**

DESCRIPTION

The 'F350 is a combination logic circuit that shifts a 4-bit word from 0 to 3 places. No clocking is required as with shift registers.

The 'F350 can be used to shift any number of bits any number of places up or down by suitable interconnection. Shifting can be:

1. Logical — with logic zeros filled in at either end of the shifting field.
2. Arithmetic — where the sign bit is extended during a shift down.
3. End around — where the data word forms a continuous loop.

The 3-State outputs are useful for bus interface applications or expansion to a larger number of shift positions in end around shifting. The active-Low Output Enable ($\overline{OE}$) input controls the state of the outputs. The outputs are in the High-impedance "OFF" state when $\overline{OE}$ is High, and they are active when $\overline{OE}$ is Low.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F350	5.2ns	24mA

ORDERING INFORMATION

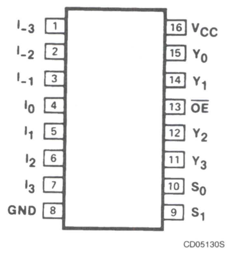
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ± 10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F350N
16-Pin Plastic SO	N74F350D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

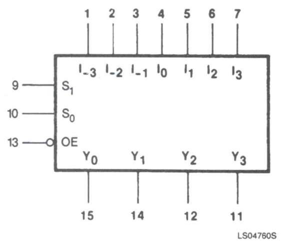
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
S_0, S_1	Select inputs	1.0/2.0	20μA/1.2mA
$I_{-3} - I_3$	Data inputs	1.0/2.0	20μA/1.2mA
$\overline{OE}$	Output enable input (active-Low)	1.0/2.0	20μA/1.2mA
$Y_0 - Y_3$	3-State outputs	150/40	3.0mA/24mA

NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION

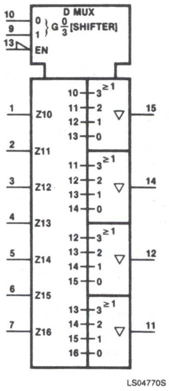

I-3 1
I-2 2
I-1 3
I0 4
I1 5
I2 6
I3 7
GND 8
16 VCC
15 Y0
14 Y1
13 OE
12 Y2
11 Y3
10 S0
9 S1
CD05130S

LOGIC SYMBOL

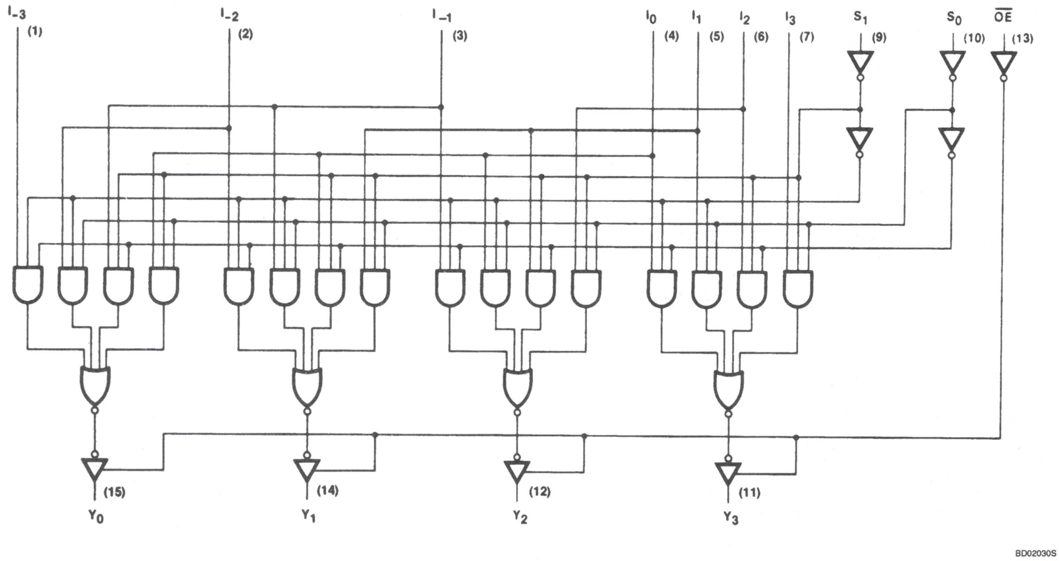

1 2 3 4 5 6 7
I-3 I-2 I-1 I0 I1 I2 I3
9 S1
10 S0
13 OE
Y0 Y1 Y2 Y3
15 14 12 11
LS04760S

V_{CC} = Pin 16
GND = Pin 8

LOGIC SYMBOL (IEEE/IEC)


D MUX
10 0
9 1
G 0/3 [SHIFTER]
13 EN
1 Z10
2 Z11
3 Z12
4 Z13
5 Z14
6 Z15
7 Z16
10 3 ≥1
11 2
12 1
13 0
15
11 3 ≥1
12 2
13 1
14 0
14
12 3 ≥1
13 2
14 1
15 0
12
13 3 ≥1
14 2
15 1
16 0
11
LS04770S

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
( ) = Pin numbers

FUNCTION TABLE

$\overline{OE}$	S_1	S_0	I_3	I_2	I_1	I_0	I_{-1}	I_{-2}	I_{-3}	Y_3	Y_2	Y_1	Y_0
H	X	X	X	X	X	X	X	X	X	Z	Z	Z	Z
L	L	L	D_3	D_2	D_1	D_0	X	X	X	D_3	D_2	D_1	D_0
L	L	H	X	D_2	D_1	D_0	D_{-1}	X	X	D_2	D_1	D_0	D_{-1}
L	H	L	X	X	D_1	D_0	D_{-1}	D_{-2}	X	D_1	D_0	D_{-1}	D_{-2}
L	H	H	X	X	X	D_0	D_{-1}	D_{-2}	D_{-3}	D_0	D_{-1}	D_{-2}	D_{-3}

H = High voltage level
L = Low voltage level
X = Don't care
Z = High-impedance (OFF) state
D_n = High or Low state of referenced I_n input

LOGIC EQUATIONS

$$Y_0 = \overline{S_0} \cdot \overline{S_1} \cdot I_0 + S_0 \cdot \overline{S_1} \cdot I_{-1} + \overline{S_0} \cdot S_1 \cdot I_{-2} + S_0 \cdot S_1 \cdot I_{-3}$$
$$Y_1 = \overline{S_0} \cdot \overline{S_1} \cdot I_1 + S_0 \cdot \overline{S_1} \cdot I_0 + \overline{S_0} \cdot S_1 \cdot I_{-1} + S_0 \cdot S_1 \cdot I_{-2}$$
$$Y_2 = \overline{S_0} \cdot \overline{S_1} \cdot I_2 + S_0 \cdot \overline{S_1} \cdot I_1 + \overline{S_0} \cdot S_1 \cdot I_0 + S_0 \cdot S_1 \cdot I_{-1}$$
$$Y_3 = \overline{S_0} \cdot \overline{S_1} \cdot I_3 + S_0 \cdot \overline{S_1} \cdot I_2 + \overline{S_0} \cdot S_1 \cdot I_1 + S_0 \cdot S_1 \cdot I_0$$

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_A	Operating free-air temperature range	0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−3	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature	0		70	°C

Shifter

FAST 74F350

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		74F350			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX V_{IH} = MIN,	±10%V_{CC}	2.4			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OL} = MAX V_{IH} = MIN,	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				−1.2	mA
I_{OZH}	Off-state output current, High-level voltage applied		V_{CC} = MAX, V_O = 2.7V				50	μA
I_{OZL}	Off-state output current, Low-level voltage applied		V_{CC} = MAX, V_O = 0.5V				−50	μA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX, V_O = 0.0V		−60		−150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			22	35	mA
		I_{CCL}				26	41	mA
		I_{CCZ}				26	42	mA

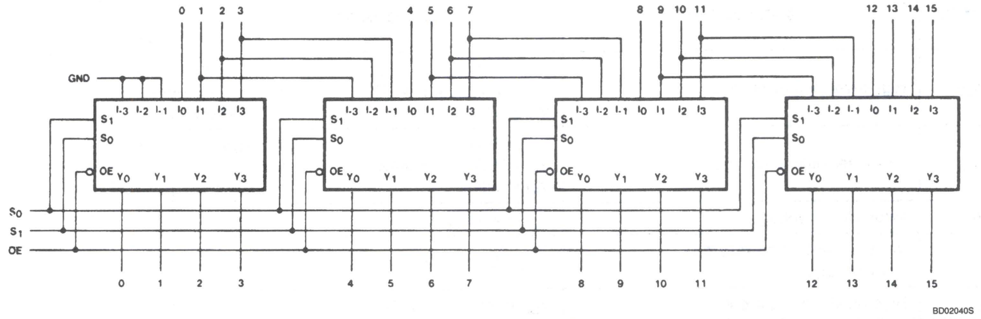
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

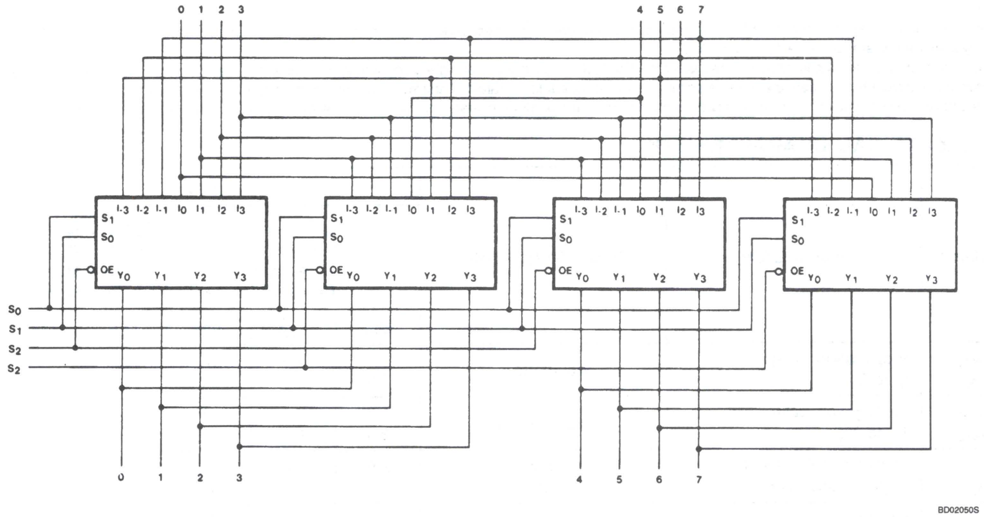
SYMBOL	PARAMETER	TEST CONDITIONS	74F350					UNIT
			T_A = +25°C V_{CC} = +5.0V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_n to Y_n	Waveform 1	3.0 2.5	4.5 4.0	6.0 5.5	3.0 2.5	7.0 6.5	ns
t_{PLH} t_{PHL}	Propagation delay S_n to Y_n	Waveform 1	4.0 3.0	7.8 6.5	10 8.5	4.0 3.0	11 9.5	ns
t_{PZH} t_{PZL}	Output enable time to High or Low level	Waveform 2 Waveform 3	2.5 4.0	5.0 7.0	7.0 9.0	2.5 4.0	8.0 10	ns
t_{PHZ} t_{PLZ}	Output disable time from High or Low level	Waveform 2 Waveform 3	2.0 2.0	3.9 4.0	5.5 5.5	2.0 2.0	6.5 6.5	ns

APPLICATIONS


0 1 2 3
4 5 6 7
8 9 10 11
12 13 14 15
GND
S1
S0
OE
I-3 I-2 I-1 I0 I1 I2 I3
Y0 Y1 Y2 Y3
S0
S1
OE
0 1 2 3
4 5 6 7
8 9 10 11
12 13 14 15
BD02040S

S_2	S_1S_0	
L	L L	No shift
L	L H	Shift end around 1
L	H L	Shift end around 2
L	H H	Shift end around 3
H	L L	Shift end around 4
H	L H	Shift end around 5
H	H L	Shift end around 6
H	H H	Shift end around 7

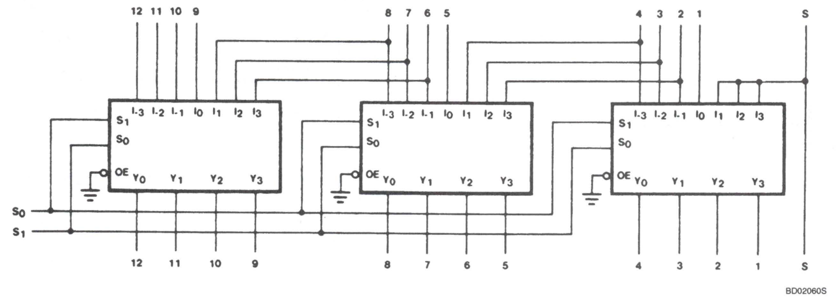
8-Bit End Around Shift 0, 1, 2, 3, 4, 5, 6, 7 Places


0 1 2 3
4 5 6 7
S1
S0
OE
I-3 I-2 I-1 I0 I1 I2 I3
Y0 Y1 Y2 Y3
S0
S1
S2
S2
0 1 2 3
4 5 6 7
BD02050S

S_1	S_0	Scale
L	L ÷ 8	1/8
L	H ÷ 4	1/4
H	L ÷ 2	1/2
H	H No change	1

13-Bit Two's Complement Scaler

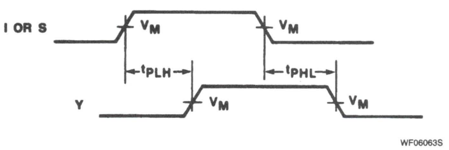
APPLICATIONS (Continued)


12 11 10 9
8 7 6 5
4 3 2 1
S
I-3 I-2 I-1 I0 I1 I2 I3
S1
S0
OE
Y0 Y1 Y2 Y3
S0
S1
12 11 10 9
8 7 6 5
4 3 2 1
S
BD02060S

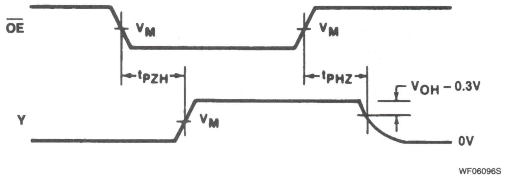
S_1	S_0	
L	L	No shift
L	H	Shift 1 place
H	L	Shift 2 places
H	H	Shift 3 places

16-Bit Shift Up 0, 1, 2, or 3 Places

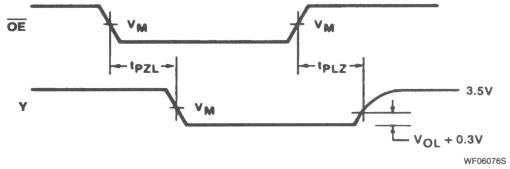
AC WAVEFORMS


I OR S
VM
VM
tPLH
tPHL
Y
VM
VM
WF06063S

Waveform 1. Propogation Delay Data and Select to Output


OE
VM
VM
tPZH
tPHZ
VOH – 0.3V
Y
VM
0V
WF06096S

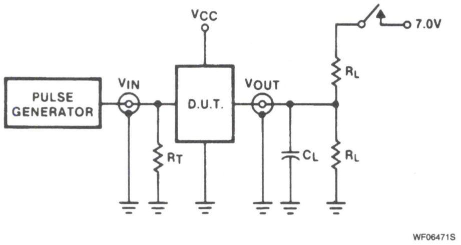
Waveform 2. 3-State Output Enable Time to High Level and Output Disable Time From High Level


OE
VM
VM
tPZL
tPLZ
3.5V
Y
VM
VOL + 0.3V
WF06076S

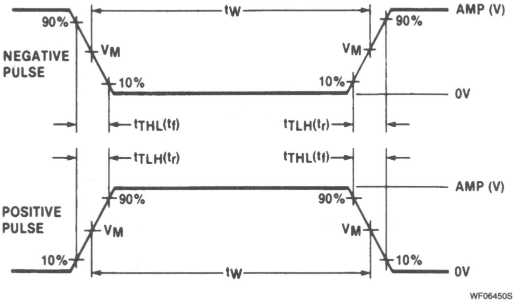
Waveform 3. 3-State Output Enable Time to Low Level and Output Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORM


VCC
7.0V
RL
PULSE GENERATOR
VIN
D.U.T.
VOUT
RT
CL
RL
WF06471S

Test Circuit for 3-State Outputs


NEGATIVE PULSE
90%
VM
10%
tW
AMP (V)
0V
tTHL(tf)
tTLH(tr)
tTLH(tr)
tTHL(tf)
POSITIVE PULSE
90%
VM
10%
tW
AMP (V)
0V
WF06450S

$V_M = 1.5V$

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F352
Multiplexer

Dual 4-Line to 1-Line Multiplexer
Product Specification

FAST Products

FEATURES
- **Inverting version of 'F153**
- **Separate Enable for each multiplexer section**
- **Common Select inputs**
- **See 'F353 for 3-State version**

DESCRIPTION
The 'F352 has a dual 4-input multiplexer that can select 2 bits of data from up to eight sources under control of the common Select inputs (S_0, S_1). The two 4-input multiplexer circuits have individual active-Low Enables ($\overline{E}_a$, $\overline{E}_b$) which can be used to strobe the outputs independently. Outputs ($\overline{Y}_a$, $\overline{Y}_b$) are forced High when the corresponding Enables ($\overline{E}_a$, $\overline{E}_b$) are High.

The device is the logical implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the two Select inputs.

The 'F352 can be used to move data to a common output bus from a group of registers. The state of the Select inputs would determine the particular register from which the data came. An alternative application is as a function generator. The device can generate two functions or three variables. This is useful for implementing highly irregular random logic.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F352	5.5ns	10mA

ORDERING INFORMATION

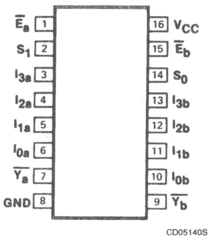
PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
16-Pin Plastic DIP	N74F352N
16-Pin Plastic SO	N74F352D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$I_{0a} - I_{3a}$	Port A data inputs	1.0/1.0	20µA/0.6mA
$I_{0b} - I_{3b}$	Port B data inputs	1.0/1.0	20µA/0.6mA
S_0, S_1	Common select inputs	1.0/1.0	20µA/0.6mA
$\overline{E}_a$, $\overline{E}_b$	Port A, B enable inputs (active-Low)	1.0/1.0	20µA/0.6mA
$\overline{Y}_a$, $\overline{Y}_b$	Multiplexer outputs	50/33	1.0mA/20mA

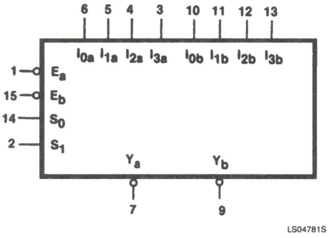
NOTE:
1. One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



$\overline{E}_a$ 1
S_1 2
I_{3a} 3
I_{2a} 4
I_{1a} 5
I_{0a} 6
$\overline{Y}_a$ 7
GND 8
16 V_{CC}
15 $\overline{E}_b$
14 S_0
13 I_{3b}
12 I_{2b}
11 I_{1b}
10 I_{0b}
9 $\overline{Y}_b$
CD05140S

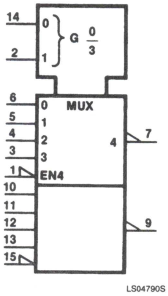
LOGIC SYMBOL



6 5 4 3 10 11 12 13
I_{0a} I_{1a} I_{2a} I_{3a} I_{0b} I_{1b} I_{2b} I_{3b}
1 E_a
15 E_b
14 S_0
2 S_1
Y_a
Y_b
7
9
LS04781S

V_{CC} = Pin 16
GND = Pin 8

LOGIC SYMBOL (IEEE/IEC)

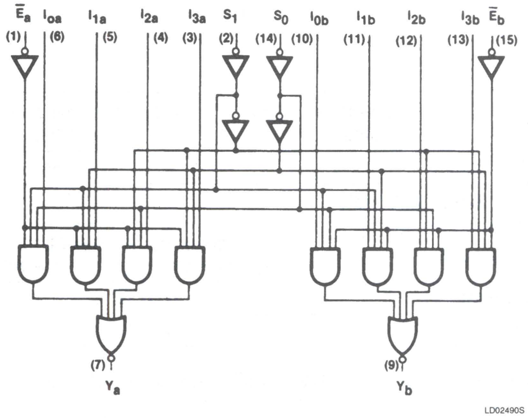


14
2
0
1
G $\frac{0}{3}$
MUX
6 0
5 1
4 2
3 3
1 EN4
4
7
10
11
12
13
15
9
LS04790S

Multiplexer

FAST 74F352

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8

FUNCTION TABLE

INPUTS							OUTPUT
S_0	S_1	$\overline{E}$	I_{0n}	I_{1n}	I_{2n}	I_{3n}	$\overline{Y}_n$
X	X	H	X	X	X	X	H
L	L	L	L	X	X	X	H
L	L	L	H	X	X	X	L
H	L	L	X	L	X	X	H
H	L	L	X	H	X	X	L
L	H	L	X	X	L	X	H
L	H	L	X	X	H	X	L
H	H	L	X	X	X	L	H
H	H	L	X	X	X	H	L

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		74F352 Min	74F352 Typ[2]	74F352 Max	UNIT
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.5			V
			±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}		0.35	0.50	V
			±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total) I_{CCH}	V_{CC} = MAX	$\overline{E}_n = S_n = I_n$ = GND		8	14	mA
	I_{CCL}		$\overline{E}_n$ = GND, $S_n = I_n$ = 4.5V		12	20	mA

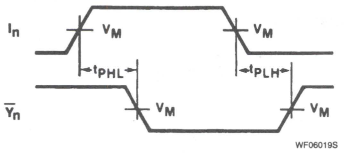
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

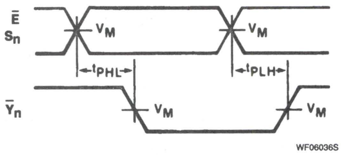
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F352 T_A = +25°C V_{CC} = +5.0V C_L = 50pF R_L = 500Ω Min	Typ	Max	T_A = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF R_L = 500Ω Min	Max	UNIT
t_{PLH} t_{PHL}	Propagation delay I_{on} to $\overline{Y}_n$	Waveform 1	2.5 1.5	5.0 3.0	7.0 4.5	2.0 1.0	8.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{Y}_n$	Waveform 2	4.5 4.0	6.5 6.0	11.0 8.5	4.0 3.5	12.5 9.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}_n$ to $\overline{Y}_n$	Waveform 2	2.5 3.5	5.0 6.0	6.5 8.0	2.0 3.0	7.0 8.5	ns

AC WAVEFORMS


I_n
V_M
V_M
t_{PHL}
t_{PLH}
$\overline{Y}_n$
V_M
V_M
WF06019S

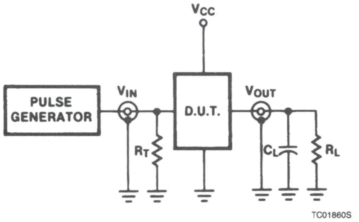
Waveform 1. Propagation Delay for Data to Output


$\overline{E}$
S_n
V_M
V_M
t_{PHL}
t_{PLH}
$\overline{Y}_n$
V_M
V_M
WF06036S

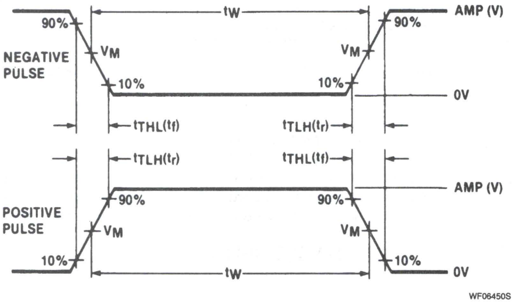
Waveform 2. Propagation Delay for Select or Enable to Output

NOTE: For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORM


V_{CC}
PULSE GENERATOR
V_{IN}
D.U.T.
V_{OUT}
R_T
C_L
R_L
TC01860S

Test Circuit for Totem-Pole Outputs


NEGATIVE PULSE
90%
V_M
10%
t_W
90%
V_M
10%
AMP (V)
0V
$t_{THL}(t_f)$
$t_{TLH}(t_r)$
$t_{TLH}(t_r)$
$t_{THL}(t_f)$
POSITIVE PULSE
90%
V_M
10%
90%
V_M
10%
AMP (V)
0V
t_W
WF06450S

$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F353
Multiplexer

Dual 4-Input Multiplexer (3-State)
Product Specification

FAST Products

FEATURES

- **Inverting version of 'F253**
- **3-State outputs for bus interface and multiplex expansion**
- **Common Select inputs**
- **Separate Output Enable inputs**

DESCRIPTION

The 'F353 has two identical 4-input multiplexers with 3-State outputs which select two bits from eight sources selected by common Select inputs (S_0, S_1). When the individual Output Enable ($\overline{E}_{0a}$, $\overline{E}_{0b}$) inputs of the 4-input multiplexers are High, the outputs are forced to a High-impedance (Hi-Z) state.

The 'F353 is the logic implementation of a 2-pole, 4-position switch; the position of the switch being determined by the logic levels supplied to the two Select inputs.

Logic equations for the outputs are shown below:

$$\overline{Y}_a = \overline{OE}_a \bullet (I_{0a} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1a} \bullet \overline{S}_1 \bullet S_0 + I_{2a} \bullet S_1 \bullet \overline{S}_0 + I_{3a} \bullet S_1 \bullet S_0)$$

$$\overline{Y}_b = \overline{OE}_b \bullet (I_{0b} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1b} \bullet \overline{S}_1 \bullet S_0 + I_{2b} \bullet S_1 \bullet \overline{S}_0 + I_{3b} \bullet S_1 \bullet S_0)$$

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F353	6.0ns	11mA

ORDERING INFORMATION

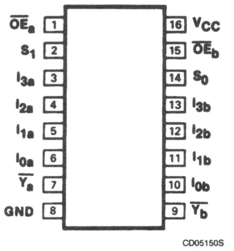
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ± 10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F353N
16-Pin Plastic SO	N74F353D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

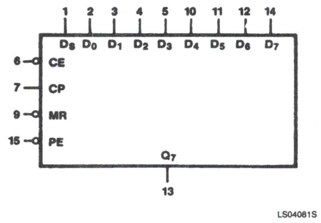
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$I_{0a} - I_{3a}$	Port A data inputs	1.0/1.0	20μA/0.6mA
$I_{0b} - I_{1b}$	Port B data inputs	1.0/1.0	20μA/0.6mA
S_0, S_1	Common select inputs	1.0/1.0	20μA/0.6mA
$\overline{OE}_a$, $\overline{OE}_b$	Port A, B output enable inputs (active-Low)	1.0/1.0	20μA/0.6mA
$\overline{Y}_a$, $\overline{Y}_b$	3-State outputs (inverted)	150/40	3.0mA/24mA

NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION

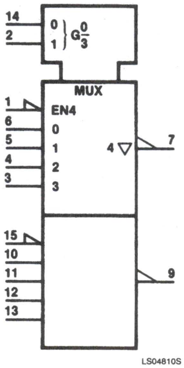

OE̅a 1
S1 2
I3a 3
I2a 4
I1a 5
I0a 6
Y̅a 7
GND 8
16 VCC
15 OE̅b
14 S0
13 I3b
12 I2b
11 I1b
10 I0b
9 Y̅b
CD05150S

LOGIC SYMBOL


1 2 3 4 5 10 11 12 14
DS D0 D1 D2 D3 D4 D5 D6 D7
6 CE
7 CP
9 MR
15 PE
Q7
13
LS04081S

V_{CC} = Pin 16
GND = Pin 8

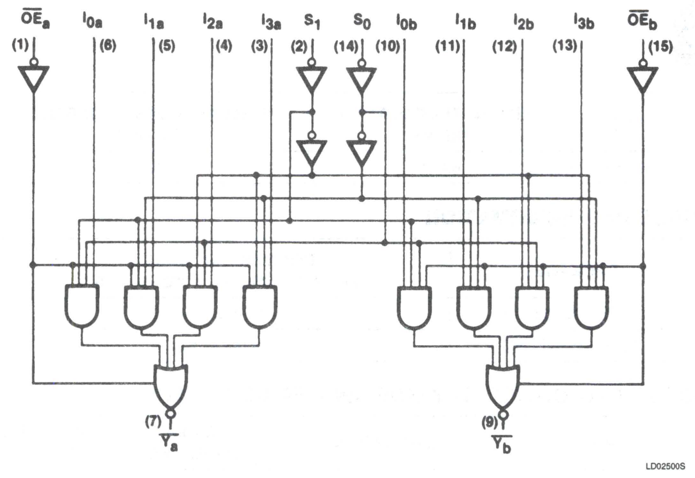
LOGIC SYMBOL (IEEE/IEC)


14
2
0
1
G 0/3
MUX
1
EN4
6 0
5 1
4 2
3 3
4
7
15
10
11
12
13
9
LS04810S

Multiplexer

FAST 74F353

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8

FUNCTION TABLE

INPUTS							OUTPUT
S_0	S_1	I_0	I_1	I_2	I_3	$\overline{OE}$	Y
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	H
L	L	H	X	X	X	L	L
H	L	X	L	X	X	L	H
H	L	X	H	X	X	L	L
L	H	X	X	L	X	L	H
L	H	X	X	H	X	L	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	L	L

H = High voltage level
L = Low voltage level
X = Don't care
Z = High-impedance (OFF) state

All but one device must be in the High-impedance state to avoid high currents exceeding the maximum ratings, if the outputs of the 3-State devices are tied together. Design of the Output Enable signals must ensure that there is no overlap.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_A	Operating free-air temperature range	0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−3	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		74F353			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.4			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				−0.6	mA
I_{OZH}	Off-state output current, High-level voltage applied		V_{CC} = MAX, V_O = 2.7V				50	μA
I_{OZL}	Off-state output current Low-level voltage applied		V_{CC} = MAX, V_O = 0.5V				−50	μA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	$\overline{OE}_n = S_n = I_n$ = GND		9	14	mA
		I_{CCL}		$S_n = \overline{OE}_n$ = GND; I_n = 4.5		11	20	mA
		I_{CCZ}		$\overline{OE}_n$ = 4.5V; $S_n = I_n$ = GND		13	23	mA

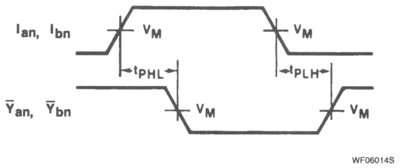
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

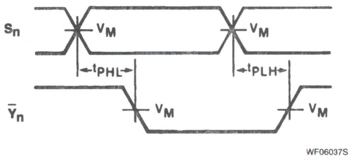
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F353					UNIT
			T_A = +25°C V_{CC} = +5.0V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_n to $\overline{Y}_n$	Waveform 1	3.0 1.5	5.0 3.0	7.0 5.0	3.0 1.0	8.0 5.5	ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{Y}_n$	Waveform 2	5.0 3.0	9.0 6.0	12.0 8.5	4.5 3.0	12.5 9.5	ns
t_{PZH} t_{PZL}	Output enable time to High or Low level	Waveform 3 Waveform 4	4.0 4.0	6.0 6.5	8.0 8.0	3.5 3.5	9.0 9.0	ns
t_{PHZ} t_{PLZ}	Output disable time from High or Low level	Waveform 3 Waveform 4	2.5 1.5	4.0 2.5	5.5 6.0	2.0 1.5	6.0 7.0	ns

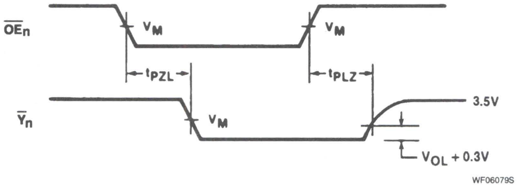
AC WAVEFORMS


Ian, Ibn
VM
VM
tPHL
tPLH
Ȳan, Ȳbn
VM
VM
WF06014S

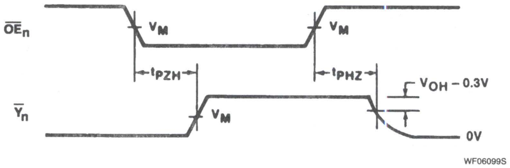
Waveform 1. Propagation Delay (I_n) to Output (Y_n)


Sn
VM
VM
tPHL
tPLH
Ȳn
VM
VM
WF06037S

Waveform 2. Propagation Delay Select (S_n) to Output (Y_n)


OEn
VM
VM
tPZL
tPLZ
Ȳn
VM
3.5V
VOL + 0.3V
WF06079S

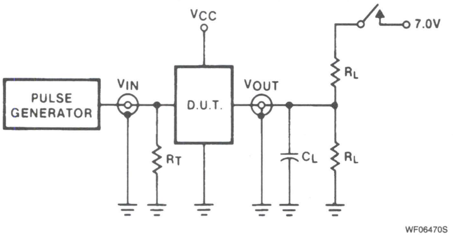
Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time From High Level


OEn
VM
VM
tPZH
tPHZ
VOH – 0.3V
Ȳn
VM
0V
WF06099S

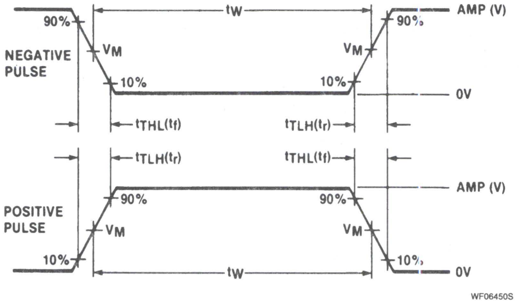
Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORM


VCC
7.0V
RL
PULSE GENERATOR
VIN
D.U.T.
VOUT
RT
CL
RL
WF06470S

Test Circuit for 3-State Outputs


90%
tW
90%
AMP (V)
NEGATIVE PULSE
VM
VM
10%
10%
0V
tTHL(tf)
tTLH(tr)
tTLH(tr)
tTHL(tf)
AMP (V)
90%
90%
POSITIVE PULSE
VM
VM
10%
10%
tW
0V
WF06450S

$V_M = 1.5V$

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST Products

FAST 74F365, F366, F367, F368
Buffers/Drivers

'F365, 'F367 Hex Buffer/Driver (3-State)
'F366, 'F368 Hex Inverter Buffer (3-State)
Product Specification

FEATURES

- High-impedance NPN base inputs for reduced loading (20μA in Low and High states)
- 3-State buffer outputs sink 64mA
- High-speed
- Bus-oriented

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F365	5.0ns	36mA
74F366	5.0ns	33mA
74F367	5.0ns	36mA
74F368	5.0ns	33mA

FUNCTION TABLE, 'F365, 'F366

INPUTS			OUTPUTS	
$\overline{OE}_1$	$\overline{OE}_2$	I	Y_n	$\overline{Y}_n$
L	L	L	L	H
L	L	H	H	L
X	H	X	Z	Z
H	X	X	Z	Z

FUNCTION TABLE, 'F367, 'F368

INPUTS		OUTPUTS	
$\overline{OE}_n$	I	Y_n	$\overline{Y}_n$
L	L	L	H
L	H	H	L
H	X	Z	Z

L = Low voltage level
H = High voltage level
X = Don't care
Z = High-impedance (OFF) state

ORDERING INFORMATION

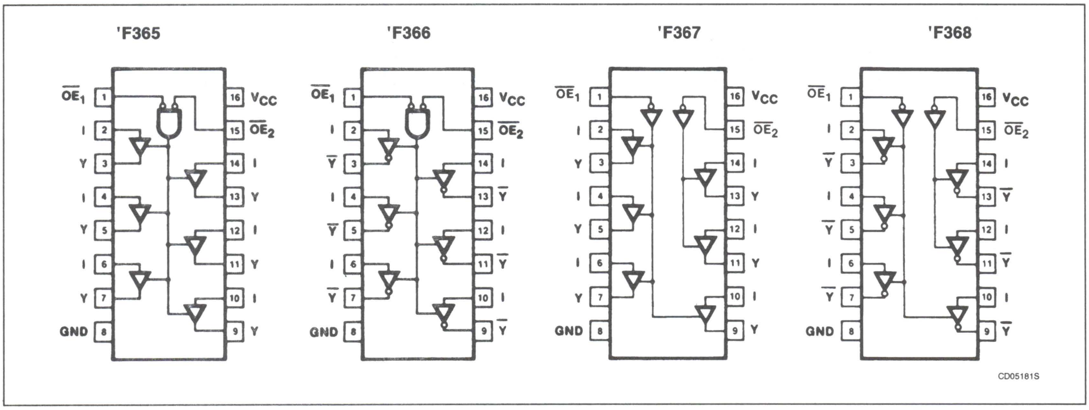
PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
16-Pin Plastic DIP	N74F365N, N74F366N N74F367N, N74F368N
16-Pin Plastic SO	N74F365D, N74F366D N74F367D, N74F368D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

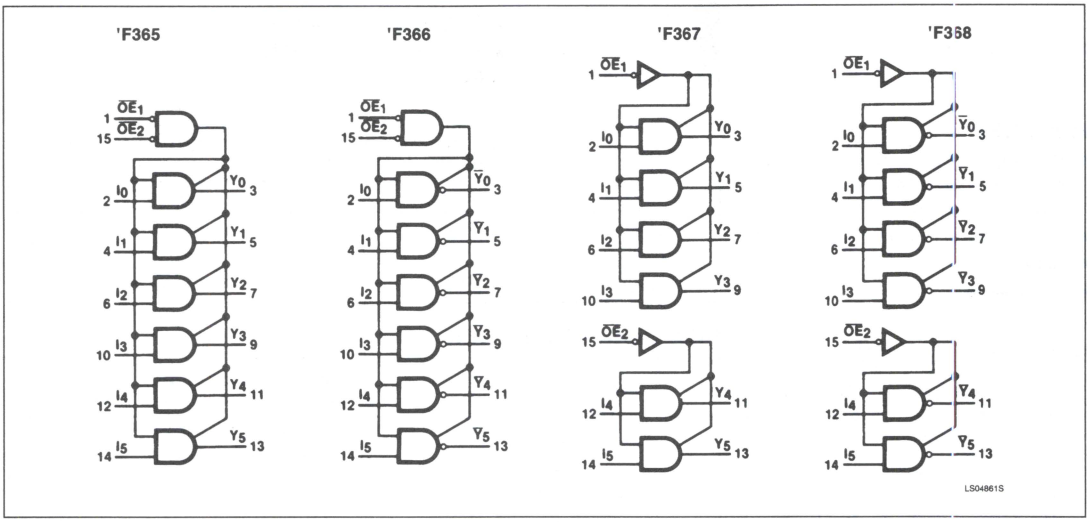
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$\overline{OE}_1$, $\overline{OE}_2$	3-State output enable input (active-Low)	1.0/0.033	20μA/20μA
$I_0 - I_5$	Inputs	1.0/0.033	20μA/20μA
$Y_0 - Y_5$, $\overline{Y}_0 - \overline{Y}_5$	Outputs	750/106.7	15mA/64mA

NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

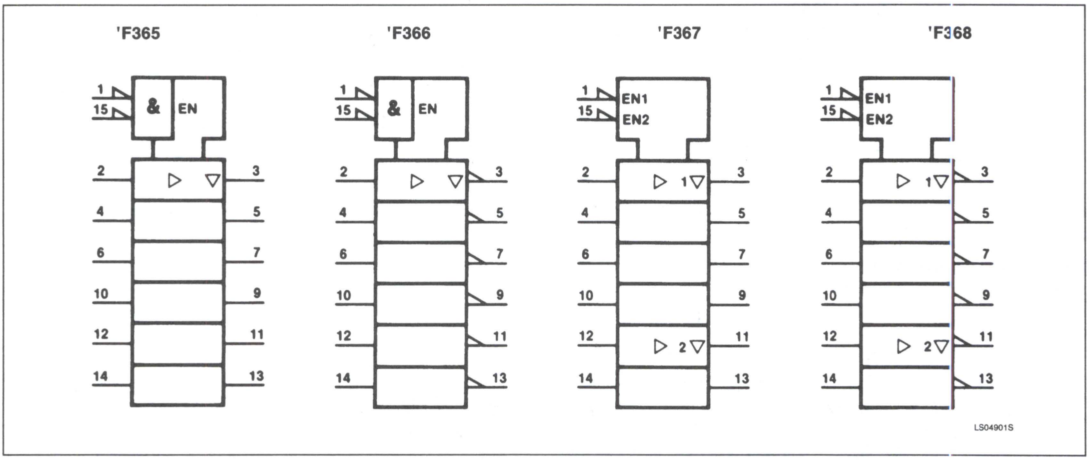
PIN CONFIGURATION



LOGIC SYMBOL


'F365
'F366
'F367
'F368
$\overline{OE}_1$
$\overline{OE}_2$
I_0
I_1
I_2
I_3
I_4
I_5
Y_0
Y_1
Y_2
Y_3
Y_4
Y_5
$\overline{Y}_0$
$\overline{Y}_1$
$\overline{Y}_2$
$\overline{Y}_3$
$\overline{Y}_4$
$\overline{Y}_5$
1
15
2
3
4
5
6
7
10
9
12
11
14
13
LS04861S

LOGIC SYMBOL (IEEE/IEC)


'F365
'F366
'F367
'F368
&
EN
EN1
EN2
1▽
2▽
1
15
2
3
4
5
6
7
10
9
12
11
14
13
LS04901S

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	128	mA
T_A	Operating free-air temperature range	0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−15	mA
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]			74F365, 'F366 'F367, 'F368			UNIT
							Min	Typ[2]	Max	
V_{OH}	High-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = −3mA	±10%V_{CC}	2.4			V
						±5%V_{CC}	2.7	3.4		V
					I_{OH} = −15mA	±10%V_{CC}	2.0			V
						±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 48mA	±10%V_{CC}		0.35	0.50	V
					I_{OL} = 64mA	±5%V_{CC}		0.40	0.55	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, I_I = I_{IK}				−0.73	−1.2	V
I_I	Input current at maximum input voltage			V_{CC} = 0.0V, V_I = 7.0V					100	μA
I_{IH}	High-level input current			V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	Low-level input current			V_{CC} = MAX, V_I = 0.5V					−20	μA
I_{OZH}	Off-state current High-level voltage applied			V_{CC} = MAX, V_O = 2.7V					50	μA
I_{OZL}	Off-state current Low-level voltage applied			V_{CC} = MAX, V_O = 0.5V					−50	μA
I_{OS}	Short-circuit output current[3]			V_{CC} = MAX			−100		−225	mA
I_{CC}	Supply current (total)	'F365, 'F367	I_{CCH}	V_{CC} = MAX				25	35	mA
			I_{CCL}					47	62	mA
			I_{CCZ}					35	48	mA
		'F366, 'F368	I_{CCH}					18	25	mA
			I_{CCL}					47	62	mA
			I_{CCZ}					35	48	mA

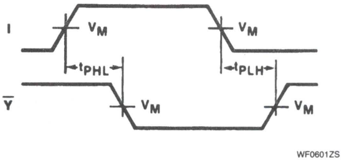
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

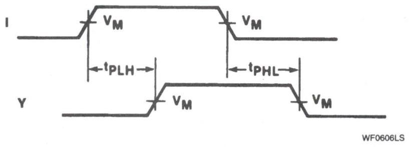
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	74F365, 'F366, 'F367, 'F368					UNIT
				T_A = +25°C V_{CC} = +5.0V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF R_L = 500Ω		
				Min	Typ	Max	Min	Max	
t_{PLH}	Propagation delay I_n to $\overline{Y}_n$	'F366, 'F368	Waveform 1	3.0	5.0	6.5	3.0	7.5	ns
t_{PHL}				2.0	3.0	5.0	1.5	5.5	
t_{PLH}	Propagation delay I_n to Y_n	'F365, 'F367	Waveform 2	2.5	4.5	6.5	2.0	7.0	ns
t_{PHL}				2.5	5.5	7.0	2.0	7.5	
t_{PZH}	Output enable time to High or Low level	'F365, 'F366	Waveform 3 & 4	2.5	6.5	9.5	2.5	10.0	ns
t_{PZL}				2.5	6.0	9.0	2.5	9.5	
t_{PZH}	Output enable time to High or Low level	'F367, 'F368	Waveform 3 & 4	3.0	5.5	7.5	3.0	8.5	ns
t_{PZL}				3.0	6.5	8.5	3.0	9.0	
t_{PHZ}	Output disable time from High or Low level		Waveform 3 & 4	2.0	4.5	6.5	2.0	7.0	ns
t_{PLZ}				2.0	4.0	6.5	2.0	7.0	

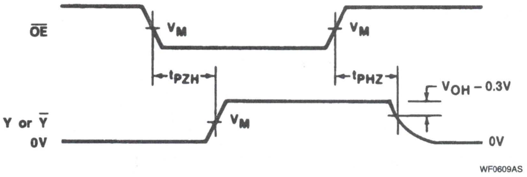
AC WAVEFORMS


I
VM
VM
tPHL
tPLH
Y̅
VM
VM
WF0601ZS

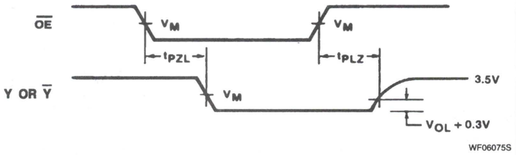
Waveform 1. For Inverting Outputs


I
VM
VM
tPLH
tPHL
Y
VM
VM
WF0606LS

Waveform 2. For Non-Inverting Outputs


OE̅
VM
VM
tPZH
tPHZ
VOH − 0.3V
Y or Y̅
0V
VM
0V
WF0609AS

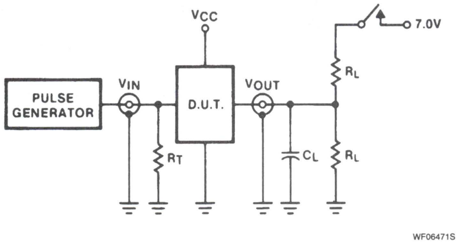
Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time From High Level


OE̅
VM
VM
tPZL
tPLZ
3.5V
Y OR Y̅
VM
VOL + 0.3V
WF06075S

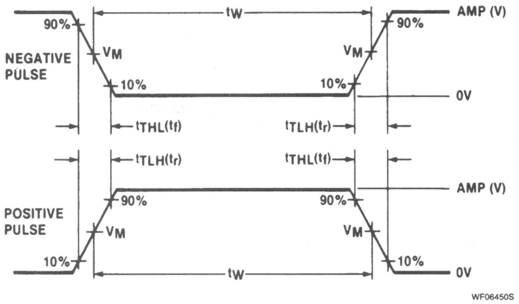
Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORMS


VCC
7.0V
PULSE GENERATOR
VIN
D.U.T.
VOUT
RL
RT
CL
RL
WF06471S

Test Circuit for 3-State Outputs


90%
tW
AMP (V)
90%
NEGATIVE PULSE
VM
VM
10%
10%
0V
tTHL(tf)
tTLH(tr)
tTLH(tr)
tTHL(tf)
AMP (V)
90%
90%
POSITIVE PULSE
VM
VM
10%
10%
0V
tW
WF06450S

$V_M = 1.5V$

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor to GND; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F373, 74F374

Latches/Flip-Flops

'F373 Octal Transparent Latch (3-State)
'F374 Octal D Flip-Flop (3-State)
Product Specification

FAST Products

FEATURES

- **8-bit transparent latch – 'F373**
- **8-bit positive, edge-triggered register – 'F374**
- **3-State output buffers**
- **Common 3-State Output Enable**
- **Independent register and 3-State buffer operation**

DESCRIPTION

The 'F373 is an octal transparent latch coupled to eight 3-State output buffers. The two sections of the device are controlled independently by Enable (E) and Output Enable ($\overline{OE}$) control gates.

The data on the D inputs are transferred to the latch outputs when the Latch Enable (E) input is High. The latch remains transparent to the data inputs while E is High, and stores the data that is present one setup time before the High-to-Low enable transition.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active-Low Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the latch operation.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F373	4.5ns	35mA
74F374	6.5ns	55mA

ORDERING INFORMATION

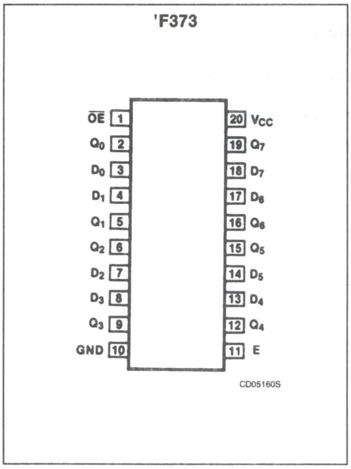
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V=14± 10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F373N, N74F374N
20-Pin Plastic SOL	N74F373D, N74F374D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

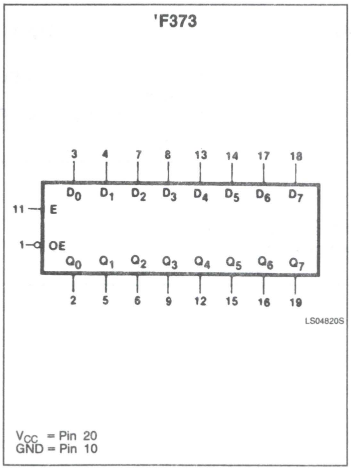
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$D_0 - D_7$	Data inputs	1.0/1.0	20μA/0.6mA
E ('F373)	Latch enable input (active-High)	1.0/1.0	20μA/0.6mA
$\overline{OE}$	Output enable input (active-Low)	1.0/1.0	20μA/0.6mA
CP ('F374)	Clock Pulse input (active rising edge)	1.0/1.0	20μA/0.6mA
$Q_0 - Q_7$	3-State outputs	150/40	3mA/24mA

NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION

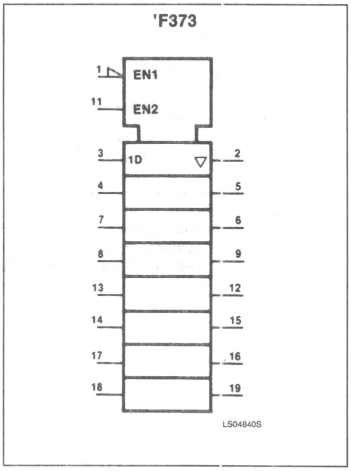

'F373
$\overline{OE}$ 1
Q0 2
D0 3
D1 4
Q1 5
Q2 6
D2 7
D3 8
Q3 9
GND 10
20 Vcc
19 Q7
18 D7
17 D6
16 Q6
15 Q5
14 D5
13 D4
12 Q4
11 E
CD05160S

LOGIC SYMBOL


'F373
3 4 7 8 13 14 17 18
D0 D1 D2 D3 D4 D5 D6 D7
11 E
1 OE
Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
2 5 6 9 12 15 16 19
LS04820S

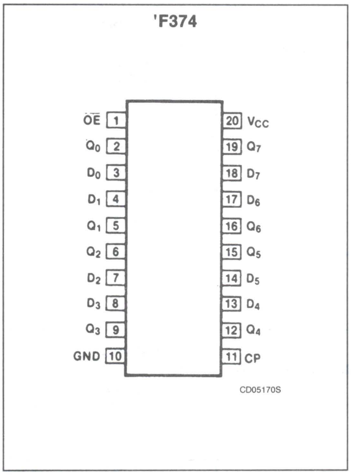
V_{CC} = Pin 20
GND = Pin 10

LOGIC SYMBOL (IEEE/IEC)


'F373
1 EN1
11 EN2
3 1D 2
4 5
7 6
8 9
13 12
14 15
17 16
18 19
LS04840S

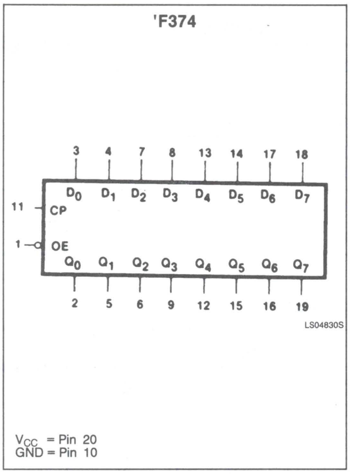
PIN CONFIGURATION

'F374


$\overline{OE}$ 1
Q_0 2
D_0 3
D_1 4
Q_1 5
Q_2 6
D_2 7
D_3 8
Q_3 9
GND 10
20 V_{CC}
19 Q_7
18 D_7
17 D_6
16 Q_6
15 Q_5
14 D_5
13 D_4
12 Q_4
11 CP
CD05170S

LOGIC SYMBOL

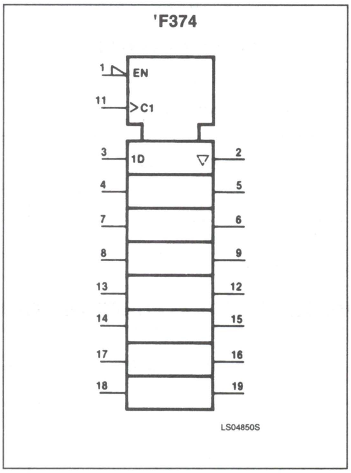
'F374


3 4 7 8 13 14 17 18
D_0 D_1 D_2 D_3 D_4 D_5 D_6 D_7
11 CP
1 OE
Q_0 Q_1 Q_2 Q_3 Q_4 Q_5 Q_6 Q_7
2 5 6 9 12 15 16 19
LS04830S

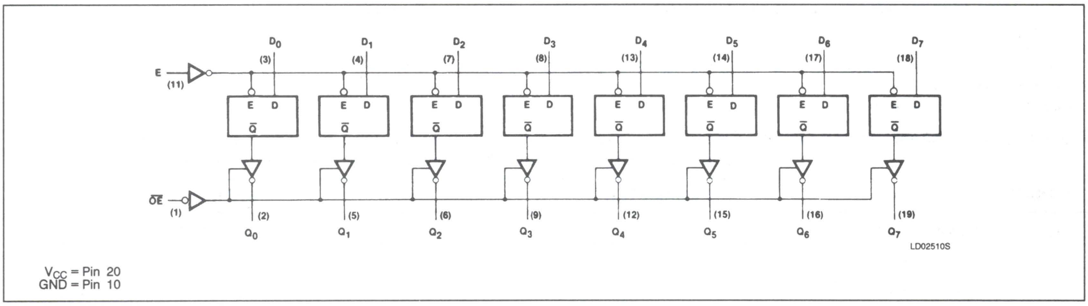
V_{CC} = Pin 20
GND = Pin 10

LOGIC SYMBOL (IEEE/IEC)

'F374

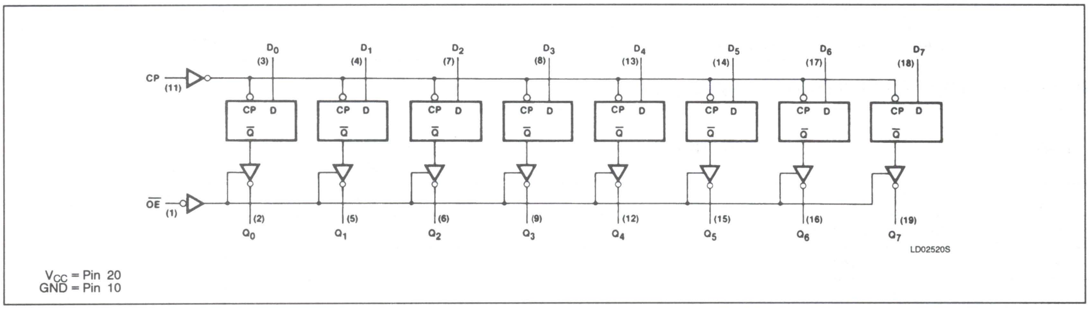

1 EN
11 >C1
3 1D 2
4 5
7 6
8 9
13 12
14 15
17 16
18 19
LS04850S

LOGIC DIAGRAM, 'F373


E (11)
D_0 (3) D_1 (4) D_2 (7) D_3 (8) D_4 (13) D_5 (14) D_6 (17) D_7 (18)
E D
$\overline{Q}$
$\overline{OE}$ (1)
(2) Q_0 (5) Q_1 (6) Q_2 (9) Q_3 (12) Q_4 (15) Q_5 (16) Q_6 (19) Q_7
LD02510S

V_{CC} = Pin 20
GND = Pin 10

LOGIC DIAGRAM, 'F374


CP (11)
D_0 (3) D_1 (4) D_2 (7) D_3 (8) D_4 (13) D_5 (14) D_6 (17) D_7 (18)
CP D
$\overline{Q}$
$\overline{OE}$ (1)
(2) Q_0 (5) Q_1 (6) Q_2 (9) Q_3 (12) Q_4 (15) Q_5 (16) Q_6 (19) Q_7
LD02520S

V_{CC} = Pin 20
GND = Pin 10

When $\overline{OE}$ is Low, the latched or transparent data appears at the outputs. When $\overline{OE}$ is High, the outputs are in the High-impedance "OFF" state, which means they will neither drive nor load the bus.

The 'F374 is an 8-bit, edge-triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by the Clock (CP) and Output Enable ($\overline{OE}$) control gates. The register is fully edge triggered. The state of each D input, one setup time before the Low-to-High clock transition, is transferred to the corresponding flip-flop's Q output.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active-Low Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the register operation. When $\overline{OE}$ is Low, the data in the register appears at the outputs. When $\overline{OE}$ is High, the outputs are in the High-impedance "OFF" state, which means they will neither drive nor load the bus.

MODE SELECT — FUNCTION TABLE, 'F373

OPERATING MODES	INPUTS			INTERNAL REGISTER	OUTPUTS
	$\overline{OE}$	E	D_n		$Q_0 - Q_7$
Enable and read register	L L	H H	L H	L H	L H
Latch and read register	L L	↓ ↓	l h	L H	L H
Hold	L	L	X	NC	NC
Disable outputs	H	X	X	X	Z

NC = No change

MODE SELECT — FUNCTION TABLE, 'F374

OPERATING MODES	INPUTS			INTERNAL REGISTER	OUTPUTS
	$\overline{OE}$	CP	D_n		$Q_0 - Q_7$
Load and read register	L L	↑ ↑	l h	L H	L H
Disable outputs	H	X	X	X	Z

H = High voltage level
h = High voltage level one setup time prior to the Low-to-High clock transition or High-to-Low E transition
L = Low voltage level
X = Don't care
l = Low voltage level one setup time prior to the Low-to-High clock transition or High-to-Low E transition
Z = High-impedance "OFF" state
↑ = Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_A	Operating free-air temperature range	0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−3	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		74F373, 'F374			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX V_{IH} = MIN,	±10%V_{CC}	2.4			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OL} = MAX V_{IH} = MIN,	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				−0.6	mA
I_{OZH}	OFF-state output current, High-level voltage applied		V_{CC} = MAX, V_O = 2.7V				50	μA
I_{OZL}	OFF-state output current, Low-level voltage applied		V_{CC} = MAX, V_O = 0.5V				−50	μA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current (total)	'F373	V_{CC} = MAX	I_{CCZ} $\overline{OE}$ = 4.5V D inputs = E = GND		35	55	mA
		'F374		I_{CCZ} CP = $\overline{OE}$ = 4.5V D inputs = GND		57	86	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of High-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

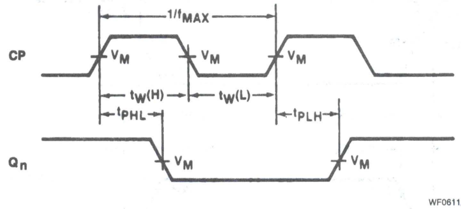
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	74F373, 74F374					UNIT
				$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	'F373	Waveform 3	3.0 2.0	5.3 3.7	7.0 5.0	3.0 2.0	8.0 6.0	ns
t_{PLH} t_{PHL}	Propagation delay E to $\overline{Q}_n$		Waveform 2	5.0 3.0	9.0 4.0	11.5 7.0	5.0 3.0	13.0 8.0	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level		Waveform 6 Waveform 7	2.0 2.0	5.0 5.6	11.0 7.5	2.0 2.0	12.0 8.5	ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level		Waveform 6 Waveform 7	2.0 2.0	4.5 3.8	6.5 5.0	2.0 2.0	7.5 6.0	ns
f_{MAX}	Maximum clock frequency	'F374	Waveform 1	100			70		MHz
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{Q}_n$		Waveform 1	4.0 4.0	6.5 6.5	8.5 8.5	4.0 4.0	10.0 10.0	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level		Waveform 6 Waveform 7	2.0 2.0	9.0 5.3	11.5 7.5	2.0 2.0	12.5 8.5	ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level		Waveform 6 Waveform 7	2.0 2.0	5.3 4.3	7.0 5.5	2.0 2.0	8.0 6.5	ns

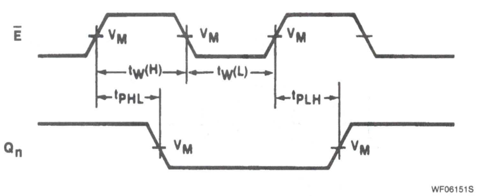
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER		TEST CONDITIONS	74F373, 74F374					UNIT
				$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
				Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time D_n to E	'F373	Waveform 4	2.0 2.0			2.0 2.0		ns
$t_h(H)$ $t_h(L)$	Hold time, D_n to E		Waveform 4	3.0 3.0			3.0 3.0		ns
$t_w(H)$	E pulse width, High or Low		Waveform 2	6.0			6.0		ns
$t_s(H)$ $t_s(L)$	Setup time D_n to CP	'F374	Waveform 5	2.0 2.0			2.0 2.0		ns
$t_h(H)$ $t_h(L)$	Hold time, D_n to CP		Waveform 5	2.0 2.0			2.0 2.0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low		Waveform 1	7.0 6.0			7.0 6.0		ns

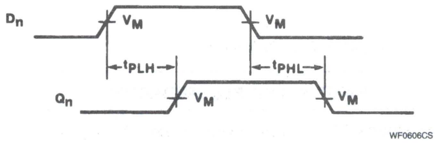
AC WAVEFORMS


CP
Qn
1/fMAX
VM
tW(H)
tW(L)
tPHL
tPLH
WF06112S

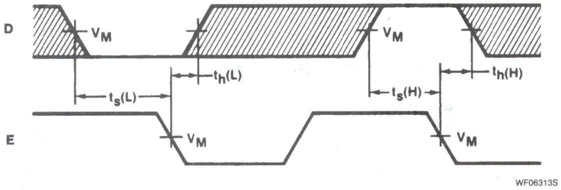
Waveform 1. Clock to Output Delays and Pulse Width


Ē
Qn
VM
tW(H)
tW(L)
tPHL
tPLH
WF06151S

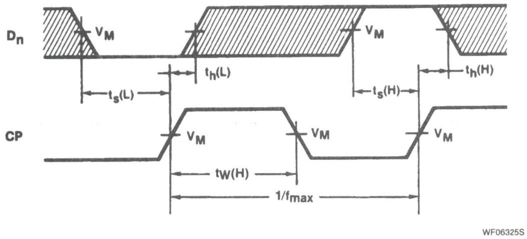
Waveform 2. Latch Enable to Output Delays and Latch Enable Pulse Width


Dn
Qn
VM
tPLH
tPHL
WF0606CS

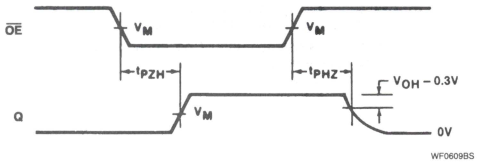
Waveform 3. Propagation Delay Data to Q Outputs


D
E
VM
th(L)
ts(L)
ts(H)
th(H)
WF06313S

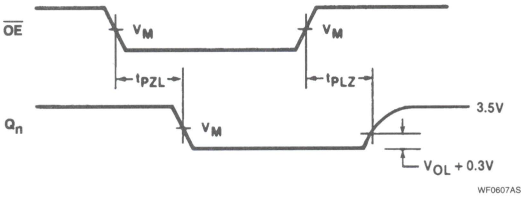
Waveform 4. Data Setup and Hold Times


Dn
CP
VM
th(L)
ts(L)
ts(H)
th(H)
tW(H)
1/fmax
WF06325S

Waveform 5. Data Setup and Hold Times


OE
Q
VM
tPZH
tPHZ
VOH − 0.3V
0V
WF0609BS

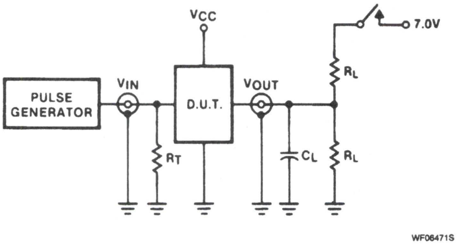
Waveform 6. 3-State Output Enable Time to High Level and Output Disable Time From High Level


OE
Qn
VM
tPZL
tPLZ
3.5V
VOL + 0.3V
WF0607AS

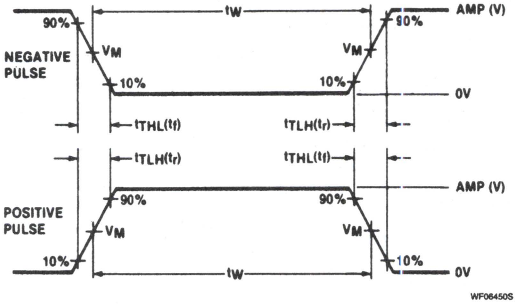
Waveform 7. 3-State Output Enable Time to Low Level and Output Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS


VCC
7.0V
RL
PULSE GENERATOR
VIN
D.U.T.
VOUT
RT
CL
RL
WF06471S

Test Circuit for 3-State Outputs


tW
90%
AMP (V)
NEGATIVE PULSE
VM
VM
10%
10%
0V
tTHL(tf)
tTLH(tr)
tTLH(tr)
tTHL(tf)
90%
90%
AMP (V)
POSITIVE PULSE
VM
VM
10%
10%
0V
tW
WF06450S

$V_M = 1.5V$

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F377
Flip-Flop

Octal D Flip-Flop With Enable
Product Specification

FAST Products

FEATURES

- High-impedance NPN Base Inputs for reduced loading (20μA in High and Low states)
- Ideal for addressable register applications
- Enable for address and data synchronization applications
- Eight edge-triggered D flip-flops
- Buffered common Clock
- See 'F273 for Master Reset version
- See 'F373 for transparent latch version
- See 'F374 for 3-State version

DESCRIPTION

The 'F377 has eight edge-triggered, D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) input loads all flip-flops simultaneously when the Enable ($\overline{E}$) is Low.

The register is fully edge-triggered. The state of each D input, one setup time before the Low-to-High clock transition, is transferred to the corresponding flip-flop's Q output. The $\overline{E}$ input must be stable one setup time prior to the Low-to-High clock transition for predictable operation.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F377	120MHz	65mA

ORDERING INFORMATION

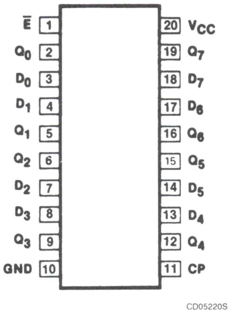
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ± 10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F377N
20-Pin Plastic SOL	N74F377D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$D_0 - D_7$	Data inputs	1.0/0.033	20μA/20μA
CP	Clock input (active rising edge)	1.0/0.033	20μA/20μA
$\overline{E}$	Enable input (active-Low)	1.0/0.033	20μA/20μA
$Q_0 - Q_7$	Data outputs	50/33	1mA/20mA

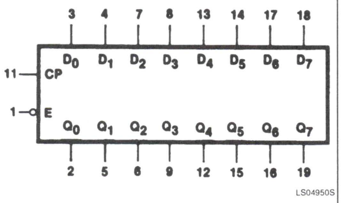
NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



Ē 1
Q0 2
D0 3
D1 4
Q1 5
Q2 6
D2 7
D3 8
Q3 9
GND 10
20 VCC
19 Q7
18 D7
17 D6
16 Q6
15 Q5
14 D5
13 D4
12 Q4
11 CP
CD05220S

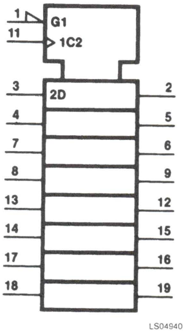
LOGIC SYMBOL



3 4 7 8 13 14 17 18
D0 D1 D2 D3 D4 D5 D6 D7
11 CP
1 E
Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
2 5 6 9 12 15 16 19
LS04950S

V_{CC} = Pin 20
GND = Pin 10

LOGIC SYMBOL (IEEE/IEC)



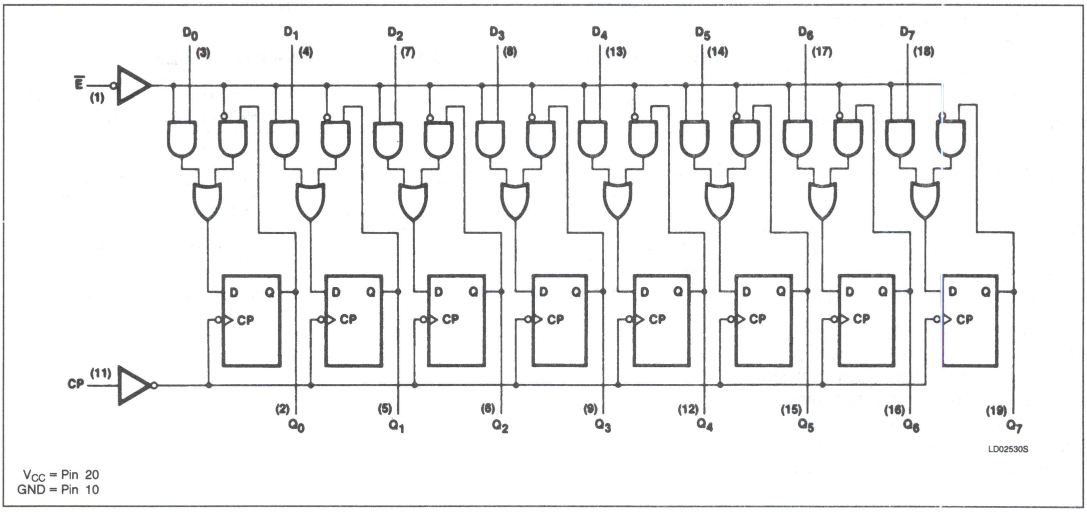
1
11
G1
1C2
3
2D
2
4
5
7
6
8
9
13
12
14
15
17
16
18
19
LS04940S

MODE SELECT — FUNCTION TABLE

OPERATING MODE	INPUTS			OUTPUTS
	CP	$\overline{E}$	D_n	Q_n
Load "1"	↑	l	h	H
Load "0"	↑	l	l	L
Hold (do nothing)	↑ X	h H	X X	no change no change

H = High voltage level steady state
h = High voltage level one setup time prior to the Low-to-High Clock transition
L = Low voltage level steady state
l = Low voltage level one setup time prior to the Low-to-High Clock transition
X = Don't care
↑ = Low-to-High clock transition

LOGIC DIAGRAM


D_0
(3)
D_1
(4)
D_2
(7)
D_3
(8)
D_4
(13)
D_5
(14)
D_6
(17)
D_7
(18)
$\overline{E}$
(1)
D Q
CP
CP
(11)
(2)
Q_0
(5)
Q_1
(6)
Q_2
(9)
Q_3
(12)
Q_4
(15)
Q_5
(16)
Q_6
(19)
Q_7
LD02530S

V_{CC} = Pin 20
GND = Pin 10

Flip-Flop

FAST 74F377

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage	$\overline{E}$ & CP inputs[3]	V_{CC} = MIN, V_{IL} = 0.0V, V_{IH} = 4.5V, I_{OH} = MAX	$\pm 10\% V_{CC}$	2.5			V
				$\pm 5\% V_{CC}$	2.7	3.4		V
		other inputs	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	$\pm 10\% V_{CC}$	2.5			V
				$\pm 5\% V_{CC}$	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	$\pm 10\% V_{CC}$		0.35	0.50	V
				$\pm 5\% V_{CC}$		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = 0.0V, V_I = 7.0V				100	μA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				−20	μA
I_{OS}	Short-circuit output current[4]		V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	D_n = 4.5V, CP = ↑, $\overline{E}$ = GND		55	72	mA
		I_{CCL}		$D_n = \overline{E}$ = GND, CP = ↑		70	90	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. To reduce the effect of external noise during test.
4. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

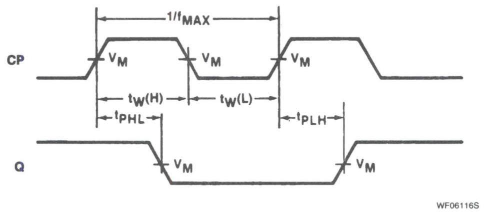
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F377					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	110	120		100		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	Waveform 1	4.0 4.0	6.5 7.0	8.5 9.0	4.0 4.0	10.0 10.5	ns

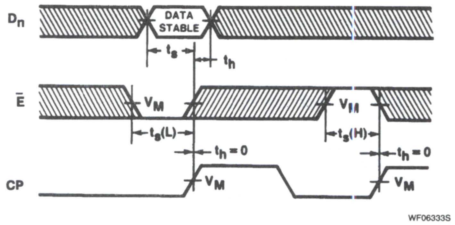
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	74F377					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to CP	Waveform 2	2.0 2.0			2.5 2.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to CP	Waveform 2	0 0			1.0 1.0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{E}$ to CP	Waveform 2	2.5 4.0			2.5 4.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{E}$ to CP	Waveform 2	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	Clock pulse width, High or Low	Waveform 1	4.0 4.0			5.0 5.0		ns

AC WAVEFORMS



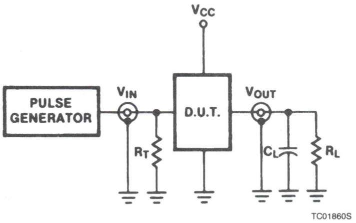
Waveform 1. Clock to Output Delays and Clock Pulse Width



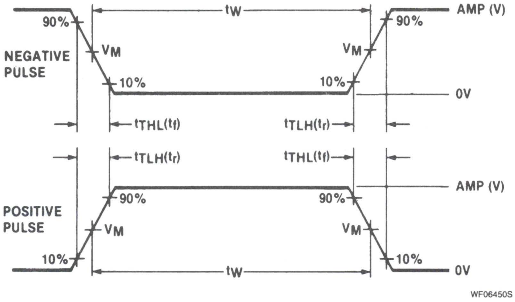
Waveform 2. Data and Clock Enable Setup and Hold Times

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS


VCC
PULSE GENERATOR
VIN
D.U.T.
VOUT
RT
CL
RL
TC01860S

Test Circuit for Totem-Pole Outputs


NEGATIVE PULSE
90%
VM
10%
tW
AMP (V)
0V
tTHL(tf)
tTLH(tr)
POSITIVE PULSE
tTLH(tr)
tTHL(tf)
90%
VM
10%
tW
AMP (V)
0V
WF06450S

$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS

R_L = Load resistor to GND; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F378
Flip-Flop

Hex D Flip-Flop With Enable
Product Specification

FAST Products

FEATURES
- **6-bit high-speed Parallel Register**
- **Positive edge-triggered D-type inputs**
- **Fully buffered common Clock and Enable inputs**
- **Input clamp diodes limit high-speed termination effects**
- **Fully TTL and CMOS compatible**

DESCRIPTION
The 'F378 has six edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) input loads all flip-flops simultaneously when the Enable ($\overline{E}$) is Low.

The register is fully edge-triggered. The state of each D input, one setup time before the Low-to-High Clock transition is transferred to the corresponding flip-flop's Q output. The $\overline{E}$ input must be stable only one setup time prior to the Low-to-High Clock transition for predictable operation.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F378	100MHz	35mA

ORDERING INFORMATION

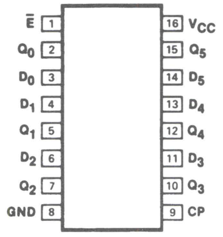
PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
16-Pin Plastic DIP	N74F378N
16-Pin Plastic SO	N74F378D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$D_0 - D_5$	Data inputs	1.0/1.0	20μA/0.6mA
CP	Clock input (active rising edge)	1.0/1.0	20μA/0.6mA
$\overline{E}$	Enable input (active-Low)	1.0/1.0	20μA/0.6mA
$Q_0 - Q_5$	Data outputs	50/33	1mA/20mA

NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

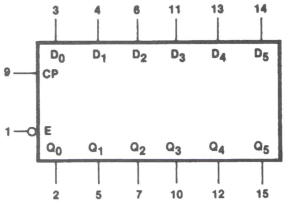
PIN CONFIGURATION



$\overline{E}$ 1
Q_0 2
D_0 3
D_1 4
Q_1 5
D_2 6
Q_2 7
GND 8
9 CP
10 Q_3
11 D_3
12 Q_4
13 D_4
14 D_5
15 Q_5
16 V_{CC}

CD05380S

LOGIC SYMBOL

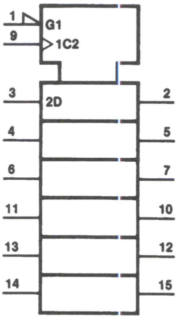


3
4
6
11
13
14
D_0
D_1
D_2
D_3
D_4
D_5
9
CP
1
E
Q_0
Q_1
Q_2
Q_3
Q_4
Q_5
2
5
7
10
12
15

LS05070S

V_{CC} = Pin 16
GND = Pin 8

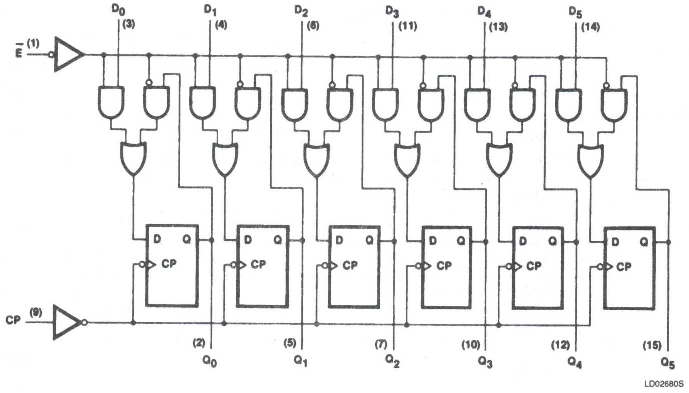
LOGIC SYMBOL (IEEE/IEC)



1
9
G1
1C2
3
2D
2
4
5
6
7
11
10
13
12
14
15

LS05080S

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
( ) = Pin numbers

MODE SELECT — FUNCTION TABLE

OPERATING MODE	INPUTS			OUTPUTS
	CP	Ē	D_n	Q_n
Load "1"	↑	l	h	H
Load "0"	↑	l	l	L
Hold (do nothing)	↑ X	h H	X X	no change no change

H = High voltage level steady state
h = High voltage level one setup time prior to the Low-to-High clock transition
L = Low voltage steady state
l = Low voltage level one setup time prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		74F378			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				−0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			32	45	mA
		I_{CCL}				35	45	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

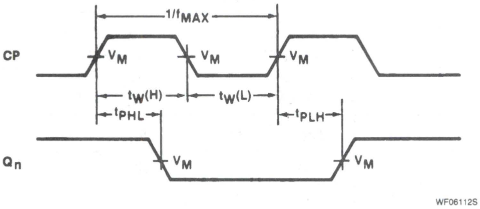
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum Clock frequency	Waveform 1	80	100		80		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	Waveform 1	3.0 3.5	5.5 6.0	7.5 8.5	3.0 3.5	8.5 9.5	ns ns

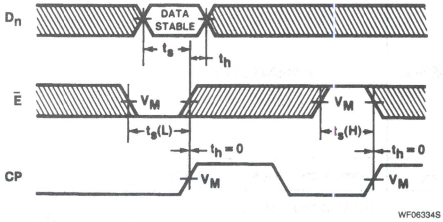
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to CP	Waveform 2	4.0 4.0			4.0 4.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to CP	Waveform 2	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{E}$ to CP	Waveform 2	4.0 10.0			4.0 10.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{E}$ to CP	Waveform 2	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	CP pulse width High or Low	Waveform 1	4.0 6.0			4.0 6.0		ns

AC WAVEFORMS


1/fMAX
CP
VM
VM
VM
tW(H)
tW(L)
tPHL
tPLH
Qn
VM
VM
WF06112S

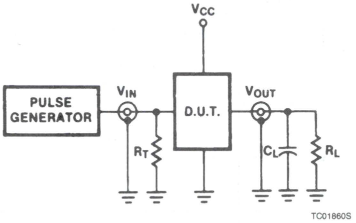
Waveform 1. Clock to Output Delays, Clock Pulse Width, and Maximum Clock Frequency


Dn
DATA STABLE
ts
th
Ē
VM
ts(L)
th = 0
VM
ts(H)
th = 0
CP
VM
VM
WF06334S

Waveform 2. Data and Enable Setup and Hold Times

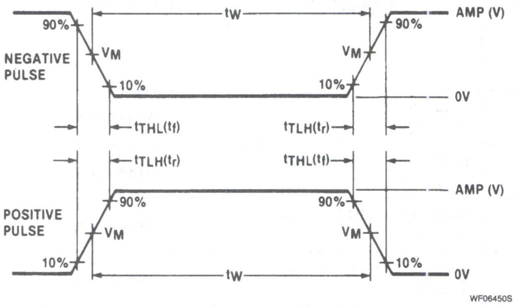
NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS


VCC
PULSE GENERATOR
VIN
D.U.T.
VOUT
RT
CL
RL
TC01860S

Test Circuit for Totem-Pole Outputs

DEFINITIONS
R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.


tW
90%
90%
AMP (V)
NEGATIVE PULSE
VM
VM
10%
10%
0V
tTHL(tf)
tTLH(tr)
tTLH(tr)
tTHL(tf)
AMP (V)
90%
90%
POSITIVE PULSE
VM
VM
10%
10%
0V
tW
WF06450S

$V_M = 1.5V$
Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F379
Quad Register

Quad Parallel Register (with Enable)
Product Specification

FAST Products

FEATURES

- **Edge-triggered D-type inputs**
- **Buffered positive edge-triggered Clock**
- **Buffered common Enable input**
- **True and complementary outputs**

DESCRIPTION

The 'F379 is a 4-bit register with buffered common Enable. This device is similar to the 'F175 but features the common Enable rather than common Master Reset.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F379	120MHz	28mA

ORDERING INFORMATION

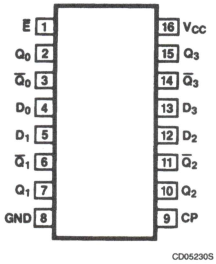
PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
16-Pin Plastic DIP	N74F379N
16-Pin Plastic SO	N74F379D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$\overline{E}$	Enable input (active-Low)	1.0/1.0	20μA/0.6mA
$D_0 - D_3$	Data inputs	1.0/1.0	20μA/0.6mA
CP	Clock Pulse input (active rising edge)	1.0/1.0	20μA/0.6mA
$Q_0 - Q_3$	Flip-flop outputs	50/33	1.0mA/20mA
$\overline{Q}_0 - \overline{Q}_3$	Complementary outputs	50/33	1.0mA/20mA

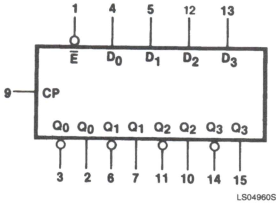
NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



$\overline{E}$ 1
Q_0 2
$\overline{Q}_0$ 3
D_0 4
D_1 5
$\overline{Q}_1$ 6
Q_1 7
GND 8
16 V_{CC}
15 Q_3
14 $\overline{Q}_3$
13 D_3
12 D_2
11 $\overline{Q}_2$
10 Q_2
9 CP
CD05230S

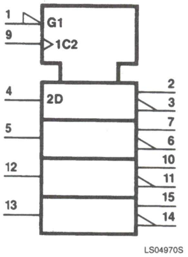
LOGIC SYMBOL



1
4
5
12
13
$\overline{E}$
D_0
D_1
D_2
D_3
9
CP
Q_0 $\overline{Q}_0$ Q_1 $\overline{Q}_1$ Q_2 $\overline{Q}_2$ Q_3 $\overline{Q}_3$
3 2 6 7 11 10 14 15
LS04960S

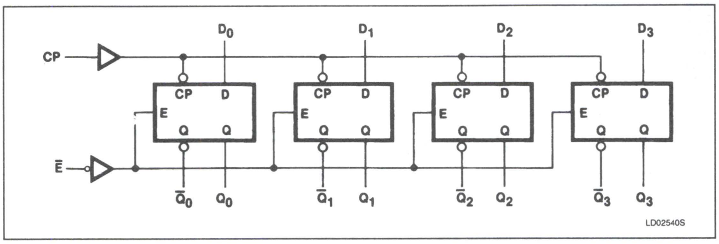
V_{CC} = Pin 16
GND = Pin 8

LOGIC SYMBOL (IEEE/IEC)



1
9
G1
>1C2
4
2D
5
12
13
2
3
7
6
10
11
15
14
LS04970S

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			OUTPUTS	
$\overline{E}$	CP	D_n	Q_n	$\overline{Q}_n$
H	↑	X	NC	NC
L	↑	h	H	L
L	↑	l	L	H

H = High voltage level steady state
h = High voltage level one setup time prior to the Low-to-High clock transition
L = Low voltage level steady state
l = Low voltage level one setup time prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition
NC = No Change

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

Quad Register FAST 74F379

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		74F379			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX V_{IH} = MIN,	±10%V_{CC}	2.5			V
			±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, I_{OL} = MAX V_{IH} = MIN,	±10%V_{CC}		0.35	0.50	V
			±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, $I_I = I_{IK}$			−0.73	−1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V				−0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current (total)	V_{CC} = MAX, $D_n = \overline{MR}$ = 4.5V, CP = ↑			28	40	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

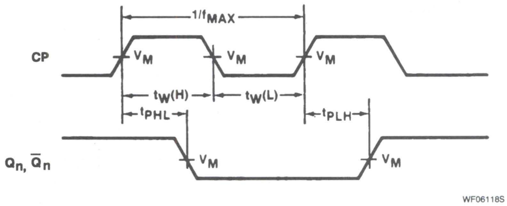
SYMBOL	PARAMETER	TEST CONDITIONS	74F379					UNIT
			T_A = +25°C V_{CC} = +5.0V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum Clock frequency	Waveform 1	100	120		90		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n, $\overline{Q_n}$	Waveform 1	3.5 4.5	5.0 6.5	7.0 8.5	3.5 4.5	8.0 9.5	ns

AC SETUP REQUIREMENTS

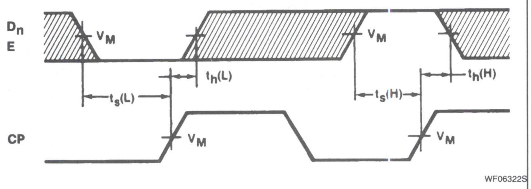
SYMBOL	PARAMETER	TEST CONDITIONS	74F379					UNIT
			T_A = +25°C V_{CC} = +5.0V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to CP	Waveform 2	3.0 3.0			3.0 3.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to CP	Waveform 2	1.0 1.0			1.0 1.0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{E}$ to CP	Waveform 2	6.0 6.0			6.0 6.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{E}$ to CP	Waveform 2	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	CP pulse width, High or Low	Waveform 1	4.0 5.0			4.0 5.0		ns

Quad Register FAST 74F379

AC WAVEFORMS


1/fMAX
CP
VM
VM
VM
tW(H)
tW(L)
tPHL
tPLH
Qn, Q̄n
VM
VM
WF06118S

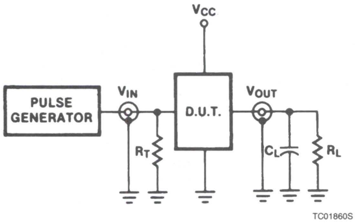
Waveform 1. Clock to Output Delays and Clock Pulse Width


Dn
E
VM
VM
th(L)
th(H)
ts(L)
ts(H)
CP
VM
VM
WF06322S

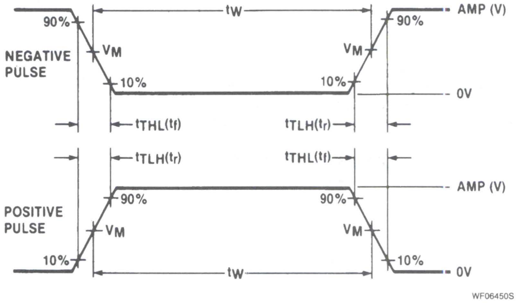
Waveform 2. Data Setup and Hold Times

NOTE: For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORMS


VCC
PULSE GENERATOR
VIN
D.U.T.
VOUT
RT
CL
RL
TC01860S

Test Circuit for Totem-Pole Outputs


tW
90%
AMP (V)
NEGATIVE PULSE
VM
VM
10%
10%
0V
tTHL(tf)
tTLH(tr)
tTLH(tr)
tTHL(tf)
90%
90%
AMP (V)
POSITIVE PULSE
VM
VM
10%
10%
0V
tW
WF06450S

$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS

R_L = Load resistor to GND; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F381
Arithmetic Logic Unit

4-Bit Arithmetic Logic Unit
Product Specification

FAST Products

FEATURES

- **Low-input loading minimizes drive requirements**
- **Performs six arithmetic and logic functions**
- **Selectable Low (clear) and High (preset) functions**
- **Carry Generate and Propagate outputs for use with Carry look-ahead generator**

DESCRIPTION

The 'F381 performs three arithmetic and three logic operations on two 4-bit words, A and B. Two additional Select ($S_0 - S_2$) input codes force the Function outputs Low or High. Carry Propagate ($\overline{P}$) and Generate ($\overline{G}$) outputs are provided for use with the 'F182 Carry Look-ahead Generator for high-speed expansion to longer word lengths. For ripple expansion, refer to the 'F382 ALU data sheet.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F381	6.5ns	59mA

ORDERING INFORMATION

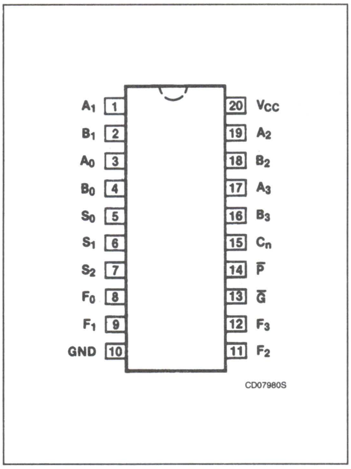
PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
20-Pin Plastic DIP	74F381N
20-Pin Plastic SOL	74F381D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

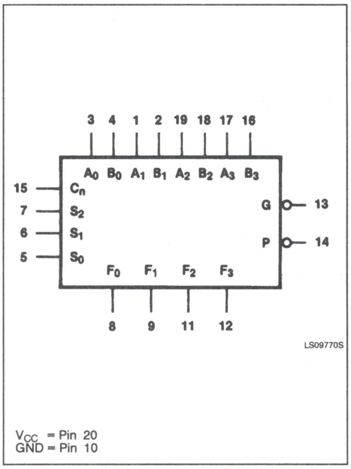
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$A_0 - A_3$	A operand inputs	1.0/4.0	20μA/0.6mA
$B_0 - B_3$	B operand inputs	1.0/4.0	20μA/0.6mA
$S_0 - S_2$	Function select inputs	1.0/1.0	20μA/0.6mA
C_n	Carry input	1.0/4.0	20μA/0.6mA
$\overline{G}$	Carry generate output (active-Low)	50/33	1.0mA/20mA
$\overline{P}$	Carry propagate output (active-Low)	50/33	1.0mA/20mA
$F_0 - F_3$	Function Outputs	50/33	1.0mA/20mA

NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION

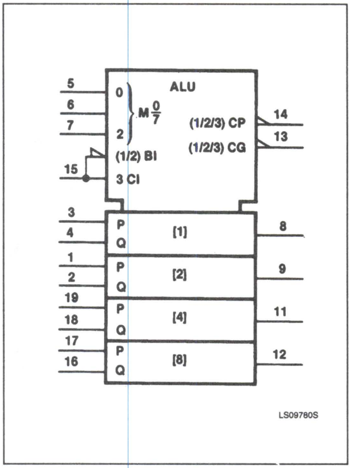

A1 1
B1 2
A0 3
B0 4
S0 5
S1 6
S2 7
F0 8
F1 9
GND 10
20 VCC
19 A2
18 B2
17 A3
16 B3
15 Cn
14 P̄
13 Ḡ
12 F3
11 F2
CD07980S

LOGIC SYMBOL


3 4 1 2 19 18 17 16
A0 B0 A1 B1 A2 B2 A3 B3
15 Cn
7 S2
6 S1
5 S0
G 13
P 14
F0 F1 F2 F3
8 9 11 12
LS09770S

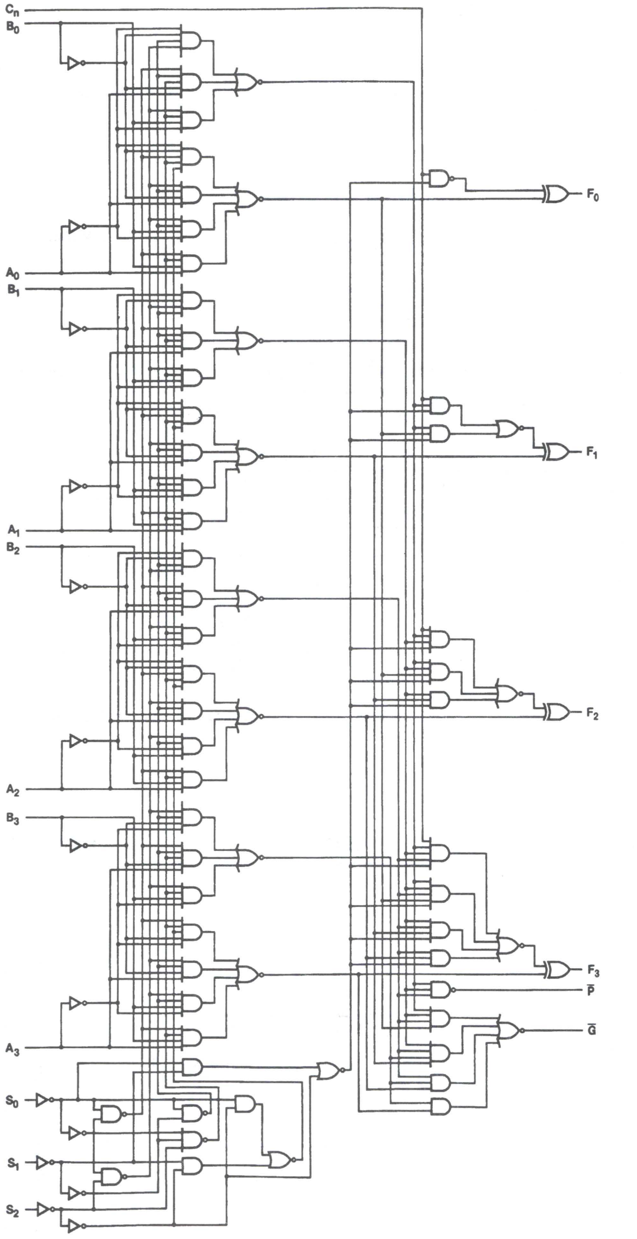
V_{CC} = Pin 20
GND = Pin 10

LOGIC SYMBOL (IEEE/IEC)


ALU
5
6
7
0
M 0/7
2
15
(1/2) BI
3 CI
(1/2/3) CP
(1/2/3) CG
14
13
3
4
P
Q
[1]
8
1
2
P
Q
[2]
9
19
18
P
Q
[4]
11
17
16
P
Q
[8]
12
LS09780S

Arithmetic Logic Unit FAST 74F381

LOGIC DIAGRAM


C_n
B_0
A_0
B_1
A_1
B_2
A_2
B_3
A_3
S_0
S_1
S_2
F_0
F_1
F_2
F_3
$\overline{P}$
$\overline{G}$

LD04071S

Arithmetic Logic Unit FAST 74F381

FUNCTIONAL DESCRIPTION

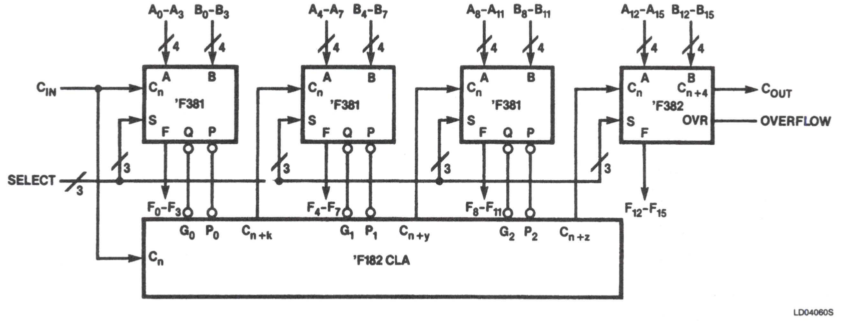
Signals applied to the Select inputs $S_0 - S_2$ determine the mode of operation, as indicated in the Function Select Table. An extensive listing of input and output function levels is shown in the Function Table. The circuit performs the arithmetic functions for either active-High or active-Low operands, with output levels in the same convention. In the Subtract operating modes, it is necessary to force a Carry (High for active-High operands, Low for active-Low operands) into the C_n input of the least significant package.

The Carry Generate ($\overline{G}$) and Carry Propagate ($\overline{P}$) outputs supply input signals to the 'F182 Carry look-ahead generator for expansion to longer word length, as shown in Figure 1. Note that an 'F382 ALU is used for the most significant package. Typical delays for Figure 1 are given in Table 1.

FUNCTION SELECT TABLE

SELECT			OPERATION
S_0	S_1	S_2	
L	L	L	Clear
H	L	L	B Minus A
L	H	L	A Minus B
H	H	L	A Plus B
L	L	H	A ⊕ B
H	L	H	A + B
L	H	H	AB
H	H	H	Preset

H = High voltage level
L = Low voltage level



A_0-A_3 B_0-B_3
A_4-A_7 B_4-B_7
A_8-A_{11} B_8-B_{11}
A_{12}-A_{15} B_{12}-B_{15}
4
C_{IN}
SELECT
3
A B C_n 'F381 S F Q P
A B C_n C_{n+4} 'F382 OVR S F
C_{OUT}
OVERFLOW
F_0-F_3
F_4-F_7
F_8-F_{11}
F_{12}-F_{15}
G_0 P_0 C_{n+k}
G_1 P_1 C_{n+y}
G_2 P_2 C_{n+z}
C_n
'F182 CLA
LD04060S

Figure 1. 16-Bit Look-Ahead Carry ALU Expansion

Table 1. 16-Bit Delay Tabulation

PATH SEGMENT	TOWARD F	OUTPUT C_{n+4}, OVR
A_i or B_i to $\overline{P}$	7.2ns	7.2ns
$\overline{P}_i$ to C_{n+j} ('F182)	6.2ns	6.2ns
C_n to F	8.1ns	—
C_n to C_{n+4}, OVR	—	8.0ns
Total delay	21.5ns	21.4ns

FUNCTION TABLE

	INPUTS						OUTPUTS					
Function	S_0	S_1	S_2	C_n	A_n	B_n	F_0	F_1	F_2	F_3	$\overline{G}$	$\overline{P}$
Clear	0	0	0	X	X	X	0	0	0	0	0	0
B Minus A	1	0	0	0	0	0	1	1	1	1	1	0
				0	0	1	0	1	1	1	0	0
				0	1	0	0	0	0	0	1	1
				0	1	1	1	1	1	1	1	0
				1	0	0	0	0	0	0	1	0
				1	0	1	1	1	1	1	0	0
				1	1	0	1	0	0	0	1	1
				1	1	1	0	0	0	0	1	0
A Minus B	0	1	0	0	0	0	1	1	1	1	1	0
				0	0	1	0	0	0	0	1	1
				0	1	0	0	1	1	1	0	0
				0	1	1	1	1	1	1	1	0
				1	0	0	0	0	0	0	1	0
				1	0	1	1	0	0	0	1	1
				1	1	0	1	1	1	1	0	0
				1	1	1	0	0	0	0	1	0
A Plus B	1	1	0	0	0	0	0	0	0	0	1	1
				0	0	1	1	1	1	1	1	0
				0	1	0	1	1	1	1	1	0
				0	1	1	0	1	1	1	0	0
				1	0	0	1	0	0	0	1	1
				1	0	1	0	0	0	0	1	0
				1	1	0	0	0	0	0	1	0
				1	1	1	1	1	1	1	0	0
A ⊕ B	0	0	1	X	0	0	0	0	0	0	1	1
				X	0	1	1	1	1	1	1	1
				X	1	0	1	1	1	1	1	0
				X	1	1	0	0	0	0	0	0
A + B	1	0	1	X	0	0	0	0	0	0	1	1
				X	0	1	1	1	1	1	1	1
				X	1	0	1	1	1	1	1	1
				X	1	1	1	1	1	1	1	0
AB	0	1	1	X	0	0	0	0	0	0	0	0
				X	0	1	0	0	0	0	1	1
				X	1	0	0	0	0	0	0	0
				X	1	1	1	1	1	1	1	0
Preset	1	1	1	X	0	0	1	1	1	1	1	1
				X	0	1	1	1	1	1	1	1
				X	1	0	1	1	1	1	1	1
				X	1	1	1	1	1	1	1	0

1 = High voltage level
0 = Low voltage level
X = Don't care

Arithmetic Logic Unit FAST 74F381

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +1	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.50	5.0	5.50	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current	$A_0 - A_3$, $B_0 - B_3$, C_n	V_{CC} = MAX, V_I = 0.5V				−2.4	mA
		S_0, S_1, S_2					−0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current (total)		V_{CC} = MAX			59	89	mA

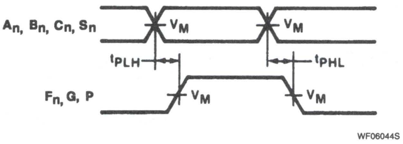
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F381					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH}	Propagation delay C_n to F_n	Waveform 1	2.5	6.0	11.0	2.5	12.5	ns
t_{PHL}			2.5	4.5	6.5	2.5	7.5	ns
t_{PLH}	Propagation delay Any A or B to any F	Waveform 1	3.5	7.0	13.0	3.5	16.0	ns
t_{PHL}			3.0	6.0	9.0	3.0	10.0	ns
t_{PLH}	Propagation delay S_n to F_n	Waveform 1	5.0	9.0	20.0	5.0	21.5	ns
t_{PHL}			4.0	7.5	10.5	4.0	11.5	ns
t_{PLH}	Propagation delay A_n or B_n to $\overline{G}$	Waveform 1	3.5	6.5	9.0	3.5	10.0	ns
t_{PHL}			3.0	6.0	8.5	3.0	9.0	ns
t_{PLH}	Propagation delay A_n or B_n to $\overline{P}$	Waveform 1	3.0	5.5	8.0	3.0	9.0	ns
t_{PHL}			3.5	6.0	8.5	3.5	9.0	ns
t_{PLH}	Propagation delay S_n to $\overline{G}$ or $\overline{P}$	Waveform 1	5.0	7.5	11.0	5.0	12.5	ns
t_{PHL}			5.5	8.5	12.5	5.0	14.0	ns

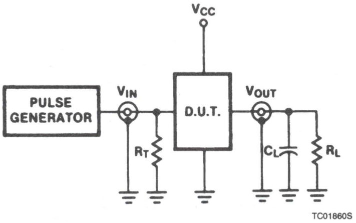
AC WAVEFORM



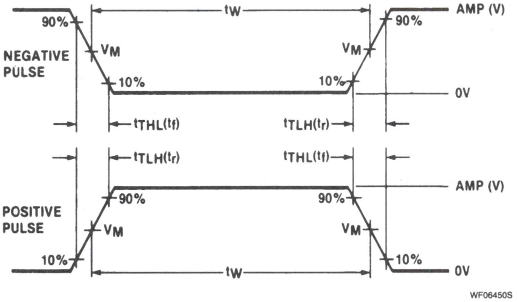
NOTE: For all waveforms, $V_M = 1.5V$.

Waveform 1. Propagation Delay for Carry Input (C_n) to Function Output (F_n) A Or B Operand Input (A_n Or B_n) to Function Outputs (F_n) Function Select Inputs (S_n) to Function Outputs (F_n) A Or B Operand Input (A_n Or B_n) to Carry Generate (G) and Propagate (P) Output Function Select Inputs (S_n) to Carry Generate (G) and Propagate (P) Output.

TEST CIRCUIT AND WAVEFORMS


VCC
PULSE GENERATOR
VIN
D.U.T.
VOUT
RT
CL
RL
TC01860S

Test Circuit for Totem-Pole Outputs


NEGATIVE PULSE
POSITIVE PULSE
90%
10%
VM
tW
AMP (V)
0V
tTHL(tf)
tTLH(tr)
WF06450S

$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS

R_L = Load resistor to GND; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST Products

FAST 74F382
Arithmetic Logic Unit (ALU)

4-Bit Arithmetic Logic Unit
Product Specification

FEATURES

- **Performs six arithmetic logic functions**
- **Selectable Low (clear) and High (preset) functions**
- **Low input loading minimizes drive requirements**
- **Carry output for ripple expansion**
- **Overflow output for Two's Complement arithmetic**

DESCRIPTION

The 'F382 performs three arithmetic and three logic operations on two 4-bit words: A and B. Two additional Select ($S_0 - S_2$) input codes force the Function outputs Low or High. An Overflow output is provided for convenience in Two's Complement arithmetic. A Carry output is provided for ripple expansion. For high-speed expansion using a Carry look-ahead generator, refer to the 'F381 data sheet.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F382	7.0ns	54mA

ORDERING INFORMATION

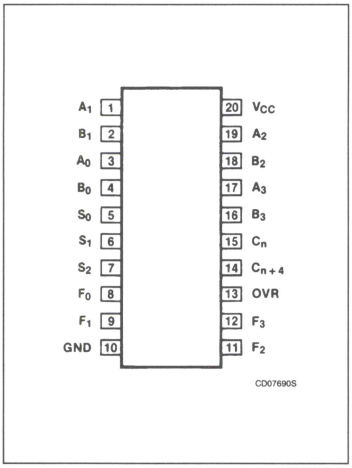
PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
20-Pin Plastic DIP	N74F382N
20-Pin Plastic SOL	N74F382D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

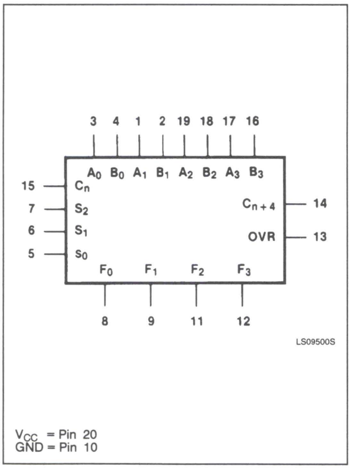
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$A_0 - A_3$	A operand inputs	1.0/4.0	20μA/2.4mA
$B_0 - B_3$	B operand inputs	1.0/4.0	20μA/2.4mA
$S_0 - S_2$	Function select inputs	1.0/4.0	20μA/0.6mA
C_n	Carry input	1.0/5.0	20μA/3mA
C_n	Carry output	50/33.3	1mA/20mA
OVR	Overflow output	50/33.3	1mA/20mA
$F_0 - F_3$	Outputs	50/33.3	1mA/20mA

NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION

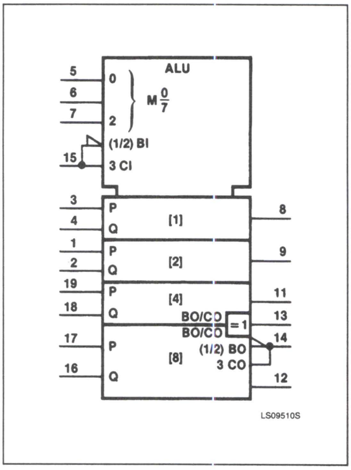

A1 1
B1 2
A0 3
B0 4
S0 5
S1 6
S2 7
F0 8
F1 9
GND 10
20 VCC
19 A2
18 B2
17 A3
16 B3
15 Cn
14 Cn+4
13 OVR
12 F3
11 F2
CD07690S

LOGIC SYMBOL

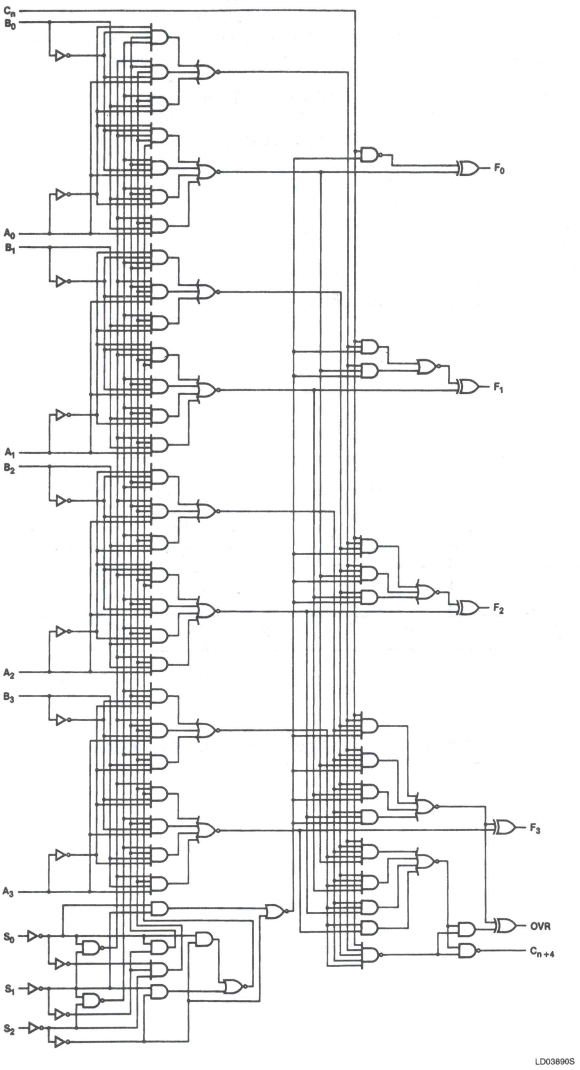

3 4 1 2 19 18 17 16
A0 B0 A1 B1 A2 B2 A3 B3
15 Cn
7 S2
6 S1
5 S0
Cn+4 14
OVR 13
F0 F1 F2 F3
8 9 11 12
LS09500S

V_{CC} = Pin 20
GND = Pin 10

LOGIC SYMBOL (IEEE/IEC)


ALU
5
6
7
0
2
M 0/7
(1/2) BI
15
3 CI
3
4
P
Q
[1]
8
1
2
P
Q
[2]
9
19
18
P
Q
[4]
11
BO/CO
=1
13
BO/CO
14
17
16
P
Q
[8]
(1/2) BO
3 CO
12
LS09510S

LOGIC DIAGRAM



C_n
B_0
A_0
B_1
A_1
B_2
A_2
B_3
A_3
S_0
S_1
S_2
F_0
F_1
F_2
F_3
OVR
C_{n+4}
LD03890S

FUNCTIONAL DESCRIPTION

Signals applied to the Select inputs S0 – S2 determine the mode of operation, as indicated in the Function Select Table. An extensive listing of input and output levels is shown in the Truth Table. The circuit performs the arithmetic functions for either active-High or active-Low operands, with output levels in the same convention. In the Subtract operating modes, it is necessary to force a carry (High for active-High operands, Low for active-Low operands) into the C_n input of the least significant package. Ripple expansion is illustrated in Figure 1. The overflow output OVR is the Exclusive-OR of C_{n+3} and C_{n+4}; a High signal on OVR indicates overflow in Two's complement operation. Typical delays for Figure 1 are given in Table 1.

FUNCTION SELECT TABLE

SELECT			OPERATION
S_0	S_1	S_2	
L	L	L	Clear
H	L	L	B Minus A
L	H	L	A Minus B
H	H	L	A Plus B
L	L	H	$A \oplus B$
H	L	H	A + B
L	H	H	AB
H	H	H	Preset

H = High Voltage Level
L = Low Voltage Level

Table 1. 16 Bit-Delay Tabulation

PATH SEGMENT	TOWARD F	OUTPUT C_{n+4}, OVR
A_i or B_i to C_{n+4}	6.5 ns	6.5 ns
C_n to C_{n+4}	6.3 ns	6.3 ns
C_n to C_{n+4}	6.3 ns	6.3 ns
C_n to F	8.1 ns	—
C_n to C_{n+4}, OVR	—	8.0 ns
Total Delay	27.2 ns	27.1 ns

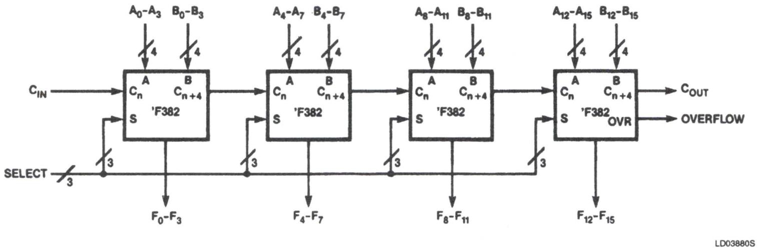


Figure 1. 16-Bit Ripple Carry ALU Expansion

Arithmetic Logic Unit (ALU)

FAST 74F382

FUNCTION TABLE

FUNCTION	INPUTS						OUTPUTS					
	S_0	S_1	S_2	C_n	A_n	B_n	F_0	F_1	F_2	F_3	OVR	C_{n+4}
CLEAR	0	0	0	0	X	X	0	0	0	0	1	1
				1	X	X	0	0	0	0	1	1
B MINUS A	1	0	0	0	0	0	1	1	1	1	0	0
				0	0	1	0	0	0	0	0	1
				0	1	0	0	0	0	0	0	0
				0	1	1	1	1	1	1	0	0
				1	0	0	0	0	0	0	0	1
				1	0	1	1	1	1	1	0	1
				1	1	0	1	0	0	0	0	0
				1	1	1	0	0	0	0	0	1
A MINUS B	0	1	0	0	0	0	1	1	1	1	0	0
				0	0	1	0	0	0	0	0	0
				0	1	0	0	1	1	1	0	1
				0	1	1	1	1	1	1	0	0
				1	0	0	0	0	0	0	0	1
				1	0	1	1	0	0	0	0	0
				1	1	0	1	1	1	1	0	1
				1	1	1	0	0	0	0	0	1
A PLUS B	1	1	0	0	0	0	0	0	0	0	0	0
				0	0	1	1	1	1	1	0	0
				0	1	0	1	1	1	1	0	0
				0	1	1	0	1	1	1	0	1
				1	0	0	1	0	0	0	0	0
				1	0	1	0	0	0	0	0	1
				1	1	0	0	0	0	0	0	1
				1	1	1	1	1	1	1	0	1
A ⊕ B	0	0	1	X	0	0	0	0	0	0	0	0
				X	0	1	1	1	1	1	0	0
				0	1	0	1	1	1	1	0	0
				X	1	1	0	0	0	0	1	1
				1	1	0	1	1	1	1	1	1
A + B	1	0	1	X	0	0	0	0	0	0	0	0
				X	0	1	1	1	1	1	0	0
				X	1	0	1	1	1	1	0	0
				0	1	1	1	1	1	1	0	0
				1	1	1	1	1	1	1	1	1
AB	0	1	1	X	0	0	0	0	0	0	1	1
				X	0	1	0	0	0	0	0	0
				X	1	0	0	0	0	0	1	1
				0	1	1	1	1	1	1	0	0
				1	1	1	1	1	1	1	1	1
PRESET	1	1	1	X	0	0	1	1	1	1	0	0
				X	0	1	1	1	1	1	0	0
				X	1	0	1	1	1	1	0	0
				0	1	1	1	1	1	1	0	0
				1	1	1	1	1	1	1	1	1

1 = High Voltage Level   0 = Low Voltage Level   X = Don't care

Arithmetic Logic Unit (ALU)

FAST 74F382

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +1	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

Arithmetic Logic Unit (ALU) FAST 74F382

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		74F382			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX V_{IH} = MIN,	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OL} = MAX V_{IH} = MIN,	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current	C_n	V_{CC} = MAX, V_I = 0.5V				−3.0	mA
		$A_0 - A_3$, $B_0 - B_3$					−2.4	mA
		S_0, S_1, S_2					−0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current (total)		V_{CC} = MAX			54	81	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

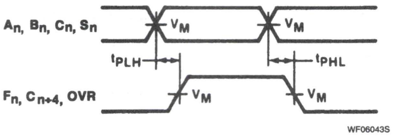
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F382					UNIT
			T_A = +25°C V_{CC} = +5.0V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = +5.0V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay C_n to F_n	Waveform 1	3.0 2.5	7.0 4.5	12.0 6.5	2.5 2.5	13.5 7.5	ns ns
t_{PLH} t_{PHL}	Propagation delay Any A or B to any F	Waveform 1	3.5 3.0	8.0 6.0	13.5 10.0	3.5 2.5	17.0 11.0	ns ns
t_{PLH} t_{PHL}	Propagation delay S_i to F_i	Waveform 1	5.5 5.5	9.0 7.5	15.0 10.5	5.5 5.5	16.0 12.0	ns ns
t_{PLH} t_{PHL}	Propagation delay A_i or B_i to C_{n+4}	Waveform 1	3.5 3.5	7.0 6.5	10.5 9.5	3.5 3.5	11.5 10.5	ns ns
t_{PLH} t_{PHL}	Propagation delay S_i to OVR or C_{n+4}	Waveform 1	7.0 5.0	10.5 8.0	14.5 11.0	6.5 5.0	17.0 12.0	ns ns
t_{PLH} t_{PHL}	Propagation delay C_n to C_{n+4}	Waveform 1	3.0 3.5	4.5 5.0	6.0 6.5	2.5 3.5	6.5 7.0	ns ns
t_{PLH} t_{PHL}	Propagation delay C_n to OVR	Waveform 1	4.5 3.0	9.0 5.0	13.5 6.5	4.0 3.0	15.0 7.0	ns ns
t_{PLH} t_{PHL}	Propagation delay A_i or B_i to OVR	Waveform 1	6.0 3.5	9.0 6.5	12.5 9.0	5.5 3.5	16.5 10.0	ns ns

Arithmetic Logic Unit (ALU)

FAST 74F382

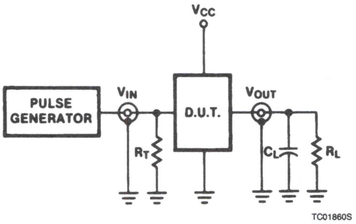
AC WAVEFORM


A_n, B_n, C_n, S_n
V_M
V_M
t_{PLH}
t_{PHL}
F_n, C_{n+4}, OVR
V_M
V_M
WF06043S

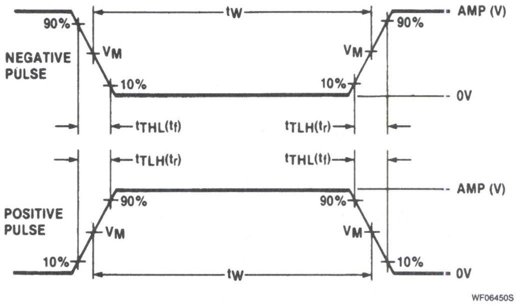
Waveform 1. Propagation Delay for Carry Input (C_n) to Function Output (F_n) A or B Operand Input (A_n or B_n) to Function Outputs (F_n) Function Select Inputs (S_n) to Overflow Output (OVR) or Carry Output (C_{n+4}) A or B Operand Input (A_n or B_n) to Carry Output (C_{n+4}) and Overflow Output (OVR)

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS


V_{CC}
PULSE GENERATOR
V_{IN}
D.U.T.
V_{OUT}
R_T
C_L
R_L
TC01860S

Test Circuit for 3-State Outputs


NEGATIVE PULSE
90%
V_M
10%
t_W
AMP (V)
0V
$t_{THL}(t_f)$
$t_{TLH}(t_r)$
POSITIVE PULSE
$t_{TLH}(t_r)$
$t_{THL}(t_f)$
90%
V_M
10%
WF06450S

V_M = 1.5V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F384
Multiplier

8-Bit Serial/Parallel Two's Complement Multiplier
Preliminary Specification

FAST Products

FEATURES

- **8-bit by 1-bit sequential logic element**
- **Multiplies two numbers represented in Two's Complement**
- **Parallel inputs accept and store an 8-bit multiplicand ($X_0 - X_7$)**
- **K input is used for expansion to longer words**
- **Mode Control (M) is used to establish the most significant device**
- **Asynchronous Parallel Load (PL) input clears the internal flip-flop to the start condition and enables the X latches to accept new multiplicand data**

DESCRIPTION

The 'F384 is an 8-bit sequential logic element that multiplies two numbers represented in Two's Complement notation. The device implements Booth's algorithm internally to produce a Two's Complement product that needs no subsequent correction. Parallel inputs accept and store an 8-bit multiplicand ($X_0 - X_7$). The multiplier word is applied to the Y input in a serial bit stream, least significant bit first. The product is clocked out at the SP output, least significant bit first.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F384	100MHz	60mA

ORDERING INFORMATION

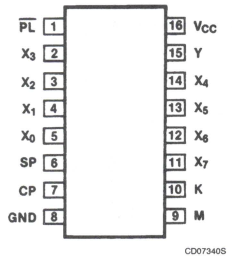
PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
16-Pin Plastic DIP	N74F384N
16-Pin Plastic SOL	N74F384D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

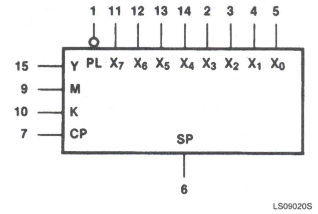
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$X_0 - X_7$	Multiplicand data inputs	1.0/1.0	20μA/0.6mA
CP	Clock input (active rising edge)	1.0/1.0	20μA/0.6mA
K	Serial expansion input	1.0/1.0	20μA/0.6mA
M	Mode control input	1.0/1.0	20μA/0.6mA
$\overline{PL}$	Asynchronous Parallel Load input	1.0/1.0	20μA/0.6mA
Y	Serial multiplier inputs	1.0/1.0	20μA/0.6mA
SP	Serial X,Y product output	50/33.3	1mA/20mA

NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION

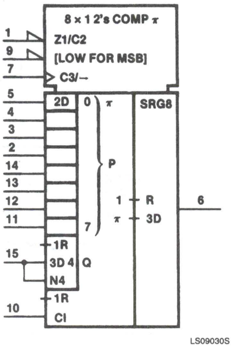

PL 1
X3 2
X2 3
X1 4
X0 5
SP 6
CP 7
GND 8
16 Vcc
15 Y
14 X4
13 X5
12 X6
11 X7
10 K
9 M
CD07340S

LOGIC SYMBOL


1 11 12 13 14 2 3 4 5
Y PL X7 X6 X5 X4 X3 X2 X1 X0
15
9 M
10 K
7 CP
SP
6
LS09020S

V_{CC} = Pin 16
GND = Pin 8

LOGIC SYMBOL (IEEE/IEC)


8 × 1 2's COMP π
Z1/C2
[LOW FOR MSB]
C3/→
1
9
7
5
4
3
2
14
13
12
11
15
10
2D
0
π
P
7
SRG8
1 R
π 3D
6
1R
3D 4
Q
N4
1R
CI
LS09030S

The K input is used for expansion to longer X words, using two or more 'F384 devices. The Mode Control (M) input is used to establish the most significant device. An asynchronous Parallel Load (PL) input clears the internal flip-flops to the start condition and enables the X latches to accept new multiplicand data.

Referring to the Logic Diagram, the multiplicand ($X_0 - X_7$) latches are enabled to receive new data when $\overline{PL}$ is Low. Data that meets the setup time requirements is latched and stored when $\overline{PL}$ goes High. The Low signal on $\overline{PL}$ also clears the Y_{a-1} flip-flop as well as the Carry-save flip-flops and the partial product register in the arithmetic section. Figure 1 is a conceptual logic diagram of a typical cell in the arithmetic section, except for the first (X_7) cell, in which K is the B_i input and M is incorporated into the Carry logic. The cells use the Carry-save technique to avoid the complexity and delays inherent in look-ahead Carry schemes for longer words.

Figure 2 is a timing diagram for an 8 × 8 multiplication process. New multiplicand data enters the X latches during bit time T_0. It is assumed that $\overline{PL}$ goes Low shortly after the CP rising edge that marks the beginning of T_0 and goes High again shortly after the beginning of T_1. The LSB (Y_0) of the multiplier is applied to the Y input during T_1 and combines with X_0 in the least significant cell to form the appropriate D input (X_0Y_0) to the sum flip-flop. This is clocked into the sum flip-flop by the CP rising edge at the beginning of T_2 and this LSB (S_0) of the product is available shortly thereafter at the SP output of the package.

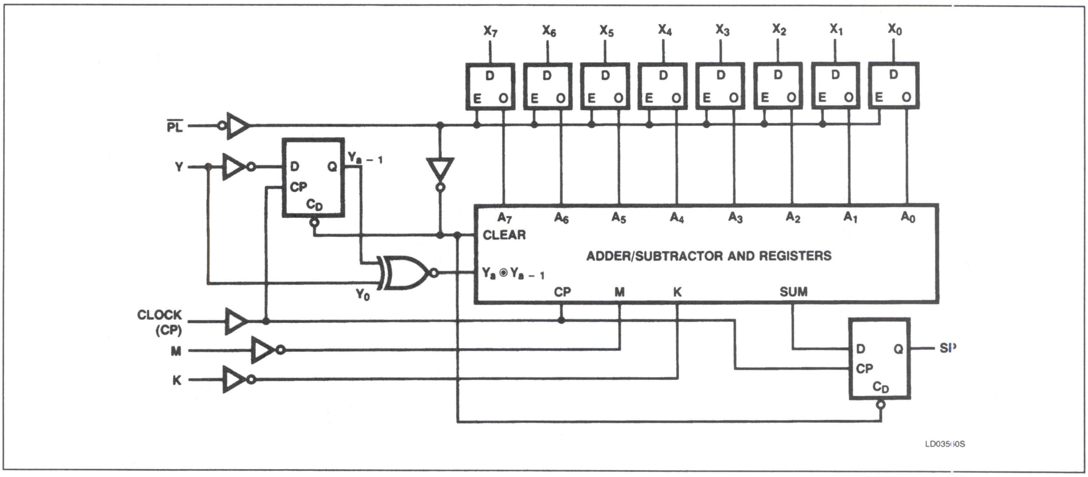
FUNCTION TABLE

INPUTS						INTERNAL	OUTPUT	FUNCTION
$\overline{PL}$	CP	K	M	X_1	Y	Y_{a-1}	SP	
X	X	L	L	X	X	X	X	Most significant multiplier device
X	X	CS	H	X	X	X	X	Device cascaded in multiplier string
L	X	X	X	OP	X	L	L	Load new multiplicand and clear internal sum and carry registers
H	X	X	X	X	X	X	X	Device enabled
H	↑	X	X	X	L	L	AR	Shift sum register
H	↑	X	X	X	L	H	AR	Add multiplicand to sum register and shift
H	↑	X	X	X	H	L	AR	Subtract multiplicand from sum register and shift
H	↑	X	X	X	H	H	AR	Shift sum register

H = High voltage level
L = Low voltage level
↑ = Low-to-High Transition
CS = Connected to SP output of high-order device
OP = X_1 latches open for new data (I = 0 – 7)
AR = Output as required per Booth's algorithm
X = Don't care

The next-least bit (Y_1) of the multiplier is also applied during T_2. The detailed logic design of the cell is such that during T_2 the D input to the sum flip-flop of the least significant cell contains not only X_0Y_1 but also, the X_1Y_0 product. Thus the term ($X_1Y_0 + X_0Y_1$) is formed at the D input of the least significant sum flip-flop during T_2 and this next-least term S_1 of the product is available at the SP output shortly after the CP rising edge at the beginning of T_3. Due to storage in the two preceding cells and in its own Carry flip-flop, the D input to the least significant sum flip-flop during T_3 will contain the products X_2Y_0 and X_1Y_1 as well as X_0Y_2. During each succeeding bit time the SP output contains information formed one stage further upstream. For example, the SP output during T_9 contains X_7Y_0, which was actually formed during T_1.

LOGIC DIAGRAM



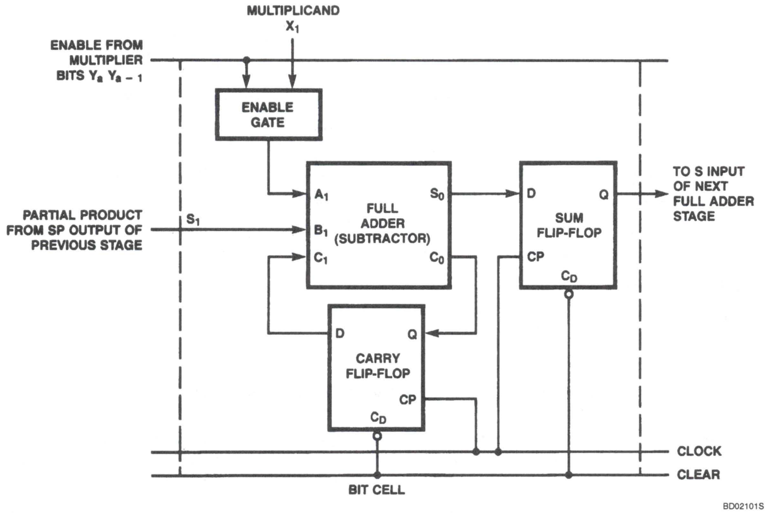

MULTIPLICAND
X_1
ENABLE FROM MULTIPLIER BITS Y_a Y_{a-1}
ENABLE GATE
PARTIAL PRODUCT FROM SP OUTPUT OF PREVIOUS STAGE
S_1
A_1
B_1
C_1
FULL ADDER (SUBTRACTOR)
S_0
C_0
D
Q
SUM FLIP-FLOP
CP
C_D
TO S INPUT OF NEXT FULL ADDER STAGE
D
Q
CARRY FLIP-FLOP
CP
C_D
CLOCK
CLEAR
BIT CELL
BD02101S

Figure 1. Conceptual Carry Save Adder Cell

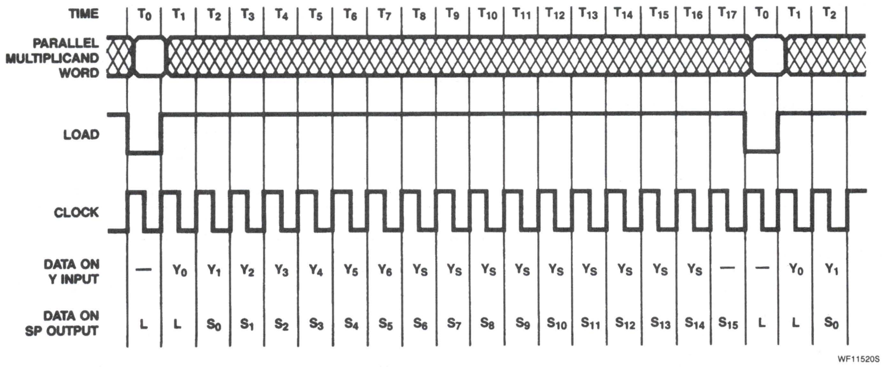

TIME
T_0 T_1 T_2 T_3 T_4 T_5 T_6 T_7 T_8 T_9 T_{10} T_{11} T_{12} T_{13} T_{14} T_{15} T_{16} T_{17} T_0 T_1 T_2
PARALLEL MULTIPLICAND WORD
LOAD
CLOCK
DATA ON Y INPUT
— Y_0 Y_1 Y_2 Y_3 Y_4 Y_5 Y_6 Y_S Y_S Y_S Y_S Y_S Y_S Y_S Y_S Y_S — — Y_0 Y_1
DATA ON SP OUTPUT
L L S_0 S_1 S_2 S_3 S_4 S_5 S_6 S_7 S_8 S_9 S_{10} S_{11} S_{12} S_{13} S_{14} S_{15} L L S_0
WF11520S

Figure 2. Timing Diagram Showing 18 Clock Cycle Operation of 8 × 8 Multiplication

The MSB Y_7 (the sign bit Y_S) of the multiplier is first applied to the Y input during T_8 and must also be applied during bit times T_9 through T_{16}. This extension of the sign bit is a necessary adjunct to the implementation of Booth's algorithm and is a built-in feature of the 'F322 Shift Register. Figure 3 shows the method of using two 'F384s to perform a $12 \times n$ bit multiplication. Notice that the sign of X is effectively extended by connecting X_{11} to $X_4 - X_7$ of the most significant package. Whereas the 8 × 8 multiplication required 18 clock periods ($m + n$ to form the product terms plus T_0 to clear the multiplier plus T_{17} to recognize and store S_{15}), the arrangement of Figure 3 requires $12 + n$ bits to form the product terms plus the bit times to clear the multiplier and to recognize and store SP_{n+11}.

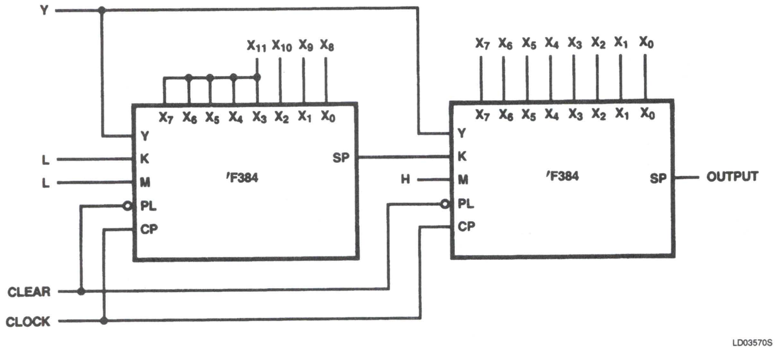

Y
X11 X10 X9 X8
X7 X6 X5 X4 X3 X2 X1 X0
X7 X6 X5 X4 X3 X2 X1 X0
Y
K
M
PL
CP
SP
'F384
L
L
H
X7 X6 X5 X4 X3 X2 X1 X0
Y
K
M
PL
CP
'F384
SP
OUTPUT
CLEAR
CLOCK
LD03570S

Figure 3. 12-Bit by n-Bit Two's Complement Multiplier

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +1	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		74F384			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX V_{IH} = MIN	±10%V_{CC}	2.5			V
			±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, I_{OL} = MAX V_{IH} = MIN	±10%V_{CC}		0.35	0.50	V
			±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, $I_I = I_{IK}$			−0.73	−1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V			−0.4	−0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		−75		−250	mA
I_{CC}	Supply current (total)	V_{CC} = MAX			60	90	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

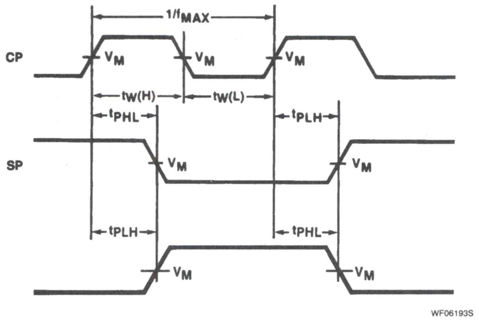
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F384					UNIT
			T_A = +25°C V_{CC} = +5.0V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = +5.0V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	80	100		70		MHz
t_{PLH} t_{PHL}	Propagation delay CP to SP	Waveform 1	3.5 3.5	4.5 4.5	5.5 5.5	3.5 3.5	10.0 10.0	ns
t_{PHL}	Propagation delay $\overline{PL}$ to SP	Waveform 2	6.0	10.0	13.0	6.0	14.0	ns

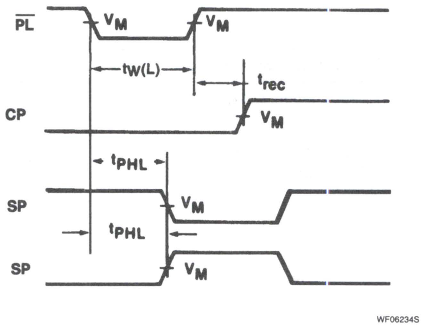
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	74F384					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$, $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low K to CP	Waveform 3	13.5 13.5			15.0 15.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low K to CP	Waveform 3	2.0 2.0			2.0 2.0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low Y to CP	Waveform 3	15.0 15.0			15.0 15.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low Y to CP	Waveform 3	2.0 2.0			2.0 2.0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low X_n to $\overline{PL}$	Waveform 3	5.5 5.5			6.5 6.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low X_n to $\overline{PL}$	Waveform 3	2.0 2.0			2.0 2.0		ns
$t_w(H)$ $t_w(L)$	CP pulse width High or Low	Waveform 1	7.0 5.5			7.5 6.0		ns
$t_w(L)$	$\overline{PL}$ pulse width Low	Waveform 2	6.5			7.0		ns
t_{rec}	Recovery time $\overline{PL}$ to CP	Waveform 2	5.5			6.0		ns

AC WAVEFORMS



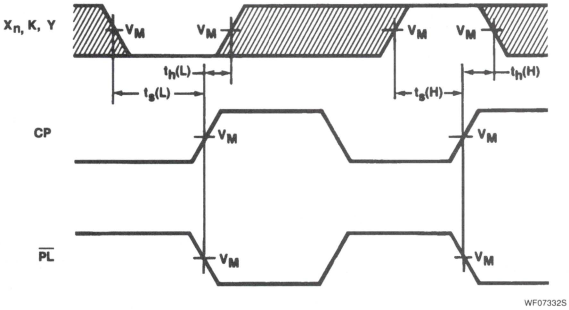
Waveform 1. Clock to Output Delays, Clock Pulse Width and Maximum Clock Frequency



Waveform 2. Master Reset Pulse Width, Master to Output Delay and Master Reset to Clock Recovery Time

NOTE: For all waveforms, $V_M = 1.5V$.

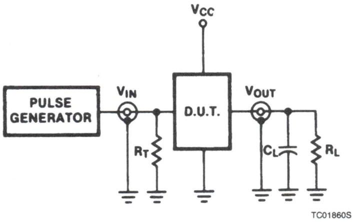
AC WAVEFORMS (Continued)


Xn, K, Y
VM
VM
VM
VM
th(L)
ts(L)
ts(H)
th(H)
CP
VM
VM
PL
VM
VM
WF07332S

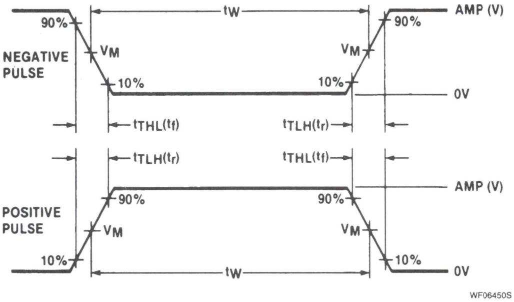
Waveform 3. Data and Select Setup and Hold Times

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS


VCC
PULSE GENERATOR
VIN
RT
D.U.T.
VOUT
CL
RL
TC01860S

Test Circuit for Totem-Pole Outputs


NEGATIVE PULSE
90%
VM
10%
tW
AMP (V)
0V
tTHL(tf)
tTLH(tr)
tTLH(tr)
tTHL(tf)
POSITIVE PULSE
90%
VM
10%
tW
AMP (V)
0V
WF06450S

$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS

R_L = Load resistor to GND; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F385
Adder/Subtracter

Quad Serial Adder/Subtracter
Product Specification

FAST Products

FEATURES

- **Four independent adder/subtracters**
- **Two's Complement arithmetic**
- **Synchronous operation**
- **Common Clear and Clock**
- **One's Complement or magnitude-only capability**
- **'F385 is designed for use with serial multipliers in implementing digital filters and butterfly networks in fast Fourier transforms**

DESCRIPTION

The 'F385 contains four serial adder/subtracters with common Clock and Master Reset, but independent Operand and Select inputs.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F385	140MHz	55mA

ORDERING INFORMATION

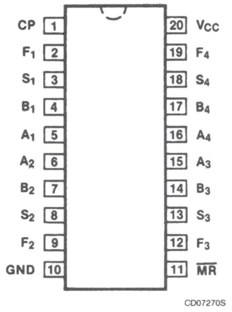
PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
20-Pin Plastic DIP	N74F385N
20-Pin Plastic SOL	N74F385D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

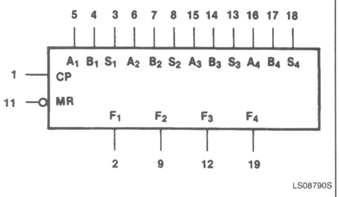
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$A_1 - A_4$	A operand inputs	1.0/1.0	20μA/0.6mA
$B_1 - B_4$	B operand inputs	1.0/1.0	20μA/0.6mA
$S_1 - S_4$	Function select inputs	1.0/1.0	20μA/0.6mA
CP	Clock Pulse input (active rising edge)	1.0/1.0	20μA/0.6mA
$\overline{MR}$	Asynchronous Master Reset input (active-Low)	1.0/1.0	20μA/0.6mA
$F_1 - F_4$	Sum or difference outputs	50/33	1mA/20mA

NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION

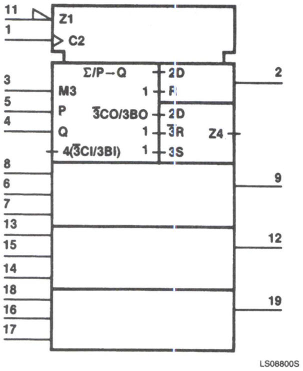

CP 1
F1 2
S1 3
B1 4
A1 5
A2 6
B2 7
S2 8
F2 9
GND 10
20 Vcc
19 F4
18 S4
17 B4
16 A4
15 A3
14 B3
13 S3
12 F3
11 MR
CD07270S

LOGIC SYMBOL


5 4 3 6 7 8 15 14 13 16 17 18
A1 B1 S1 A2 B2 S2 A3 B3 S3 A4 B4 S4
1 CP
11 MR
F1 F2 F3 F4
2 9 12 19
LS08790S

V_{CC} = Pin 20
GND = Pin 10

LOGIC SYMBOL (IEEE/IEC)


11
1
Z1
C2
3
5
4
M3
P
Q
Σ/P−Q
3CO/3BO
4(3CI/3BI)
2D
1 F
2D
1 3R
1 3S
Z4
2
8
6
7
9
13
15
14
12
18
16
17
19
LS08800S

Adder/Subtracter

FAST 74F385

Each adder contains two edge-triggered flip-flops to store the sum and carry, as shown in the Logic Diagram. Flip-flop state changes occur on the rising edge of the Clock Pulse (CP) input signal. The Select (S) input should be Low for the Add (A plus B) mode and High for the Subtract (A minus B) mode. A Low signal on the asynchronous Master Reset (MR) input clears the sum flip-flop and resets the Carry flip-flop to zero in the Add mode or presets it to one in the Subtract mode.

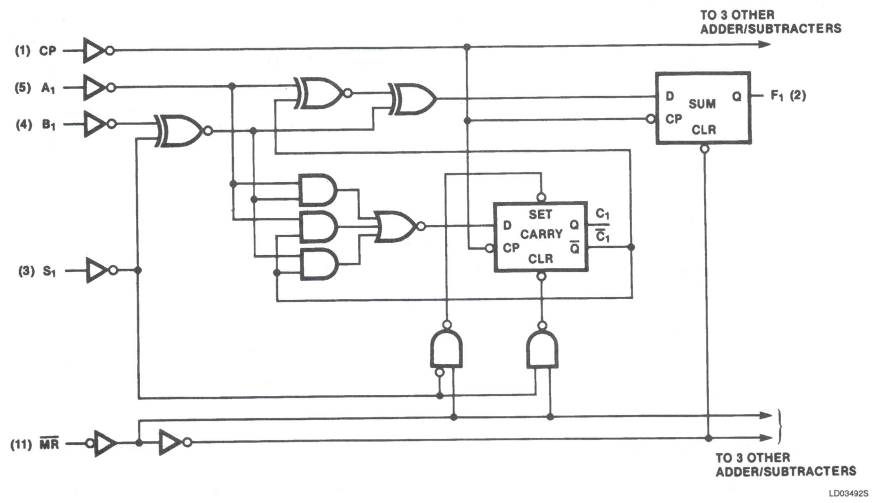
In the Subtract mode, the B operand is internally complemented. Presetting the Carry flip-flop to one completes the Two's Complement transformation by adding one to "A plus B" during the first (LSB) operation after $\overline{MR}$ is released. For One's Complement subtraction, the Carry flip-flop can be set to zero by making S Low during the reset, then making S High after the reset but before the next Clock.

TRUTH TABLE

INPUTS*				INTERNAL CARRY		OUTPUT*	FUNCTION
$\overline{MR}$	S	A	B	C	C_1	F	
L	L	X	X	L	L	L	Clear
L	H	X	X	H	H	L	
H	L	L	L	L	L	L	Add
H	L	L	L	H	L	H	
H	L	L	H	L	L	H	
H	L	L	H	H	H	L	
H	L	H	L	L	L	H	
H	L	H	L	H	H	L	
H	L	H	H	L	H	L	
H	L	H	H	H	H	H	
H	H	L	L	L	L	H	Subtract
H	H	L	L	H	H	L	
H	H	L	H	L	L	L	
H	H	L	H	H	L	H	
H	H	H	L	L	H	L	
H	H	H	L	H	H	H	
H	H	H	H	L	L	H	
H	H	H	H	H	H	L	

H = High voltage level
L = Low voltage level
X = Don't care
* = Inputs before CP transition, output after C
C_1= Carry flip-flop state before (C) and after (C_1) Clock transition

LOGIC DIAGRAM (One Adder/Subtracter shown)



V_{CC} = Pin 20
GND = Pin 10
( ) = Pin numbers

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	–0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Store temperature	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			–18	mA
I_{OH}	High-level output current			–1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		74F384, 74F385			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$			–0.73	–1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V			5	100	μA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V			–0.4	–0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		–60		–150	mA
I_{CC}	Supply current (total)	'F385	V_{CC} = MAX			55	80	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

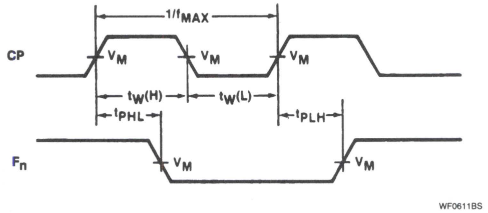
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F385					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	100	140		90		MHz
t_{PLH} t_{PHL}	Propagation delay CP to F_n	Waveform 1	3.0 3.5	5.0 5.5	8.0 9.0	2.5 3.5	9.0 10	ns
t_{PLH}	Propagation delay $\overline{MR}$ to F_n	Waveform 2	4.0	6.5	9.5	4.0	10.5	ns

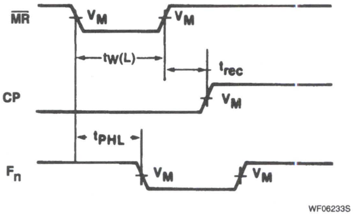
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	74F385					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low A_n, B_n or S_n to CP	Waveform 3	12.0 12.0			12.0 12.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low A_n, B_n or S_n to CP	Waveform 3	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low	Waveform 3	6.0 6.0			6.0 6.0		ns
$t_w(L)$	$\overline{MR}$ Pulse width Low	Waveform 2	6.0			6.0		ns
t_{rec}	Recovery time, $\overline{MR}$ to CP	Waveform 2	8.5			9.5		ns

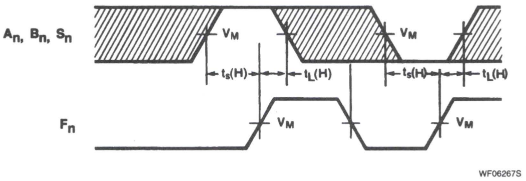
AC WAVEFORMS


1/fMAX
CP
VM
VM
VM
tW(H)
tW(L)
tPHL
tPLH
Fn
VM
VM
WF06118S

Waveform 1. Propagation Delay, Clock Input to Output, Clock Widths, and Maximum Clock Frequency


MR
VM
VM
tW(L)
trec
CP
VM
tPHL
Fn
VM
VM
WF06233S

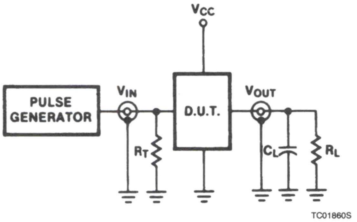
Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay, and Master Reset to Clock Recovery Time


An, Bn, Sn
VM
VM
ts(H)
tL(H)
ts(H)
tL(H)
Fn
VM
VM
WF06267S

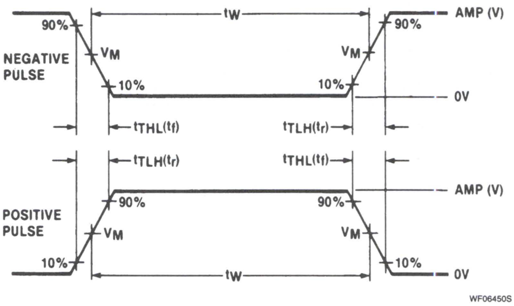
Waveform 3. Data and Select Setup and Hold Times

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS


VCC
PULSE GENERATOR
VIN
D.U.T.
VOUT
RT
CL
RL
TC01860S

Test Circuit for Totem-Pole Outputs


NEGATIVE PULSE
90%
VM
10%
tW
90%
VM
10%
AMP (V)
0V
tTHL(tf)
tTLH(tr)
tTLH(tr)
tTHL(tf)
POSITIVE PULSE
90%
VM
10%
90%
VM
10%
tW
AMP (V)
0V
WF06450S

$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS
R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST Products

FAST 74F393

Dual 4-Bit Binary Ripple Counter

Product Specification

FEATURES

- **Two 4-bit binary counters**
- **Two Master Resets to clear each 4-bit counter individually**

DESCRIPTION

The 'F393 is a Dual Binary Ripple Counter with separate Clock ($\overline{CP}_n$) and Master Reset (MR) inputs to each counter. The two counters are identified by the "a" and "b" suffixes in the pin configuration. The operation of each half of the 'F393 is the same. The counters are triggered by a High-to-Low transition of the Clock ($\overline{CP}_a$ and $\overline{CP}_b$) inputs. The counter outputs are internally connected to provide Clock inputs to succeeding stages. The outputs of the ripple counter do not change synchronously and should not be used for High-speed address decoding. The Master Resets (MR_a and MR_b) are active-High asynchronous inputs; one for each 4-bit counter. A High level on the MR input overrides the clock and sets the outputs Low.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F393	125MHz	mA

ORDERING INFORMATION

PACKAGE	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
14-Pin Plastic DIP	74F393N
14-Pin Plastic SO	74F393D

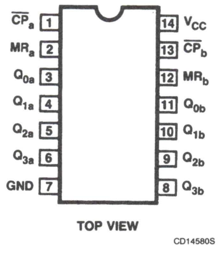
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$\overline{CP}_a$, $\overline{CP}_b$	Clock inputs	1.0/1.0	20μA/0.6mA
MR_a, MR_b	Master Reset inputs	1.0/1.0	20μA/0.6mA
Q_{na}, Q_{nb}	Data outputs	50/33.3	1.0mA/20mA

NOTE:

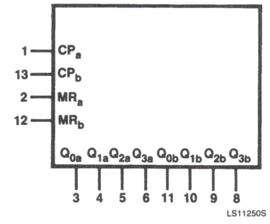
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



$\overline{CP}_a$ 1
MR_a 2
Q_{0a} 3
Q_{1a} 4
Q_{2a} 5
Q_{3a} 6
GND 7
14 V_{CC}
13 $\overline{CP}_b$
12 MR_b
11 Q_{0b}
10 Q_{1b}
9 Q_{2b}
8 Q_{3b}
TOP VIEW
CD14580S

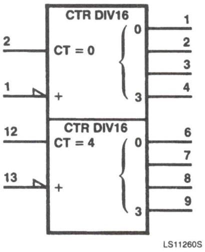
LOGIC SYMBOL



1 $\overline{CP}_a$
13 $\overline{CP}_b$
2 MR_a
12 MR_b
Q_{0a} Q_{1a} Q_{2a} Q_{3a} Q_{0b} Q_{1b} Q_{2b} Q_{3b}
3 4 5 6 11 10 9 8
LS11250S

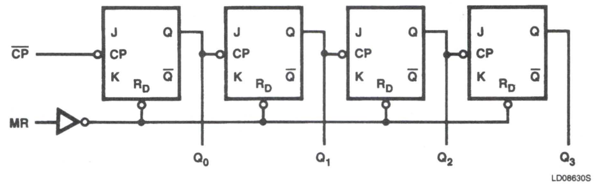
V_{CC} = Pin 14
GND = Pin 7

LOGIC SYMBOL (IEEE/IEC)



CTR DIV16
CT = 0
2
1
+
0
3
1
2
3
4
CTR DIV16
CT = 4
12
13
+
0
3
6
7
8
9
LS11260S

LOGIC DIAGRAM



$\overline{CP}$
MR
J
CP
K
R_D
Q
$\overline{Q}$
Q_0
Q_1
Q_2
Q_3
LD08630S

V_{CC} = Pin 14
GND = Pin 7

COUNT SEQUENCE FOR EACH COUNTER

COUNT	OUTPUTS			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

H = High voltage level
L = Low voltage level

Dual 4-Bit Binary Ripple Counter FAST 74F393

ABSOLUTE MAXIMUM RATINGS

(Operating beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX V_{IH} = MIN	±10% V_{CC}	2.5			V
				±5% V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OL} = MAX V_{IH} = MIN	±10% V_{CC}		0.35	0.50	V
				±5% V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				−0.6	mA
I_{OS}	Short-circuit output current[3]		V_{cc} = MAX		−60		−150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			25	36	mA
		I_{CCL}	V_{CC} = MAX			42	58	mA

NOTES:

1. For conditons shown as MIN or MAX, use the appropriate value under the recommended operating conditions for the applicable conditions.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of High-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} should be performed last.

Dual 4-Bit Binary Ripple Counter

FAST 74F393

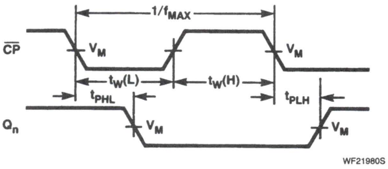
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNIT
			$T_A = +25°C$ $V_{CC} = 5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			T_A=0°C to +70°C $V_{CC} = +5.0V \pm 10\%$ CL = 50pF $R_L = 500\Omega$			
			Min	Typ	Max	Min	Typ	Max	
f_{MAX}	Maximum Clock frequency	Waveform 1	100	130		100			MHz
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}$ to Q_0	Waveform 1	3.5 5.0	5.5 7.0	8.0 10.0	3.5 5.0		9.0 10.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}$ to Q_1	Waveform 1	5.0 7.5	7.0 9.5	10.0 12.0	4.5 7.0		13.0 13.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}$ to Q_2	Waveform 1	8.0 9.5	10.0 11.5	13.0 14.5	7.0 9.0		15.0 15.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}$ to Q_3	Waveform 1	10.5 12.0	12.5 14.0	15.5 16.5	10.0 11.5		17.0 17.5	ns
t_{PHL}	Propagation delay MR to Q_n	Waveform 2	4.0	6.0	9.0	4.0		9.0	ns

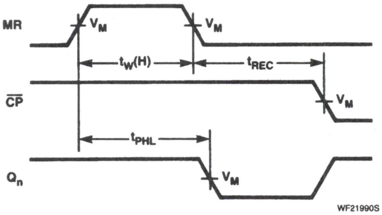
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNIT
			$T_A = +25°C$ $V_{CC} = 5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			T_A=0°C to +70°C $V_{CC} = +5.0V \pm 10\%$ CL = 50pF $R_L = 500\Omega$			
			Min	Typ	Max	Min	Typ	Max	
$t_w(H)$ $t_w(L)$	$\overline{CP}$ pulse width	Waveform 1	4.5 3.5			5.0 4.0			ns
$t_w(H)$	MR pulse width	Waveform 2	3.5			4.5			ns
t_{rec}	Recovery time, MR to $\overline{CP}$	Waveform 2	2.5			3.0			ns

AC WAVEFORMS


1/fMAX
CP
VM
VM
tW(L)
tW(H)
tPHL
tPLH
Qn
VM
VM
WF21980S

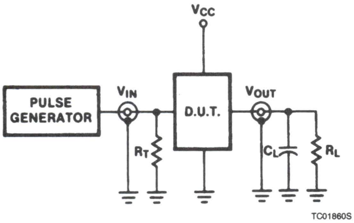
Waveform 1. Propagation Delay, Clock to Output


MR
VM
VM
tW(H)
tREC
CP
VM
tPHL
Qn
VM
WF21990S

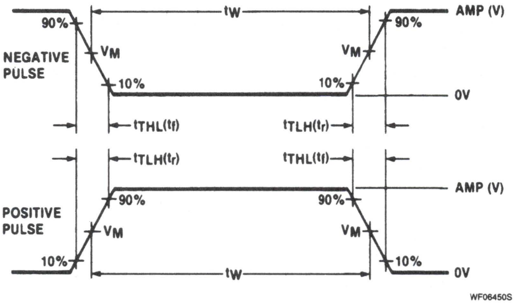
Waveform 2. Propagation Delay, Master Reset Input to Output

NOTE: $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORMS


VCC
PULSE GENERATOR
VIN
D.U.T.
VOUT
RT
CL
RL
TC01860S

Test Circuit for Totem-Pole Outputs


tW
AMP (V)
90%
90%
NEGATIVE PULSE
VM
VM
10%
10%
0V
tTHL(tf)
tTLH(tr)
tTLH(tr)
tTHL(tf)
AMP (V)
90%
90%
POSITIVE PULSE
VM
VM
10%
10%
0V
tW
WF06450S

$V_M = 1.5V$

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor to GND; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F395
Shift Register

4-Bit Cascadable Shift Register (3-State)
Product Specification

FAST Products

FEATURES

- **4-bit parallel load shift register**
- **Independent 3-State buffer outputs, $Q_0 - Q_3$**
- **Separate Q_S output for serial expansion**
- **Asynchronous Master Reset**

DESCRIPTION

The 'F395 is a 4-Bit Shift Register with serial and parallel synchronous operating modes and four 3-State buffer outputs. The shifting and loading operations are controlled by the state of the Parallel Enable (PE) input. When PE is High, data is loaded from the Parallel Data inputs ($D_0 - D_3$) into the register synchronous with the High-to-Low transition of the Clock input ($\overline{CP}$). When PE is Low, the data at the Serial Data input (D_S) is loaded into the Q_0 flip-flop, and the data in the register is shifted one bit to the right in the direction ($Q_0 \rightarrow Q_1 \rightarrow Q_2 \rightarrow Q_3$) synchronous with the negative clock transition. The PE and Data inputs are fully edge-triggered and must be stable only one setup prior to the High-to-Low transition of the clock.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F395	120MHz	32mA

ORDERING INFORMATION

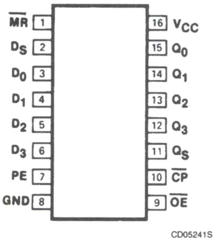
PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
16-Pin Plastic DIP	N74F395N
16-Pin Plastic SO	N74F395D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

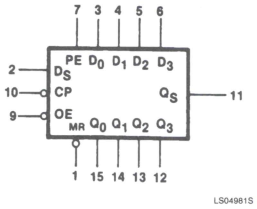
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$D_0 - D_3$	Data inputs	1.0/1.0	20μA/0.6mA
D_S	Serial data input	1.0/1.0	20μA/0.6mA
PE	Enable input	1.0/1.0	20μA/0.6mA
$\overline{MR}$	Master Reset input (active-Low)	1.0/1.0	20μA/0.6mA
$\overline{OE}$	Output enable input (active-Low)	1.0/1.0	20μA/0.6mA
$\overline{CP}$	Clock Pulse input (active falling edge)	1.0/1.0	20μA/0.6mA
Q_S	Serial expansion output	50/33	1.0mA/20mA
$Q_0 - Q_3$	Data outputs (3-States)	150/40	3.0mA/24mA

NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION

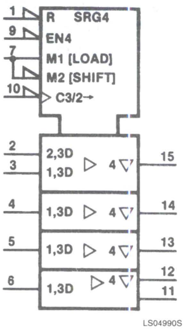

MR 1
DS 2
D0 3
D1 4
D2 5
D3 6
PE 7
GND 8
16 VCC
15 Q0
14 Q1
13 Q2
12 Q3
11 QS
10 CP
9 OE
CD05241S

LOGIC SYMBOL


7 3 4 5 6
PE D0 D1 D2 D3
2 DS
10 CP
9 OE
QS 11
MR Q0 Q1 Q2 Q3
1 15 14 13 12
LS04981S

V_{CC} = Pin 16
GND = Pin 8

LOGIC SYMBOL (IEEE/IEC)


1 R SRG4
9 EN4
7 M1 [LOAD]
M2 [SHIFT]
10 C3/2→
2 2,3D
3 1,3D
15
4 1,3D 14
5 1,3D 13
6 1,3D 12 11
4▽
LS04990S

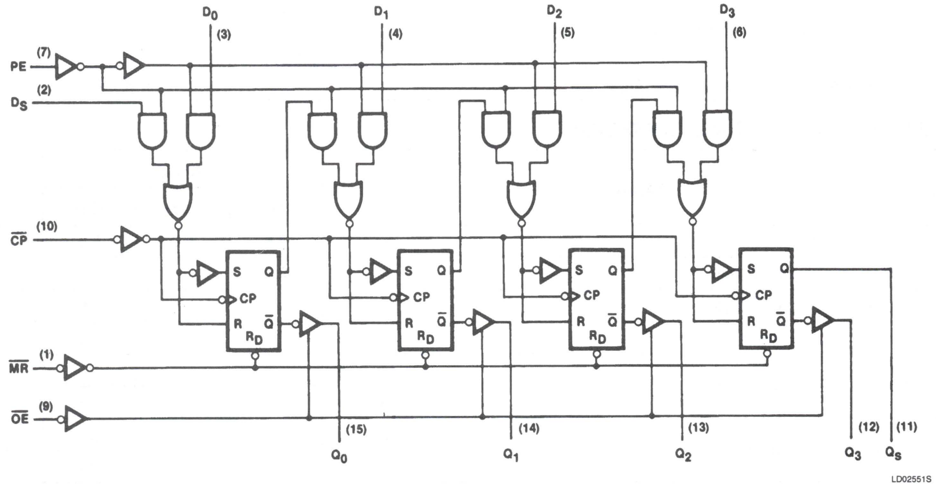
Shift Register

FAST 74F395

The Master Reset ($\overline{MR}$) is an asynchronous active-Low input. When Low, the $\overline{MR}$ overrides the clock and all other inputs and clears the register.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, or large capacitive loads. The active-Low Output Enable ($\overline{OE}$) controls all four 3-State buffers independent of the register operation. The data in the register appears at the outputs when $\overline{OE}$ is Low. The outputs are in the High-impedance "OFF" state, which means they will neither drive nor load the bus when $\overline{OE}$ is High. The output from the last stage is brought out separately. This output (Q_S) is tied to the Serial Data input (D_S) of the next register for serial expansion applications. The Q_S output is not affected by the 3-State buffer operation.

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
( ) = Pin numbers

MODE SELECT—FUNCTION TABLE

REGISTER OPERATING MODES	INPUTS					OUTPUTS			
	$\overline{MR}$	$\overline{CP}$	PE	D_S	D_n	Q_0	Q_1	Q_2	Q_3
Reset (clear)	L	X	X	X	X	L	L	L	L
Shift right	H	↓	l	l	X	L	q_0	q_1	q_2
	H	↓	l	h	X	H	q_0	q_1	q_2
Parallel load	H	↓	h	X	l	L	L	L	L
	H	↓	h	X	h	H	H	H	H

3-STATE BUFFER OPERATING MODES	INPUTS		OUTPUTS	
	$\overline{OE}$	Q_n (Register)	Q_0, Q_1, Q_2, Q_3	Q_s
Read	L	L	L	L
	L	H	H	H
Disable buffers	H	L	Z	L
	H	H	Z	H

H = High voltage level
h = High voltage level one setup time prior to the High-to-Low clock transition
L = Low voltage level
l = Low voltage voltage level one setup time prior to the High-to-Low clock transition
q_n = Lower case letters indicate the state of the referenced output one setup time prior to the High-to-Low clock transition
X = Don't care
Z = High-impedance "OFF" state
↓ = High-to-Low transition

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		−0.5 to +7.0	V
V_{IN}	Input voltage		−0.5 to +7.0	V
I_{IN}	Input current		−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		−0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	Q_S	40	mA
		$Q_0 - Q_3$	48	mA
T_A	Operating free-air temperature range		0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	High-level output current	Q_S			−1	mA
		$Q_0 - Q_3$			−3	mA
I_{OL}	Low-level output current	Q_S			20	mA
		$Q_0 - Q_3$			24	mA
T_A	Operating free-air temperature		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			74F395			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage	Q_S	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = −1mA	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7	3.4		V
		$Q_0 - Q_3$		I_{OH} = −3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.3		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX		±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$				−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V					100	μA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					−0.6	mA
I_{OZH}	OFF-state current High-level voltage applied	$Q_0 - Q_3$ only	V_{CC} = MAX, V_O = 2.7V					50	μA
I_{OZL}	OFF-state current Low-level voltage applied	$Q_0 - Q_3$ only	V_{CC} = MAX, V_O = 0.5V					−50	μA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX			−60		−150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	$\overline{MR} = PE = D_n = D_s = 4.5V$, $\overline{OE} = GND$, $\overline{CP} = \downarrow$			33	48	mA
		I_{CCL}		$PE = 4.5V$, $\overline{MR} = \overline{OE} = D_n = D_s = GND$, $\overline{CP} = \downarrow$			35	50	mA
		I_{CCZ}		$\overline{OE} = 4.5V$, $\overline{MR} = D_n = D_s = GND$			32	46	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of High-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

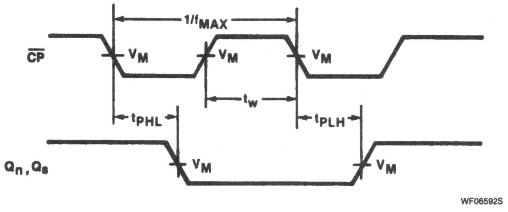
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F395					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	105	120		95		MHz
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}$ to Q_n	Waveform 1	3.5 5.0	6.0 8.0	8.5 11.0	3.5 5.0	9.5 11.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}$ to Q_s	Waveform 1	5.0 5.5	6.5 7.0	9.0 9.5	4.5 5.0	10.0 10.0	ns
t_{PHL}	Propagation delay, $\overline{MR}$ to Q_n	Waveform 2	5.0	7.5	10.0	5.0	10.5	ns
t_{PHL}	Propagation delay, $\overline{MR}$ to Q_s	Waveform 2	4.5	6.5	8.5	4.5	9.0	ns
t_{PZH} t_{PZL}	Output enable time to High or Low level	Waveform 4 Waveform 5	4.0 3.5	6.5 6.0	9.0 8.0	4.0 3.5	10.0 8.5	ns
t_{PHZ} t_{PLZ}	Output disable time from High or Low	Waveform 4 Waveform 5	1.0 1.0	2.5 3.5	4.5 5.5	1.0 1.0	5.5 6.5	ns

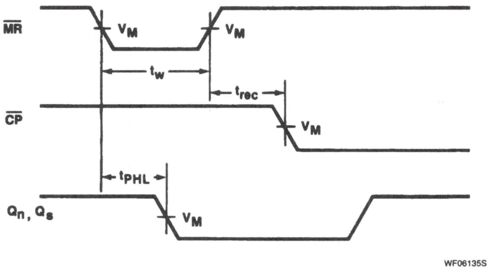
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	74F395					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to $\overline{CP}$	Waveform 3	1.0 1.0			1.0 1.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to $\overline{CP}$	Waveform 3	1.0 1.5			1.0 1.5		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low PE to $\overline{CP}$	Waveform 3	6.5 4.0			7.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low PE to $\overline{CP}$	Waveform 3	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	$\overline{CP}$ pulse width, High or Low	Waveform 1	5.0 4.0			5.5 4.5		ns
$t_w(L)$	$\overline{MR}$ pulse width Low	Waveform 2	2.5			3.0		ns
t_{rec}	Recovery time $\overline{MR}$ to $\overline{CP}$	Waveform 2	6.0			7.0		ns

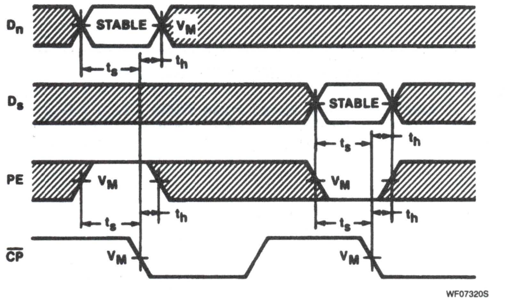
AC WAVEFORMS


1/fMAX
CP
VM
VM
VM
tw
tPHL
tPLH
Qn, Qs
VM
VM
WF06592S

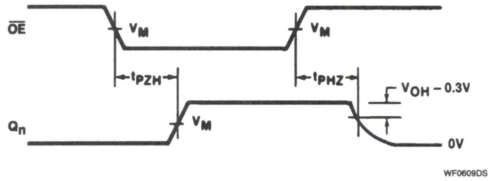
Waveform 1. Clock to Output Delays and Clock Pulse Width


MR
VM
VM
tw
trec
CP
VM
tPHL
Qn, Qs
VM
WF06135S

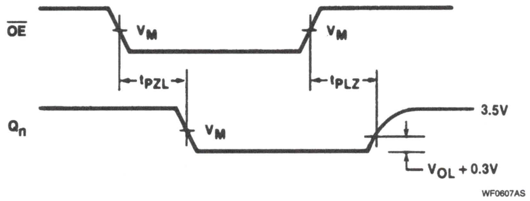
Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time


Dn
STABLE
VM
ts
th
Ds
STABLE
ts
th
PE
VM
VM
ts
th
ts
th
CP
VM
VM
WF07320S

Waveform 3. Parallel Enable and Data Setup and Hold Times


OE
VM
VM
tPZH
tPHZ
VOH − 0.3V
Qn
VM
0V
WF0609DS

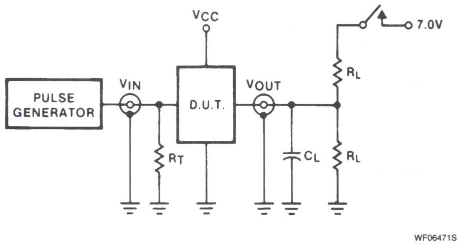
Waveform 4. 3-State Output Enable Time to High Level and Disable Output Time From High Level


OE
VM
VM
tPZL
tPLZ
Qn
VM
3.5V
VOL + 0.3V
WF0607AS

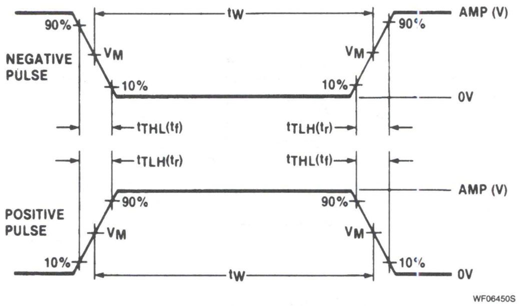
Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS


VCC
7.0V
RL
PULSE GENERATOR
VIN
D.U.T.
VOUT
RT
CL
RL
WF06471S

Test Circuit for 3-State Outputs and Totem-Pole Output (Q_s)


90%
tw
90%
AMP (V)
NEGATIVE PULSE
VM
VM
10%
10%
0V
tTHL(tf)
tTLH(tr)
tTLH(tr)
tTHL(tf)
AMP (V)
90%
90%
POSITIVE PULSE
VM
VM
10%
tw
10%
0V
WF06450S

$V_M = 1.5V$

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PZH}	open
t_{PZL}	closed
t_{PHZ}	open
t_{PLZ}	closed

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST Products

FAST 74F398, F399

Registers

'F398 – Quad 2-Port Register With True & Complementary Outputs
'F399 – Quad 2-Port Register
Product Specification

FEATURES

- **Select inputs from two data sources**
- **Fully positive edge-triggered**
- **Both True and Complementary outputs – 'F398**

DESCRIPTION

The 'F398 and 'F399 are the logical equivalent of a quad 2-input multiplexer feeding into four edge-triggered flip-flops. A common Select input determines which of the two 4-bit words is accepted. The selected data enters the flip-flops on the rising edge of the clock. The 'F399 is the 16-pin version of the 'F398, with only the Q outputs of the flip-flops available.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F398	120MHz	25mA
74F399	120MHz	22mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
Plastic DIP	N74F398N, N74F399N
20-Pin Plastic SOL	N74F398D
16-Pin Plastic SO	N74F399D

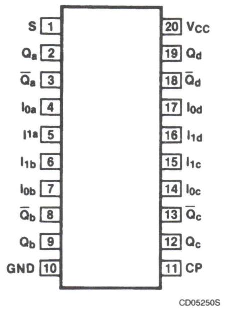
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$I_{0a} - I_{0d}$	Data inputs from source 0	1.0/1.0	20μA/0.6mA
$I_{1a} - I_{1d}$	Data inputs from source 1	1.0/1.0	20μA/0.6mA
S	Common select input	1.0/1.0	20μA/0.6mA
CP	Clock Pulse input (active rising edge)	1.0/1.0	20μA/0.6mA
$Q_a - Q_d$	Register true outputs	50/33	1.0mA/20mA
$\overline{Q}_a - \overline{Q}_d$	Register complementary outputs ('F398)	50/33	1.0mA/20mA

NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

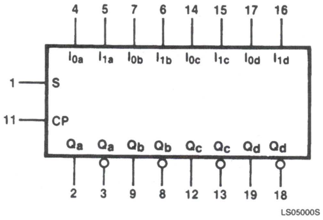
PIN CONFIGURATION

'F398


S 1
Qa 2
Q̄a 3
I0a 4
I1a 5
I1b 6
I0b 7
Q̄b 8
Qb 9
GND 10
20 Vcc
19 Qd
18 Q̄d
17 I0d
16 I1d
15 I1c
14 I0c
13 Q̄c
12 Qc
11 CP
CD05250S

LOGIC SYMBOL

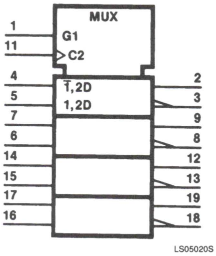
'F398


4 5 7 6 14 15 17 16
I0a I1a I0b I1b I0c I1c I0d I1d
1 S
11 CP
Qa Q̄a Qb Q̄b Qc Q̄c Qd Q̄d
2 3 9 8 12 13 19 18
LS05000S

V_{CC} = Pin 20
GND = Pin 10

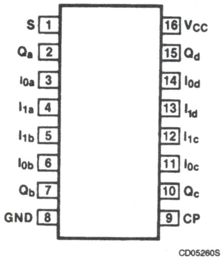
LOGIC SYMBOL (IEEE/IEC)

'F398


MUX
1 G1
11 C2
4 5 7 6 14 15 17 16
1̄,2D
1,2D
2 3 9 8 12 13 19 18
LS05020S

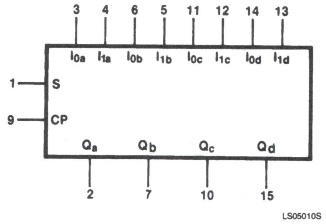
PIN CONFIGURATION

'F399


S 1
Qa 2
I0a 3
I1a 4
I1b 5
I0b 6
Qb 7
GND 8
16 VCC
15 Qd
14 I0d
13 I1d
12 I1c
11 I0c
10 Qc
9 CP
CD05260S

LOGIC SYMBOL

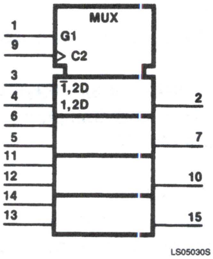
'F399


3
4
6
5
11
12
14
13
I0a
I1a
I0b
I1b
I0c
I1c
I0d
I1d
1
S
9
CP
Qa
Qb
Qc
Qd
2
7
10
15
LS05010S

V_{CC} = Pin 20
GND = Pin 10

LOGIC SYMBOL (IEEE/IEC)

'F399


MUX
1
G1
9
C2
3
4
$\overline{1}$,2D
1,2D
6
5
11
12
14
13
2
7
10
15
LS05030S

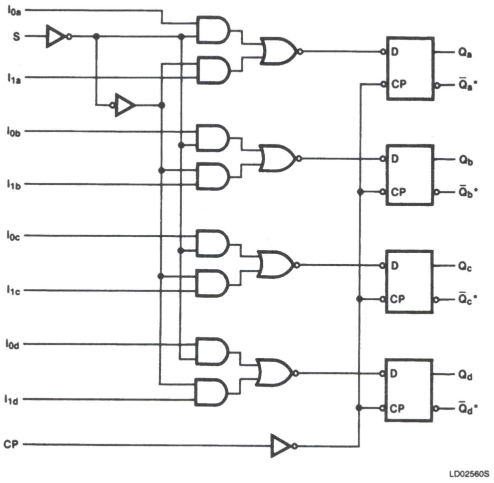
The 'F398 and 'F399 are high-speed quad 2-port registers. They select 4 bits of data from either of two sources (Ports) under control of a common Select input (S). The selected data is transferred to a 4-bit output register synchronous with the Low-to-High transition of the Clock input (CP). The 4-bit D-type output register is fully edge-triggered. The Data inputs (I_{0x}, I_{1x}) and Select input (S) must be stable only a setup time prior to and hold time after the Low-to-High transition of the Clock input for predictable operation. The 'F398 has both Q and $\overline{Q}$ outputs.

FUNCTION TABLE

INPUTS			OUTPUTS	
S	I_0	I_1	Q	$\overline{Q}$*
l	l	X	L	H
l	h	X	H	L
h	X	l	L	H
h	X	h	H	L

*F398 only
l = Low voltage level one setup time prior to the Low-to-High clock transition
h = High voltage level one setup time prior to the Low-to-High clock transition
L = Low voltage level
H = High voltage level
X = Don't care

LOGIC DIAGRAM


I0a
S
I1a
I0b
I1b
I0c
I1c
I0d
I1d
CP
D
CP
Qa
$\overline{Q}_a$*
Qb
$\overline{Q}_b$*
Qc
$\overline{Q}_c$*
Qd
$\overline{Q}_d$*
LD02560S

*'F398 only

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		74F398, 74F399			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX, V_{IH} = MIN	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OL} = MAX, V_{IH} = MIN	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				−0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current[4] (total)	'F398	V_{CC} = MAX			25	38	mA
		'F399				22	34	

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. I_{CCH} V_{IN} = GND; I_{CCL} = Open

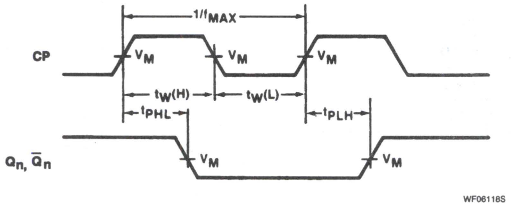
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F398, 74F399					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	100	120		90		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q or $\overline{Q}$	Waveform 1	3.0 3.0	5.7 6.5	7.5 8.5	3.0 3.0	8.5 9.0	ns

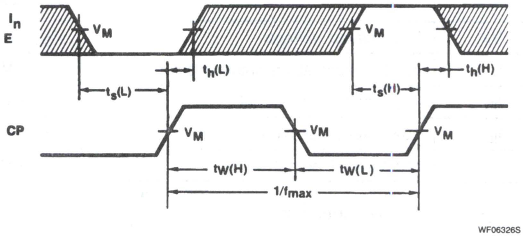
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	74F398, 'F399					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_l = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low I_n to CP	Waveform 2	3.0 3.0			3.0 3.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low I_n to CP	Waveform 2	1.0 1.0			1.0 1.0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low S to CP	Waveform 2	7.5 7.5			8.5 8.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low S to CP	Waveform 2	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	CP pulse width, High or Low	Waveform 1	4.0 6.0			4.0 6.0		ns

AC WAVEFORMS



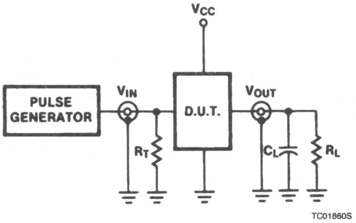
Waveform 1. Clock to Output Delays and Clock Pulse Width



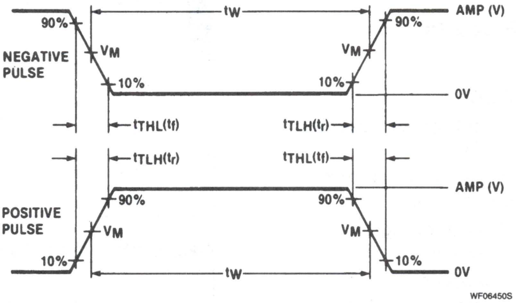
Waveform 2. Data Setup and Hold Times

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS


VCC
PULSE GENERATOR
VIN
D.U.T.
VOUT
RT
CL
RL
TC01860S

Test Circuit for Totem-Pole Outputs


NEGATIVE PULSE
90%
VM
10%
tW
AMP (V)
0V
tTHL(tf)
tTLH(tr)
POSITIVE PULSE
90%
VM
10%
tTLH(tr)
tTHL(tf)
tW
AMP (V)
0V
WF06450S

$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS

R_L = Load resistor to GND; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST Products

FAST 74F412, 74F432
Multi-Mode Buffered Latches

'F412 Multi-Mode Buffered Latch, Non-Inverting (3-State)
'F432 Multi-Mode Buffered Latch, Inverting (3-State)
Product Specification

FEATURES

- **Status flip-flop for interrupt commands**
- **Asynchronous or latched Receiver modes**
- **'F412 Non-inverting 'F432 Inverting**
- **3-State outputs**
- **300mil-wide Slim DIP package**
- **Functional equivalent to Intel 8212 except that 'F432 has inverting outputs**

DESCRIPTION

The 'F412/'F432 are 8-bit latch with 3-State output buffers. Also included is a status flip-flop for providing device-busy or request-interrupt commands.

Separate Mode (M) and Select ($\overline{S}_0$, S_1) inputs allow data to be stored with the outputs enabled or disabled. The devices can be also be operated in a fully transparent mode.

Both 'F412 and 'F432 are functional equivalent to the Intel 8212 except that 'F432 has the inverting outputs.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F412	8.0ns	45mA
74F432	9.0ns	50mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
24-Pin Plastic Slim DIP (300mil)	N74F412N, N74F432N
24-Pin Plastic SOL	N74F412D, N74F432D

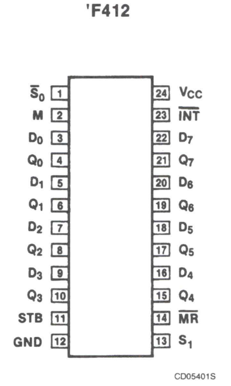
NOTE:
1. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

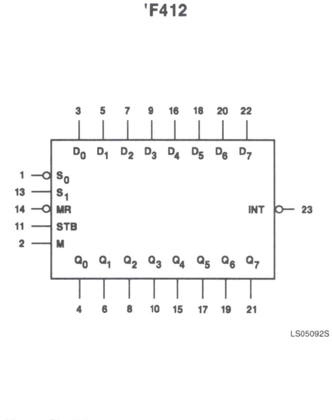
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$D_0 - D_7$	Data Inputs	1.0/1.0	20μA/0.6mA
$\overline{S}_0$, S_1	Select Inputs	1.0/1.0	20μA/0.6mA
STB	Strobe Input	1.0/1.0	20μA/0.6mA
M	Mode Control Input	1.0/1.0	20μA/0.6mA
$\overline{MR}$	Master Reset Input	1.0/1.0	20μA/0.6mA
$\overline{INT}$	Interrupt Output	50/40	1mA/24mA
$Q_0 - Q_7$	Data Latched Outputs	50/40	1mA/24mA

NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION

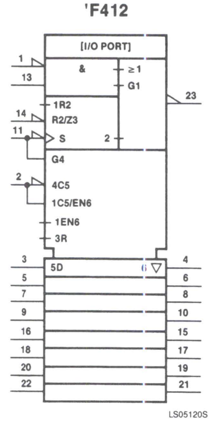

'F412
S̄0 1
M 2
D0 3
Q0 4
D1 5
Q1 6
D2 7
Q2 8
D3 9
Q3 10
STB 11
GND 12
24 VCC
23 INT
22 D7
21 Q7
20 D6
19 Q6
18 D5
17 Q5
16 D4
15 Q4
14 MR
13 S1
CD05401S

LOGIC SYMBOL


'F412
3 5 7 9 16 18 20 22
D0 D1 D2 D3 D4 D5 D6 D7
1 S0
13 S1
14 MR
11 STB
2 M
INT 23
Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
4 6 8 10 15 17 19 21
LS05092S

V_{CC} = Pin 24
GND = Pin 12

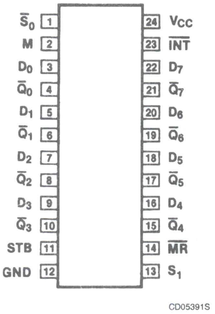
LOGIC SYMBOL (IEEE/IEC)


'F412
[I/O PORT]
&
≥1
G1
1
13
23
1R2
R2/Z3
14
11
S
2
G4
2
4C5
1C5/EN6
1EN6
3R
3 5D 6 ▽ 4
5 6
7 8
9 10
16 15
18 17
20 19
22 21
LS05120S

Multi-Mode Buffered Latches FAST 74F412, 74F432

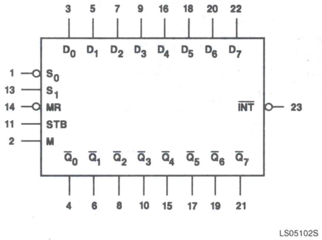
PIN CONFIGURATION

'F432


$\overline{S}_0$ 1
M 2
D_0 3
$\overline{Q}_0$ 4
D_1 5
$\overline{Q}_1$ 6
D_2 7
$\overline{Q}_2$ 8
D_3 9
$\overline{Q}_3$ 10
STB 11
GND 12
24 V_{CC}
23 $\overline{INT}$
22 D_7
21 $\overline{Q}_7$
20 D_6
19 $\overline{Q}_6$
18 D_5
17 $\overline{Q}_5$
16 D_4
15 $\overline{Q}_4$
14 $\overline{MR}$
13 S_1
CD05391S

LOGIC SYMBOL

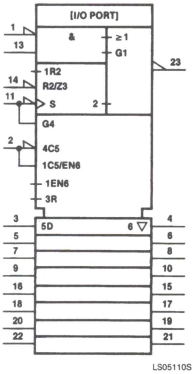
'F432


3 5 7 9 16 18 20 22
D_0 D_1 D_2 D_3 D_4 D_5 D_6 D_7
1 S_0
13 S_1
14 MR
11 STB
2 M
$\overline{INT}$ 23
$\overline{Q}_0$ $\overline{Q}_1$ $\overline{Q}_2$ $\overline{Q}_3$ $\overline{Q}_4$ $\overline{Q}_5$ $\overline{Q}_6$ $\overline{Q}_7$
4 6 8 10 15 17 19 21
LS05102S

V_{CC} = Pin 24
GND = Pin 12

LOGIC SYMBOL (IEEE/IEC)

'F432


[I/O PORT]
1
13
&
≥1
G1
23
14
1R2
R2/Z3
11
S
2
G4
2
4C5
1C5/EN6
1EN6
3R
3
5D
6 ▽
4
5
6
7
8
9
10
16
15
18
17
20
19
22
21
LS05110S

FUNCTIONAL DESCRIPTION

This high-performance eight-bit parallel expandable buffer register incorporates package and mode selection inputs and an edge-triggered status flip-flop designed specifically for implementing bus-organized input/output ports. The 3-State data outputs can be connected to a common data bus and controlled from the appropriate select inputs to receive or transmit data. An integral status flip-flop provides busy or request interrupt commands.

The eight data latches are fully transparent when the internal gate enable, G, input is High and the outputs are enabled. Latch transparency is selected by the mode control (M), select ($\overline{S}_0$ and S_1), and the strobe (STB) inputs and during transparency each data output (Q_n) follows its respective data input (D_n). This mode of operation can be terminated by clearing, de-selecting, or holding the data latches.

An input mode or an output mode is selectable from the M input. In the input mode, M = L, the eight data latch inputs are enabled when the strobe is High regardless of device selection. If selected during an input mode, the outputs will follow the data inputs. When the strobe input is taken Low, the latches will store the most-recently setup data.

In the output mode, M = H, the output buffers are enabled regardless of any other control input. During the output mode the content of the register is under control of the select ($\overline{S}_0$ and S_1) inputs.

FUNCTION TABLE

(for Data Latches)

INPUTS					DATA IN	DATA OUT		OPERATING MODE
$\overline{MR}$	M	$\overline{S}_0$	S_1	STB		'F412	'F432	
L	H	H	X	X	X	L	H	Clear
L	L	L	H	L	X	L	H	
X	L	X	L	X	X	Z	Z	De – select
X	L	H	X	X	X	Z	Z	
H	H	H	L	X	X	Q_0	$\overline{Q}_0$	Hold
H	L	L	H	L	X	Q_0	$\overline{Q}_0$	
H	H	L	H	X	L	L	H	Data Bus
H	H	L	H	X	H	H	L	
H	L	L	H	H	L	L	H	Data Bus
H	L	L	H	H	H	H	L	

FUNCTION TABLE

(for Status Flip-flop)

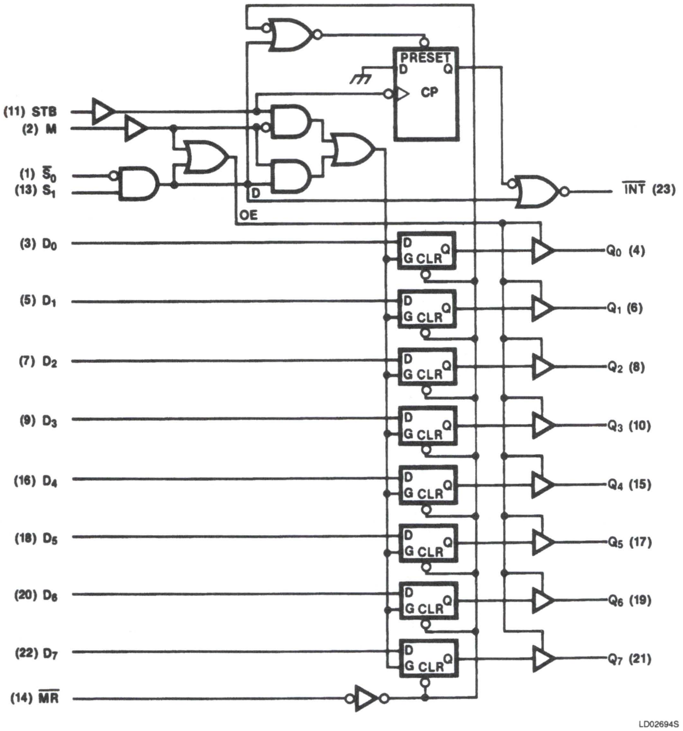
INPUTS				$\overline{INT}$
$\overline{MR}$	$\overline{S}_0$	S_1	STB	
L	H	X	X	H
L	X	L	X	H
H	X	X	↑	L
H	L	H	X	L

NOTES:
H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-to-High clock transition

Multi-Mode Buffered Latches

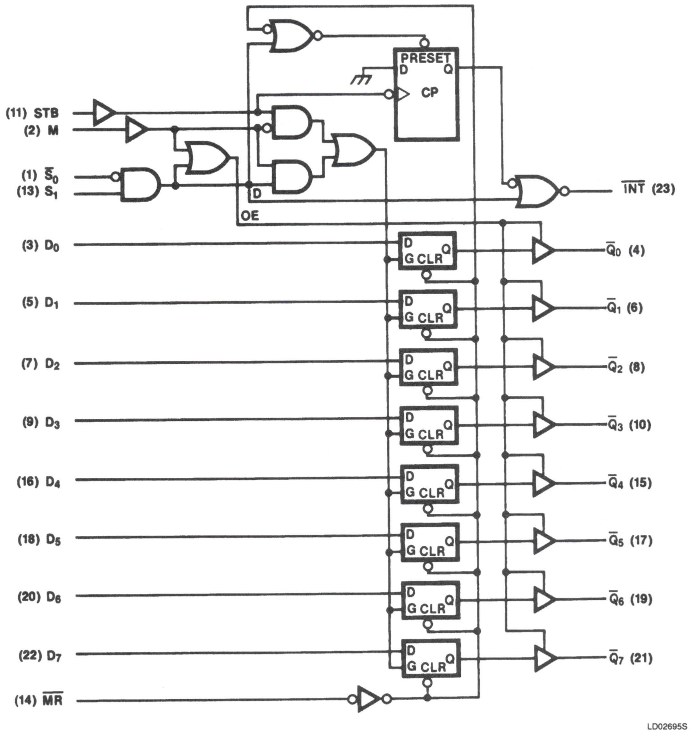
FAST 74F412, 74F432

LOGIC DIAGRAM for 'F412


PRESET
D
Q
CP
(11) STB
(2) M
(1) $\overline{S}_0$
(13) S_1
D
OE
$\overline{INT}$ (23)
(3) D_0
(5) D_1
(7) D_2
(9) D_3
(16) D_4
(18) D_5
(20) D_6
(22) D_7
(14) $\overline{MR}$
D
G CLR
Q
Q_0 (4)
Q_1 (6)
Q_2 (8)
Q_3 (10)
Q_4 (15)
Q_5 (17)
Q_6 (19)
Q_7 (21)
LD02694S

V_{CC} = Pin 24
GND = Pin 12
( ) = Pin numbers

LOGIC DIAGRAM for 'F432


(11) STB
(2) M
(1) $\bar{S}_0$
(13) S_1
PRESET
D
Q
CP
D
OE
$\overline{INT}$ (23)
(3) D_0
(5) D_1
(7) D_2
(9) D_3
(16) D_4
(18) D_5
(20) D_6
(22) D_7
(14) $\overline{MR}$
D
G CLR
Q
$\bar{Q}_0$ (4)
$\bar{Q}_1$ (6)
$\bar{Q}_2$ (8)
$\bar{Q}_3$ (10)
$\bar{Q}_4$ (15)
$\bar{Q}_5$ (17)
$\bar{Q}_6$ (19)
$\bar{Q}_7$ (21)
LD02695S

V_{CC} = Pin 24
GND = Pin 12
( ) = Pin numbers

DATA LATCHES FUNCTION TABLE

INPUTS					DATA IN	DATA OUT		OPERATING MODE
$\overline{MR}$	M	$\overline{S}_0$	S_1	STB		'F412	'F432	
L	H	H	X	X	X	L	H	Clear
L	L	L	H	L	X	L	H	
X	L	X	L	X	X	Z	Z	De-select
X	L	H	X	X	X	Z	Z	
H	H	H	X	X	X	Q_0	$\overline{Q}_0$	Hold
H	L	L	H	L	X	Q_0	$\overline{Q}_0$	
H	H	L	H	X	L	L	H	Data Bus
H	H	L	H	X	H	H	L	
H	L	L	H	H	L	L	H	Data Bus
H	L	L	H	H	H	H	L	

H = High voltage level
L = Low voltage level
X = Don't care
Z = High-impedance

STATUS FLIP-FLOP FUNCTION TABLE

INPUTS				OUTPUT
$\overline{MR}$	$\overline{S}_0$	S_1	STB	$\overline{INT}$
L	H	X	X	H
L	X	L	X	H
H	X	X	↓	L
H	H	H	X	L

H = High voltage level
L = Low voltage level
X = Don't care
↓= High-to-Low clock transition

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		−0.5 to +7.0	V
V_{IN}	Input voltage		−0.5 to +7.0	V
I_{IN}	Input current		−30 to +5.0	mA
V_{OUT}	Voltage applied to output in High output state		−0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	$\overline{INT}$	40	mA
		$Q_0 - Q_7$	48	mA
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	High-level output current	$\overline{INT}$			−1.0	mA
		$Q_0 - Q_7$			−3.0	mA
I_{OL}	Low-level output current	$\overline{INT}$			20	mA
		$Q_0 - Q_7$			24	mA
T_A	Operating free-air temperature		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]			74F412, 74F532			UNIT
							Min	Typ[2]	Max	
V_{OH}	High-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	$I_{OH} = -1mA$	±10%V_{CC}	2.5			V
						±5%V_{CC}	2.7	3.4		V
					$I_{OH} = -3mA$	±10%V_{CC}	2.4			V
						±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = MAX	±10%V_{CC}		0.35	0.50	V
						±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, $I_I = I_{IK}$				-0.73	-1.2	V
I_I	Input current at maximum input voltage			V_{CC} = MAX, $V_I = 7.0V$					100	μA
I_{IH}	High-level input current			V_{CC} = MAX, $V_I = 2.7V$					20	μA
I_{IL}	Low-level input current			V_{CC} = MAX, $V_I = 0.5V$					-0.6	mA
I_{OZH}	OFF-state output current, High-level voltage applied			V_{CC} = MAX, $V_O = 2.7V$					50	μA
I_{OZL}	OFF-state output current, Low-level voltage applied			V_{CC} = MAX, $V_O = 0.5V$					-50	μA
I_{OS}	Short-circuit output current[3]			V_{CC} = MAX, $V_O = 0.0V$			-60		-150	mA
I_{CC}	Supply current (total)	'F412	I_{CCH}	V_{CC} = MAX				35	50	mA
			I_{CCL}					45	60	mA
			I_{CCZ}					45	60	mA
		'F432	I_{CCH}	V_{CC} = MAX				40	55	mA
			I_{CCL}					50	70	mA
			I_{CCZ}					50	65	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Multi-Mode Buffered Latches

FAST 74F412, 74F432

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F412					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	Waveform 1	3.5 2.0	6.0 3.5	8.5 6.5	3.0 2.0	9.5 7.5	ns
t_{PLH} t_{PHL}	Propagation delay S_0, S_1 or STB to Q_n	Waveform 1, 2	7.5 7.0	13.0 9.0	17.0 14.0	7.0 6.5	18.5 15.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{S}_0$ or S_1 to $\overline{INT}$	Waveform 1, 2	3.0 3.0	6.0 6.5	9.5 10.5	3.0 3.0	10.5 11.5	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	Waveform 1	6.0	8.0	12.0	5.5	13.0	ns
t_{PHL}	Propagation delay STB to $\overline{INT}$	Waveform 2	6.5	10.0	13.0	5.5	15.0	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level $\overline{S}_0$ to Q_n	Waveform 5 Waveform 6	7.0 7.0	9.0 10.0	12.5 13.5	6.0 6.0	14.0 15.0	ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level $\overline{S}_0$ to Q_n	Waveform 5 Waveform 6	4.5 6.5	7.5 12.0	10.5 15.0	4.0 6.0	12.0 16.5	ns
t_{PZH} t_{PZL}	Output enable time to High or Low level S_1 to Q_n	Waveform 5 Waveform 6	6.0 6.0	10.0 9.0	13.0 12.0	5.0 5.5	14.0 13.0	ns
t_{PHZ} t_{PLZ}	Output disable time from High or Low level S_1 to Q_n	Waveform 5 Waveform 6	4.0 6.5	6.0 10.0	9.5 13.5	3.5 6.0	10.5 15.0	ns
t_{PZH} t_{PZL}	Output enable time to High or Low level M to Q_n	Waveform 5 Waveform 6	5.0 5.0	8.5 8.5	11.0 11.0	4.5 4.5	12.0 12.0	ns
t_{PHZ} t_{PLZ}	Output disable time from High or Low level M to Q_n	Waveform 5 Waveform 6	4.0 6.0	6.5 9.5	9.0 12.5	3.5 5.5	10.0 14.0	ns

AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	74F412					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to $\overline{S}_0$, S_1 or STB	Waveform 3	0 0			1.0 1.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to $\overline{S}_0$, S_1, STB, or M	Waveform 3	8.0 8.0			9.0 9.0		ns
$t_w(H)$ $t_w(L)$	$\overline{S}_0$, S_1, M, or STB pulse Pulse width, High or Low	Waveform 3	8.0 8.0			9.0 9.0		ns
$t_w(L)$	$\overline{MR}$ pulse width	Waveform 4	8.0			9.0		ns
t_{rec}	Recovery time $\overline{MR}$ to STB	Waveform 4	0			0		ns

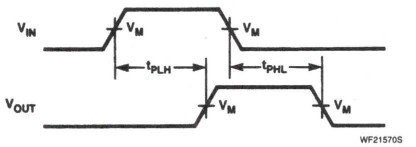
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F432					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	Waveform 2	4.5 2.5	7.5 4.5	10.5 7.0	4.0 2.5	12.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{S}_0$, S_1 or STB to Q_n	Waveform 1, 2	8.5 6.0	14.0 9.5	17.0 13.0	8.0 5.5	19.0 14.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{S}_0$ or S_1 to $\overline{INT}$	Waveform 1, 2	3.0 3.5	6.0 6.5	9.5 10.0	2.5 3.0	10.5 10.5	ns
t_{PLH}	Propagation delay $\overline{MR}$ to Q_n	Waveform 2	8.0	12.0	16.0	7.5	17.0	ns
t_{PHL}	Propagation delay STB to $\overline{INT}$	Waveform 2	7.0	10.0	13.5	6.5	14.5	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level $\overline{S}_0$ or S_1 to Q_n	Waveform 5 Waveform 6	6.0 6.0	9.0 11.0	12.5 14.0	5.5 5.5	14.0 15.0	ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level $\overline{S}_0$ or S_1 to Q_n	Waveform 5 Waveform 6	4.0 6.0	7.5 11.5	11.5 15.0	3.5 5.5	12.5 16.5	ns
t_{PZH} t_{PZL}	Output enable time to High or Low level M to Q_n	Waveform 5 Waveform 6	5.0 6.0	7.5 8.0	11.0 11.5	4.5 5.5	12.0 13.0	ns
t_{PHZ} t_{PLZ}	Output disable time from High or Low level M to Q_n	Waveform 5 Waveform 6	3.5 6.0	6.0 10.0	9.5 13.0	3.0 5.5	10.5 13.5	ns

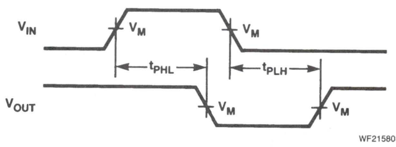
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	74F432					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to $\overline{S}_0$, S_1 or STB or M	Waveform 3	0 0			1.0 1.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to $\overline{S}_0$, S_1 or STB or M	Waveform 3	9.0 8.0			9.5 8.5		ns
$t_w(H)$ $t_w(L)$	$\overline{S}_0$, S_1, M or STB Pulse width, High or Low	Waveform 3	8.0 8.0			9.0 9.0		ns
$t_w(L)$	$\overline{MR}$ pulse width Low	Waveform 4	8.0			9.0		ns
t_{rec}	Recovery Time $\overline{MR}$ to STB	Waveform 4	0			0		ns

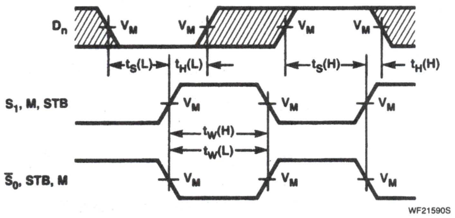
AC WAVEFORMS


V_IN
V_M
V_M
t_PLH
t_PHL
V_OUT
V_M
V_M
WF21570S

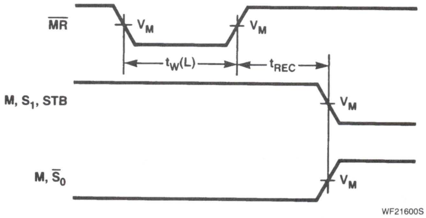
Waveform 1. Propagation Delay for Non-Inverting Outputs


V_IN
V_M
V_M
t_PHL
t_PLH
V_OUT
V_M
V_M
WF21580S

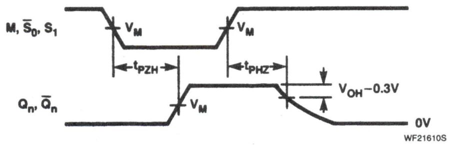
Waveform 2. Propagation Delay for Inverting Outputs


D_n
V_M
V_M
V_M
V_M
t_S(L)
t_H(L)
t_S(H)
t_H(H)
S_1, M, STB
V_M
V_M
V_M
t_W(H)
t_W(L)
S̄_0, STB, M
V_M
V_M
V_M
WF21590S

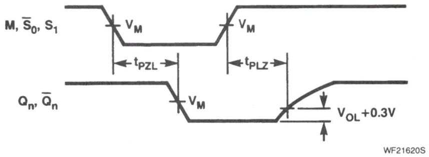
Waveform 3. Setup and Hold Times


M̄R̄
V_M
V_M
t_W(L)
t_REC
M, S_1, STB
V_M
M, S̄_0
V_M
WF21600S

Waveform 4. Recovery Times


M, S̄_0, S_1
V_M
V_M
t_PZH
t_PHZ
V_OH−0.3V
Q_n, Q̄_n
V_M
0V
WF21610S

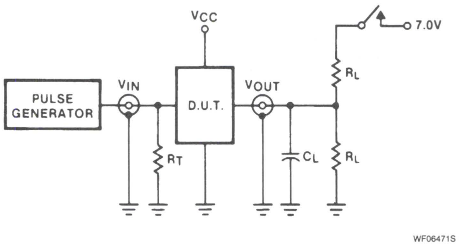
Waveform 5. 3-State Output Enable Time to High Level and Output Disable Time From High Level


M, S̄_0, S_1
V_M
V_M
t_PZL
t_PLZ
Q_n, Q̄_n
V_M
V_OL+0.3V
WF21620S

Waveform 6. 3-State Output Enable Time to Low Level and Output Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS


VCC
7.0V
RL
PULSE GENERATOR
VIN
D.U.T.
VOUT
RT
CL
RL
WF06471S

Test Circuit for 3-State Outputs

SWITCH POSITION

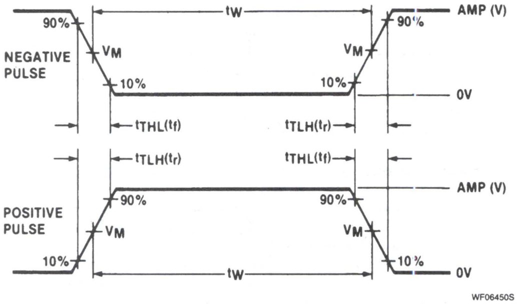
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.


tw
90%
90%
AMP (V)
NEGATIVE PULSE
VM
VM
10%
10%
0V
tTHL(tf)
tTLH(tr)
tTLH(tr)
tTHL(tf)
AMP (V)
90%
90%
POSITIVE PULSE
VM
VM
10%
10%
0V
tw
WF06450S

$V_M = 1.5V$

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST Products

FAST 74F455, 74F456

Buffers/Drivers

'F455 Octal Buffer/Line Driver with Parity, Inverting (3-State)
'F456 Octal Buffer/Line Driver with Parity, Non-Inverting (3-State)
Product Specification

FEATURES

- **High-impedance NPN base inputs for reduced loading (20μA in High and Low states)**
- **'F455 combines 'F240 and 'F280A functions in one package**
- **'F456 combines 'F244 and 'F280A functions in one package**
- **'F455A and 'F456A are center pin versions of the 'F655A and 'F656A respectively**
- **'F455 Inverting**
  'F456 Non-inverting
- **3-State outputs sink 64mA and source 15mA**
- **24-pin plastic Slim DIP (300mil) package**
- **Broadside pinout simplifies PC board layout**

DESCRIPTION

The 'F455 and 'F456 are octal buffers and line drivers with parity generation/checking designed to be employed as memory address drivers, clock drivers, and bus-oriented transmitters/receivers. These parts include parity generator/checker to improve PC board density.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F455	6.5ns	64mA
74F456	7.5ns	64mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
24-Pin Plastic Slim DIP	N74F455N, N74F456N
24-Pin Plastic SOL	N74F455D, N74F456D

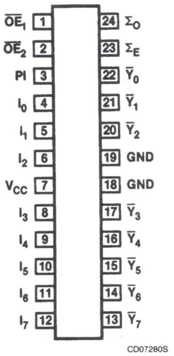
NOTE:
1. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I_n	Data input	2.0/0.066	40μA/40μA
PI	Parity input	1.0/0.033	20μA/20μA
$\overline{OE}_1$, $\overline{OE}_2$	3-State output enable inputs (active-Low)	1.0/0.033	20μA/20μA
$\overline{Y}_n$	Data output ('F455)	750/106.7	15mA/64mA
Y_n	Data output ('F456)	750/106.7	15mA/64mA
Σ_E, Σ_O	Parity outputs	750/106.7	15mA/64mA

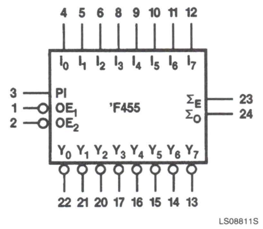
PIN CONFIGURATION

'F455


$\overline{OE}_1$ 1
$\overline{OE}_2$ 2
PI 3
I_0 4
I_1 5
I_2 6
V_{CC} 7
I_3 8
I_4 9
I_5 10
I_6 11
I_7 12
24 Σ_O
23 Σ_E
22 $\overline{Y}_0$
21 $\overline{Y}_1$
20 $\overline{Y}_2$
19 GND
18 GND
17 $\overline{Y}_3$
16 $\overline{Y}_4$
15 $\overline{Y}_5$
14 $\overline{Y}_6$
13 $\overline{Y}_7$
CD07280S

LOGIC SYMBOL

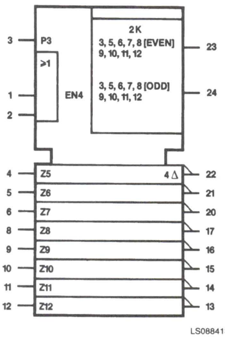
'F455


4 5 6 8 9 10 11 12
I_0 I_1 I_2 I_3 I_4 I_5 I_6 I_7
3 PI
1 OE_1
2 OE_2
'F455
Σ_E 23
Σ_O 24
Y_0 Y_1 Y_2 Y_3 Y_4 Y_5 Y_6 Y_7
22 21 20 17 16 15 14 13
LS08811S

V_{CC} = Pin 16
GND = Pin 18 and 19

LOGIC SYMBOL (IEEE/IEC)

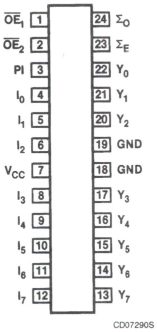
'F455


3 P3
≥1
1
2
EN4
2K
3, 5, 6, 7, 8 [EVEN] 9, 10, 11, 12 23
3, 5, 6, 7, 8 [ODD] 9, 10, 11, 12 24
4 Z5 4 Δ 22
5 Z6 21
6 Z7 20
8 Z8 17
9 Z9 16
10 Z10 15
11 Z11 14
12 Z12 13
LS08841S

Buffers/Drivers FAST 74F455, 74F456

PIN CONFIGURATION

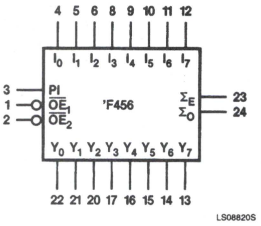
'F456



$\overline{OE}_1$ 1
$\overline{OE}_2$ 2
PI 3
I_0 4
I_1 5
I_2 6
V_{CC} 7
I_3 8
I_4 9
I_5 10
I_6 11
I_7 12
24 Σ_O
23 Σ_E
22 Y_0
21 Y_1
20 Y_2
19 GND
18 GND
17 Y_3
16 Y_4
15 Y_5
14 Y_6
13 Y_7
CD07290S

LOGIC SYMBOL

'F456

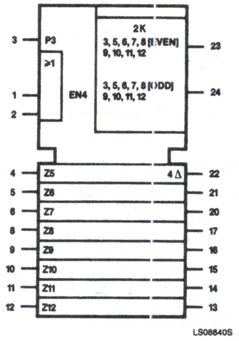


4 5 6 8 9 10 11 12
I_0 I_1 I_2 I_3 I_4 I_5 I_6 I_7
3 PI
1 $\overline{OE}_1$
2 $\overline{OE}_2$
'F456
Σ_E 23
Σ_O 24
Y_0 Y_1 Y_2 Y_3 Y_4 Y_5 Y_6 Y_7
22 21 20 17 16 15 14 13
LS08820S

V_{CC} = Pin 16
GND = Pin 18 and 19

LOGIC SYMBOL (IEEE/IEC)

'F456



3 P3
≥1
1
2
EN4
2K
3, 5, 6, 7, 8 (EVEN) 9, 10, 11, 12
23
3, 5, 6, 7, 8 (ODD) 9, 10, 11, 12
24
4 Z5
5 Z6
6 Z7
8 Z8
9 Z9
10 Z10
11 Z11
12 Z12
4Δ
22
21
20
17
16
15
14
13
LS08840S

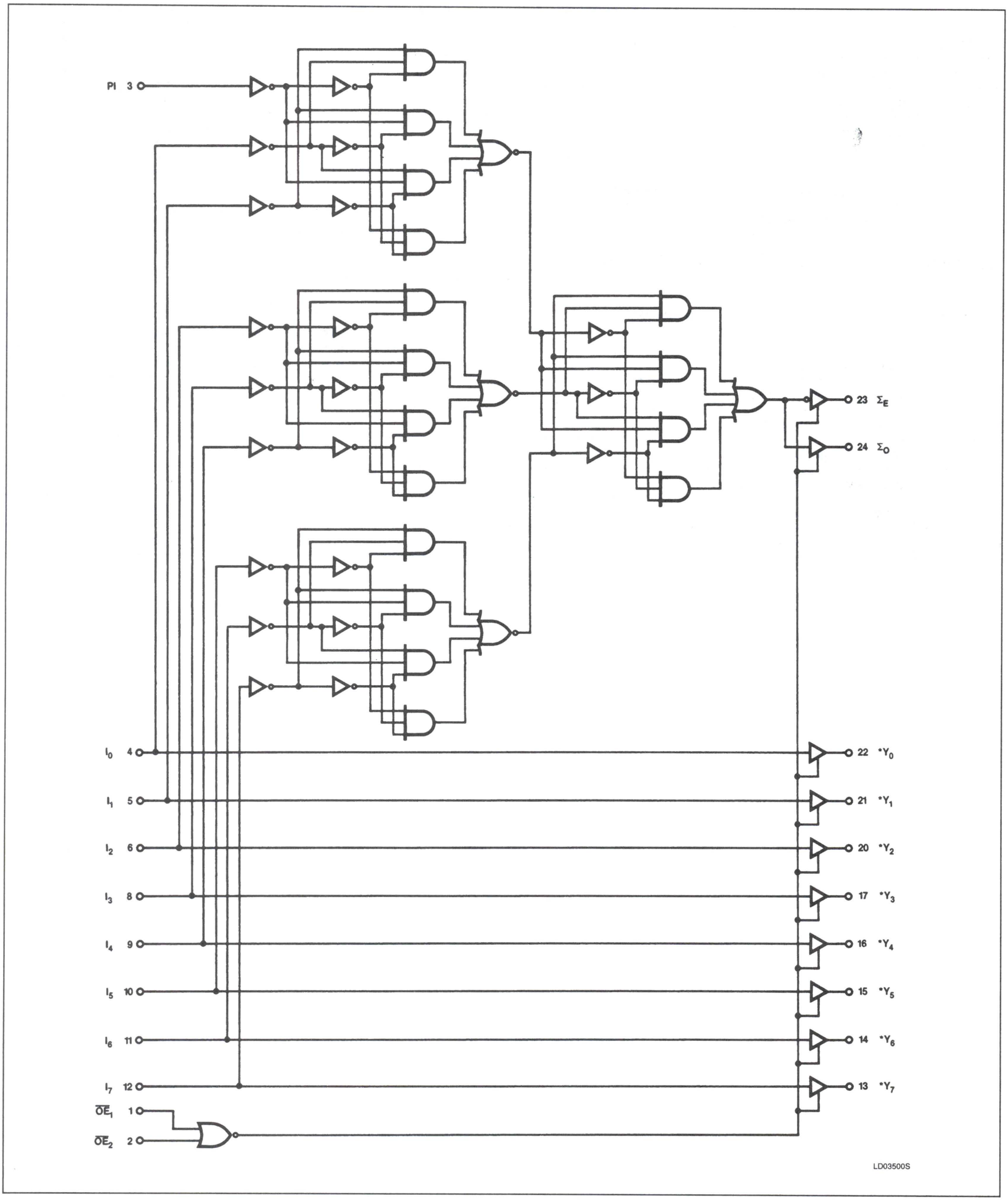
FUNCTION TABLE

INPUTS			DATA OUTPUTS	
$\overline{OE}_1$	$\overline{OE}_2$	I_n	'F455	'F456
L	L	L	H	L
L	L	H	L	H
H	X	X	Z	Z
X	H	X	Z	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High-impedance level

INPUTS	PARITY OUTPUTS	
Number of inputs High (PI, $I_0 - I_7$)	Σ_E	Σ_O
Even – 0, 2, 4, 6, 8	H	L
Odd – 1, 3, 5, 7, 9	L	H
Any $\overline{OE}$ = High	Z	Z

LOGIC DIAGRAM FOR 'F456 (*outputs are inverted for 'F455)


PI 3
I_0 4
I_1 5
I_2 6
I_3 8
I_4 9
I_5 10
I_6 11
I_7 12
$\overline{OE}_1$ 1
$\overline{OE}_2$ 2
23 Σ_E
24 Σ_O
22 *Y_0
21 *Y_1
20 *Y_2
17 *Y_3
16 *Y_4
15 *Y_5
14 *Y_6
13 *Y_7
LD03500S

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	128	mA
T_A	Operating free-air temperature range	0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−15	mA
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature	0		70	°C

Buffers/Drivers

FAST 74F455, 74F456

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS^1			74F455, 74F456			UNIT
						Min	Typ^2	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = −3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.4		V
				I_{OH} = −15mA	±10%V_{CC}	2.0			V
					±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 48mA	±10%V_{CC}		0.35	0.50	V
				I_{OL} = 64mA	±5%V_{CC}		0.40	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$				−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = 0.0V, V_I = 7.0V					100	μA
I_{IH}	High-level input current	In	V_{CC} = MAX, V_I = 2.7V					40	μA
		PI, OE, OE_2						20	μA
I_{IL}	Low-level input current	In	V_{CC} = MAX, V_I = 0.5V					−40	μA
		PI, OE, OE_2						−20	μA
I_{OZH}	Off-state current High-level voltage applied		V_{CC} = MAX, V_O = 2.7V					50	μA
I_{OZL}	Off-state current Low-level voltage applied		V_{CC} = MAX, V_O = 0.5V					−50	μA
I_{OS}	Short-circuit output current^3		V_{CC} = MAX			−100		−225	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				50	80	mA
		I_{CCL}					78	110	mA
		I_{CCZ}					63	90	mA

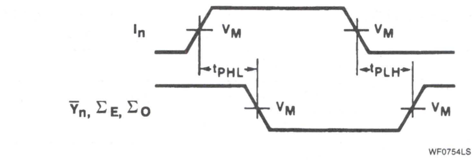
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

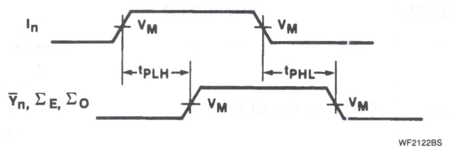
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	74F455, 74F456					UNIT
				$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_n to $\overline{Y}_n$	'F455	Waveform 1	2.0 1.0	4.5 2.0	6.5 4.0	2.0 1.0	7.5 4.5	ns
t_{PLH} t_{PHL}	Propagation delay I_n to Y_n	'F456	Waveform 2	2.0 2.5	4.5 5.0	6.5 7.0	2.0 2.5	7.0 7.5	ns
t_{PLH} t_{PHL}	Propagation delay I_n to Σ_E, Σ_O		Waveform 1, 2	5.5 5.5	10.0 11.0	13.0 14.5	5.5 5.5	14.0 16.5	ns
t_{PZH} t_{PZL}	Enable Time to High level Enable Time to Low level		Waveform 3 Waveform 4	4.0 4.0	7.0 8.0	9.5 10.5	4.0 4.0	10.5 11.5	ns
t_{PHZ} t_{PLZ}	Disable Time from High level Disable Time from Low level		Waveform 3 Waveform 4	1.5 2.0	4.0 5.0	6.5 7.5	1.5 2.0	7.5 8.0	ns

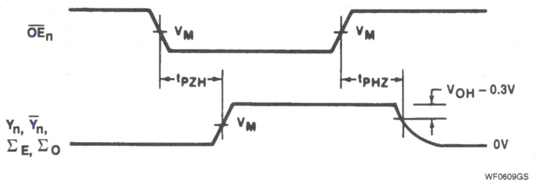
AC WAVEFORMS


I_n
V_M
V_M
t_{PHL}
t_{PLH}
$\overline{Y}_n, \Sigma_E, \Sigma_O$
V_M
V_M
WF0754LS

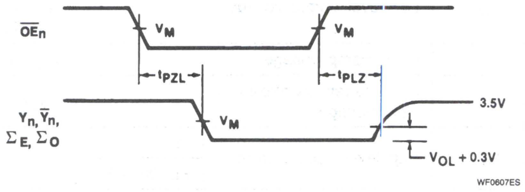
Waveform 1. Propagation Delay for I_n to Σ_E, Σ_O, $\overline{Y}_n$


I_n
V_M
V_M
t_{PLH}
t_{PHL}
$\overline{Y}_n, \Sigma_E, \Sigma_O$
V_M
V_M
WF2122BS

Waveform 2. Propagation Delay for I_n to Σ_E, Σ_O, $\overline{Y}_n$


$\overline{OE}_n$
V_M
V_M
t_{PZH}
t_{PHZ}
$V_{OH} - 0.3V$
$Y_n, \overline{Y}_n, \Sigma_E, \Sigma_O$
V_M
0V
WF0609GS

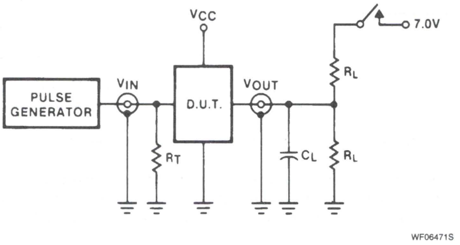
Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time From High Level


$\overline{OE}_n$
V_M
V_M
t_{PZL}
t_{PLZ}
3.5V
$Y_n, \overline{Y}_n, \Sigma_E, \Sigma_O$
V_M
$V_{OL} + 0.3V$
WF0607ES

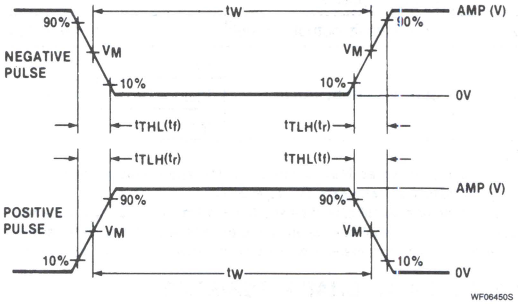
Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORMS


VCC
7.0V
R_L
PULSE GENERATOR
VIN
D.U.T.
VOUT
R_T
C_L
R_L
WF06471S

Test Circuit for 3-State Outputs


tw
90%
90%
AMP (V)
NEGATIVE PULSE
VM
VM
10%
10%
0V
tTHL(tf)
tTLH(tr)
tTLH(tr)
tTHL(tf)
AMP (V)
90%
90%
POSITIVE PULSE
VM
VM
10%
10%
0V
tw
WF06450S

$V_M = 1.5V$

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS
R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F521
Comparator

8 Bit Identity Comparator
Product Specification

FAST Products

FEATURES

- **Compares two 8-bit words in 6.5ns typical**
- **Expandable to any word length**
- **High-Speed version of ALS688**

DESCRIPTION

The 'F521 is an expandable 8-bit comparator. It compares two words of up to 8 bits each and provides a Low output when the two words match bit for bit. The expansion input $\bar{I}_{A=B}$ also serves as an active-Low enable input.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F521	7.0ns	20.0mA

ORDERING INFORMATION

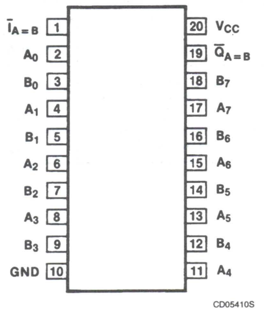
PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
20-Pin Plastic DIP	N74F521N
20-Pin Plastic SOL	N74F521D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0-A_7	Word A inputs	1.0/1.0	20µA/0.6mA
B_0-B_7	Word B inputs	1.0/1.0	20µA/0.6mA
$\bar{I}_{A=B}$	Expansion or enable input (active-Low)	1.0/1.0	20µA/0.6mA
$\bar{Q}_{A=B}$	Identity output (active-Low)	50/33	1.0mA/20mA

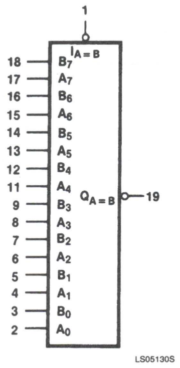
NOTE:
1. One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



ĪA=B 1
A0 2
B0 3
A1 4
B1 5
A2 6
B2 7
A3 8
B3 9
GND 10
20 VCC
19 Q̄A=B
18 B7
17 A7
16 B6
15 A6
14 B5
13 A5
12 B4
11 A4
CD05410S

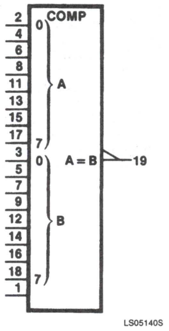
LOGIC SYMBOL



1
ĪA=B
18 B7
17 A7
16 B6
15 A6
14 B5
13 A5
12 B4
11 A4
9 B3
8 A3
7 B2
6 A2
5 B1
4 A1
3 B0
2 A0
QA=B 19
LS05130S

V_{CC} = Pin 20
GND = Pin 10

LOGIC SYMBOL (IEEE/IEC)

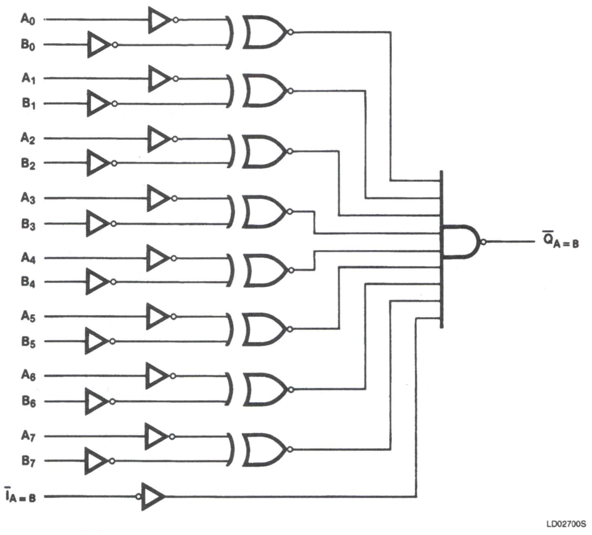


COMP
2
4
6
8
11
13
15
17
0
A
7
3
5
7
9
12
14
16
18
0
B
7
A=B
19
1
LS05140S

Comparator

FAST 74F521

LOGIC DIAGRAM



TRUTH TABLE

INPUTS		OUTPUT
$\overline{I}_{A=B}$	A, B	$\overline{Q}_{A=B}$
L	A = B*	L
L	A ≠ B	H
H	A = B*	H
H	A ≠ B	H

H = High voltage level
L = Low voltage level
*$A_0 = B_0$, $A_1 = B_1$, $A_2 = B_2$, etc.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C

Comparator FAST 74F521

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX V_{IH} = MIN,	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OL} = MAX V_{IH} = MIN,	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current[4] (total)	I_{CCH}	V_{CC} = MAX			24	36	mA
		I_{CCL}				15.5	23	mA

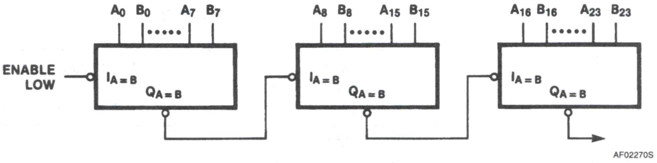
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. For I_{CCH} all inputs are grounded except B_0 can be any one input, which is at 4.5V. For I_{CCL} all inputs are grounded.

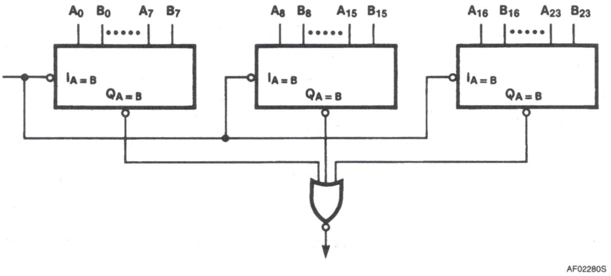
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F521					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n or B_n to $\overline{Q}_{A=B}$	Waveform 1, 2	3.5 3.0	8.0 8.0	9.5 9.0	3.5 2.5	11 10.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{I}_{A=B}$ to $\overline{Q}_{A=B}$	Waveform 2	3.0 3.5	5.0 6.5	6.5 7.0	3.0 3.5	7.5 8.0	ns

APPLICATION DIAGRAMS

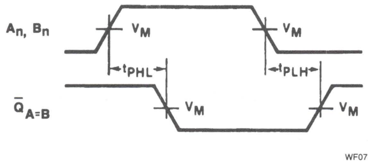

A0 B0 A7 B7
A8 B8 A15 B15
A16 B16 A23 B23
ENABLE LOW
IA=B
QA=B
AF02270S

Ripple Expansion

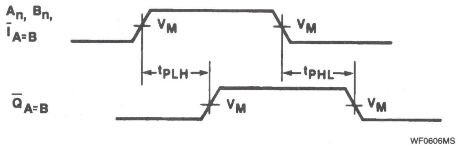

A0 B0 A7 B7
A8 B8 A15 B15
A16 B16 A23 B23
IA=B
QA=B
AF02280S

Parallel Expansion

AC WAVEFORMS


An, Bn
VM
VM
tPHL
tPLH
QA=B
VM
VM
WF07541S

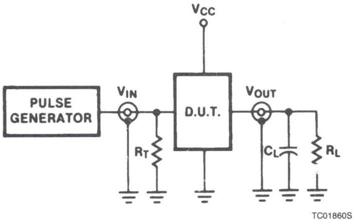
Waveform 1. For Inverting Outputs


An, Bn,
IA=B
VM
VM
tPLH
tPHL
QA=B
VM
VM
WF0606MS

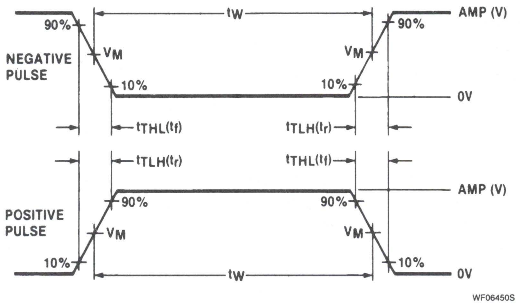
Waveform 2. For Non-Inverting Outputs

NOTE: For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORMS


VCC
PULSE GENERATOR
VIN
D.U.T.
VOUT
RT
CL
RL
TC01860S

Test Circuit for Totem-Pole Outputs


90%
tW
90%
AMP (V)
NEGATIVE PULSE
VM
VM
10%
10%
0V
tTHL(tf)
tTLH(tr)
tTLH(tr)
tTHL(tf)
AMP (V)
90%
90%
POSITIVE PULSE
VM
VM
10%
10%
0V
tW
WF06450S

$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F524
Comparator

8-Bit Register Comparator (Open-Collector + 3-State)
Product Specification

FAST Products

FEATURES

- **8-bit bidirectional register with bus-oriented input-output**
- **Independent serial input-output to register**
- **Register bus comparator with 'equal to', 'greater than' and 'less than' outputs**
- **Cascadable in groups of 8 bits**
- **Open-Collector comparator outputs for AND-wired expansion**
- **Two's Complement or magnitude compare**

DESCRIPTION

The 'F524 is an 8-bit bidirectional register with parallel input and output plus serial input and output progressing from LSB to MSB. All data inputs, serial and parallel, are loaded by the rising edge of the input clock. The device functions are controlled by two control lines (S_0, S_1) to execute shift, load, hold and read out.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F524	65MHz	110mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V± 5%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F524N
20-Pin Plastic SOL	N74F524D

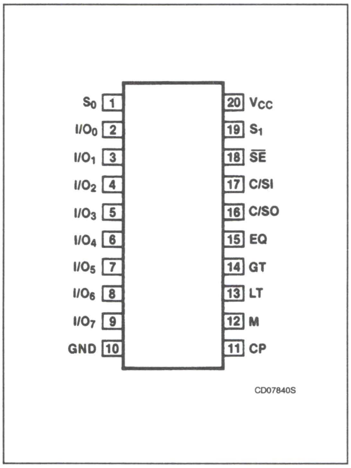
NOTE:
1. Thermal mounting techniques are recommended. See App Note AN SMD-100 for a discussion of thermal considerations for surface mounted devices.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I/O_n	Parallel data inputs	1.0/1.0	20μA/0.6mA
S_0, S_1	Mode select inputs	1.0/1.0	20μA/0.6mA
C/SI	Status priority or Serial data Input	1.0/1.0	20μA/0.6mA
CP	Clock Pulse input (active rising edge)	1.0/1.0	20μA/0.6mA
$\overline{SE}$	Status enable input (active-Low)	1.0/1.0	20μA/0.6mA
M	Compare mode select input	1.0/1.0	20μA/0.6mA
I/O_n	3-State parallel data outputs	150/40	3.0mA/24mA
C/SO	Status priority or Serial data Output	50/33	1.0mA/20mA
LT	Register less than bus output	OC*/33	OC*/20mA
EQ	Register equal to bus output	OC*/33	OC*/20mA
GT	Register greater than bus output	OC*/33	OC*/20mA

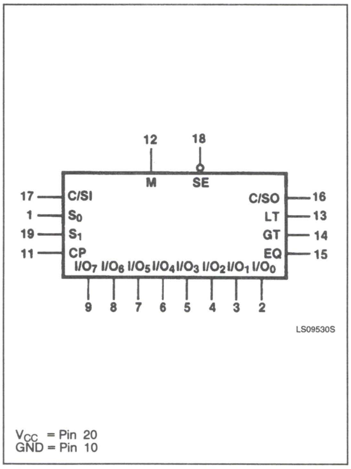
NOTES:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.
*OC = Open Collector

PIN CONFIGURATION



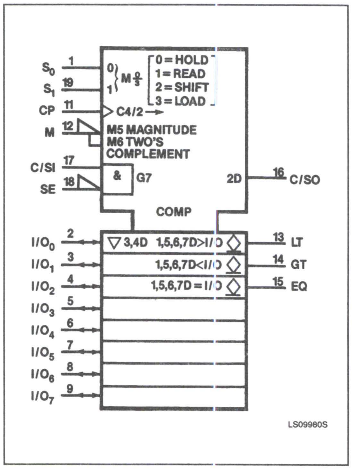
S0 1
I/O0 2
I/O1 3
I/O2 4
I/O3 5
I/O4 6
I/O5 7
I/O6 8
I/O7 9
GND 10
20 VCC
19 S1
18 SE
17 C/SI
16 C/SO
15 EQ
14 GT
13 LT
12 M
11 CP
CD07840S

LOGIC SYMBOL



12
18
M
SE
17
1
19
11
C/SI
S0
S1
CP
C/SO
LT
GT
EQ
16
13
14
15
I/O7 I/O6 I/O5 I/O4 I/O3 I/O2 I/O1 I/O0
9 8 7 6 5 4 3 2
LS09530S
VCC = Pin 20
GND = Pin 10

LOGIC SYMBOL (IEEE/IEC)



S0 1
S1 19
CP 11
M 12
C/SI 17
SE 18
0 = HOLD
1 = READ
2 = SHIFT
3 = LOAD
M 0/3
C4/2→
M5 MAGNITUDE
M6 TWO'S COMPLEMENT
& G7
2D
16 C/SO
COMP
I/O0 2
I/O1 3
I/O2 4
I/O3 5
I/O4 6
I/O5 7
I/O6 8
I/O7 9
▽3,4D 1,5,6,7D>I/O
1,5,6,7D<I/O
1,5,6,7D=I/O
13 LT
14 GT
15 EQ
LS09980S

Comparator | FAST 74F524

An 8-bit comparator examines the data stored in the registers and on the data bus. Three true-High, Open-Collector outputs representing 'register equal to bus', 'register greater than bus' and 'register less than bus' are provided. These outputs can be disabled to the OFF state by the use of Status Enable ($\overline{SE}$). A mode control has also been provided to allow Two's Complement as well as magnitude compare. Linking inputs are provided for expansion to longer words.

FUNCTIONAL DESCRIPTION

The 'F524 contains eight D-type flip-flops connected as a shift register with provision for either parallel or serial loading. Parallel data may be read from or loaded into the registers via the data bus $I/O_0 - I/O_7$. Serial data is entered from the C/SI input and may be shifted into the register and out through the C/SO output. Both parallel and serial data entry occurs on the rising edge of the input clock (CP). The operation of the shift register is controlled by two signals, S_0 and S_1, according to the Select Truth Table. The 3-State parallel output buffers are enabled only in the Read mode.

SELECT TRUTH TABLE

S_0	S_1	OPERATION
L	L	HOLD — Retains data in shift register
L	H	READ — Read contents in register onto data bus
H	L	SHIFT — Allows serial shifting on next rising clock edge
H	H	LOAD — Load data on bus into register.

H = High Voltage Level
L = Low Voltage Level

One port of an 8-bit comparator is attached to the data bus while the other port is tied to the outputs of the internal register. Three active-OFF, Open-Collector outputs indicate whether the contents held in the shift register are 'greater than' (GT), 'less than' (LT), or 'equal to (EQ) the data on the input bus. A High signal on the Status Enable ($\overline{SE}$) input disables these outputs to the OFF state. A Mode control input (M) allows selection between a straightforward magnitude compare or a comparison between Two's Complement numbers.

NUMBER REPRESENTATION SELECT TABLE

M	OPERATION
L	Magnitude compare
H	Two's Complement compare

H = High Voltage Level
L = Low Voltage Level

For 'greater than' or 'less than' detection, the C/SI input must be held High, as indicated in the Status Truth Table. The internal logic is arranged such that a Low signal on the C/SI input disables the 'greater than' and 'less than' outputs. The C/SO output will be forced High if the 'equal to' status condition exists, otherwise C/SO will be held Low. These facilities enable the 'F524 to be cascaded for word lengths greater than 8 bits.

STATUS TRUTH TABLE (Hold Mode)

INPUTS			OUTPUTS			
$\overline{SE}$	C/SI	Data Comparison	EQ	GT	LT	C/SO
H	H	X	H	H	H	①
H	L	X	H	H	H	L
L	L	$O_A - O_H > I/O_0 - I/O_7$	L	H	H	L
L	L	$O_A - O_H = I/O_0 - I/O_7$	H	H	H	L
L	L	$O_A - O_H < I/O_0 - I/O_7$	L	H	H	L
L	H	$O_A - O_H > I/O_0 - I/O_7$	L	H	L	L
L	H	$O_A - O_H = I/O_0 - I/O_7$	H	L	L	H
L	H	$O_A - O_H < I/O_0 - I/O_7$	L	L	H	L

① = High if data are not equal, otherwise Low
H = High Voltage Level
L = Low Voltage Level
X = Don't Care

Word length expansion (in groups of 8 bits) can be achieved by connecting the C/SO output of the more significant byte to the C/SI input of the next less significant byte and also to its own $\overline{SE}$ input (see Figure 1). The C/SI input of the most significant device is held High while the $\overline{SE}$ input of the least significant device is held Low. The corresponding status outputs are AND-wired together. In the case of two's complement number compare, only the Mode input to the most significant device should be High. The Mode inputs to all other cascaded devices are held Low.

Suppose that an inequality condition is detected in the most significant device. Assuming that the byte stored in the register is greater than the byte on the data bus, then the EQ and LT outputs will be pulled Low, whereas the GT output will float High. Also, the C/SO output of the most significant device will be forced Low, disabling the subsequent devices but enabling its own status outputs. The correct status condition is thus indicated. The same applies if the registered byte is less than the data byte, only in this case the EQ and GT outputs go Low, whereas LT output floats High.

If an equality condition is detected in the most significant device, its C/SO output is forced High. This enables the next less significant device and also disables its own status outputs. In this way, the status output priority is handed down to the next less significant device which now effectively becomes the most significant byte. The worst case propagation delay for a compare operation involving 'n' cascaded 'F524s will be when an equality condition is detected in all but the least significant byte. In this case, the status priority has to ripple all the way down the chain before the correct status output is established. Typically, this will take 35 + 6 (n-s) ns.

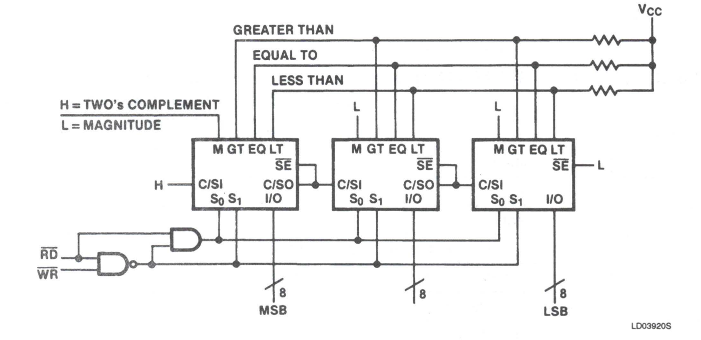
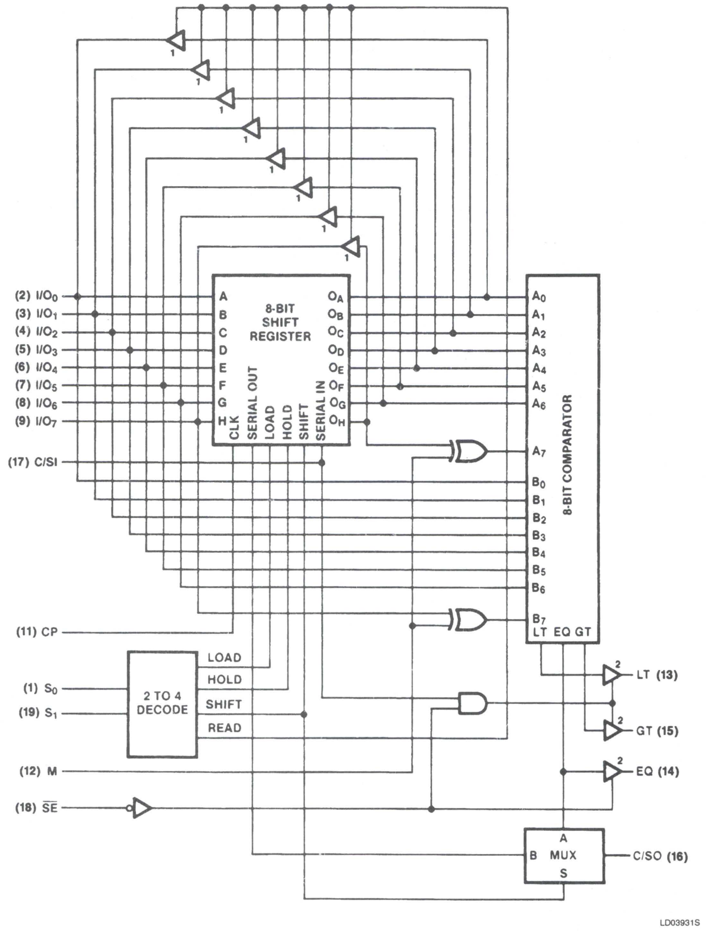


Figure 1. Cascading 'F524s for Comparing Longer Words

Comparator FAST 74F524

LOGIC DIAGRAM



(2) I/O0
(3) I/O1
(4) I/O2
(5) I/O3
(6) I/O4
(7) I/O5
(8) I/O6
(9) I/O7
(17) C/SI
(11) CP
(1) S0
(19) S1
(12) M
(18) SE
8-BIT SHIFT REGISTER
A B C D E F G H
OA OB OC OD OE OF OG OH
CLK SERIAL OUT LOAD HOLD SHIFT SERIAL IN
2 TO 4 DECODE
LOAD HOLD SHIFT READ
8-BIT COMPARATOR
A0 A1 A2 A3 A4 A5 A6 A7
B0 B1 B2 B3 B4 B5 B6 B7
LT EQ GT
LT (13)
GT (15)
EQ (14)
A B MUX S
C/SO (16)
1
2
LD03931S

V_{CC} = Pin 20
GND = Pin 10
( ) = Pin number

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		74F524			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
V_{OH}	High-level output current	LT, EQ, GT			4.5	V
I_{OH}	High-level output current	Not LT, EQ, GT, C/SO			−3	mA
		C/SO only			−1	mA
I_{OL}	Low-level output current	All except I/O			20	mA
		I/O only			24	mA
T_A	Operating free-air temperature		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		74F524			UNIT
					Min	Typ[2]	Max	
I_{OH}	High-level output current	LT, EQ, GT only	V_{CC} = MIN, V_{IL} = MAX, V_{OH} = MAX, V_{IH} = MIN				250	μA
V_{OH}	High-level output voltage	C/SO only	V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX V_{IH} = MIN,	±10%V_{CC}	2.5			V
		I/O_n only		±10%V_{CC}	2.4			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OL} = MAX V_{IH} = MIN,	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$			−0.73	−1.2	V
I_I	Input current at maximum input voltage	I/O_n	V_{CC} = 5.5V, V_I = 5.5V				1	mA
		Except I/O_n	V_{CC} = 5.5V, V_I = 7.0V				100	μA
I_{IH}	High-level input current	Except I/O_n	V_{CC} = MAX, V_I = 7.0V				20	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				−0.6	mA
I_{IH} + I_{OZH}	OFF-state output current High-level voltage applied	I/O_n only	V_{CC} = MAX, V_O = 2.7V				70	μA
I_{IL} + I_{OZL}	OFF-state output current Low-level voltage applied		V_{CC} = MAX, V_O = 0.5V				−0.6	mA
I_{OS}	Short-circuit output current[3]	Except LT, EQ, GT	V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current (total)		V_{CC} = MAX			110	150	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value under recommended operating conditions for the applicable conditions.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

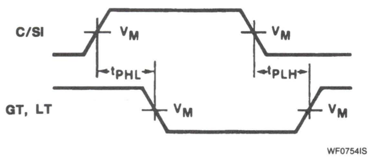
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F524					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 4	50	65		45		MHz
t_{PLH} t_{PHL}	Propagation delay I/O_n to EQ	Waveform 2	9.0 4.5	12.5 7.5	20.0 12.0	9.0 4.5	21.0 13.0	ns
t_{PLH} t_{PHL}	Propagation delay I/O_n to GT	Waveform 2	6.5 6.5	11.0 9.5	19.0 16.5	6.5 6.5	20.0 17.5	ns
t_{PLH} t_{PHL}	Propagation delay I/O_n to LT	Waveform 2	7.0 4.5	13.0 6.0	20.0 14.0	7.0 4.5	21.0 15.0	ns
t_{PLH} t_{PHL}	Propagation delay I/O_n to C/SO	Waveform 2	8.0 6.0	11.0 10.5	19.5 16.0	8.0 6.0	20.5 17.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to EQ	Waveform 4	10.0 4.0	16.0 10.0	25.0 16.5	10.0 4.0	26.0 17.5	ns
t_{PLH} t_{PHL}	Propagation delay CP to GT	Waveform 4	10.0 8.5	14.0 14.5	21.0 22.0	10.0 8.5	22.0 23.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to LT	Waveform 4	9.0 5.5	16.0 14.0	25.0 18.0	9.0 5.5	26.0 19.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to C/SO (compare)	Waveform 4	8.5 8.5	16.0 16.0	21.0 21.0	8.5 8.5	22.0 22.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to C/SO (serial shift)	Waveform 4	5.0 4.5	10.0 9.0	13.0 11.5	5.0 4.5	14.0 12.5	ns
t_{PLH} t_{PHL}	Propagation delay C/SI to GT	Waveform 1	9.0 2.5	12.5 4.5	19.0 8.5	9.0 2.0	20.0 9.5	ns
t_{PLH} t_{PHL}	Propagation delay C/SI to LT	Waveform 1	8.0 2.5	12.0 6.0	20.0 8.5	8.0 2.5	21.0 9.5	ns
t_{PLH} t_{PHL}	Propagation delay S_0, S_1 to C/SO	Waveform 2	6.5 5.5	6.0 10.0	14.5 18.0	6.5 5.5	15.5 19.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{SE}$ to EQ	Waveform 2	3.5 2.5	7.0 4.5	10.5 6.0	3.5 2.5	11.5 9.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{SE}$ to GT	Waveform 2	6.5 3.5	9.0 5.0	16.0 6.0	6.5 3.0	17.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{SE}$ to LT	Waveform 2	5.0 3.5	9.0 5.5	13.5 8.0	5.0 3.0	14.5 9.0	ns
t_{PLH} t_{PHL}	Propagation delay C/SI to C/SO	Waveform 2	4.0 4.0	7.0 7.0	11.0 11.0	4.0 4.0	12.0 12.0	ns
t_{PLH} t_{PHL}	Propagation delay M to GT	Waveform 2	8.0 6.0	13.0 10.0	19.5 15.5	8.0 6.0	20.5 16.5	ns
t_{PLH} t_{PHL}	Propagation delay M to LT	Waveform 2	8.0 4.5	15.0 0.0	22.0 12.0	8.0 4.0	23.0 13.0	ns
t_{PZH} t_{PZL}	Output enable time S_0, S_1 to I/O_n	Waveform 5, 6	4.5 5.5	7.0 9.0	13.0 15.0	4.5 5.5	14.0 16.0	ns
t_{PHZ} t_{PLZ}	Output disable time S_0, S_1 to I/O_n	Waveform 5, 6	3.0 4.5	5.0 0.0	12.0 12.5	2.0 4.5	13.0 13.5	ns

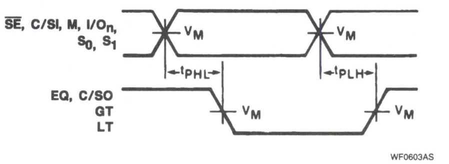
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	74F524					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low I/O_n to CP	Waveform 3	6.0 6.0			6.0 6.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low I/O_n or CP	Waveform 3	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low S_0, S_1 to CP	Waveform 3	13.5 10.0			15.0 10.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low S_0 or S_1 to CP	Waveform 3	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low C/SI to CP	Waveform 3	7.0 7.0			7.0 7.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low C/SI to CP	Waveform 3	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	CP Clock Pulse width High CP Clock Pulse width Low	Waveform 4	5.0 9.5			5.0 10.0		ns

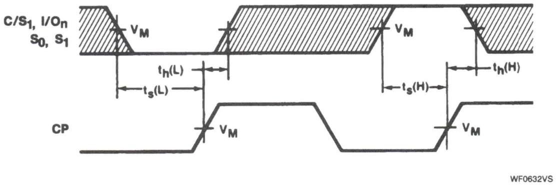
AC WAVEFORMS


C/SI
VM
VM
tPHL
tPLH
GT, LT
VM
VM
WF0754IS

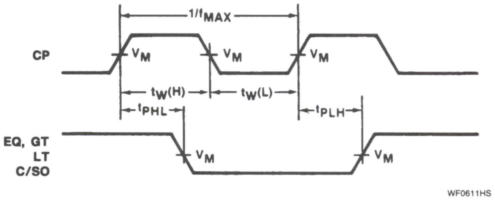
Waveform 1. For Inverting Outputs


SE, C/SI, M, I/On, S0, S1
VM
VM
tPHL
tPLH
EQ, C/SO
GT
LT
VM
VM
WF0603AS

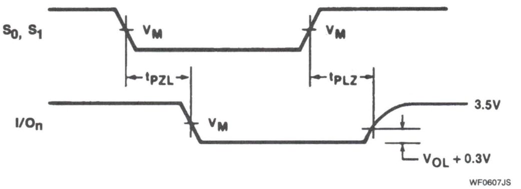
Waveform 2. For Non-Inverting Outputs


C/S1, I/On
S0, S1
VM
VM
th(L)
ts(L)
ts(H)
th(H)
CP
VM
VM
WF0632VS

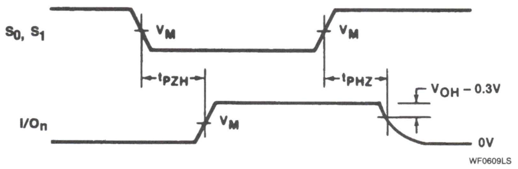
Waveform 3. Data Setup and Hold Times


1/fMAX
CP
VM
VM
VM
tW(H)
tW(L)
tPHL
tPLH
EQ, GT
LT
C/SO
VM
VM
WF0611HS

Waveform 4. Clock to Output Delays and Clock Pulse Width


S0, S1
VM
VM
tPZL
tPLZ
I/On
VM
3.5V
VOL + 0.3V
WF0607JS

Waveform 5. 3-State Enable Time to Low Level and Disable Time From Low Level


S0, S1
VM
VM
tPZH
tPHZ
VOH - 0.3V
I/On
VM
0V
WF0609LS

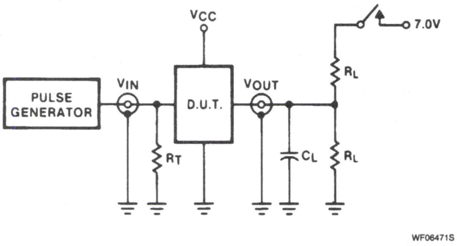
Waveform 6. 3-State Enable Time to High Level and Disable Time From High Level

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

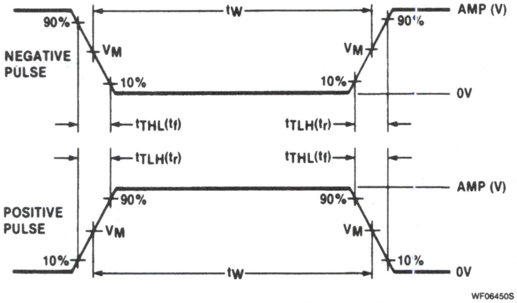
Comparator

FAST 74F524

TEST CIRCUIT AND WAVEFORMS


VCC
7.0V
RL
PULSE GENERATOR
VIN
D.U.T.
VOUT
RT
CL
RL
WF06471S

Test Circuit for 3-State and Open-Collector Outputs


90%
tW
90%
AMP (V)
NEGATIVE PULSE
VM
VM
10%
10%
0V
tTHL(tf)
tTLH(tr)
tTLH(tr)
tTHL(tf)
AMP (V)
90%
90%
POSITIVE PULSE
VM
VM
10%
10%
0V
tW
WF06450S

$V_M = 1.5V$

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
OC	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F533, 74F534
Latch/Flip-Flop

'F533 Octal Transparent Latch (3-State)
'F534 Octal D Flip-Flop (3-State)
Product Specification

FAST Products

FEATURES

- **8-bit transparent latch — 'F533**
- **8-bit positive edge-triggered register — 'F534**
- **3-State inverting output buffers**
- **Common 3-State Output Enable**
- **Independent register and 3-State buffer operation**

DESCRIPTION

The 'F533 is an octal transparent latch coupled to eight 3-State inverting output buffers. The two sections of the device are controlled independently by latch Enable (E) and Output Enable ($\overline{OE}$) control gates.

The data on the D inputs are transferred to the latch outputs when the latch Enable (E) input is High. The latch remains transparent to the data inputs while E is High, and stores the data present one setup time before the High-to-Low enable transition.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F533	6.0ns	41mA
74F534	6.6ns	55mA

ORDERING INFORMATION

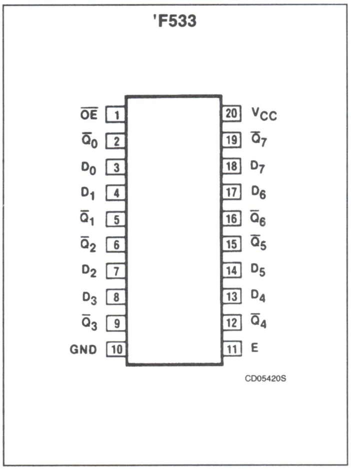
PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
20-Pin Plastic DIP	N74F533N, N74F534N
20-Pin Plastic SOL	N74F533D, N74F534D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

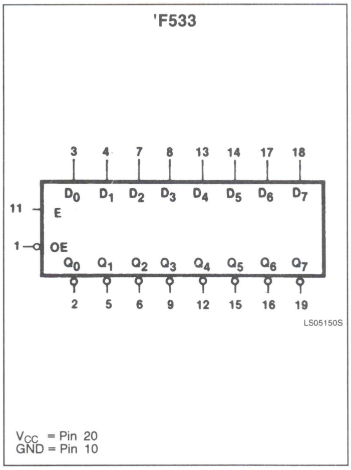
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$D_0 - D_7$	Data inputs	1.0/1.0	20μA/0.6mA
E ('F533)	Latch enable input (active-High)	1.0/1.0	20μA/0.6mA
$\overline{OE}$	Output enable input (active-Low)	1.0/1.0	20μA/0.6mA
CP ('F534)	Clock Pulse input (active rising edge)	1.0/1.0	20μA/0.6mA
$\overline{Q}_0 - \overline{Q}_7$	3-State outputs	150/40	3mA/24mA

NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION

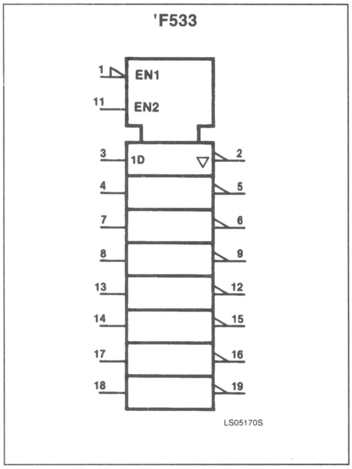

'F533
OE 1
Q0 2
D0 3
D1 4
Q1 5
Q2 6
D2 7
D3 8
Q3 9
GND 10
20 VCC
19 Q7
18 D7
17 D6
16 Q6
15 Q5
14 D5
13 D4
12 Q4
11 E
CD05420S

LOGIC SYMBOL


'F533
3 4 7 8 13 14 17 18
D0 D1 D2 D3 D4 D5 D6 D7
11 E
1 OE
Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
2 5 6 9 12 15 16 19
LS05150S

V_{CC} = Pin 20
GND = Pin 10

LOGIC SYMBOL (IEEE/IEC)

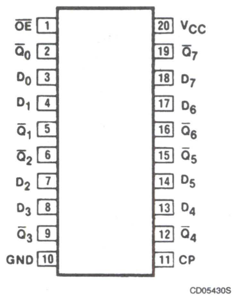

'F533
1 EN1
11 EN2
3 1D 2
4 5
7 6
8 9
13 12
14 15
17 16
18 19
LS05170S

Latch/Flip-Flop

FAST 74F533, 74F534

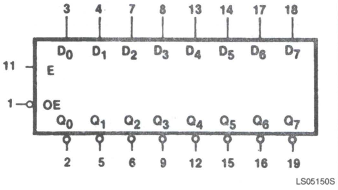
PIN CONFIGURATION

'F534


$\overline{OE}$ 1
$\overline{Q}_0$ 2
D_0 3
D_1 4
$\overline{Q}_1$ 5
$\overline{Q}_2$ 6
D_2 7
D_3 8
$\overline{Q}_3$ 9
GND 10
20 V_{CC}
19 $\overline{Q}_7$
18 D_7
17 D_6
16 $\overline{Q}_6$
15 $\overline{Q}_5$
14 D_5
13 D_4
12 $\overline{Q}_4$
11 CP
CD05430S

LOGIC SYMBOL

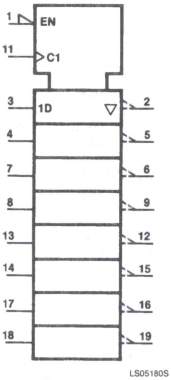
'F534


3 4 7 8 13 14 17 18
D_0 D_1 D_2 D_3 D_4 D_5 D_6 D_7
11 E
1 OE
Q_0 Q_1 Q_2 Q_3 Q_4 Q_5 Q_6 Q_7
2 5 6 9 12 15 16 19
LS05150S

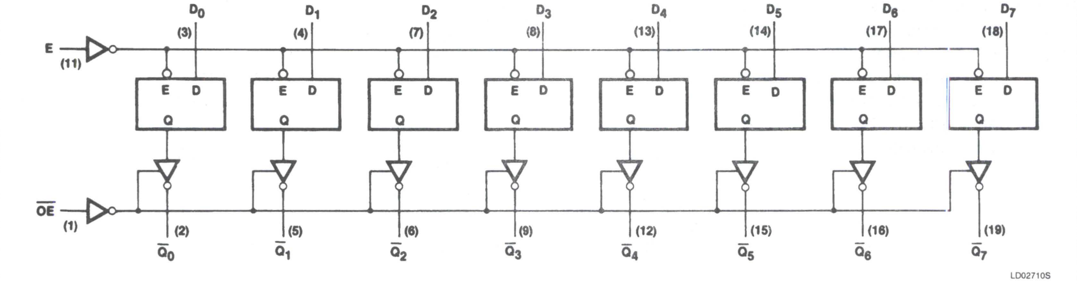
V_{CC} = Pin 20
GND = Pin 10

LOGIC SYMBOL (IEEE/IEC)

'F534

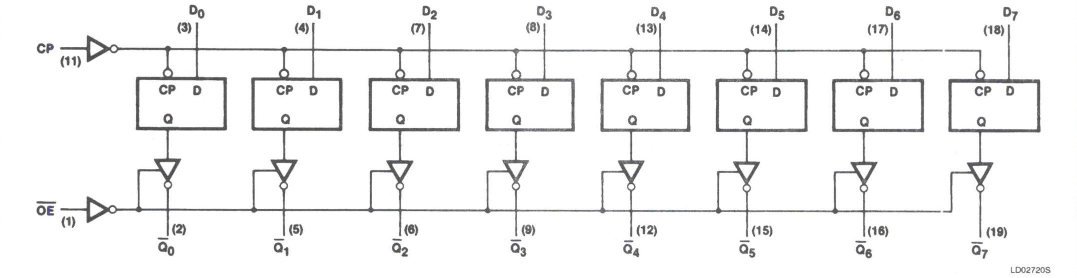

1 EN
11 C1
3 1D 2
4 5
7 6
8 9
13 12
14 15
17 16
18 19
LS05180S

LOGIC DIAGRAM, 'F533


E (11)
D_0 (3) D_1 (4) D_2 (7) D_3 (8) D_4 (13) D_5 (14) D_6 (17) D_7 (18)
E D Q
$\overline{OE}$ (1)
(2) $\overline{Q}_0$ (5) $\overline{Q}_1$ (6) $\overline{Q}_2$ (9) $\overline{Q}_3$ (12) $\overline{Q}_4$ (15) $\overline{Q}_5$ (16) $\overline{Q}_6$ (19) $\overline{Q}_7$
LD02710S

V_{CC} = Pin 20
GND = Pin 10

LOGIC DIAGRAM, 'F534


CP (11)
D_0 (3) D_1 (4) D_2 (7) D_3 (8) D_4 (13) D_5 (14) D_6 (17) D_7 (18)
CP D Q
$\overline{OE}$ (1)
(2) $\overline{Q}_0$ (5) $\overline{Q}_1$ (6) $\overline{Q}_2$ (9) $\overline{Q}_3$ (12) $\overline{Q}_4$ (15) $\overline{Q}_5$ (16) $\overline{Q}_6$ (19) $\overline{Q}_7$
LD02720S

V_{CC} = Pin 20
GND = Pin 10

MODE SELECT — FUNCTION TABLE, 'F533

OPERATING MODES	INPUTS			INTERNAL REGISTER	OUTPUTS
	$\overline{OE}$	E	D_n		$\overline{Q}_0 - \overline{Q}_7$
Enable and read register	L	H	L	L	H
	L	H	H	H	L
Latch and read register	L	↓	l	L	H
	L	↓	h	H	L
Hold	L	L	X	NC	NC
Disable outputs	H	X	X	X	Z

NC = No change

MODE SELECT — FUNCTION TABLE, 'F534

OPERATING MODES	INPUTS			INTERNAL REGISTER	OUTPUTS
	$\overline{OE}$	CP	D_n		$\overline{Q}_0 - \overline{Q}_7$
Load and read register	L	↑	l	L	H
	L	↑	h	H	L
Disable outputs	H	X	X	X	Z

H = High voltage level
h = High voltage level one setup time prior to the Low-to-High clock transition or High-to-Low $\overline{OE}$ transition
L = Low voltage level
X = Don't care
l = Low voltage level one setup time prior to the Low-to-High clock transition or High-to-Low $\overline{E}$ transition
Z = High-impedance "OFF" state
↓= High-to-Low clock transition

The 3-State inverting output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active-Low Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the latch operation. When $\overline{OE}$ is Low, the latched or transparent data appears at the outputs. When $\overline{OE}$ is High, the outputs are in the High impedance "OFF" state, which means they will neither drive nor load the bus.

The 'F534 is an 8-bit edge-triggered register coupled to eight 3-State inverting output buffers. The two sections of the device are controlled independently by the Clock (CP) and Output Enable ($\overline{OE}$) control gates.

The register is fully edge triggered. The state of each D input, one setup time before the Low-to-High clock transition, transferred to the corresponding flip-flop's Q output. The clock buffer has about 400mV of hysteresis built in to help minimize problems that signal and ground noise can cause the clocking operation.

The 3-State inverting output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active-Low Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the register operation. When $\overline{CE}$ is Low, data in the register appears at the outputs. When $\overline{OE}$ is High, the outputs are in the High impedance "OFF" state, which means they will neither drive nor load the bus.

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_A	Operating free-air temperature range	0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−3	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		74F533, 'F534			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX V_{IH} = MIN,	±10%V_{CC}	2.4			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OL} = MAX V_{IH} = MIN	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				−0.6	mA
I_{OZH}	OFF-stage output current, High-level voltage applied		V_{CC} = MAX, V_O = 2.7V				50	μA
I_{OZL}	OFF-state output current, Low-level voltage applied		V_{CC} = MAX, V_O = 0.5V				−50	μA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX, V_O = 0.0V		−60		−150	mA
I_{CC}	Supply current[4] (total)	'F533	V_{CC} = MAX			41	61	mA
		'F534				55	86	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. 'F533 measure I_{CCZ} with $\overline{OE}$ input at 4.5V, D_n and E inputs at ground and all outputs open.
   'F534 measure I_{CCZ} with $\overline{OE}$ inputs at 4.5V and D_n inputs at ground and all outputs open.

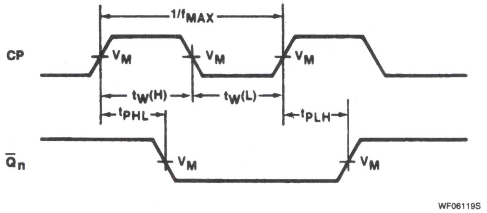
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	74F533, 74F534					UNIT
				$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	'F533	Waveform 2	4.0 3.0	6.9 5.2	9.0 7.0	4.0 3.0	10.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay E to $\overline{Q}_n$		Waveform 3	5.0 3.0	8.5 5.6	11.0 7.0	5.0 3.0	13.0 8.0	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level		Waveform 6 Waveform 7	2.0 2.0	7.7 5.1	10.0 6.5	2.0 2.0	11.0 7.5	ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level		Waveform 6 Waveform 7	2.0 2.0	4.7 4.1	6.0 5.5	2.0 2.0	7.0 6.5	ns
f_{MAX}	Maximum clock frequency	'F534	Waveform 1	100			70		MHz
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{Q}_n$		Waveform 1	4.0 4.0	6.5 6.5	8.5 8.5	4.0 4.0	10.0 10.0	ns
t_{PZH}	Output Enable time to High or Low level		Waveform 6 Waveform 7	2.0 2.0	9.0 5.8	11.5 7.5	2.0 2.0	12.5 8.5	ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level		Waveform 6 Waveform 7	2.0 2.0	5.3 4.3	7.0 5.5	2.0 2.0	8.0 6.5	ns

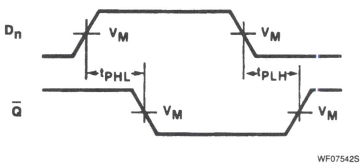
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER		TEST CONDITIONS	74F533, 'F534					UNIT
				$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
				Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, D_n to E	'F533	Waveform 5	2.0 2.0			2.0 2.0		ns
$t_h(H)$ $t_h(L)$	Hold time, D_n to E		Waveform 5	3.0 3.0			3.0 3.0		ns
$t_w(H)$	E pulse width High or Low		Waveform 3	6.0			6.0		ns
$t_s(H)$ $t_s(L)$	Setup time, D_n to CP	'F534	Waveform 4	2.0 2.0			2.0 2.0		ns
$t_h(H)$ $t_h(L)$	Hold time D_n to CP		Waveform 4	2.0 2.0			2.0 2.0		ns
$t_w(H)$ $t_w(L)$	CP pulse width, High or Low		Waveform 1	5.0 5.0			7.0 6.0		ns

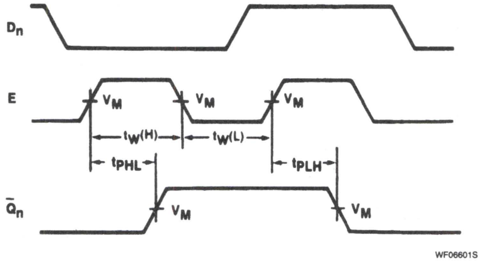
AC WAVEFORMS


1/fMAX
CP
VM
VM
VM
tW(H)
tW(L)
tPHL
tPLH
Q̄n
VM
VM
WF06119S

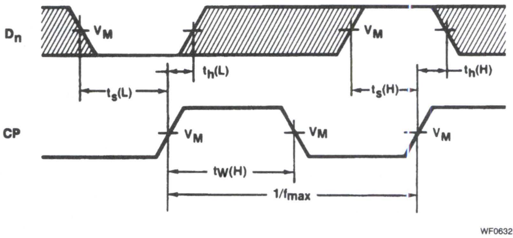
Waveform 1. Clock to Output Delays and Clock Pulse Width


Dn
VM
VM
tPHL
tPLH
Q̄
VM
VM
WF07542S

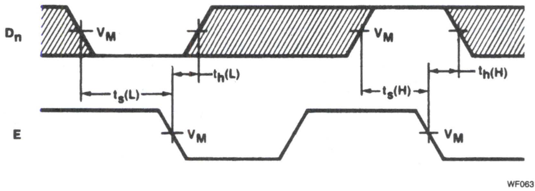
Waveform 2. Data to Output Delays


Dn
E
VM
VM
VM
tW(H)
tW(L)
tPHL
tPLH
Q̄n
VM
VM
WF06601S

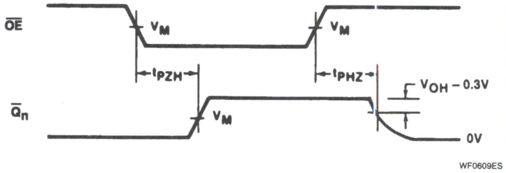
Waveform 3. Latch Enable to Output Delays


Dn
VM
VM
th(L)
th(H)
ts(L)
ts(H)
CP
VM
VM
VM
tW(H)
1/fmax
WF06325S

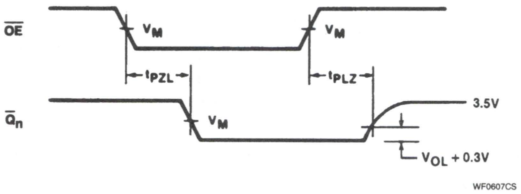
Waveform 4. Data Setup and Hold Times


Dn
VM
VM
th(L)
th(H)
ts(L)
ts(H)
E
VM
VM
WF06314S

Waveform 5. Data Setup and Hold Times


OE
VM
VM
tPZH
tPHZ
VOH − 0.3V
Q̄n
VM
0V
WF0609ES

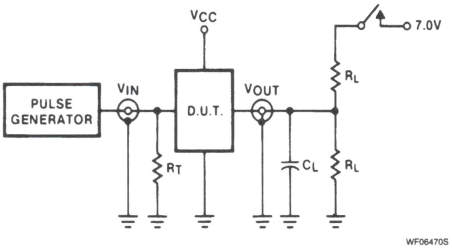
Waveform 6. 3-State Output Enable Time to High Level and Output Disable Time From High Level


OE
VM
VM
tPZL
tPLZ
Q̄n
VM
3.5V
VOL + 0.3V
WF0607CS

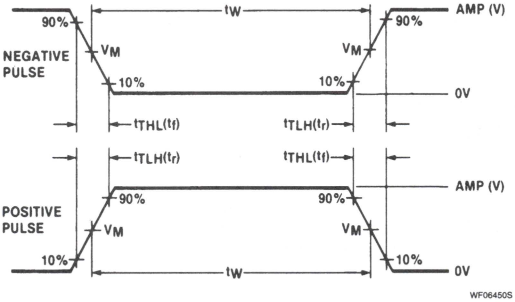
Waveform 7. 3-State Output Enable Time to Low Level and Output Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS


VCC
7.0V
RL
PULSE GENERATOR
VIN
D.U.T.
VOUT
RT
CL
RL
WF06470S

Test Circuit for 3-State Outputs


NEGATIVE PULSE
90%
VM
10%
tW
AMP (V)
0V
tTHL(tf)
tTLH(tr)
POSITIVE PULSE
90%
VM
10%
tW
AMP (V)
0V
WF06450S

$V_M = 1.5V$
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS
R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F537
1-Of-10 Decoder (3-State)

Product Specification

FAST Products

DESCRIPTION

The 'F537 is one-of-ten decoder/demultiplexer with four active-High BCD inputs and ten mutually exclusive outputs. A Polarity control (P) input determines whether the outputs are active-Low or active-High. The 'F537 has 3-State outputs, and a High signal on the Output Enable ($\overline{OE}$) input forces all outputs to the high-impedance state. Two input Enables, active-High (E_1) and active Low ($\overline{E}_0$), are available for demultiplexing data to the selected output in either non-inverted or inverted form. Input codes greater than BCD nine cause all outputs to go to the inactive state (i.e., same polarity as the P input).

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F537	9ns	44mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
20-Pin Plastic DIP	N74F537N
20-Pin Plastic SOL	N74F537D

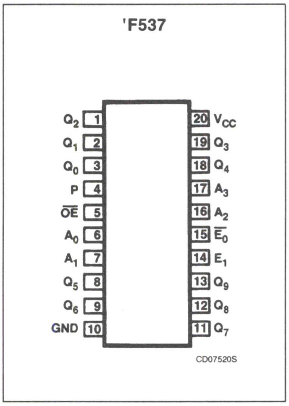
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$A_0 - A_3$	Address inputs	1.0/1.0	20μA/0.6mA
$\overline{E}_0$	Enable input (active-Low)	1.0/1.0	20μA/0.6mA
E_1	Enable input (active-High)	1.0/1.0	20μA/0.6mA
P	Polarity control input	1.0/1.0	20μA/0.6mA
$\overline{OE}$	Output enable input (active-Low)	1.0/1.0	20μA/0.6mA
$Q_0 - Q_9$	Data outputs	150/40	3.0mA/24mA

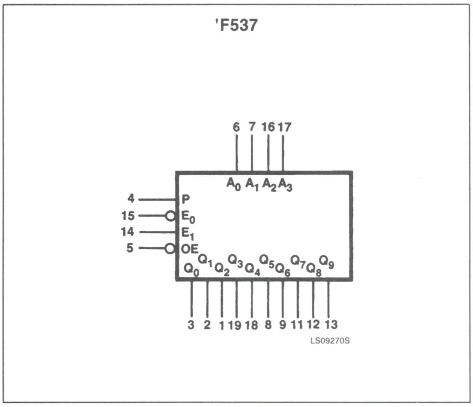
NOTE:

1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

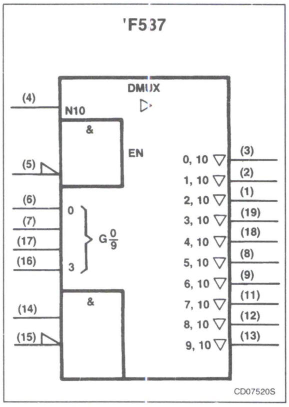
PIN CONFIGURATION


'F537
Q2 1
Q1 2
Q0 3
P 4
OE 5
A0 6
A1 7
Q5 8
Q6 9
GND 10
20 VCC
19 Q3
18 Q4
17 A3
16 A2
15 E0
14 E1
13 Q9
12 Q8
11 Q7
CD07520S

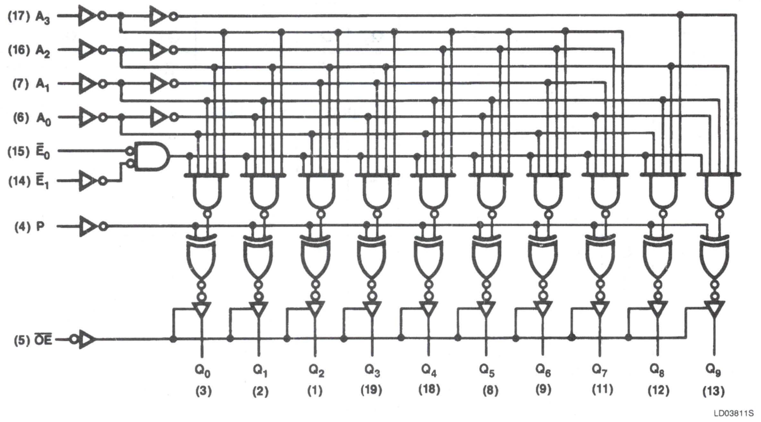
LOGIC SYMBOL


'F537
6 7 16 17
A0 A1 A2 A3
4 P
15 E0
14 E1
5 OE
Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7 Q8 Q9
3 2 1 19 18 8 9 11 12 13
LS09270S

LOGIC SYMBOL (IEEE/IEC)


'F537
DMUX
(4) N10
&
(5)
EN
(6) (7) (17) (16)
0
3
G 0/9
(14)
&
(15)
0, 10 (3)
1, 10 (2)
2, 10 (1)
3, 10 (19)
4, 10 (18)
5, 10 (8)
6, 10 (9)
7, 10 (11)
8, 10 (12)
9, 10 (13)
CD07520S

LOGIC DIAGRAM


(17) A_3
(16) A_2
(7) A_1
(6) A_0
(15) $\bar{E}_0$
(14) $\bar{E}_1$
(4) P
(5) $\overline{OE}$
Q_0 (3)
Q_1 (2)
Q_2 (1)
Q_3 (19)
Q_4 (18)
Q_5 (8)
Q_6 (9)
Q_7 (11)
Q_8 (12)
Q_9 (13)
LD03811S

V_{CC} = Pin 20
GND = Pin 10
( ) = Pin numbers

1-Of-10 Decoder (3-State) FAST 74F537

FUNCTION TABLE

INPUTS							OUTPUTS										OPERATING MODE
$\overline{OE}$	$\overline{E}_0$	E_1	A_3	A_2	A_1	A_0	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	Q_8	Q_9	
H	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	High-impedance
L	H	X	X	X	X	X	Outputs equal P input										Disable
L	X	L	X	X	X	X											
L	L	H	L	L	L	L	H	L	L	L	L	L	L	L	L	L	Active-High output (P = L)
L	L	H	L	L	L	H	L	H	L	L	L	L	L	L	L	L	
L	L	H	L	L	H	L	L	L	H	L	L	L	L	L	L	L	
L	L	H	L	L	H	H	L	L	L	H	L	L	L	L	L	L	
L	L	H	L	H	L	L	L	L	L	L	H	L	L	L	L	L	
L	L	H	L	H	L	H	L	L	L	L	L	H	L	L	L	L	
L	L	H	L	H	H	L	L	L	L	L	L	L	H	L	L	L	
L	L	H	L	H	H	H	L	L	L	L	L	L	L	H	L	L	
L	L	H	H	L	L	L	L	L	L	L	L	L	L	L	H	L	
L	L	H	H	L	L	H	L	L	L	L	L	L	L	L	L	H	
L	L	H	H	X	H	X	L	L	L	L	L	L	L	L	L	L	
L	L	H	H	L	X	X	L	L	L	L	L	L	L	L	L	L	
L	L	H	L	L	L	L	L	H	H	H	H	H	H	H	H	H	Active-Low output (P = H)
L	L	H	L	L	L	H	H	L	H	H	H	H	H	H	H	H	
L	L	H	L	L	H	L	H	H	L	H	H	H	H	H	H	H	
L	L	H	L	L	H	H	H	H	H	L	H	H	H	H	H	H	
L	L	H	L	H	L	L	H	H	H	H	L	H	H	H	H	H	
L	L	H	L	H	L	H	H	H	H	H	H	L	H	H	H	H	
L	L	H	L	H	H	L	H	H	H	H	H	H	L	H	H	H	
L	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	
L	L	H	H	L	L	L	H	H	H	H	H	H	H	H	L	H	
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	L	
L	L	H	H	X	H	X	H	H	H	H	H	H	H	H	H	H	
L	L	H	H	H	X	X	H	H	H	H	H	H	H	H	H	H	

H = High voltage level
L = Low voltage level
X = Don't care
Z = High-impedance

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature range	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−3	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.4			V
			±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.35	0.50	V
			±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, $I_I = I_{IK}$			−0.73	−1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V				−0.6	mA
I_{OZH}	OFF-state current High-level voltage applied	V_{CC} = MAX, V_O = 2.7V				50	μA
I_{OZL}	OFF-state current Low-level voltage applied	V_{CC} = MAX, V_O = 0.5V				−50	μA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current (total)	V_{CC} = MAX			44	66	mA

NOTES:

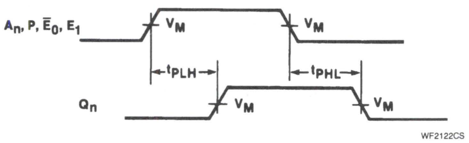
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable conditions.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

1-Of-10 Decoder (3-State) FAST 74F537

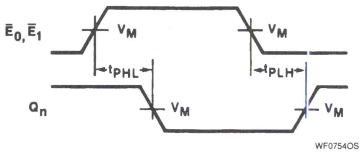
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F537					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to Q_n	Waveform 1	4.5 3.0	9.0 7.5	14.0 11.0	4.5 3.0	16.0 12.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}_0$ to Q_n	Waveform 2	4.0 3.0	8.0 8.0	11.0 11.0	4.0 3.0	12.0 12.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}_1$ to Q_n	Waveform 2	6.0 4.0	8.5 8.5	11.5 11.5	6.0 4.0	13.0 12.5	ns
t_{PLH} t_{PHL}	Propagation delay P to Q_n	Waveform 1	5.0 3.5	12.5 6.5	16.0 10.0	5.0 3.5	17.0 11.0	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}$ to Q_n	Waveform 3 Waveform 4	2.5 4.0	4.5 5.5	7.0 8.0	2.5 4.0	8.0 9.0	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}$ to Q_n	Waveform 3 Waveform 4	1.5 2.0	3.0 4.0	6.0 6.5	1.0 2.0	7.0 7.0	ns

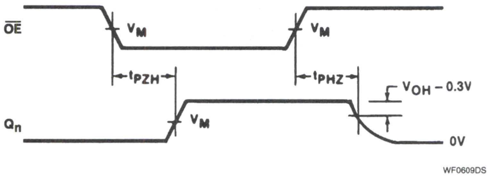
AC WAVEFORMS


A_n, P, Ē₀, E₁
V_M
V_M
t_{PLH}
t_{PHL}
Q_n
V_M
V_M
WF2122CS

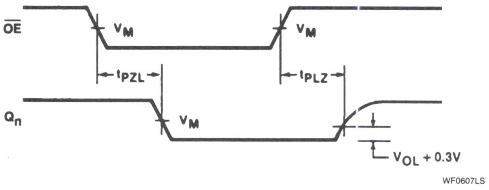
Waveform 1. Propagation Delay for Non-Inverting Outputs


Ē₀, Ē₁
V_M
V_M
t_{PHL}
t_{PLH}
Q_n
V_M
V_M
WF0754OS

Waveform 2. Propagation Delay for Inverting Outputs


OE
V_M
V_M
t_{PZH}
t_{PHZ}
V_{OH} – 0.3V
Q_n
V_M
0V
WF0609DS

Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time From High Level

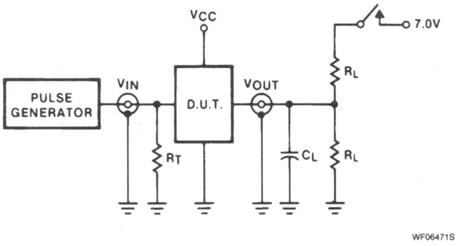

OE
V_M
V_M
t_{PZL}
t_{PLZ}
Q_n
V_M
V_{OL} + 0.3V
WF0607LS

Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time From Low Level

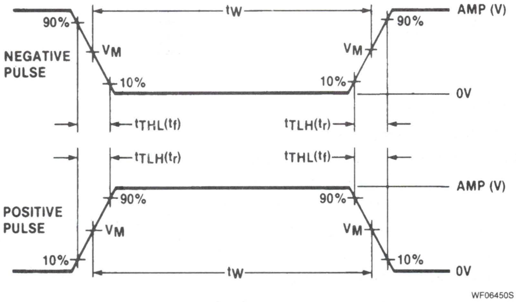
NOTE: $V_M = 1.5V$.

1-Of-10 Decoder (3-State) FAST 74F537

TEST CIRCUIT AND WAVEFORMS


VCC
7.0V
RL
PULSE GENERATOR
VIN
D.U.T.
VOUT
RT
CL
RL
WF06471S

Test Circuit for 3-State Outputs


tW
AMP (V)
90%
90%
NEGATIVE PULSE
VM
VM
10%
10%
0V
tTHL(tf)
tTLH(tr)
tTLH(tr)
tTHL(tf)
AMP (V)
90%
90%
POSITIVE PULSE
VM
VM
10%
10%
tW
0V
WF06450S

$V_M = 1.5V$

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F538

1-Of-8 Decoder (3-State)

Product Specification

FAST Products

DESCRIPTION

The 'F538 decoder/demultiplexer accepts three Address ($A_0 - A_3$) input signals and decodes them to select one of eight mutually exclusive outputs. A Polarity control (P) input determines whether the outputs are active-Low or active-High. The 'F538 has 3-State outputs, and a High signal on the Output Enables ($\overline{OE}n$) will force all outputs to the High-impedance state. Two active-High and two active-Low Enable inputs are available for easy expansion to 1-of-32 decoding with four packages, or for data demultiplexing to 1-of-8 or 1-of-16 destinations.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F538	8.5ns	35mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
20-Pin Plastic DIP	N74F538N
20-Pin Plastic SOL	N74F538

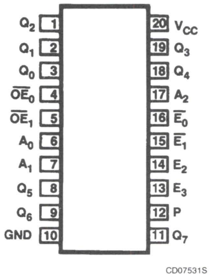
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$A_0 - A_2$	Address inputs	1.0/1.0	20μA/0.6mA
$\overline{E}_0$, $\overline{E}_1$	Enable input (active-Low)	1.0/1.0	20μA/0.6mA
E_2, E_3	Enable input (active-High)	1.0/1.0	20μA/0.6mA
P	Polarity control input	1.0/1.0	20μA/0.6mA
$\overline{OE}_0$, $\overline{OE}_1$	Output Enable input (active-Low)	1.0/1.0	20μA/0.6mA
$Q_0 - Q_9$	Data outputs	150/40	3mA/24mA

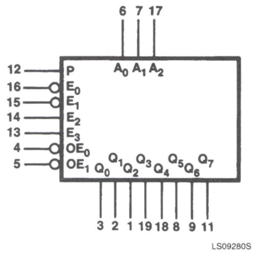
NOTE:

1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION

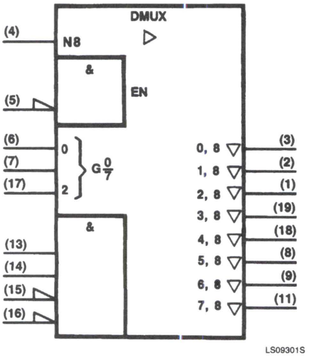

Q2 1
Q1 2
Q0 3
OE0 4
OE1 5
A0 6
A1 7
Q5 8
Q6 9
GND 10
20 VCC
19 Q3
18 Q4
17 A2
16 E0
15 E1
14 E2
13 E3
12 P
11 Q7
CD07531S

LOGIC SYMBOL


6 7 17
12 P
16 E0
15 E1
14 E2
13 E3
4 OE0
5 OE1
A0 A1 A2
Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
3 2 1 19 18 8 9 11
LS09280S

V_{CC} = Pin 16
GND = Pin 8

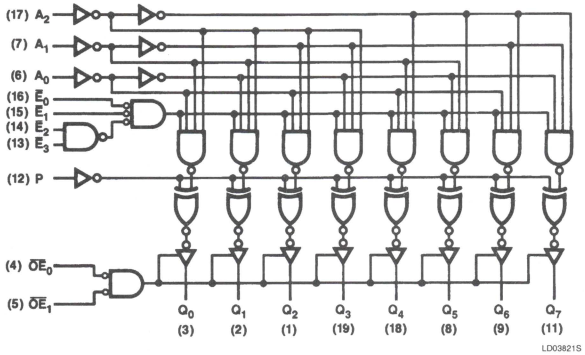
LOGIC SYMBOL (IEEE/IEC)


DMUX
N8
&
EN
(4)
(5)
(6)
(7)
(17)
0
2
G 0/7
&
(13)
(14)
(15)
(16)
0, 8 (3)
1, 8 (2)
2, 8 (1)
3, 8 (19)
4, 8 (18)
5, 8 (8)
6, 8 (9)
7, 8 (11)
LS09301S

1-Of-8 Decoder (3-State)

FAST 74F538

LOGIC DIAGRAM



V_{CC} = Pin 20
GND = Pin 10
( ) = Pin numbers

FUNCTION TABLE

INPUTS									OUTPUTS								OPERATING MODE
$\overline{OE}_0$	$\overline{OE}_1$	$\overline{E}_0$	$\overline{E}_1$	E_2	E_3	A_2	A_1	A_0	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	
H	X	X	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z	High-impedance
X	H	X	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z	
L	L	H	X	X	X	X	X	X	Outputs equal P input								Disable
L	L	X	H	X	X	X	X	X									
L	L	X	X	L	X	X	X	X									
L	L	X	X	X	L	X	X	X									
L	L	L	L	H	H	L	L	L	H	L	L	L	L	L	L	L	Active-High output (P = L)
L	L	L	L	H	H	L	L	H	L	H	L	L	L	L	L	L	
L	L	L	L	H	H	L	H	L	L	L	H	L	L	L	L	L	
L	L	L	L	H	H	L	H	H	L	L	L	H	L	L	L	L	
L	L	L	L	H	H	H	L	L	L	L	L	L	H	L	L	L	
L	L	L	L	H	H	H	L	H	L	L	L	L	L	H	L	L	
L	L	L	L	H	H	H	H	L	L	L	L	L	L	L	H	L	
L	L	L	L	H	H	H	H	H	L	L	L	L	L	L	L	H	
L	L	L	L	H	H	L	L	L	L	H	H	H	H	H	H	H	Active-Low output (P = H)
L	L	L	L	H	H	L	L	H	H	L	H	H	H	H	H	H	
L	L	L	L	H	H	L	H	L	H	H	L	H	H	H	H	H	
L	L	L	L	H	H	L	H	H	H	H	H	L	H	H	H	H	
L	L	L	L	H	H	H	L	L	H	H	H	H	L	H	H	H	
L	L	L	L	H	H	H	L	H	H	H	H	H	H	L	H	H	
L	L	L	L	H	H	H	H	L	H	H	H	H	H	H	L	H	
L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	

H = High voltage level
L = Low voltage level
X = Don't care
Z = High-impedance

1-Of-8 Decoder (3-State) FAST 74F538

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature range	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−3	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		74F538			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.4			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OZH}	OFF-state current High-Level voltage applied		V_{CC} = MAX, V_0 = 2.7V				50	μA
I_{OZL}	OFF-state current Low-Level voltage applied		V_{CC} = MAX, V_0 = 0.5V				-50	μA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			30	40	mA
		I_{CCL}				35	50	mA
		I_{CCZ}				35	50	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of High-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

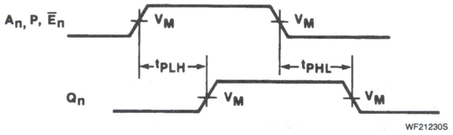
1-Of-8 Decoder (3-State)

FAST 74F538

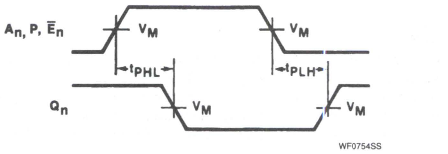
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F538					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH}	Propagation delay A_n to Q_n	Waveform 1, 2	5.5	8.5	13.0	5.0	14.0	ns
t_{PHL}			3.0	7.5	12.5	3.0	13.5	
t_{PLH}	Propagation delay $\overline{E}_0$ or $\overline{E}_1$ to Q_n	Waveform 1, 2	5.5	8.5	12.0	5.0	13.0	ns
t_{PHL}			3.0	7.5	12.0	3.0	12.5	
t_{PLH}	Propagation delay $\overline{E}_2$ or $\overline{E}_3$ to Q_n	Waveform 1, 2	6.5	9.0	12.5	5.5	13.5	ns
t_{PHL}			4.0	7.0	12.5	3.5	13.0	
t_{PLH}	Propagation delay P to Q_n	Waveform 1, 2	4.5	9.5	15.0	4.0	16.5	ns
t_{PHL}			3.5	6.5	10.0	3.5	10.5	
t_{PZH}	Output enable time $\overline{OE}_0$ or $\overline{OE}_1$ to Q_n	Waveform 3	2.5	5.5	9.5	2.0	11.0	ns
t_{PZL}		Waveform 4	6.5	9.5	13.5	6.0	15.0	
t_{PHZ}	Output Disable time $\overline{OE}_0$ or $\overline{OE}_1$ to Q_n	Waveform 3	1.0	3.0	6.0	1.0	7.0	ns
t_{PLZ}		Waveform 4	1.0	3.5	8.5	1.0	9.5	

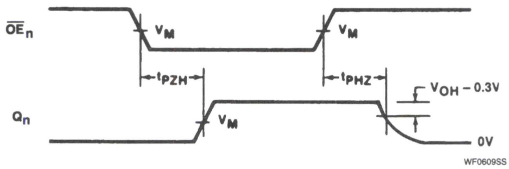
AC WAVEFORMS


A_n, P, $\overline{E}_n$
V_M
V_M
t_{PLH}
t_{PHL}
Q_n
V_M
V_M
WF21230S

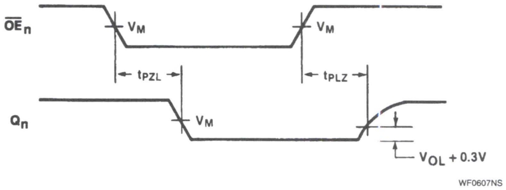
Waveform 1. Propagation Delay for Non-Inverting Outputs


A_n, P, $\overline{E}_n$
V_M
V_M
t_{PHL}
t_{PLH}
Q_n
V_M
V_M
WF0754SS

Waveform 2. Propagation Delay for Inverting Outputs


$\overline{OE}_n$
V_M
V_M
t_{PZH}
t_{PHZ}
$V_{OH} - 0.3V$
Q_n
V_M
0V
WF0609SS

Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time From High Level

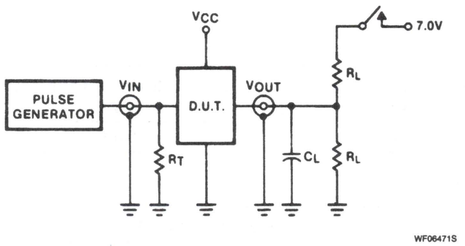

$\overline{OE}_n$
V_M
V_M
t_{PZL}
t_{PLZ}
Q_n
V_M
$V_{OL} + 0.3V$
WF0607NS

Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time From Low Level

NOTE: $V_M = 1.5V$.

1-Of-8 Decoder (3-State) FAST 74F538

TEST CIRCUIT AND WAVEFORMS


VCC
7.0V
RL
PULSE GENERATOR
VIN
D.U.T.
VOUT
RT
CL
RL
WF06471S

Test Circuit for 3-State Outputs

SWITCH POSITION

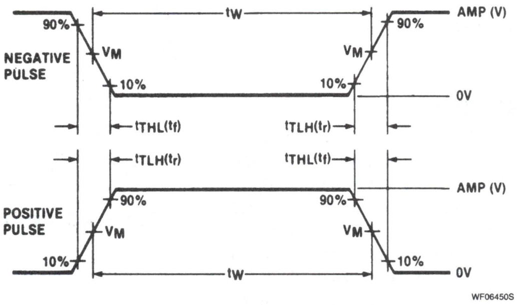
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.


tW
90%
AMP (V)
NEGATIVE PULSE
VM
10%
0V
tTHL(tf)
tTLH(tr)
tTLH(tr)
tTHL(tf)
90%
AMP (V)
POSITIVE PULSE
VM
10%
0V
tW
WF06450S

V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F539
Dual 1-Of-4 Decoder (3-State)

Product Specification

FAST Products

DESCRIPTION

The 'F539 contains two independent decoders. Each accepts two Address (A0, A1) input signals and decodes them to select one of four mutually exclusive outputs. A Polarity control (P) input determines whether the outputs are active-Low (P = H) or active-High (P = L). An active-Low Enable ($\overline{E}$) is available for data demultiplexing. Data is routed to the selected output in non-inverted or inverted form in the active-Low mode or in inverted form in the active-High mode. A High signal on the active-Low Output Enable ($\overline{OE}$) input forces the 3-State outputs to the High-impedance state.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F539	7.5ns	40mA

ORDERING INFORMATION

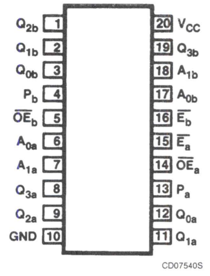
PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
20-Pin Plastic DIP	N74F537N
20-Pin Plastic SOL	N74F537D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_{0a}, A_{1a}	Decoder A Address inputs	1.0/1.0	20µA/0.6mA
A_{0b}, A_{1b}	Decoder B Address inputs	1.0/1.0	20µA/0.6mA
$\overline{E}_a$, $\overline{E}_b$	Enable input (active-Low)	1.0/1.0	20µA/0.6mA
$\overline{E}_a$, $\overline{E}_b$ $\overline{OE}_a$, $\overline{OE}_b$	Enable input (active-High) Output Enable input (active-Low)	1.0/1.0 1.0/1.0	20µA/0.6mA 20µA/0.6mA
$\overline{OE}$	Output enable input (active-Low)	1.0/1.0	20µA/0.6mA
P_a, P_b $Q_{0a} - Q_{3a}$	Polarity control inputs Decoder A Data outputs	1.0/1.0 150/40	20µA/0.6mA 3.0mA/24mA
$Q_{0b} - Q_{3b}$	Decoder B Data outputs	150/40	3.0mA/24mA

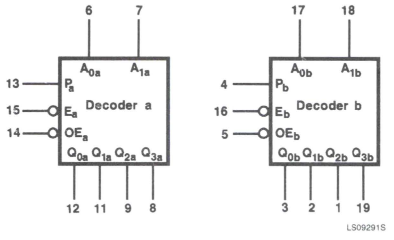
NOTE:
1. One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



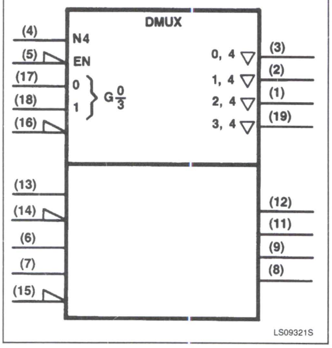
Q_{2b} 1
Q_{1b} 2
Q_{0b} 3
P_b 4
$\overline{OE}_b$ 5
A_{0a} 6
A_{1a} 7
Q_{3a} 8
Q_{2a} 9
GND 10
20 V_{CC}
19 Q_{3b}
18 A_{1b}
17 A_{0b}
16 $\overline{E}_b$
15 $\overline{E}_a$
14 $\overline{OE}_a$
13 P_a
12 Q_{0a}
11 Q_{1a}
CD07540S

LOGIC SYMBOL



6
7
A_{0a}
A_{1a}
13
P_a
15
E_a
Decoder a
14
OE_a
Q_{0a} Q_{1a} Q_{2a} Q_{3a}
12 11 9 8
17
18
A_{0b}
A_{1b}
4
P_b
16
E_b
Decoder b
5
OE_b
Q_{0b} Q_{1b} Q_{2b} Q_{3b}
3 2 1 19
LS09291S

LOGIC SYMBOL (IEEE/IEC)

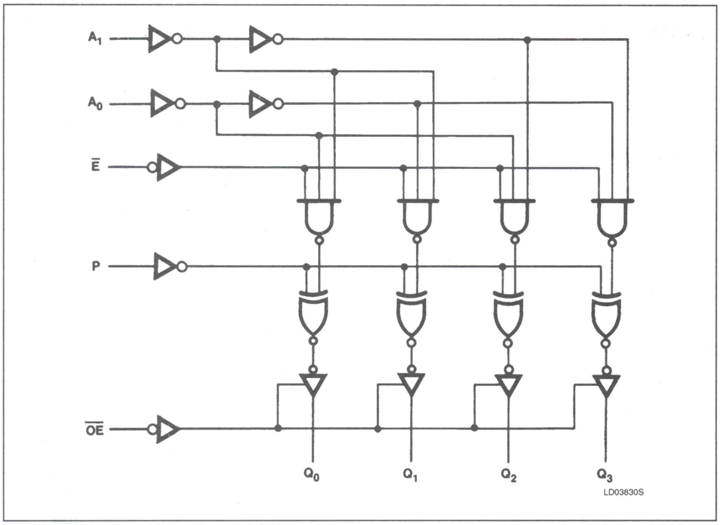


DMUX
(4)
N4
(5)
EN
(17)
0
(18)
1
$G\frac{0}{3}$
(16)
0, 4
1, 4
2, 4
3, 4
(3)
(2)
(1)
(19)
(13)
(14)
(6)
(7)
(15)
(12)
(11)
(9)
(8)
LS09321S

Dual 1-Of-4 Decoder (3-State)

FAST 74F539

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUTS				OPERATING MODE
$\overline{OE}_0$	$\overline{E}$	A_1	A_0	Q_0	Q_1	Q_2	Q_3	
H	X	X	X	Z	Z	Z	Z	High-impedance
L	H	X	X	$Q_n = P$				Disable
L L L L	L L L L	L L H H	L H L H	H L L L	L H L L	L L H L	L L L H	Active-High Output (P = L)
L L L L	L L L L	L L H H	L H L H	L H H H	H L H H	H H L H	H H H L	Active-Low Output (P = H)

H = High voltage level
L = Low voltage level
X = Don't care
Z = High-impedance

Dual 1-Of-4 Decoder (3-State)

FAST 74F539

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature range	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−3	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX V_{IH} = MIN,	±10%V_{CC}	2.4			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OL} = MAX V_{IH} = MIN,	±10%V_{CC}		.35	.50	V
				±5%V_{CC}		.35	.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				−0.6	mA
I_{OZH}	OFF-state current High-level voltage applied		V_{CC} = MAX, V_O = 2.7V				50	μA
I_{OZL}	OFF-state current Low-level voltage applied		V_{CC} = MAX, V_O = 0.5V				−50	μA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			35	50	mA
		I_{CCL}				40	55	mA
		I_{CCZ}				40	60	mA

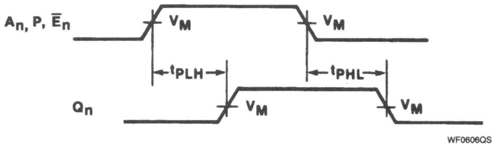
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

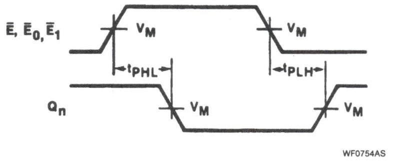
SYMBOL	PARAMETER	TEST CONDITIONS	74F539					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	Waveform 1	4.5 3.0	8.5 8.0	12.5 12.5	4.0 3.0	13.5 13.0	ns
t_{PLH} t_{PHL}	Propagation delay E to $\overline{Q}_n$	Waveform 2	5.0 3.0	7.5 7.0	11.0 11.0	4.5 3.0	12.0 11.5	ns
t_{PLH} t_{PHL}	Propagation delay P_n to Q_n	Waveform 1	4.0 3.5	6.5 5.5	9.5 9.0	3.5 3.0	10.5 9.5	ns
t_{PLH} t_{PHL}	Propagation delay P_n to Q_n (INV)	Waveform 2	6.0 4.0	11.5 6.0	14.5 9.0	5.0 4.0	15.5 9.5	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}_n$ to Q_n	Waveform 3 Waveform 4	2.5 5.5	4.0 7.0	7.5 10.5	2.0 5.0	8.5 11.5	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}_n$ to Q_n	Waveform 3 Waveform 4	1.5 2.0	3.0 4.0	6.0 8.0	1.0 1.5	6.5 8.5	ns

AC WAVEFORMS



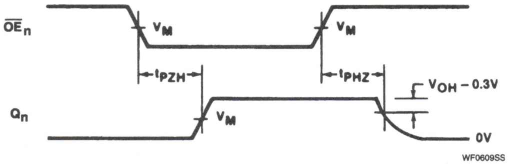
A_n, P, $\overline{E}_n$
V_M
V_M
t_{PLH}
t_{PHL}
Q_n
V_M
V_M
WF06060S

Waveform 1. Propagation Delay for Non-Inverting Outputs



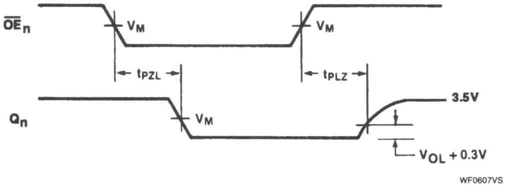
$\overline{E}$, $\overline{E}_0$, $\overline{E}_1$
V_M
V_M
t_{PHL}
t_{PLH}
Q_n
V_M
V_M
WF0754AS

Waveform 2. Propagation Delay for Inverting Outputs



$\overline{OE}_n$
V_M
V_M
t_{PZH}
t_{PHZ}
$V_{OH} - 0.3V$
Q_n
V_M
0V
WF0609SS

Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time From High Level

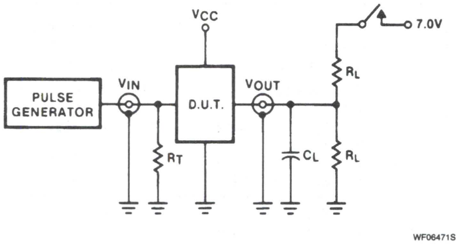


$\overline{OE}_n$
V_M
V_M
t_{PZL}
t_{PLZ}
3.5V
Q_n
V_M
$V_{OL} + 0.3V$
WF0607VS

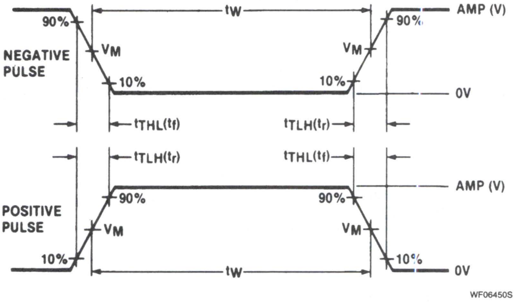
Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time From Low Level

NOTE: $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORM


VCC
7.0V
RL
PULSE GENERATOR
VIN
D.U.T.
VOUT
RT
CL
RL
WF06471S

Test Circuit for 3-State Outputs


NEGATIVE PULSE
90%
VM
10%
tW
AMP (V)
0V
tTHL(tf)
tTLH(tr)
POSITIVE PULSE
tTLH(tr)
tTHL(tf)
90%
VM
10%
WF06450S

$V_M = 1.5V$

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F540, 74F541
Buffers

'540 Octal Inverter Buffer (3-State)
'541 Octal Buffer (3-State)
Product Specification

FAST Products

FEATURES

- High-impedance npn base inputs for reduced loading (20μA in High and Low states)
- Low power, light bus loading
- Functionally similar to the 'F240 and 'F244
- Provides ideal interface and increases fanout of MOS Microprocessors
- Efficient pinout to facilitate PC board layout
- Octal bus interface
- 3-State buffer outputs sink 64mA
- 15mA source current

DESCRIPTION

The 'F540 and 'F541 are octal buffers that are ideal for driving bus lines or buffer memory address registers. The outputs are capable of sinking 64mA and sourcing up to 15mA, producing very good capacitive drive characteristics. The devices feature input and outputs on opposite sides of the package to facilitate printed circuit board layout.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F540	3.5ns	58mA
74F541	5.5ns	55mA

ORDERING INFORMATION

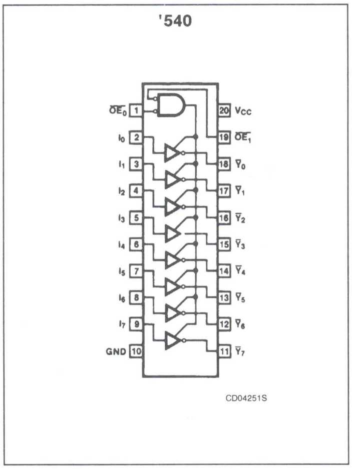
PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
20-Pin Plastic DIP	N74F540N, N74F541N
20-Pin Plastic SOL	N74F540D, N74F541D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

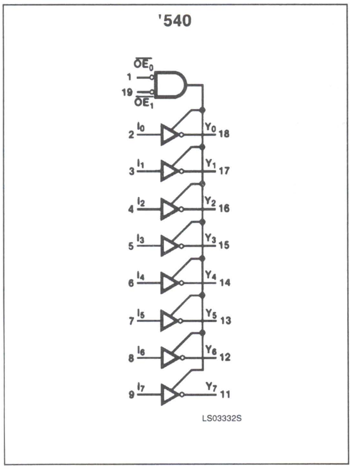
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$\overline{OE}_0$, $\overline{OE}_1$	3-State output enable inputs (active-Low)	1.0/0.033	20μA/20μA
$I_0 - I_7$	Data inputs	1.0/0.033	20μA/20μA
$\overline{Y}_0 - \overline{Y}_7$	Data outputs, 'F540	750/106.7	15mA/64mA
$Y_0 - Y_7$	Data outputs, 'F541		

NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

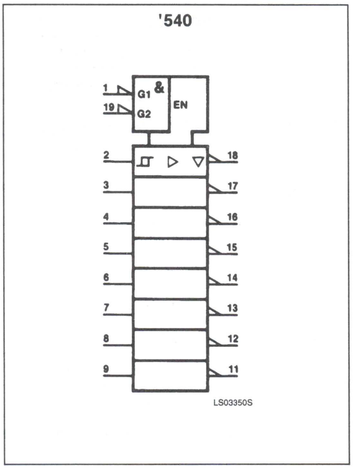
PIN CONFIGURATION


'540
$\overline{OE}_0$ 1
I_0 2
I_1 3
I_2 4
I_3 5
I_4 6
I_5 7
I_6 8
I_7 9
GND 10
20 V_{CC}
19 $\overline{OE}_1$
18 $\overline{Y}_0$
17 $\overline{Y}_1$
16 $\overline{Y}_2$
15 $\overline{Y}_3$
14 $\overline{Y}_4$
13 $\overline{Y}_5$
12 $\overline{Y}_6$
11 $\overline{Y}_7$
CD04251S

LOGIC SYMBOL


'540
$\overline{OE}_0$
1
19
$\overline{OE}_1$
2 I_0 Y_0 18
3 I_1 Y_1 17
4 I_2 Y_2 16
5 I_3 Y_3 15
6 I_4 Y_4 14
7 I_5 Y_5 13
8 I_6 Y_6 12
9 I_7 Y_7 11
LS03332S

LOGIC SYMBOL (IEEE/IEC)

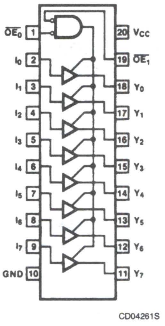

'540
1
19
G1
G2
&
EN
2
3
4
5
6
7
8
9
18
17
16
15
14
13
12
11
LS03350S

Buffers

FAST 74F540, 74F541

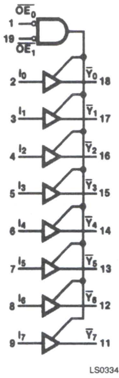
PIN CONFIGURATION

'541


$\overline{OE}_0$ 1
I_0 2
I_1 3
I_2 4
I_3 5
I_4 6
I_5 7
I_6 8
I_7 9
GND 10
20 V_{CC}
19 $\overline{OE}_1$
18 Y_0
17 Y_1
16 Y_2
15 Y_3
14 Y_4
13 Y_5
12 Y_6
11 Y_7
CD04261S

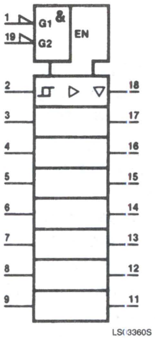
LOGIC SYMBOL

'541


$\overline{OE}_0$
1
19
$\overline{OE}_1$
2 I_0
$\overline{Y}_0$ 18
3 I_1
$\overline{Y}_1$ 17
4 I_2
$\overline{Y}_2$ 16
5 I_3
$\overline{Y}_3$ 15
6 I_4
$\overline{Y}_4$ 14
7 I_5
$\overline{Y}_5$ 13
8 I_6
$\overline{Y}_6$ 12
9 I_7
$\overline{Y}_7$ 11
LS03342S

LOGIC SYMBOL (IEEE/IEC)

'541


1
19
G1
G2
&
EN
2
3
4
5
6
7
8
9
18
17
16
15
14
13
12
11
LS03360S

FUNCTION TABLE

INPUTS			OUTPUTS	
$\overline{OE}_0$	$\overline{OE}_1$	I_n	Y_n	$\overline{Y}_n$
L	L	L	L	H
L	L	H	H	L
X	H	X	Z	Z
H	X	X	Z	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High-impedance (OFF) state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	128	mA
T_A	Operating free-air temperature range	0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−15	mA
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]			74F540, 74F541			UNIT
							Min	Typ[2]	Max	
V_{OH}	High-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = −3mA	±10%V_{CC}	2.4			V
						±5%V_{CC}	2.7	3.4		V
					I_{OH} = −15mA	±10%V_{CC}	2.0			V
						±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 48mA	±10%V_{CC}		0.35	.50	V
					I_{OL} = 64mA	±5%V_{CC}		0.40	.55	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, I_I = I_{IK}				−0.73	−1.2	V
I_I	Input current at maximum input voltage			V_{CC} = 0.0V, V_I = 7.0V					100	μA
I_{IH}	High-level input current			V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	Low-level input current			V_{CC} = MAX, V_I = 0.5V					−20	μA
I_{OZH}	OFF-state output current, High-level voltage applied			V_{CC} = MAX, V_O = 2.7V					50	μA
I_{OZL}	OFF-state output current, Low-level voltage applied			V_{CC} = MAX, V_O = 0.5V					−50	μA
I_{OS}	Short-circuit output current[3]			V_{CC} = MAX			−100		−225	mA
I_{CC}	Supply current (total)	I_{CCH}	'F540	V_{CC} = MAX	I_n = $\overline{OE}_n$ = GND			22	30	mA
		I_{CCL}			I_n = 4.5V, $\overline{OE}_n$ = GND			58	75	mA
		I_{CCZ}			I_n = GND, $\overline{OE}_n$ = 4.5V			40	55	mA
		I_{CCH}	'F541		I_n = 4.5V, $\overline{OE}_n$ = GND			30	40	mA
		I_{CCL}			I_n = $\overline{OE}_n$ = GND			55	72	mA
		I_{CCZ}			I_n = GND, $\overline{OE}_n$ = 4.5V			45	58	mA

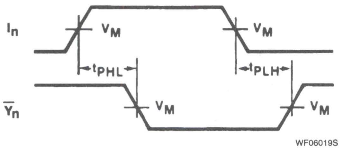
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

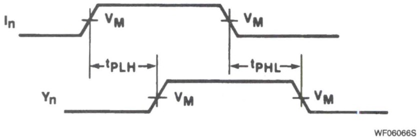
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	74F540, 75F541					UNIT
				T_A = +25°C V_{CC} = +5.0V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = +5.0V± 10% C_L = 50pF R_L = 500Ω		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_n to $\overline{Y}_n$	'F540	Waveform 1	3.0 1.5	4.5 2.5	6.5 4.5	2.5 1.5	7.5 5.0	ns
t_{PZH} t_{PZL}	Output enable time to High or Low		Waveform 3 Waveform 4	3.0 4.0	5.5 7.5	7.5 9.5	3.0 4.0	8.0 10.0	ns
t_{PHZ} t_{PLZ}	Output disable time from High or Low		Waveform 3 Waveform 4	2.0 2.0	4.0 4.0	6.0 5.5	2.0 2.0	6.5 6.0	ns
t_{PLH} t_{PHL}	Propagation delay I_n to Y_n	'F541	Waveform 2	2.5 3.5	5.0 6.0	6.5 7.0	2.5 3.0	7.0 7.5	ns
t_{PZH} t_{PZL}	Output enable time to High or Low		Waveform 3 Waveform 4	3.0 3.0	5.5 6.5	7.0 8.5	3.0 3.0	7.5 9.5	ns
t_{PHZ} t_{PLZ}	Output disable time from High or Low		Waveform 3 Waveform 4	2.0 2.0	4.0 4.0	7.0 7.0	2.0 2.0	7.5 7.5	ns

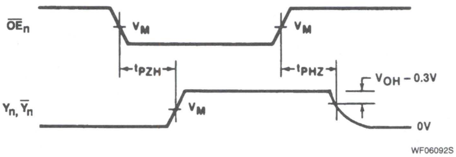
AC WAVEFORMS


In
VM
VM
tPHL
tPLH
Yn
VM
VM
WF06019S

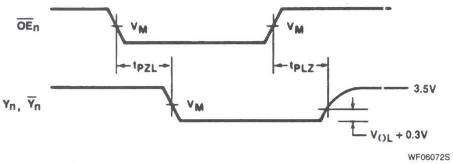
Waveform 1. Propagation Delay Data to Output for 'F540


In
VM
VM
tPLH
tPHL
Yn
VM
VM
WF06066S

Waveform 2. Propagation Delay Data to Output for 'F540


OEn
VM
VM
tPZH
tPHZ
VOH − 0.3V
Yn, Yn
VM
0V
WF06092S

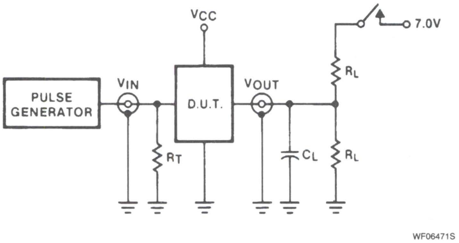
Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time From High Level


OEn
VM
VM
tPZL
tPLZ
3.5V
Yn, Yn
VM
VOL + 0.3V
WF06072S

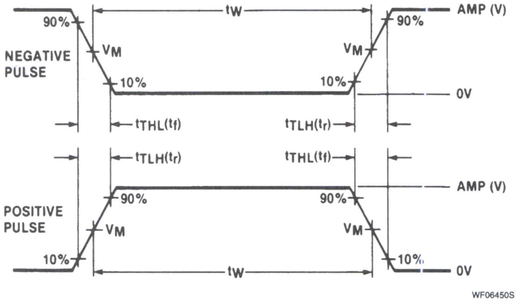
Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORM


VCC
7.0V
RL
PULSE GENERATOR
VIN
D.U.T.
VOUT
RT
CL
RL
WF06471S

Test Circuit for 3-State Outputs


90%
tW
AMP (V)
90%
NEGATIVE PULSE
VM
VM
10%
10%
0V
tTHL(tf)
tTLH(tr)
tTLH(tr)
tTHL(tf)
AMP (V)
90%
90%
POSITIVE PULSE
VM
VM
10%
10%
0V
tW
WF06450S

$V_M = 1.5V$

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor to GND; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Signetics

FAST 74F543, 74F544
Transceivers

Octal Registered Transceiver, Non-Inverting (3-State)
Octal Registered Transceiver, Inverting (3-State)
Product Specification

FAST Products

FEATURES

- **Combines F245 and F373 type functions in one chip**
- **8-bit Octal Transceiver with D type latch**
- **'F543 Non-Inverting**
  'F544 Inverting
- **Back-to-Back Registers for storage**
- **Separate controls for Data flow in each direction**
- **A outputs sink 24mA and source 15mA**
- **B outputs sink 64mA and source 3mA**
- **24-pin plastic Slim DIP (300mil) package**
- **3-State outputs for bus oriented applications**

DESCRIPTION

The 'F543 and 'F544 Octal Registered Transceivers contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate Latch Enable ($\overline{\text{LEAB}}$, $\overline{\text{LEBA}}$) and Enable ($\overline{\text{OEAB}}$, $\overline{\text{OEBA}}$) inputs are provided for each register to permit independent control of inputting and outputting in either direction of data flow. While the 'F543 has non-inverting data path, the 'F544 inverts data in both direction. The A outputs are guaranteed to sink 24mA while the B outputs are rated for 64mA.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F543	6.0ns	80mA
74F544	6.5ns	95mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
24-Pin Plastic Slim DIP	N74F543N, N74F544N
24-Pin Plastic SOL	N74F543D, N74F544D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$A_0 - A_7$ ('F543)	Port A, 3-State inputs	3.5/1.08	70μA/0.65mA
$B_0 - B_7$ ('F543)	Port B, 3-State inputs	3.5/1.08	70μA/0.65mA
$\overline{A}_0 - \overline{A}_7$ ('F544)	Port $\overline{A}$, 3-State inputs	3.5/1.08	70μA/0.65mA
$\overline{B}_0 - \overline{B}_7$ ('F544)	Port $\overline{B}$, 3-State inputs	3.5/1.08	70μA/0.65mA
$\overline{\text{OEAB}}$	A-to-B output enable input (active-Low)	1.0/1.0	20μA/0.6mA
$\overline{\text{OEBA}}$	B-to-A output enable input (active-Low)	1.0/1.0	20μA/0.6mA
$\overline{\text{EAB}}$	A-to-B enable input (active-Low)	1.0/2.0	20μA/1.2mA
$\overline{\text{EBA}}$	B-to-A enable input (active-Low)	1.0/2.0	20μA/1.2mA
$\overline{\text{LEAB}}$	A-to-B latch enable input (active-Low)	1.0/1.0	20μA/0.6mA
$\overline{\text{LEBA}}$	B-to-A latch enable input (active-Low)	1.0/1.0	20μA/0.6mA
$A_0 - A_7$ ('F543)	Port A, 3-State outputs	150/40	3.0mA/24mA
$B_0 - B_7$ ('F543)	Port B, 3-State outputs	750/106.7	15mA/64mA
$\overline{A}_0 - \overline{A}_7$ ('F544)	Port $\overline{A}$, 3-State outputs	150/40	3.0mA/24mA
$\overline{B}_0 - \overline{B}_7$ ('F544)	Port $\overline{B}$, 3-State outputs	750/106.7	15mA/64mA

NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

Transceivers FAST 74F543, 74F544

FUNCTIONAL DESCRIPTION

The 'F543 and 'F544 contains two sets of eight D-type latches, with separate input and controls for each set. For data flow from A to B, for example, the A-to-B Enable ($\overline{\text{EAB}}$) Input must be Low in order to enter data from $A_0 - A_7$ or take data from $B_0 - B_7$, as indicated in the Function Table. With $\overline{\text{EAB}}$ Low, a Low signal on the A-to-B Latch Enable ($\overline{\text{LEAB}}$) input makes the A-to-B latches transparent; a subsequent Low-to-High transition fof the $\overline{\text{LEAB}}$ signal puts the A latches in the storage mode and their outputs no longer change with the A inputs. With $\overline{\text{EAB}}$ and $\overline{\text{OEAB}}$ both Low, the 3-State B output buffers are active and reflects the data present at the output of the A latches. Control of data flow from B to A is similar, but using the $\overline{\text{EBA}}$, $\overline{\text{LEBA}}$, and $\overline{\text{OEBA}}$ inputs.

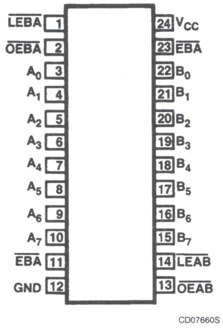
FUNCTION TABLE for 'F543 and 'F544

INPUTS				OUTPUTS		STATUS
$\overline{\text{OEXX}}$	$\overline{\text{EXX}}$	$\overline{\text{LEXX}}$	Data	'F543	'F544	
H	X	X	X	Z	Z	Outputs disabled
L	H	L	l	Z	Z	Outputs disabled
L	H	L	h	Z	Z	Data latched
L	L	H	l	L	H	Data latched
L	L	H	h	H	L	
L	L	L	L	L	H	Transparent
L	L	L	H	H	L	

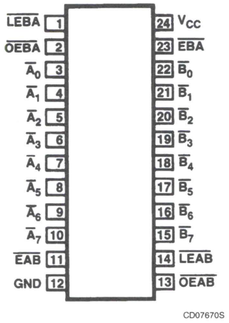
H = High voltage level
h = High state must be present one setup time before the Low-to-High transition of $\overline{\text{LEXX}}$ or $\overline{\text{EXX}}$ (XX = AB or BA)
L = Low voltage level
l = Low state must be present one setup time before the Low-to-High transition of $\overline{\text{LEXX}}$ or $\overline{\text{EXX}}$ (XX = AB or BA)
X = Don't care
Z = High-impedance state

PIN CONFIGURATION

'F543

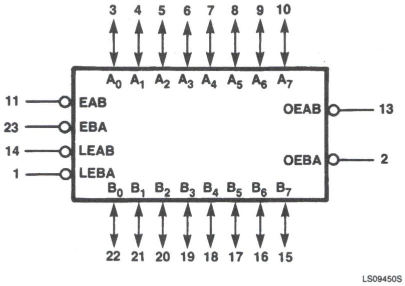

LEBA 1
OEBA 2
A0 3
A1 4
A2 5
A3 6
A4 7
A5 8
A6 9
A7 10
EBA 11
GND 12
24 VCC
23 EBA
22 B0
21 B1
20 B2
19 B3
18 B4
17 B5
16 B6
15 B7
14 LEAB
13 OEAB
CD07660S

'F544

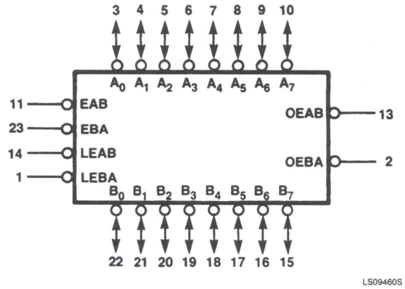

LEBA 1
OEBA 2
A0 3
A1 4
A2 5
A3 6
A4 7
A5 8
A6 9
A7 10
EAB 11
GND 12
24 VCC
23 EBA
22 B0
21 B1
20 B2
19 B3
18 B4
17 B5
16 B6
15 B7
14 LEAB
13 OEAB
CD07670S

LOGIC SYMBOL

'F543

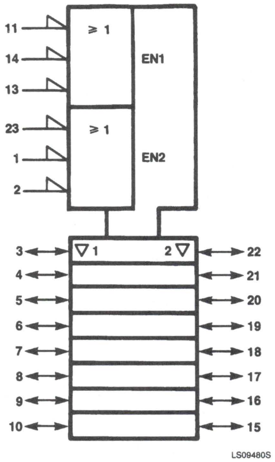

3 4 5 6 7 8 9 10
A0 A1 A2 A3 A4 A5 A6 A7
11 EAB
23 EBA
14 LEAB
1 LEBA
OEAB 13
OEBA 2
B0 B1 B2 B3 B4 B5 B6 B7
22 21 20 19 18 17 16 15
LS09450S

'F544

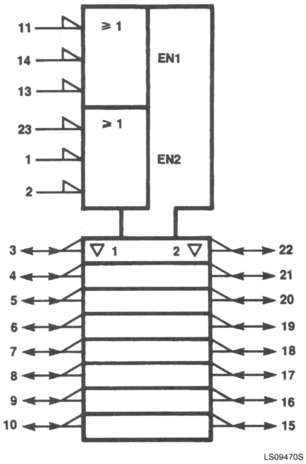

3 4 5 6 7 8 9 10
A0 A1 A2 A3 A4 A5 A6 A7
11 EAB
23 EBA
14 LEAB
1 LEBA
OEAB 13
OEBA 2
B0 B1 B2 B3 B4 B5 B6 B7
22 21 20 19 18 17 16 15
LS09460S

LOGIC SYMBOL (IEEE/IEC)

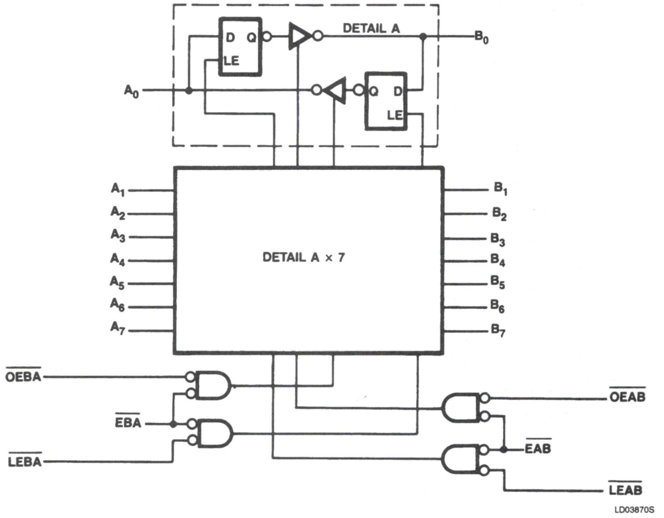
'F543


11
14
13
23
1
2
≥ 1
EN1
≥ 1
EN2
▽ 1
2 ▽
3
4
5
6
7
8
9
10
22
21
20
19
18
17
16
15
LS09480S

'F544

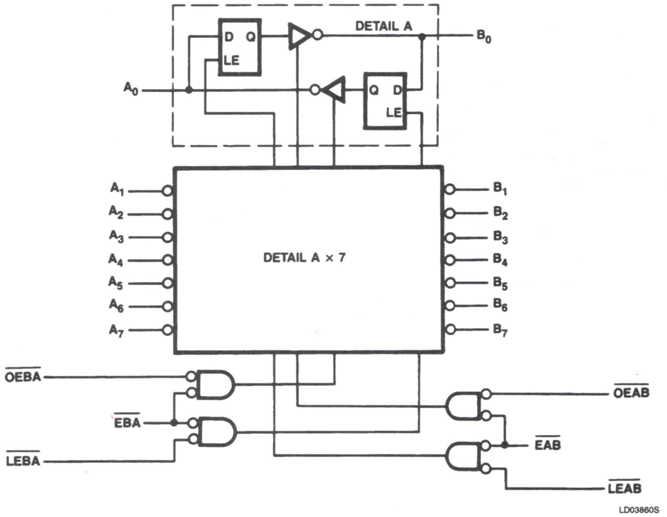

11
14
13
23
1
2
≥ 1
EN1
≥ 1
EN2
▽ 1
2 ▽
3
4
5
6
7
8
9
10
22
21
20
19
18
17
16
15
LS09470S

LOGIC DIAGRAM FOR 'F543


DETAIL A
D
Q
LE
B_0
A_0
Q
D
LE
A_1
A_2
A_3
A_4
A_5
A_6
A_7
DETAIL A × 7
B_1
B_2
B_3
B_4
B_5
B_6
B_7
$\overline{OEBA}$
$\overline{EBA}$
$\overline{LEBA}$
$\overline{OEAB}$
$\overline{EAB}$
$\overline{LEAB}$
LD03870S

NOTE:
Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

LOGIC DIAGRAM FOR 'F544


DETAIL A
D
Q
LE
B_0
A_0
Q
D
LE
A_1
A_2
A_3
A_4
A_5
A_6
A_7
DETAIL A × 7
B_1
B_2
B_3
B_4
B_5
B_6
B_7
$\overline{OEBA}$
$\overline{EBA}$
$\overline{LEBA}$
$\overline{OEAB}$
$\overline{EAB}$
$\overline{LEAB}$
LD03860S

NOTE:
Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		−0.5 to +7.0	V
V_{IN}	Input voltage		−0.5 to +7.0	V
I_{IN}	Input current		−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		−0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	$A_0 - A_7$, $\overline{A}_0 - \overline{A}_7$	48	mA
		$B_0 - B_7$, $\overline{B}_0 - \overline{B}_7$	128	mA
T_A	Operating free-air temperature range		0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.50	5.0	5.50	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	High-level output current	$A_0 - A_7$, $\overline{A}_0 - \overline{A}_7$			−3	mA
		$B_0 - B_7$, $\overline{B}_0 - \overline{B}_7$			−15	mA
I_{OL}	Low-level output current	$A_0 - A_7$, $\overline{A}_0 - \overline{A}_7$			24	mA
		$B_0 - B_7$, $\overline{B}_0 - \overline{B}_7$			64	mA
T_A	Operating free-air temperature		0		70	°C

Transceivers

FAST 74F543, 74F544

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]			LIMITS			UNIT
							Min	Typ[2]	Max	
V_{OH}	High-level output voltage	$A_0 - A_7$ $\overline{A}_0 - \overline{A}_7$		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	$I_{OH} = -3mA$	±10%V_{CC}	2.4			V
						±5%V_{CC}	2.7	3.4		V
		$B_0 - B_7$ $\overline{B}_0 - \overline{B}_7$			$I_{OH} = -15mA$	±10%V_{CC}	2.0			V
						±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage	$A_0 - A_7$ $\overline{A}_0 - \overline{A}_7$		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	$I_{OL} = 24mA$	±10%V_{CC}		0.35	0.50	V
						±5%V_{CC}		0.35	0.50	V
		$B_0 - B_7$ $\overline{B}_0 - \overline{B}_7$			$I_{OL} = 48mA$	±10%V_{CC}		0.40	0.55	V
					$I_{OL} = 64mA$	±5%V_{CC}		0.40	0.55	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, $I_I = I_{IK}$				-0.73	-1.2	V
I_I	Input current at maximum input voltage	$\overline{OEAB}$, $\overline{OEBA}$ $\overline{EAB}$, $\overline{EBA}$ $\overline{LEAB}$, $\overline{LEBA}$		V_{CC} = 0.0V, V_I = 7.0V					100	μA
		Others		V_{CC} = 5.5V, V_I = 5.5V					1	mA
I_{IH}	High-level input current			V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	Low-level input current	Others		V_{CC} = MAX, V_I = 0.5V					-0.6	mA
		$\overline{EAB}$, $\overline{EBA}$							-1.2	mA
I_{IH} + I_{OZH}	OFF-state current High-level voltage applied			V_{CC} = MAX, V_O = 2.7V					70	μA
I_{IL} + I_{OZL}	OFF-state current Low-level voltage applied			V_{CC} = MAX, V_O = 0.5V					-600	μA
I_{OS}	Short circuit output current[3]	$A_0 - A_7$, $\overline{A}_0 - \overline{A}_7$		V_{CC} = MAX			-60		-150	mA
		$B_0 - B_7$, $\overline{B}_0 - \overline{B}_7$					-100		-225	mA
I_{CC}	Supply current (total)	'F543	I_{CCH}	V_{CC} = MAX				70	105	mA
			I_{CCL}					95	135	mA
			I_{CCZ}					95	135	mA
I_{CC}	Supply current (total)	'F544	I_{CCH}	V_{CC} = MAX				80	110	mA
			I_{CCL}					105	140	mA
			I_{CCZ}					100	135	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of High-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Transceivers

FAST 74F543, 74F544

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F543					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n	Waveform 2	3.5 3.0	5.5 5.0	8.5 8.0	3.0 2.5	9.0 8.5	ns
t_{PLH} t_{PHL}	Propagation delay B_n to A_n	Waveform 2	2.0 2.5	4.0 4.5	7.0 7.5	1.5 2.5	7.5 8.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{\text{LEBA}}$ to A_n	Waveform 1, 2	5.0 4.0	7.0 6.0	10.0 9.0	4.5 4.0	11.0 9.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{\text{LEAB}}$ to B_n	Waveform 1, 2	6.0 4.5	8.5 6.5	11.5 9.5	5.5 4.0	12.5 10.0	ns
t_{PZH} t_{PZL}	Output enable time $\overline{\text{OEBA}}$ or $\overline{\text{OEAB}}$ to A_n or B_n	Waveform 4 Waveform 5	2.0 3.5	4.0 5.0	7.5 9.5	1.5 3.0	8.0 10.0	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{\text{OEBA}}$ or $\overline{\text{OEAB}}$ to A_n or B_n	Waveform 4 Waveform 5	1.0 1.5	3.0 4.0	6.5 7.5	1.0 1.0	7.5 8.5	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{\text{EBA}}$ or $\overline{\text{EAB}}$ to A_n or B_n	Waveform 4 Waveform 5	4.5 5.5	7.0 7.5	10.5 11.0	4.0 5.0	12.0 12.0	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{\text{EBA}}$ or $\overline{\text{EAB}}$ to A_n or B_n	Waveform 4 Waveform 5	2.5 4.5	5.0 7.0	8.5 11.0	2.0 3.0	9.5 12.0	ns

AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	74F543					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low A_n or B_n to $\overline{\text{LEAB}}$ or $\overline{\text{LEBA}}$ A_n or B_n to $\overline{\text{EAB}}$ or $\overline{\text{EBA}}$	Waveform 3	2.0 3.5			2.0 3.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low A_n or B_n to $\overline{\text{LEAB}}$ or $\overline{\text{LEBA}}$ A_n or B_n to $\overline{\text{EAB}}$ or $\overline{\text{EBA}}$	Waveform 3	1.0 2.0			1.0 2.0		ns
$t_w(L)$	Latch enable pulse width	Waveform 3	4.0			4.5		ns

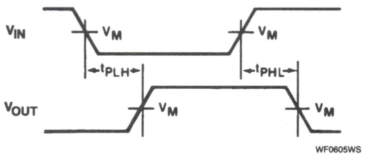
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F544					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n or $\overline{B}_n$ to $\overline{A}_n$	Waveform 1	3.0 3.0	6.5 5.0	9.5 8.0	3.0 3.0	10.5 8.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{\text{LEBA}}$ to $\overline{A}_n$	Waveform 1, 2	4.0 4.0	7.0 7.0	9.5 9.5	4.0 4.0	10.5 10.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{\text{LEAB}}$ to $\overline{B}_n$	Waveform 1, 2	5.0 4.0	8.0 7.5	11.5 9.5	4.0 4.0	12.5 10.5	ns
t_{PZH} t_{PZL}	Output enable time $\overline{\text{OEBA}}$ or $\overline{\text{OEAB}}$ to $\overline{A}_n$ or $\overline{B}_n$	Waveform 4 Waveform 5	3.0 4.0	5.0 7.0	8.0 10.0	2.5 4.0	8.5 10.5	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{\text{OEBA}}$ or $\overline{\text{OEAB}}$ to $\overline{A}_n$ or $\overline{B}_n$	Waveform 4 Waveform 5	1.0 2.5	4.0 5.5	6.5 8.5	1.0 2.5	7.0 9.0	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{\text{EBA}}$ or $\overline{\text{EAB}}$ to $\overline{A}_n$ or $\overline{B}_n$	Waveform 4 Waveform 5	4.0 4.5	7.0 8.0	9.5 11.0	4.0 4.5	10.5 12.0	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{\text{EBA}}$ or $\overline{\text{EAB}}$ to $\overline{A}_n$ or $\overline{B}_n$	Waveform 4 Waveform 5	2.5 4.5	5.0 8.5	8.0 11.5	2.5 4.5	9.0 12.5	ns

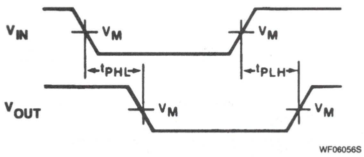
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	74F544					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low A_n or B_n to $\overline{\text{LEAB}}$ or $\overline{\text{LEBA}}$	Waveform 3	2.5 2.5			2.5 4.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low A_n or B_n to $\overline{\text{LEAB}}$ or $\overline{\text{LEBA}}$	Waveform 3	2.5 2.5			3.0 4.0		ns
$t_w(L)$	Pulse width latch enable	Waveform 3	4.0			4.5		ns

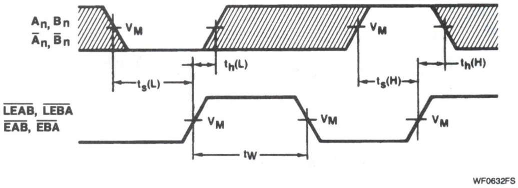
AC WAVEFORMS


V_{IN}
V_M
V_M
t_{PLH}
t_{PHL}
V_{OUT}
V_M
V_M
WF0605WS

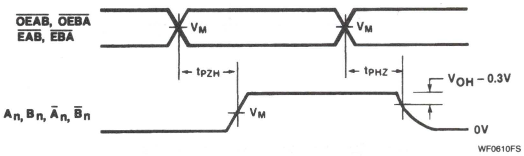
Waveform 1. Propagation Delay for Inverting Outputs


V_{IN}
V_M
V_M
t_{PHL}
t_{PLH}
V_{OUT}
V_M
V_M
WF06056S

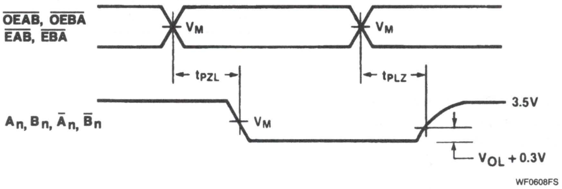
Waveform 2. Propagation Delay for Non-Inverting Outputs


A_n, B_n
$\overline{A}_n, \overline{B}_n$
V_M
V_M
$t_h(L)$
$t_h(H)$
$t_s(L)$
$t_s(H)$
$\overline{LEAB}, \overline{LEBA}$
$\overline{EAB}, \overline{EBA}$
V_M
V_M
V_M
tw
WF0632FS

Waveform 3. Data and Select Setup and Hold Times


$\overline{OEAB}, \overline{OEBA}$
$\overline{EAB}, \overline{EBA}$
V_M
V_M
t_{PZH}
t_{PHZ}
$V_{OH} - 0.3V$
$A_n, B_n, \overline{A}_n, \overline{B}_n$
V_M
0V
WF0610FS

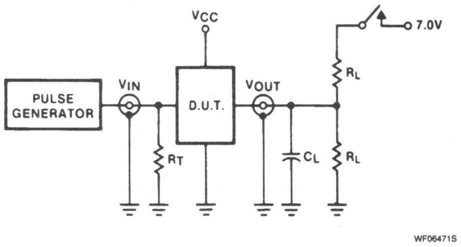
Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time From High Level


$\overline{OEAB}, \overline{OEBA}$
$\overline{EAB}, \overline{EBA}$
V_M
V_M
t_{PZL}
t_{PLZ}
3.5V
$A_n, B_n, \overline{A}_n, \overline{B}_n$
V_M
$V_{OL} + 0.3V$
WF0608FS

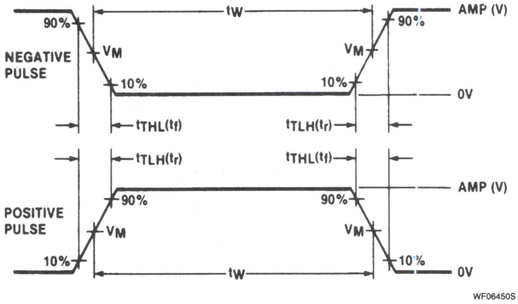
Waveform 5. 3-State Output Enable Time to Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to changed for predicatable output performance.

TEST CIRCUIT AND WAVEFORMS


VCC
7.0V
RL
PULSE GENERATOR
VIN
D.U.T.
VOUT
RT
CL
RL
WF06471S

Test Circuit for 3-State Outputs


tW
90%
AMP (V)
NEGATIVE PULSE
VM
VM
10%
10%
0V
tTHL(tf)
tTLH(tr)
tTLH(tr)
tTHL(tf)
AMP (V)
90%
90%
POSITIVE PULSE
VM
VM
10%
10%
0V
tW
WF06450S

$V_M = 1.5V$

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F545
Transceivers

Octal Bidirectional Transceiver
(With 3-State Inputs/Outputs)
Product Specification

FAST Products

FEATURES

- **High-impedance NPN base inputs for reduced loading (70μA in High and Low states)**
- **Higher drive than 8304**
- **8-bit bidirectional data flow reduces system package count**
- **3-State inputs/outputs for interfacing with bus-oriented systems**
- **20mA and 64mA bus drive capability on A and B ports, respectively**
- **Transmit/Receive and Output Enable simplify control logic**
- **Pin for pin replacement for Intel 8286**

DESCRIPTION

The 'F545 is an 8-bit, 3-State, high-speed transceiver. It provides bidirectional drive for bus-oriented microprocessor and digital communications systems. Straight through bidirectional transceivers are featured, with 20mA bus drive capability on the A ports and 64mA bus drive capability on the B ports.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F545	4.0ns	87mA

ORDERING INFORMATION

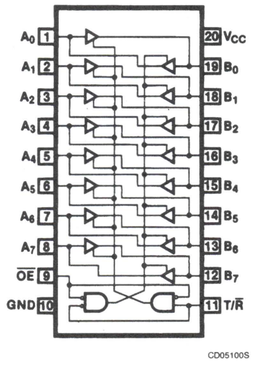
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F545N
20-Pin Plastic SOL	N74F545D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$A_0 - A_7$, $B_0 - B_7$	Data inputs	3.50/0.117	70μA/70μA
$\overline{OE}$	Output enable input (active-Low)	2.0/0.067	40μA/40μA
T/$\overline{R}$	Transmit/Receive input	2.0/0.067	40μA/40μA
$A_0 - A_7$	Port A 3-State outputs	150/40	3mA/24mA
$B_0 - B_7$	Port B 3-State outputs	750/107	15mA/64mA

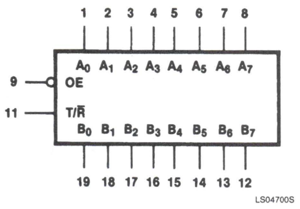
NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



A0 1
A1 2
A2 3
A3 4
A4 5
A5 6
A6 7
A7 8
OE 9
GND 10
20 VCC
19 B0
18 B1
17 B2
16 B3
15 B4
14 B5
13 B6
12 B7
11 T/R
CD05100S

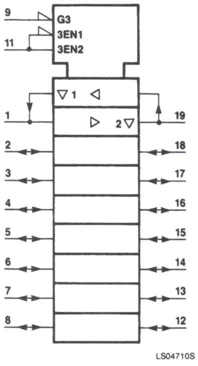
LOGIC SYMBOL



1 2 3 4 5 6 7 8
A0 A1 A2 A3 A4 A5 A6 A7
9
OE
11
T/R
B0 B1 B2 B3 B4 B5 B6 B7
19 18 17 16 15 14 13 12
LS04700S

V_{CC} = Pin 20
GND = Pin 10

LOGIC SYMBOL (IEEE/IEC)



9
11
G3
3EN1
3EN2
∇1 ◁
▷ 2∇
1
2
3
4
5
6
7
8
19
18
17
16
15
14
13
12
LS04710S

Transceivers

FAST 74F545

One input, Transmit/Receive (T/$\overline{R}$) determines the direction of logic signals through the bidirectional transceiver. Transmit enables data from A ports to B ports; Receive enables data from B ports to A ports. The Output Enable input disables both A and B ports by placing them in a 3-State condition.

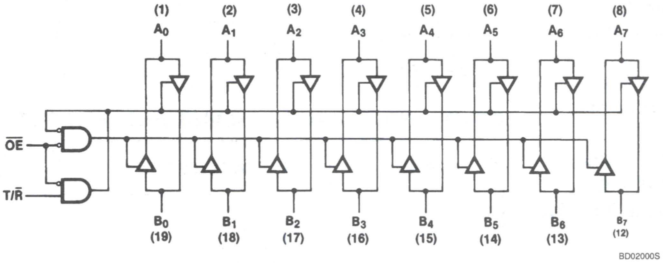
The 'F545 performs the same function as the 'F245, the only difference being package pin assignments.

FUNCTION TABLE

INPUTS		OUTPUTS
$\overline{OE}$	T/$\overline{R}$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	Hi Z

H = High voltage level
L = Low voltage level
X = Immaterial
Z = High-impedance

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		−0.5 to +7.0	V
V_{IN}	Input voltage		−0.5 to +7.0	V
I_{IN}	Input current		−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		−0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	$A_0 - A_7$	48	mA
		$B_0 - B_7$	128	mA
T_A	Operating free-air temperature range		0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	High-level output current	$A_0 - A_7$			−3	mA
		$B_0 - B_7$			−15	mA
I_{OL}	Low-level output current	$A_0 - A_7$			24	mA
		$B_0 - B_7$			64	mA
T_A	Operating free-air temperature		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			74F545			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage	$A_0 - A_7$ $B_0 - B_7$	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = -3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.4		V
		$B_0 - B_7$		I_{OH} = -15mA	±10%V_{CC}	2.0			V
					±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage	$A_0 - A_7$	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 24mA	±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
		$B_0 - B_7$		I_{OL} = 48mA	±10%V_{CC}		0.40	0.55	V
				I_{OL} = 64mA	±5%V_{CC}		0.40	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$				-0.73	-1.2	V
I_I	Input voltage at maximum input voltage	$A_0 - A_7$, $B_0 - B_7$	V_{CC} = 5.5V, V_I = 5.5V					1.0	mA
		$\overline{OE}$, T/$\overline{R}$	V_{CC} = 0.0V, V_I = 7.0V					100	μA
I_{IH}	High-level input current	$\overline{OE}$, T/$\overline{R}$ only	V_{CC} = MAX, V_I = 2.7V					40	μA
I_{IL}	Low-level input current	$\overline{OE}$, T/$\overline{R}$ only	V_{CC} = MAX, V_I = 0.5V					-40	μA
I_{OZH} + I_{IH}	Off-state current High-level voltage applied		V_{CC} = MAX, V_O = 2.7V					70	μA
I_{OZL} + I_{IH}	Off-state current Low-level voltage applied		V_{CC} = MAX, V_O = 0.5V					-70	μA
I_{OS}	Short-circuit output current[3]	$A_0 - A_7$	V_{CC} = MAX			-60		-150	mA
		$B_0 - B_7$				-100		-225	mA
I_{CC}	Supply current[4] (total)	I_{CCH}	V_{CC} = MAX	T/$\overline{R}$ = $A_0 - A_7$ = 4.5V; $\overline{OE}$ = GND			77	90	mA
		I_{CCL}		$\overline{OE}$ = T/$\overline{R}$ = $B_0 - B_7$ = GND			96	120	mA
		I_{CCZ}		$\overline{OE}$=4.5V; T/$\overline{R}$ = $B_0 - B_7$ = GND			89	110	mA

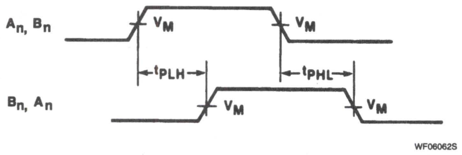
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Measure I_{CC} with outputs open.

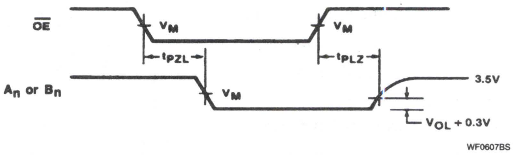
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F545					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n or B_n to A_n	Waveform 1 Waveform 1	1.5 2.5	3.5 4.5	5.5 6.5	1.5 2.5	6.5 7.0	ns
t_{PZH} t_{PZL}	Output enable time to High or Low level	Waveform 2 Waveform 3	6.0 5.5	8.5 8.0	10.5 9.5	6.0 5.5	11.0 10.0	ns
t_{PHZ} t_{PLZ}	Output disable time from High or Low level	Waveform 2 Waveform 3	2.5 2.0	5.0 4.5	7.0 6.5	2.5 2.0	8.0 7.5	ns

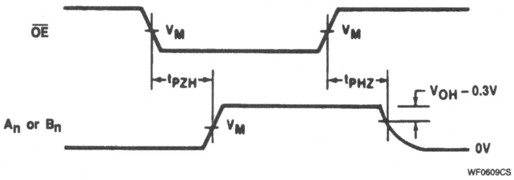
AC WAVEFORMS


An, Bn
VM
VM
tPLH
tPHL
Bn, An
VM
VM
WF06062S

Waveform 1. For Non-Inverting Outputs


OE
VM
VM
tPZL
tPLZ
An or Bn
VM
3.5V
VOL + 0.3V
WF0607BS

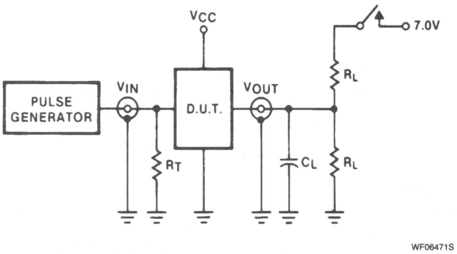
Waveform 2. 3-State Output Enable Time to High Level and Output Disable Time From High Level


OE
VM
VM
tPZH
tPHZ
VOH - 0.3V
An or Bn
VM
0V
WF0609CS

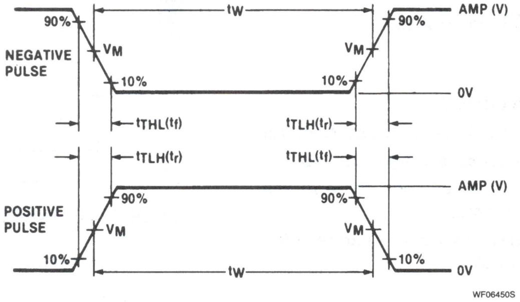
Waveform 3. 3-State Output Enable Time to Low Level and Output Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORMS


VCC
7.0V
RL
PULSE GENERATOR
VIN
D.U.T.
VOUT
RT
CL
RL
WF06471S

Test Circuit for 3-State Outputs


90%
tW
90%
AMP (V)
NEGATIVE PULSE
VM
VM
10%
10%
0V
tTHL(tf)
tTLH(tr)
tTLH(tr)
tTHL(tf)
AMP (V)
90%
90%
POSITIVE PULSE
VM
VM
10%
tW
10%
0V
WF06450S

$V_M = 1.5V$

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F547
Decoder/Demultiplexer

Octal Decoder/Demultiplexer With Address Latches And Acknowledge
Preliminary Specification

FAST Products

FEATURES

- **3- to 8-line address decoder**
- **Address storage latches**
- **Multiple enables for address extension**
- **Open-Collector Acknowledge output**

DESCRIPTION

The 'F547 is a 3- to 8-line address decoder with latches for address storage. Designed primarily to simplify multiple-chip selection in a microprocessor system, it contains one active-Low and two active-High Enables to conserve address space. Also included is an active-Low Acknowledge output that responds to either a Read or Write input signal when the Enables are active.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F547	8.0ns	17mA

ORDERING INFORMATION

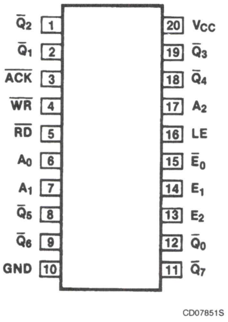
PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
20-Pin Plastic DIP	N74F547N
20-Pin Plastic SOL	N74F547D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$A_0 - A_2$	Output select address input	1.0/1.0	20μA/0.6mA
$\overline{E}_0$	Chip enable input (active-Low)	1.0/1.0	20μA/0.6mA
E_1, E_2	Chip enable inputs	1.0/1.0	20μA/0.6mA
LE	Latch enable input	1.0/1.0	20μA/0.6mA
$\overline{RD}$	Read acknowledge input (active-Low)	1.0/1.0	20μA/0.6mA
$\overline{WR}$	Write acknowledge input (active-Low)	1.0/1.0	20μA/0.6mA
$\overline{Q}_0 - \overline{Q}_7$	Decoder outputs (active-Low)	50/33.3	1mA/20mA
$\overline{ACK}$	Open-Collector acknowledge output (active-Low)	OC*/33.3	OC*/20mA

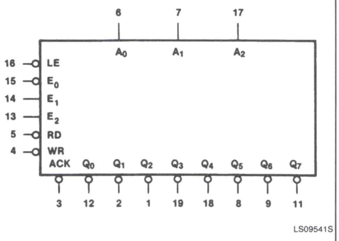
NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.
2. *OC = Open-Collector.

PIN CONFIGURATION



Q̄2 1
Q̄1 2
ACK 3
WR 4
RD 5
A0 6
A1 7
Q̄5 8
Q̄6 9
GND 10
20 VCC
19 Q̄3
18 Q̄4
17 A2
16 LE
15 Ē0
14 E1
13 E2
12 Q̄0
11 Q̄7
CD07851S

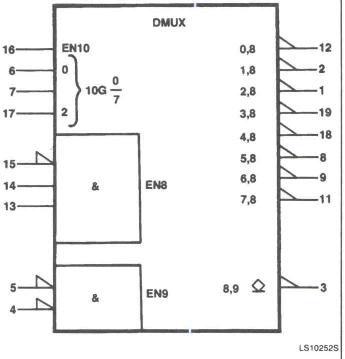
LOGIC SYMBOL



6
7
17
A0
A1
A2
16 LE
15 E0
14 E1
13 E2
5 RD
4 WR
ACK
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
3
12
2
1
19
18
8
9
11
LS09541S

V_{CC} = Pin 20
GND = Pin 10

LOGIC SYMBOL (IEEE/IEC)



DMUX
16
6
7
17
EN10
0
2
10G 0/7
15
14
13
&
EN8
5
4
&
EN9
0,8
1,8
2,8
3,8
4,8
5,8
6,8
7,8
8,9
12
2
1
19
18
8
9
11
3
LS10252S

Decoder/Demultiplexer FAST 74F547

For applications in which the separation of latch enable and chip enable functions is not required, LE and $\overline{E}_1$ can be tied together such that when High the outputs are OFF and the latches are transparent, and when Low the latches are storing and the selected output is enabled.

The Open-Collector Acknowledge ($\overline{ACK}$) output is normally High (i.e. OFF) and goes Low when $\overline{E}_0$, E_1 and E_2 are all active and either the READ ($\overline{RD}$) or Write ($\overline{WR}$) input is Low, as indicated in the Acknowledge Function Table.

FUNCTION TABLE (Decoder*)

INPUTS						OUTPUTS							
$\overline{E}_0$	E_1	E_2	A_2	A_1	A_0	$\overline{Q}_0$	$\overline{Q}_1$	$\overline{Q}_2$	$\overline{Q}_3$	$\overline{Q}_4$	$\overline{Q}_5$	$\overline{Q}_6$	$\overline{Q}_7$
L	H	H	L	L	L	L	H	H	H	H	H	H	H
L	H	H	L	L	H	H	L	H	H	H	H	H	H
L	H	H	L	H	L	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	H	H	L	H	H	H	H
L	H	H	H	L	L	H	H	H	H	L	H	H	H
L	H	H	H	L	H	H	H	H	H	H	L	H	H
L	H	H	H	H	L	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L

* Assuming $\overline{E}_1$ = Low and $E_2 = E_3$ = High

FUNCTION TABLE (Acknowledge)

INPUTS					OUTPUT
$\overline{E}_0$	E_1	E_2	$\overline{RD}$	$\overline{WR}$	$\overline{ACK}$
H	X	X	X	X	H
X	L	X	X	X	H
X	X	L	X	X	H
L	H	H	H	H	H
L	H	H	L	X	L
L	H	H	X	L	L

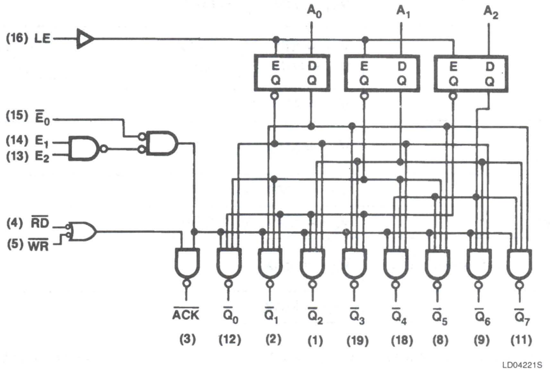
H = High voltage level
L = Low voltage level
X = Don't care

FUNCTION TABLE (Latch and Output Status)

INPUTS				LATCH STATUS	DECODER OUTPUTS
$\overline{E}_0$	E_1	E_2	LE		
L	H	H	H	Transparent	Address inputs decoded
L	H	H	↓	Storing	Latched address decoded
L	X	X	X	Storing hold	No Change
H	X	X	X	Transparent	Outputs disabled
X	L	X	X	Storing	
X	X	L	H	Transparent	

H = High voltage level
L = Low voltage level
X = Don't care
↓ = High to Low transition. A_n data must be stable one setup time before transition.

LOGIC DIAGRAM



V_{CC} = Pin 20
GND = Pin 10
( ) = Pin numbers

Decoder/Demultiplexer | FAST 74F547

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
V_{OH}	High-level output voltage	$\overline{ACK}$ only			4.5	V
I_{OH}	High-level output current	Except $\overline{ACK}$			−1	mA
I_{OL}	Low-level output current				20	mA
T_A	Operating free-air temperature		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		74F547			UNIT
					Min	Typ[2]	Max	
I_{OH}	High-level output current	$\overline{ACK}$ only	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, V_{OH} = MAX				250	μA
V_{OH}	High-level output voltage	Except $\overline{ACK}$	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				−0.6	mA
I_{OS}	Short-circuit output current[3]	Except $\overline{ACK}$	V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current (total)		V_{CC} = MAX			17	25	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

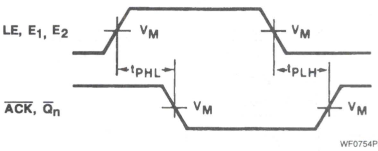
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F547					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH}	Propagation delay A_n to $\overline{Q}_n$	Waveform 3	2.0	4.5	9.0	1.5	10.0	ns
t_{PHL}			4.5	7.0	12.0	4.0	13.0	ns
t_{PLH}	Propagation delay $\overline{E}_1$ to $\overline{Q}_n$	Waveform 2	2.5	4.5	8.5	2.0	9.5	ns
t_{PHL}			3.0	5.5	8.5	3.0	9.5	ns
t_{PLH}	Propagation delay LE to $\overline{Q}_n$	Waveform 1	3.5	6.0	10.0	3.0	11.0	ns
t_{PHL}			5.0	10.5	14.0	5.0	15.0	ns
t_{PLH}	Propagation delay E_2 or E_3 to $\overline{Q}_n$	Waveform 1	4.0	6.0	10.0	3.0	11.0	ns
t_{PHL}			4.0	6.0	10.0	4.0	11.0	ns
t_{PLH}	Propagation delay $\overline{E}_1$, $\overline{RD}$, or $\overline{WR}$ to $\overline{ACK}$	Waveform 2	6.5	9.0	13.0	6.5	14.0	ns
t_{PHL}			3.5	5.5	9.5	3.0	10.5	ns
t_{PLH}	Propagation delay E_2 or E_3 to $\overline{ACK}$	Waveform 1	7.5	11.0	14.0	7.0	15.0	ns
t_{PHL}			4.5	6.5	10.0	4.0	11.0	ns

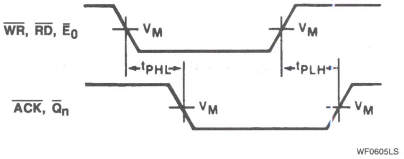
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	74F547					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$	Setup time, High or Low A_n to LE	Waveform 3	5.0			5.0		ns
$t_s(L)$			5.0			5.0		ns
$t_h(H)$	Hold time, High or Low A_n to LE	Waveform 3	6.0			6.0		ns
$t_h(L)$			6.0			6.0		ns
$t_w(H)$	LE pulse width, High	Waveform 2	6.0			6.0		ns

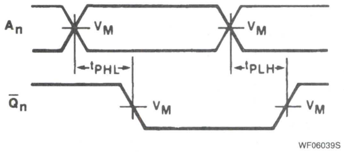
AC WAVEFORMS


LE, E_1, E_2
V_M
V_M
t_{PHL}
t_{PLH}
$\overline{ACK}$, $\overline{Q}_n$
V_M
V_M
WF0754PS

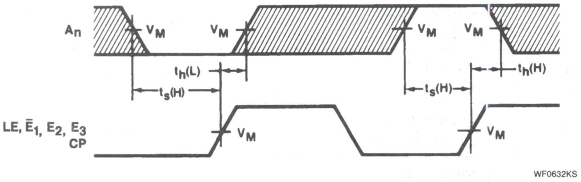
Waveform 1. Propagation Delay for Chip Enable Inputs (E_2, E_3) and Latch Enable Input (LE) to Write Acknowledge ($\overline{ACK}$) and Decoder ($\overline{Q}_n$) Outputs


$\overline{WR}$, $\overline{RD}$, $\overline{E}_0$
V_M
V_M
t_{PHL}
t_{PLH}
$\overline{ACK}$, $\overline{Q}_n$
V_M
V_M
WF0605LS

Waveform 2. Propagation Delay for Chip Enable Input (E_1) to Decoder Outputs ($\overline{Q}_n$) and Write Acknowledge Inputs ($\overline{WR}$, $\overline{RD}$) to Acknowledge Output ($\overline{ACK}$)


A_n
V_M
V_M
t_{PHL}
t_{PLH}
$\overline{Q}_n$
V_M
V_M
WF06039S

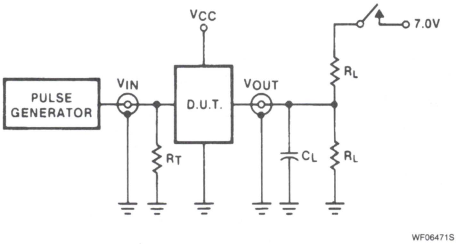
Waveform 3. Propagation Delay for Output Select Address Input (A_n) to Decoder Outputs ($\overline{Q}_n$)


A_n
V_M
V_M
V_M
V_M
$t_h(L)$
$t_s(H)$
$t_s(H)$
$t_h(H)$
LE, $\overline{E}_1$, E_2, E_3
CP
V_M
V_M
WF0632KS

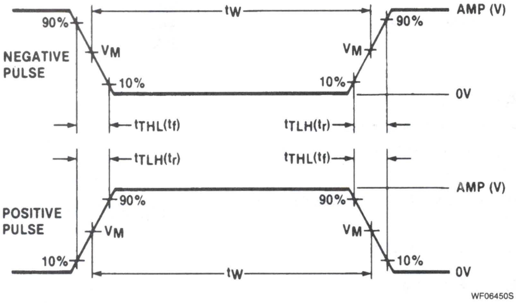
Waveform 4. Data Setup and Hold Times for Output Select Address Inputs (A_n) to Latch Enable Inputs (LE) and Chip Enable Inputs ($\overline{E}_1$, E_2, E_3)

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable performance.

TEST CIRCUIT AND WAVEFORMS


VCC
7.0V
RL
PULSE GENERATOR
VIN
D.U.T.
VOUT
RT
CL
RL
WF06471S

Test Circuit for Open-Collector and Totem-Pole Outputs


NEGATIVE PULSE
90%
VM
10%
tW
AMP (V)
0V
tTHL(tf)
tTLH(tr)
POSITIVE PULSE
tTLH(tr)
tTHL(tf)
90%
VM
10%
tW
AMP (V)
0V
WF06450S

$V_M = 1.5V$

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
Open-Collector others	closed open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F548
Decoder/Demultiplexer

Octal Decoder/Demultiplexer with Acknowledge
Product Specification

FAST Products

FEATURES

- **3- to 8-line address decoder**
- **Multiple enables for address extension**
- **Open-Collector Acknowledge output**
- **Active-Low Decoder outputs**

DESCRIPTION

The 'F548 is a 3- to 8-line address decoder with four Enable inputs. Two of the Enables are active-Low and two are active-High for maximum addressing versatility. Also provided is an active-Low Acknowledge output that responds to either a Read or Write input signal when the Enables are active.

When enabled, the 'F548 accepts the $A_0 - A_2$ address inputs and decodes them to select one of eight active-Low mutually exclusive outputs, as shown in the Decoder Function Table. When one or more Enables is active, all decoder outputs are High. Thus, the 'F548 can be used as a demultiplexer by applying data to one of the Enables.

The Open-Collector Acknowledge ($\overline{ACK}$) output is normally High (i.e. OFF) and goes Low when the Enables are all active and either the READ ($\overline{RD}$) or Write ($\overline{WR}$) input is Low, as indicated in the Acknowledge Function Table.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F548	6.5ns	14mA

ORDERING INFORMATION

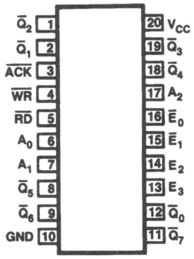
PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
20-Pin Plastic DIP	N74F548N
20-Pin Plastic SOL	N74F548D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$A_0 - A_2$	Output select address inputs	1.0/1.0	20μA/0.6mA
$\overline{E}_0$, $\overline{E}_1$	Chip enable inputs (active-Low)	1.0/1.0	20μA/0.6mA
E_2, E_3	Chip enable inputs	1.0/1.0	20μA/0.6mA
$\overline{RD}$	Read acknowledge input (active-Low)	1.0/1.0	20μA/0.6mA
$\overline{WR}$	Write acknowledge input (active-Low)	1.0/1.0	20μA/0.6mA
$\overline{Q}_0 - \overline{Q}_7$	Decoder outputs (active-Low)	50/33	1mA/20mA
ACK	Open-collector acknowledge output (active-Low)	OC*/33	OC*/20mA

NOTES:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.
2. *OC = Open-Collector.

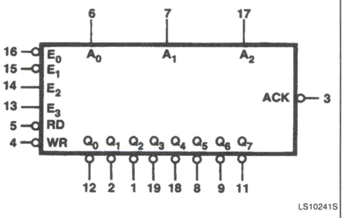
PIN CONFIGURATION



$\overline{Q}_2$ 1
$\overline{Q}_1$ 2
$\overline{ACK}$ 3
$\overline{WR}$ 4
$\overline{RD}$ 5
A_0 6
A_1 7
$\overline{Q}_5$ 8
$\overline{Q}_6$ 9
GND 10
20 V_{CC}
19 $\overline{Q}_3$
18 $\overline{Q}_4$
17 A_2
16 $\overline{E}_0$
15 $\overline{E}_1$
14 E_2
13 E_3
12 $\overline{Q}_0$
11 $\overline{Q}_7$

CD08221S

LOGIC SYMBOL

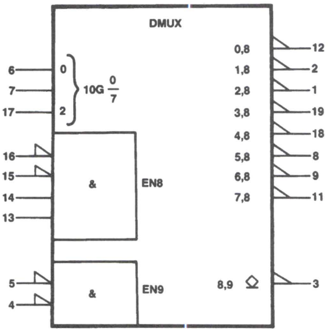


6
7
17
A_0
A_1
A_2
16 E_0
15 E_1
14 E_2
13 E_3
5 RD
4 WR
ACK 3
Q_0 Q_1 Q_2 Q_3 Q_4 Q_5 Q_6 Q_7
12 2 1 19 18 8 9 11

LS10241S

V_{CC} = Pin 20
GND = Pin 10

LOGIC SYMBOL (IEEE/IEC)

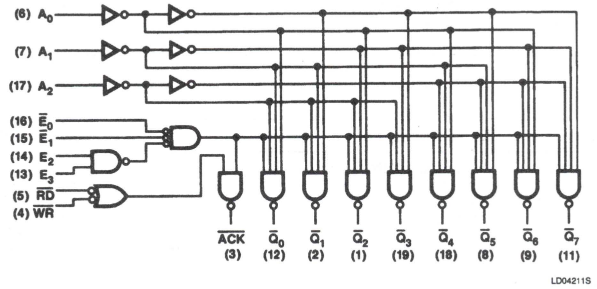


DMUX
6 0
7
17 2
10G $\frac{0}{7}$
16
15
14
13
&
EN8
5
4
&
EN9
0,8 12
1,8 2
2,8 1
3,8 19
4,8 18
5,8 8
6,8 9
7,8 11
8,9 3

LS10231S

Decoder/Demultiplexer FAST 74F548

LOGIC DIAGRAM


(6) A_0
(7) A_1
(17) A_2
(16) $\overline{E}_0$
(15) $\overline{E}_1$
(14) E_2
(13) E_3
(5) $\overline{RD}$
(4) $\overline{WR}$
$\overline{ACK}$ (3)
$\overline{Q}_0$ (12)
$\overline{Q}_1$ (2)
$\overline{Q}_2$ (1)
$\overline{Q}_3$ (19)
$\overline{Q}_4$ (18)
$\overline{Q}_5$ (8)
$\overline{Q}_6$ (9)
$\overline{Q}_7$ (11)
LD04211S

V_{CC} = Pin 20
GND = Pin 10
( ) = Pin numbers

FUNCTION TABLE (Decoder)

INPUTS							OUTPUTS							
$\overline{E}_0$	$\overline{E}_1$	E_2	E_3	A_2	A_1	A_0	$\overline{Q}_0$	$\overline{Q}_1$	$\overline{Q}_2$	$\overline{Q}_3$	$\overline{Q}_4$	$\overline{Q}_5$	$\overline{Q}_6$	$\overline{Q}_7$
H	X	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	X	H	H	H	H	H	H	H	H
X	X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	H	L	H	H	H	H	H	H
L	L	H	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	L	H	H	H	H	H	L	H	H	H	H
L	L	H	H	H	L	L	H	H	H	H	L	H	H	H
L	L	H	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	H	H	H	L	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	L

H = High voltage level
L = Low voltage level
X = Don't care

FUNCTION TABLE (Acknowledge)

INPUTS						OUTPUT
$\overline{E}_0$	$\overline{E}_1$	E_2	E_3	$\overline{RD}$	$\overline{WR}$	$\overline{ACK}$
H	X	X	X	X	X	H
X	H	X	X	X	X	H
X	X	L	X	X	X	H
X	X	X	L	X	X	H
L	L	H	H	H	H	H
L	L	H	H	L	X	L
L	L	H	H	X	L	L

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
V_{OH}	High-level output voltage	$\overline{ACK}$ only			4.5	V
I_{OH}	High-level output current	Except $\overline{ACK}$			−1	mA
I_{OL}	Low-level output current				20	mA
T_A	Operating free-air temperature		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
I_{OH}	High-level output current	$\overline{ACK}$ only	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, V_{OH} = MAX				250	μA
V_{OH}	High-level output voltage	Except $\overline{ACK}$	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				−0.6	mA
I_{OS}	Short-circuit output current[3]	Except $\overline{ACK}$	V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current (total)		V_{CC} = MAX			14	21	mA

NOTES:

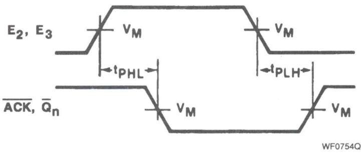
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Decoder/Demultiplexer FAST 74F548

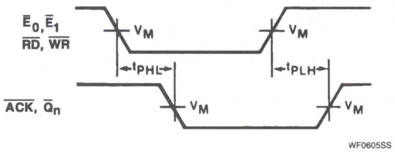
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F548					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to $\overline{Q}_n$	Waveform 3	2.0 4.0	4.5 6.5	8.0 9.5	1.5 4.0	9.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}_0$ or $\overline{E}_1$ to $\overline{Q}_n$	Waveform 2	2.5 3.5	4.5 5.5	8.5 8.5	2.0 3.0	9.5 9.5	ns
t_{PLH} t_{PHL}	Propagation delay E_2 or E_3 to $\overline{Q}_n$	Waveform 1	4.0 4.0	6.0 6.0	9.5 9.5	3.0 3.5	10.5 10.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}_0$ or $\overline{E}_1$ to $\overline{ACK}$	Waveform 1	6.5 3.0	9.5 6.0	12.5 9.5	6.5 3.0	13.0 10.5	ns
t_{PLH} t_{PHL}	Propagation delay E_2 or E_3 to $\overline{ACK}$	Waveform 1	8.0 4.0	11.0 7.0	14.0 10.0	8.0 4.0	15.0 11.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{RD}$ or $\overline{WR}$ to $\overline{ACK}$	Waveform 2	5.5 2.5	9.0 5.0	12.0 8.0	5.5 2.5	12.5 8.5	ns

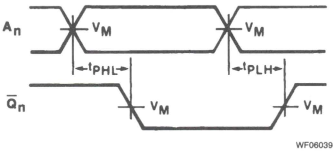
AC WAVEFORMS



Waveform 1. Propagation Delay for Chip Enable Inputs (E_3, E_4) to Write Acknowledge ($\overline{ACK}$) and Decoder (Q_n) Outputs



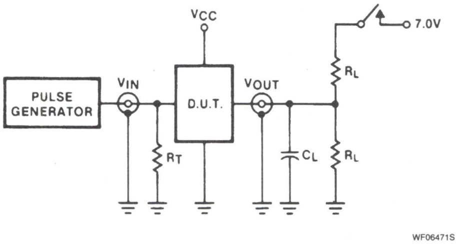
Waveform 2. Propagation Delay for Chip Enable Inputs ($\overline{E}_1$, $\overline{E}_2$) to Decoder Outputs ($\overline{Q}_n$) and Write Acknowledge Output ($\overline{ACK}$)



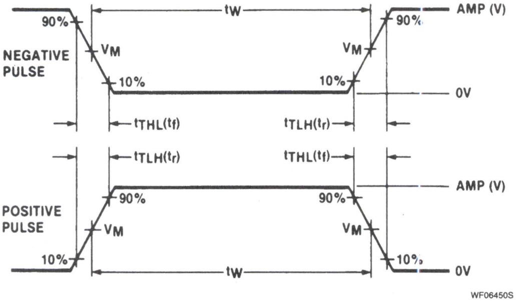
Waveform 3. Propagation Delays for Output Select Address Input (A_n) to Decoder Outputs ($\overline{Q}_n$)

NOTE: For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORMS


VCC
7.0V
RL
PULSE GENERATOR
VIN
D.U.T.
VOUT
RT
CL
RL
WF06471S

Test Circuit for Open-Collector and Totem-Pole Outputs


90%
tW
90%
AMP (V)
NEGATIVE PULSE
VM
VM
10%
10%
0V
tTHL(tf)
tTLH(tr)
tTLH(tr)
tTHL(tf)
AMP (V)
90%
90%
POSITIVE PULSE
VM
VM
10%
10%
0V
tW
WF06450S

$V_M = 1.5V$

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
Open-Collector	closed
Totem-pole	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F550, 74F551

FAST Products

'F550 Octal Registered Transceiver With Status Flags, Non-Inverting
'F551 Octal Registered Transceiver With Status Flags, Inverting

Preliminary Specification

FEATURES

- **8-bit bidirectional I/O port with handshake**
- **Back-to-back registers for storage**
- **Register status flag flip-flops**
- **Separate edge-detecting clears for flags**
- **'F550 non-inverting 'F551 inverting**
- **B outputs sink 64mA**

DESCRIPTION

The 'F550 and 'F551 octal transceivers contain two 8-bit registers for temporary storage of data flowing in either direction. Each register has its own Clock (CPA, CPB) and Clock Enable ($\overline{CEA}$, $\overline{CEB}$) inputs as well as a flag flip-flop that is set automatically as the register is loaded. Each flag flip-flop is provided with a clear input, and each register has a separate Output Enable ($\overline{OEA}$, $\overline{OEB}$) for its 3-State buffers. The separate Clocks, Flags and Enables provide considerable flexibility as I/O ports for demand-response data transfer. The 'F550 is non-inverting; the 'F551 inverts data in both directions.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F550	6.3ns	130mA
74F551	6.3ns	130mA

ORDERING INFORMATION

PACKAGE	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
28-Pin Plastic DIP	N74F550N, N74F551N
28-Pin Plastic SOL	N74F550D, N74F551D

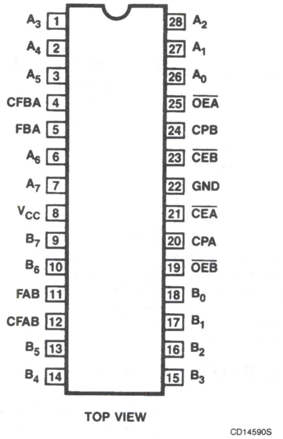
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$A_0 - A_7$	A-to-B Data inputs	3.5/1.0	70μA/0.6mA
$B_0 - B_7$	B-to-A Data inputs	3.5/1.0	70μA/0.6mA
CPA	A-to-B Clock input (active rising edge)	1.0/1.0	20μA/0.6mA
CPB	B-to-A Clock input (active rising edge)	1.0/1.0	20μA/0.6mA
$\overline{CEA}$	A-to-B Clock Enable input (active-Low)	1.0/1.0	20μA/0.6mA
$\overline{CEB}$	B-to-A Clock Enable input (active-Low)	1.0/1.0	20μA/0.6mA
$\overline{OEA}$	A-to-B Output Enable input (active-Low)	1.0/1.0	20μA/0.6mA
$\overline{OEB}$	B-to-A Output Enable input (active-Low)	1.0/1.0	20μA/0.6mA
CFAB	A-to-B Flag Clear input (active rising edge)	1.0/1.33	20μA/0.8mA
CFBA	B-to-A Flag Clear input (active rising edge)	1.0/1.33	20μA/0.8mA
$A_0 - A_7$	A-to-B Data outputs	150/40	3mA/24mA
$B_0 - B_7$	B-to-A Data outputs	150/40	3mA/24mA
FAB	A-to-B Status Flag output (active-High)	50/33.3	1mA/20mA
FBA	B-to-A Output Enable input (active-High)	50/33.3	1mA/20mA

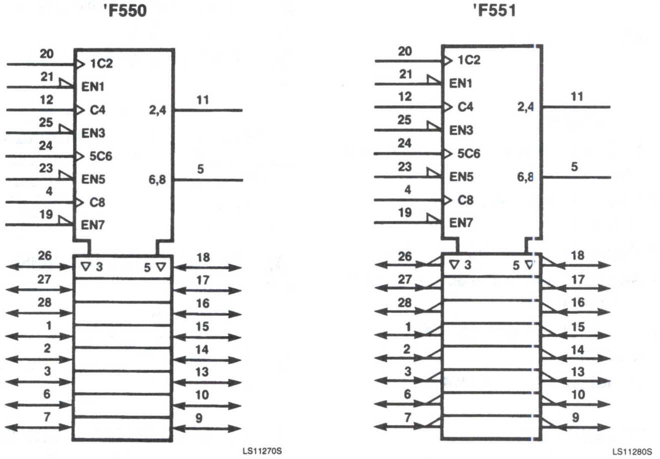
NOTE:

1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

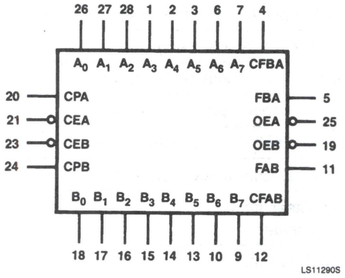
PIN CONFIGURATION


A3 1
A4 2
A5 3
CFBA 4
FBA 5
A6 6
A7 7
VCC 8
B7 9
B6 10
FAB 11
CFAB 12
B5 13
B4 14
28 A2
27 A1
26 A0
25 OEA
24 CPB
23 CEB
22 GND
21 CEA
20 CPA
19 OEB
18 B0
17 B1
16 B2
15 B3
TOP VIEW
CD14590S

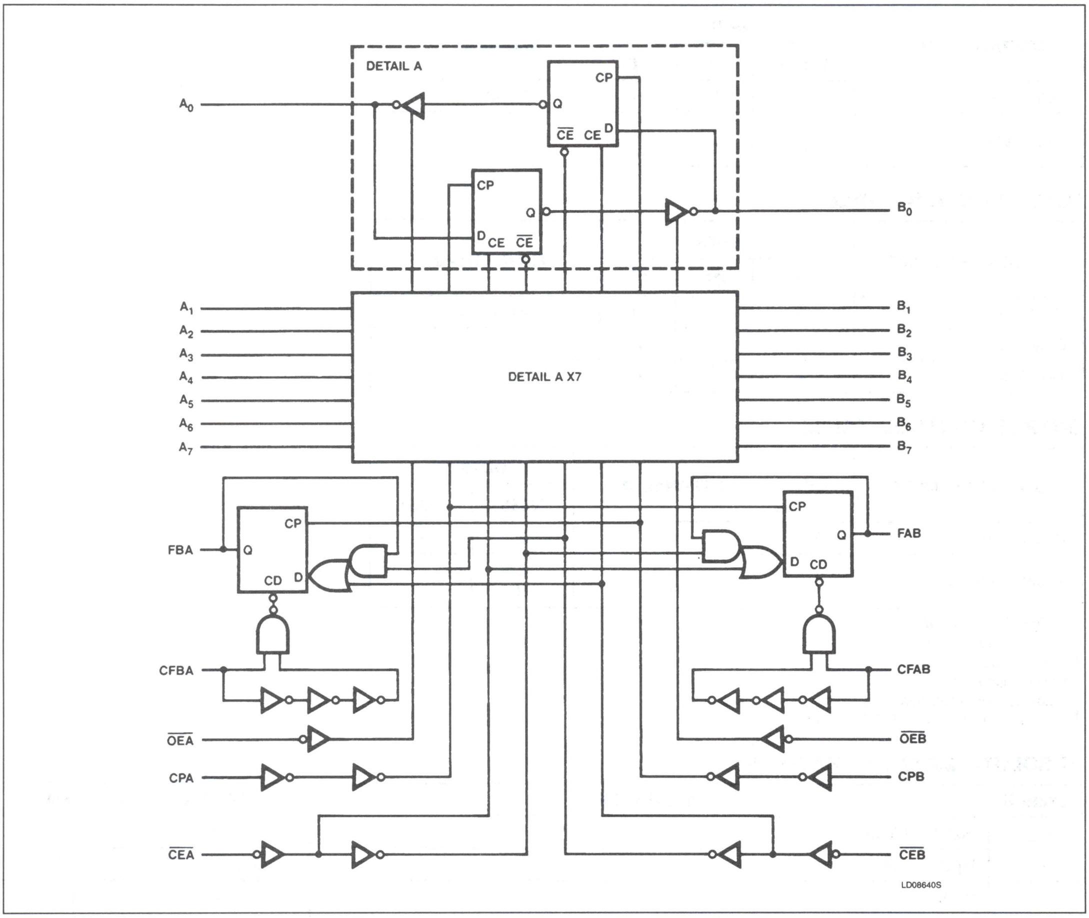
SYMBOL (IEEE/IEC)


'F550
'F551
1C2
EN1
C4
EN3
5C6
EN5
C8
EN7
2,4
6,8
▽ 3
5 ▽
20
21
12
25
24
23
4
19
11
5
26
27
28
1
2
3
6
7
18
17
16
15
14
13
10
9
LS11270S
LS11280S

LOGIC SYMBOL


26 27 28 1 2 3 6 7 4
A0 A1 A2 A3 A4 A5 A6 A7 CFBA
20 CPA
21 CEA
23 CEB
24 CPB
FBA 5
OEA 25
OEB 19
FAB 11
B0 B1 B2 B3 B4 B5 B6 B7 CFAB
18 17 16 15 14 13 10 9 12
LS11290S

LOGIC DIAGRAM for 'F550


DETAIL A
CP
Q
$\overline{CE}$ CE D
CP
Q
D CE $\overline{CE}$
A_0
B_0
A_1
A_2
A_3
A_4
A_5
A_6
A_7
DETAIL A X7
B_1
B_2
B_3
B_4
B_5
B_6
B_7
FBA
CP
Q
CD D
CP
Q
D CD
FAB
CFBA
CFAB
$\overline{OEA}$
$\overline{OEB}$
CPA
CPB
$\overline{CEA}$
$\overline{CEB}$
LD08640S

FUNCTIONAL DESCRIPTION

Data applied to the A inputs are entered and stored on the rising edge of the A Clock (CPA), provided that the A Clock Enable ($\overline{CEA}$) is Low; simultaneously, the status flip-flop is set and the A-to-B Flag (FAB) output goes High. Data entered from the A inputs is present at the inputs to the B output buffers, but only appears on the B I/O pins when the B Output Enable ($\overline{OEB}$) signal is made Low. After the B output data is assimilated, the receiving system clears the A-to-B Flag flip-flop by applying a Low-to-High transition to the CFAB input. Optionally, the OEA and CFAB pins can be tied together and operated by one function from the receiving system.

Data flow from B-to-A proceeds in the same manner described for A-to-B flow. Inputs $\overline{CEB}$ and CPB enter the B input data and set the B-to-A Flag (FBA) output High. A Low signal on $\overline{OEA}$ enables the A output buffers and a Low-to-High transition on CFBA clears the FBA Flag.

FUNCTION TABLE

OPERATING MODE	INPUTS			INTERNAL Q
	A or B	CP	$\overline{CE}$	
Hold data	X	X	H	No change
Load data	L H	↑ ↑	L L	L H

FLAG FUNCTION TABLE

OPERATING MODE	INPUTS			FLAG OUTPUT
	CF	CP	$\overline{CE}$	
Hold Flag	‡	X	H	No change
Clear Flag	↑	X	X	L
Set Flag	‡	↑	L	H

OUTPUT CONTROL TABLE

OPERATING MODE	$\overline{OE}$	INTERNAL Q	OUTPUT	
			'F550	'F551
Disable outputs	H	X	Z	Z
Enable outputs	L L	L H	L H	H L

H = High Voltage Level
L = Low Voltage Level
X = Don't care
Z = High-Impedance
↑ = Low-to-High Transition
‡ = Doesn't allow Low-to-High Transition

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		−0.5 to +7.0	V
V_{IN}	Input voltage		−0.5 to +7.0	V
I_{IN}	Input current		−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		−0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	FAB, FBA	40	mA
		$A_0 - A_7$, $B_0 - B_7$	48	
T_A	Operating free-air temperature range		0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	V
I_{OH}	High-level output current	FAB, FBA			−1	mA
		$A_0 - A_7$, $B_0 - B_7$			−3	
I_{OL}	Low-level output current	FAB, FBA			20	mA
		$A_0 - A_7$, $B_0 - B_7$			24	
T_A	Operating free-air temperature		0		70	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS[1]		74F550, 74F551			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN V_{IL} = MAX I_{OH} = MAX V_{IH} = MIN	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN V_{IL} = MAX, I_{OL} = MAX V_{IH} = MIN	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$			−0.73	−1.2	V
I_I	Input current at maximum input voltage	Others	V_{CC} = MAX, V_I = 7.0V				100	μA
		$A_0 - A_7$, $B_0 - B_7$	V_{CC} = 5.5V, V_I = 5.5V				1.0	mA
I_{IH}	High-level input current	except $A_0 - A_7$ $B_0 - B_7$	V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				−600	μA
$I_{IH}+I_{OZH}$	High-level input current	$A_0 - A_7$ $B_0 - B_7$	V_{CC} = MAX, V_O = 2.7V				70	μA
$I_{IL}+I_{OZL}$	Low-level input current		V_{CC} = MAX, V_O = 0.5V				−600	μA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current		V_{CC} = MAX			130	190	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value under the recommended operating conditions for the applicable conditions.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} should be performed last.

FAST 74F550, 74F551

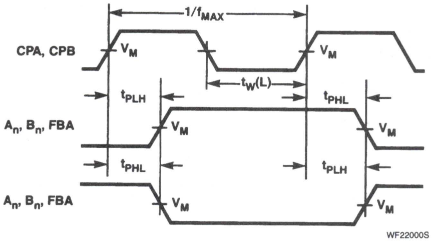
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F550, 74F551					UNIT
			$T_A = +25°C$ $V_{CC} = 5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum operating frequency	Waveform 1	60	70		50		MHz
t_{PLH}	Propagation delay CPA or CPB to B_n or A_n	Waveform 1	3.0	5.5	7.5	2.5	8.5	ns
t_{PHL}			4.0	7.0	9.0	3.5	10.0	
t_{PLH}	Propagation delay CPA or CPB to FAB or FBA	Waveform 1	3.5	6.0	6.0	3.0	9.0	ns
t_{PHL}	Propagation delay CFAB or CFBA to FAB or FBA	Waveform 2	5.0	9.0	11.5	4.5	13.0	ns
t_{PZH}	Output enable time $\overline{OEA}$ or $\overline{OEB}$ to A_n or B_n	Waveform 4, 5	2.5	5.5	7.5	2.0	8.5	ns
t_{PZL}			3.5	7.0	9.5	3.0	10.5	
t_{PHZ}	Output Disable time $\overline{OEA}$ or $\overline{OEB}$ to A_n or B_n	Waveform 4, 5	3.0	6.5	9.0	2.5	10.0	ns
t_{PLZ}			2.5	5.5	7.5	2.0	8.5	

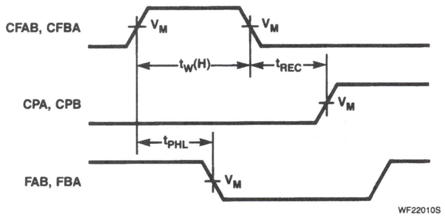
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	74F550, 74F551					UNIT
			$T_A = +25°C$ $V_{CC} = 5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ CL = 50pF $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$	Setup time, High or Low A_n or B_n to CPA or CPB	Waveform 3	4.0			4.5		ns
$t_s(L)$			4.0			4.5		
$t_h(H)$	Hold time, High or Low A_n or B_n to CPA or CPB	Waveform 3	2.0			2.5		ns
$t_h(L)$			2.0			2.5		
$t_s(H)$	Setup time, High or Low $\overline{CEA}$ or $\overline{CEB}$ to CPA or CPB	Waveform 3	4.0			4.5		ns
$t_s(L)$			4.0			4.5		
$t_h(H)$	Hold time, High or Low $\overline{CEA}$ or $\overline{CEB}$ to CPA or CPB	Waveform 3	2.0			2.5		ns
$t_h(L)$			2.0			2.5		
$t_w(H)$	Pulse width, High or Low CPA or CPB	Waveform 3	3.0			3.5		ns
$t_w(L)$			3.0			3.5		
$t_w(H)$	Pulse width, High CFAB or CFBA	Waveform 2	3.0			3.5		ns
t_{rec}	Recovery time CFAB or CFBA to CPA or CPB	Waveform 2	9.0			10.0		ns

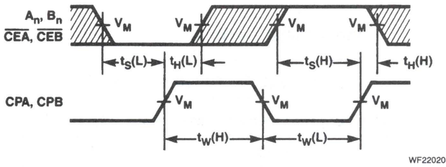
AC WAVEFORMS


1/fMAX
CPA, CPB
VM
VM
tW(L)
tPLH
tPHL
An, Bn, FBA
VM
VM
tPHL
tPLH
An, Bn, FBA
VM
VM
WF22000S

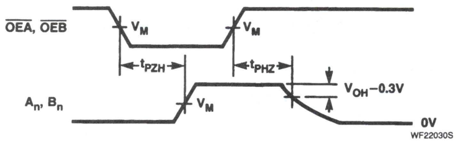
Waveform 1. Propagation Delay, Clock Input to Output


CFAB, CFBA
VM
VM
tW(H)
tREC
CPA, CPB
VM
tPHL
FAB, FBA
VM
WF22010S

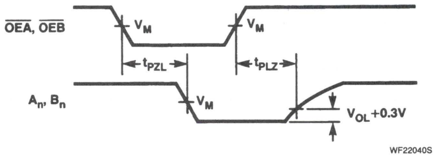
Waveform 2. Propagation Delay, Flag Clear Input to Status Flag Output, Recovery Time Flag Clear Input to Clock Output


An, Bn
CEA, CEB
VM
VM
VM
VM
tS(L)
tH(L)
tS(H)
tH(H)
CPA, CPB
VM
VM
VM
tW(H)
tW(L)
WF22020S

Waveform 3. Data Setup Time and Hold Times, and Clock Pulse Widths


OEA, OEB
VM
VM
tPZH
tPHZ
An, Bn
VM
VOH−0.3V
0V
WF22030S

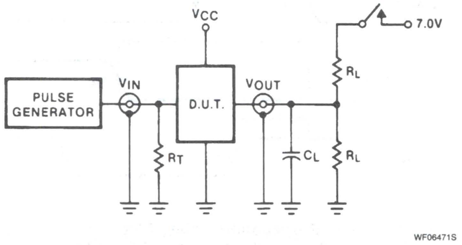
Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time From High Level


OEA, OEB
VM
VM
tPZL
tPLZ
An, Bn
VM
VOL+0.3V
WF22040S

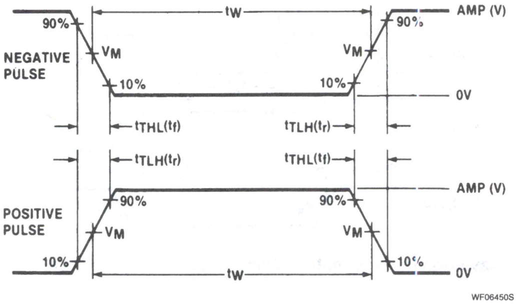
Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time From Low Level

NOTE: $V_M = 1.5V$.
The shaded area indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS


VCC
7.0V
RL
PULSE GENERATOR
VIN
D.U.T.
VOUT
RT
CL
RL
WF06471S

Test Circuit for 3-State Outputs


90%
tW
AMP (V)
90%
NEGATIVE PULSE
VM
VM
10%
10%
0V
tTHL(tf)
tTLH(tr)
tTLH(tr)
tTHL(tf)
AMP (V)
90%
90%
POSITIVE PULSE
VM
VM
10%
10%
0V
tW
WF06450S

$V_M = 1.5V$

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F552

Octal Registered Transceiver With Parity and Flags (3-State)

Preliminary Specification

FAST Products

FEATURES

- **8-bit bidirectional I/O port with handshake**
- **Register status flag flip-flops**
- **Separate Clock Enable and Output Enable**
- **Parity Generation and Parity Check**
- **B outputs and Parity output sink 64mA**

DESCRIPTION

The 'F552 octal transceiver contains two 8-bit registers for temporary storage of data flowing in either direction. Each register has its own Clock (CPR, CPS) and Clock Enable ($\overline{\text{CER}}$, $\overline{\text{CES}}$) inputs, as well as a flag flip-flop that is set automatically as the register is loaded. The flag output will be reset when the Output Enable returns to High after reading the output port. Each register has a separate Output Enable ($\overline{\text{DEAS}}$, $\overline{\text{OEBR}}$) for its 3-State buffer. The separate Clocks, Flags and Enables provide considerable flexibility as I/O ports for demand-response data transfer. When data is transferred from the A port to the B port, a parity bit is generated. On the other hand, when data is transferred from the B port to the A port, the parity of input data on $B_0 - B_7$ is checked.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F552	6.5ns	103mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V + 10\%$; $T_A = 0°C$ to $+70°C$
28-Pin Plastic DIP	N74F552N
28-Pin Plastic SOL	N74F552D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

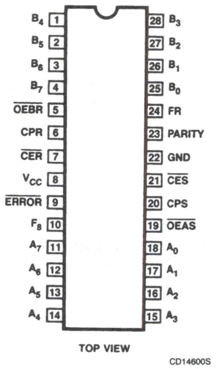
PINS	DESCRIPTION	74(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$A_0 - A_7$	A-to-B Data inputs	3.5/1.0	70μA/0.6mA
$B_0 - B_7$	B-to-A Data inputs	3.5/1.0	70μA/0.6mA
CPR	R registers Clock input (active rising edge)	1.0/1.0	20μA/0.6mA
CPS	S registers Clock input (active rising edge)	1.0/1.0	20μA/0.6mA
$\overline{\text{CER}}$	R registers Clock Enable input (active-Low)	1.0/1.0	20μA/0.6mA
$\overline{\text{CES}}$	S registers Clock Enable input (active-Low)	1.0/1.0	20μA/0.6mA
$\overline{\text{OEAS}}$	A-to-B Output Enable (active-Low) and Clear FS input (active rising edge)	1.0/2.0	20μA/1.2mA
$\overline{\text{OEBR}}$	B-to-A Output Enable (active-Low) and Clear FR input (active rising edge)	1.0/2.0	20μA/1.2mA
PARITY	Parity bit transceiver input	3.5/1.0	70μA/0.6mA
	Parity bit transceiver output	750/106.7	15mA/64mA
$\overline{\text{ERROR}}$	Parity check output (active-Low)	50/33.3	1.0mA/20mA
$A_0 - A_7$	A-to-B Data outputs	150/40	3.0mA/24mA
$B_0 - B_7$	B-to-A Data outputs	750/106.7	15mA/64mA
FS	A-to-B Status Flag output (active-High)	50/33.3	1mA/20mA
FB	B-to-A Output Enable input (active-High)	50/33.3	1mA/20mA

NOTE:

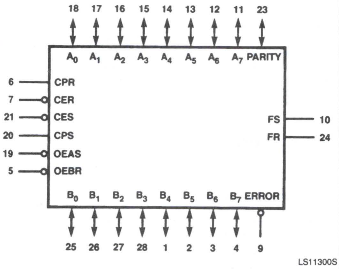
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

Octal Registered Transceiver With Parity and Flags (3-State) FAST 74F552

PIN CONFIGURATION

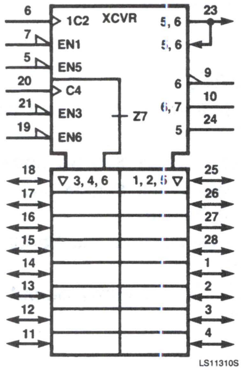

B4 1
B5 2
B6 3
B7 4
OEBR 5
CPR 6
CER 7
VCC 8
ERROR 9
FS 10
A7 11
A6 12
A5 13
A4 14
28 B3
27 B2
26 B1
25 B0
24 FR
23 PARITY
22 GND
21 CES
20 CPS
19 OEAS
18 A0
17 A1
16 A2
15 A3
TOP VIEW
CD14600S

LOGIC SYMBOL


18 17 16 15 14 13 12 11 23
A0 A1 A2 A3 A4 A5 A6 A7 PARITY
6 CPR
7 CER
21 CES
20 CPS
19 OEAS
5 OEBR
FS 10
FR 24
B0 B1 B2 B3 B4 B5 B6 B7 ERROR
25 26 27 28 1 2 3 4 9
LS11300S

V_{CC} = Pin 8
GND = Pin 22

LOGIC SYMBOL (IEEE/IEC)


6
1C2
XCVR
7
EN1
5
EN5
20
C4
21
EN3
19
EN6
Z7
5, 6
5, 6
23
6
9
6, 7
10
24
5
18
∇ 3, 4, 6
1, 2, 5 ∇
25
17
26
16
27
15
28
14
1
13
2
12
3
11
4
LS11310S

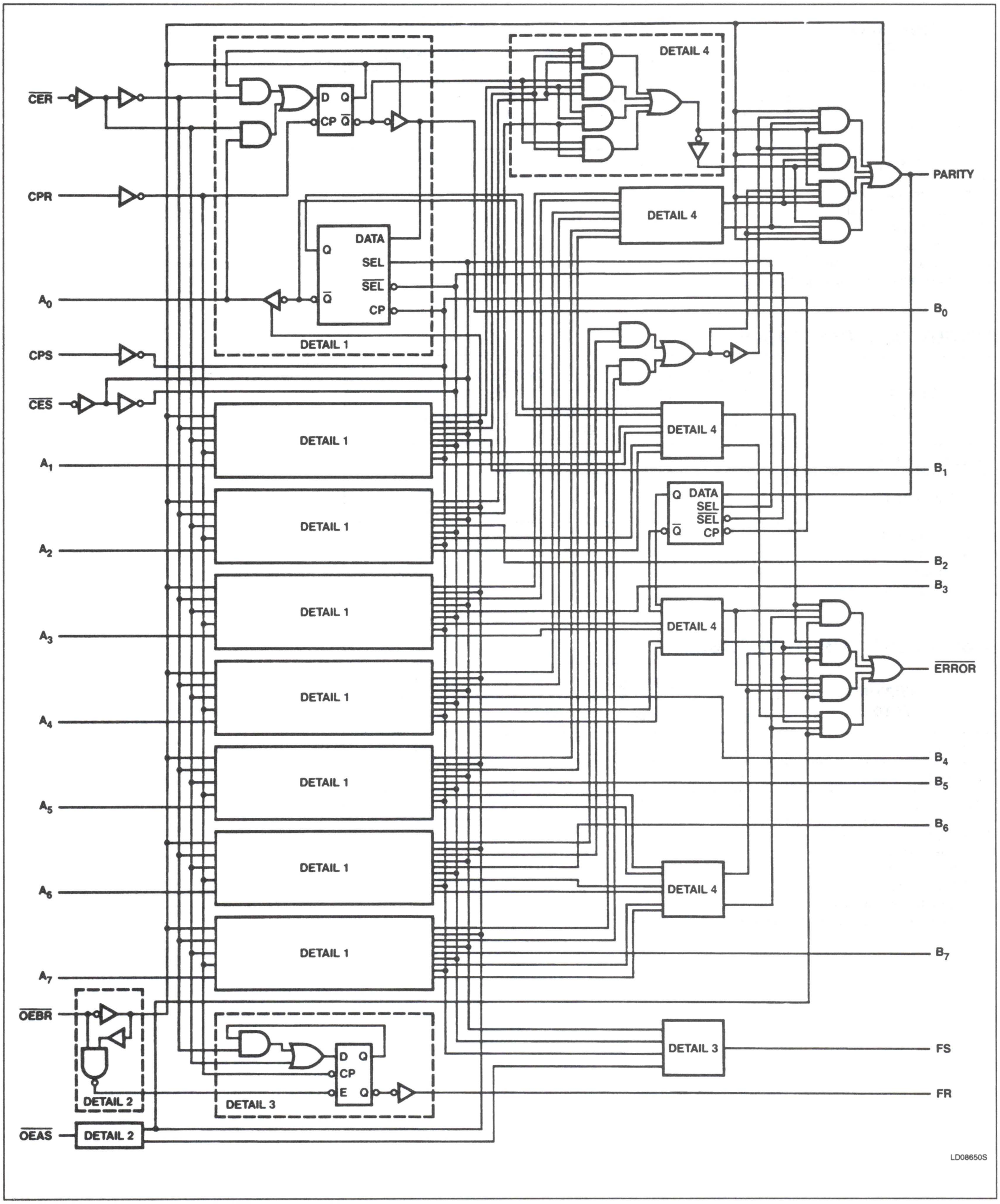
FUNCTIONAL DESCRIPTION

Data applied to the A inputs are entered and stored on the rising edge of the CPR Clock pulse, provided that CER is Low; simultaneously, the status flip-flop is set and the A-to-B flag (FR) output goes High. As the $\overline{\text{CER}}$ returns to High, the data will be held in R register. This data entered from the A inputs will appear at the B port I/O pins after the $\overline{\text{OEBR}}$ has gone Low. When $\overline{\text{OEBR}}$ is Low, a parity bit appears at the parity pin, which will be set High when there is an even number of 1's or all 0's at the Q outputs of the R register. After the data is assimilated, the receiving system clears the flag FR, by changing the signal at the $\overline{\text{OEBR}}$ pin from Low to High.

Data flow from B-to-A proceeds in the same manner described for A-to-B flow. A Low at the $\overline{\text{CES}}$ pin and a Low-to-High transition at CPS pin enters the B-input data and the parity-input data into the S register and the parity register respectively, and sets the flag output FS to High. A Low signal at the $\overline{\text{OEAS}}$ pin enables the A port I/O pins and a Low-to-High transition of the $\overline{\text{OEAS}}$ signal clears the FS flag. When $\overline{\text{OEAS}}$ is Low, the parity check output $\overline{\text{ERROR}}$ will be High if there is an odd number of 1's at the Q outputs of the S registers and the parity register. The flag FS can be cleared by a Low-to-High transition of the $\overline{\text{OEAS}}$ signal.

Octal Registered Transceiver With Parity and Flags (3-State) FAST 74F552

LOGIC DIAGRAM



CER
CPR
A0
CPS
CES
A1
A2
A3
A4
A5
A6
A7
OEBR
OEAS
DETAIL 1
DETAIL 2
DETAIL 3
DETAIL 4
D Q
CP Q
DATA
SEL
SEL
CP
Q
E Q
PARITY
B0
B1
B2
B3
ERROR
B4
B5
B6
B7
FS
FR
LD08650S

6

R or S REGISTER FUNCTION TABLE

OPERATING MODE	INPUTS			OUTPUT
	D	CP	$\overline{\text{CE}}$	INTERNAL Q
Hold data	X	X	H	NC
Load data	L H	↑ ↑	L L	L H
Keep old data	X	⍏	L	NC

H = High voltage level
L = Low voltage level
NC = No change
X = Don't care
↑ = Low to High transition
⍏ = Don't allow Low to High transition

OUTPUT CONTROL TABLE

OPERATING MODE	INPUT	OUTPUTS	
	$\overline{\text{OE}}$	INTERNAL Q	A or B
Disable outputs	H	X	Z
Enable outputs	L L	L H	L H

H = High voltage level
L = Low voltage level
X = Don't care
Z = High-impedance

R or S FLAG FUNCTION TABLE

OPERATING MODE	INPUTS			OUTPUT
	$\overline{\text{CE}}$	CP	$\overline{\text{OE}}$	FLAG
Hold Flag	H	X	⍏	NC
Set Flag	L	↑	⍏	H
Clear Flag	X	X	↑	L

H = High voltage level
L = Low voltage level
NC = No change
X = Don't care
↑ = Low to High transition
⍏ = Don't allow Low to High Transition

PARITY GENERATION FUNCTION TABLE

OPERATING MODE	INPUT	OUTPUTS	
	$\overline{\text{OEBR}}$	NUMBER OF HIGHS IN THE Q OUTPUTS OF THE R REGISTER	PARITY
Hold data	H	X	Z
Load data	L	0, 2, 4, 6, 8	H
	L	1, 3, 5, 7	L

H = High voltage level
L = Low voltage level
X = Don't care
Z = High-impedance

PARITY CHECK FUNCTION TABLE

OPERATING MODE	INPUTS		OUTPUTS	
	$\overline{\text{OEAS}}$	PARITY	NUMBER OF HIGHS IN THE Q OUTPUTS OF THE R REGISTER	$\overline{\text{ERROR}}$
Parity check	H	X	X	H
	L	L	0, 2, 4, 6, 8	L
	L	L	1, 3, 5, 7	H
	L	H	0, 2, 4, 6, 8	H
	L	H	1, 3, 5, 7	L

H = High voltage level
L = Low voltage level
X = Don't care

Octal Registered Transceiver With Parity and Flags (3-State) FAST 74F552

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		−0.5 to +7.0	V
V_{IN}	Input voltage		−0.5 to +7.0	V
I_{IN}	Input current		−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	FR, FS, $\overline{\text{ERROR}}$	40	mA
		$A_0 - A_7$	48	mA
		$B_0 - B_7$, PARITY	128	mA
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature range		−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	V
I_{OH}	High-level output current	FR, FS, $\overline{\text{ERROR}}$			−1	mA
		$A_0 - A_7$			−3	mA
		$B_0 - B_7$, PARITY			−15	mA
I_{OL}	Low-level output current	FR, FS, $\overline{\text{ERROR}}$			20	mA
		$A_0 - A_7$			24	mA
		$B_0 - B_7$, PARITY			64	mA
T_A	Operating free-air temperature		0		70	°C

Octal Registered Transceiver With Parity and Flags (3-State) FAST 74F552

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			Limits			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage	$\overline{\text{ERROR}}$, FS, FR	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = −15mA	±10% V_{CC}	2.0			V
					±5% V_{CC}	2.0			V
		$A_0 - A_7$, $B_0 - B_7$ PARITY		I_{OH} = −3mA	±10% V_{CC}	2.4			V
				I_{OH} = −1mA	±10% V_{CC}	2.5			V
			I_{OH} = −1mA or −3mA		±5% V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage	$A_0 - A_7$, $\overline{\text{ERROR}}$, FS, FR	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 20mA or I_{OL} = 24mA	±10% V_{CC}		0.35	0.50	V
					±5% V_{CC}		0.35	0.50	V
		$B_0 - B_7$ PARITY		I_{OL} = 64mA	±10% V_{CC}		0.40	0.55	V
					±5% V_{CC}		0.40	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$				−0.73	−1.2	V
I_I	Input current at maximum input voltage	others	V_{CC} = MAX, V_I = 7.0V					100	μA
		$A_0 - A_7$, $B_0 - B_7$	V_{CC} = 5.5V, V_I = 5.5V					1.0	mA
I_{IH}	High-level input current	others except $A_0 - A_7$, $B_0 - B_7$ PARITY	V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	Low-level input current	others	V_{CC} = MAX, V_I = 0.5V					−0.6	mA
		$\overline{\text{OEAS}}$, $\overline{\text{OEBR}}$						−1.2	mA
$I_{IH} + I_{OZH}$	High-level input current	$A_0 - A_7$, $B_0 - B_7$, PARITY	V_{CC} = MAX, V_O = 2.7V					70	μA
$I_{IL} + I_{OZL}$	Low-level input current		V_{CC} = MAX, V_O = 0.5V					−0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX			−100		−225	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				110	165	mA
		I_{CCL}					100	150	mA
		I_{CCZ}					100	150	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value under the recommended operating conditions for the applicable conditions.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} should be performed last.

AC ELECTRICAL CHARACTERISTICS

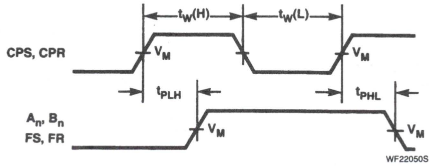
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			$T_A = +25°C$ $V_{CC} = 5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay CPS or CPR to A_n or B_n	Waveform 1	3.5 4.0	6.0 7.0	8.0 9.5	3.0 3.5	9.0 10.5	ns
t_{PHL}	Propagation delay CPS or CPR to FS or FR	Waveform 1	3.0	5.5	7.5	2.5	8.5	ns
t_{PHL}	Propagation delay $\overline{\text{OEAS}}$ to FS or $\overline{\text{OEBR}}$ to FR	Waveform 2	3.5	6.0	8.0	3.0	9.0	ns
t_{PLH} t_{PHL}	Propagation delay CPS to $\overline{\text{ERROR}}$	Waveform 4	8.0 8.5	14.0 14.5	18.0 18.5	7.0 7.5	20.0 20.5	ns
t_{PLH} t_{PHL}	Propagation delay CPR to PARITY	Waveform 4	8.0 7.5	13.5 13.0	17.5 16.5	7.0 6.5	19.5 18.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{\text{OEAS}}$ to $\overline{\text{ERROR}}$	Waveform 3	3.5 3.0	6.0 5.0	8.0 7.0	3.0 2.5	9.0 8.0	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{\text{OEAS}}$ or $\overline{\text{OEBR}}$ to B_n or A_n	Waveform 6 Waveform 7	3.0 3.5	5.5 7.0	7.5 9.5	2.5 3.0	8.5 10.5	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{\text{OEAS}}$ or $\overline{\text{OEBR}}$ to B_n or A_n	Waveform 6 Waveform 7	3.0 3.0	6.5 5.5	8.5 9.5	2.5 3.0	9.5 8.5	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{\text{OEBR}}$ to PARITY	Waveform 6 Waveform 7	2.5 3.5	4.5 6.0	6.0 8.0	2.0 3.0	7.0 9.0	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{\text{OEBR}}$ to PARITY	Waveform 6 Waveform 7	3.5 3.0	5.5 6.5	7.0 8.5	2.5 2.5	8.0 9.5	ns

Octal Registered Transceiver With Parity and Flags (3-State) FAST 74F552

AC SETUP REQUIREMENTS

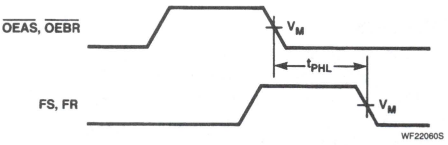
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			$T_A = +25°C$ $V_{CC} = 5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $CL = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low A_n or B_n or PARITY to CPS or CPR	Waveform 5	7.5 4.5			8.5 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low A_n or B_n or PARITY to CPS or CPR	Waveform 5	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{CES}$ or $\overline{CER}$ to CPS or CPR	Waveform 5	6.0 10.0			7.0 11.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{CES}$ or $\overline{CER}$ to CPS or CPR	Waveform 5	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	CPS or CPR Pulse width High or Low	Waveform 5	4.0 6.0			4.5 7.5		ns

AC WAVEFORMS



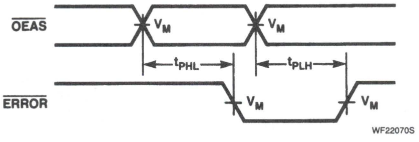
$t_W(H)$
$t_W(L)$
CPS, CPR
V_M
V_M
t_{PLH}
t_{PHL}
A_n, B_n
FS, FR
V_M
V_M
WF22050S

Waveform 1. Propagation Delay, Clock Input to Output



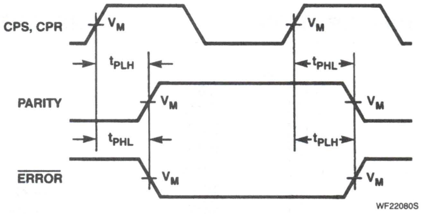
$\overline{OEAS}$, $\overline{OEBR}$
V_M
t_{PHL}
FS, FR
V_M
WF22060S

Waveform 2. Propagation Delay, Output Enable to Flag Output



$\overline{OEAS}$
V_M
V_M
t_{PHL}
t_{PLH}
$\overline{ERROR}$
V_M
V_M
WF22070S

Waveform 3. Propagation Delay, Output Enable to $\overline{ERROR}$



CPS, CPR
V_M
V_M
t_{PLH}
t_{PHL}
PARITY
V_M
V_M
t_{PHL}
t_{PLH}
$\overline{ERROR}$
V_M
V_M
WF22080S

Waveform 4. Propagation Delay, Clock to PARITY and $\overline{ERROR}$

NOTE: $V_M = 1.5V$.

Signetics

FAST 74F563, 74F564
Latch/Flip-Flop

'F563 Octal Transparent Latch (3-State)
'F564 Octal D Flip-Flop (3-State)
Preliminary Specification

FAST Products

FEATURES

- **'F563 is broadside pinout version of 'F533**
- **'F564 is broadside pinout version of 'F534**
- **Inputs and outputs on opposite side of package allow easy interface to microprocessors**
- **Useful as an Input or Output for microprocessors**
- **3-State Outputs for bus interfacing**
- **Common Output Enable**
- **'F573 and 'F574 are non-inverting versions of 'F563 and 'F564 respectively**
- **These are high-speed replacements for 8TS807 and 8TS808**

DESCRIPTION

The 'F563 is an octal transparent latch coupled to eight 3-State inverting output buffers. The two sections of the device are controlled independently by Latch Enable (E) and Output Enable ($\overline{OE}$) control gates.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F563 74F564	4.5ns 6.5ns	35mA 55mA

ORDERING INFORMATION

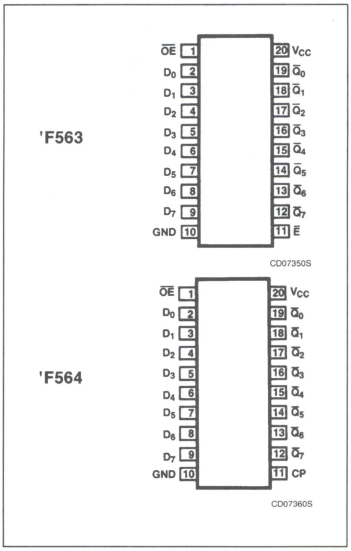
PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
20-Pin Plastic DIP	N74F563N, F74F564N
20-Pin Plastic SOL	N74F563D, N74F564D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

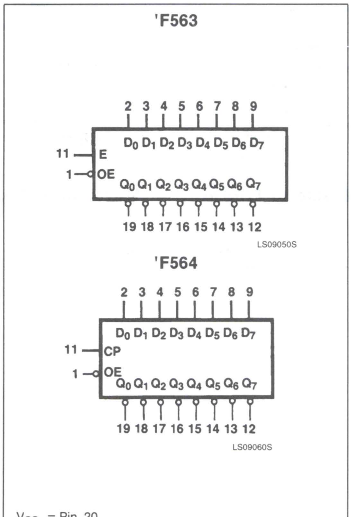
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$D_0 - D_7$	Data inputs	1.0/1.0	20μA/0.6mA
CP ('F563)	Clock Pulse Input (active rising edge)	1.0/1.0	20μA/0.6mA
E ('F564)	Enable input (active-High)	1.0/1.0	20μA/0.6mA
$\overline{OE}$	Output Enable input (active-Low)	1.0/1.0	20μA/0.6mA
$Q_0 - Q_7$	Data outputs	150/40	3mA/24mA

NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the Low state and 0.6mA in the Low state.

PIN CONFIGURATION

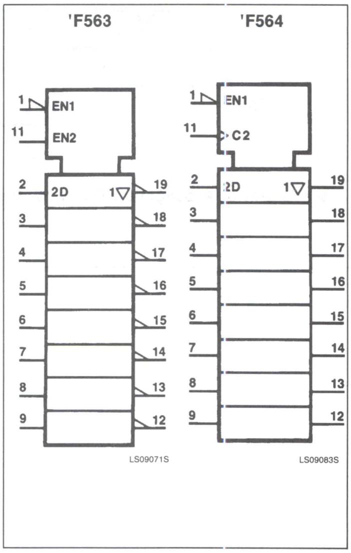

'F563
OE 1
D0 2
D1 3
D2 4
D3 5
D4 6
D5 7
D6 8
D7 9
GND 10
20 Vcc
19 Q0
18 Q1
17 Q2
16 Q3
15 Q4
14 Q5
13 Q6
12 Q7
11 E
CD07350S
'F564
OE 1
D0 2
D1 3
D2 4
D3 5
D4 6
D5 7
D6 8
D7 9
GND 10
20 Vcc
19 Q0
18 Q1
17 Q2
16 Q3
15 Q4
14 Q5
13 Q6
12 Q7
11 CP
CD07360S

LOGIC SYMBOL


'F563
2 3 4 5 6 7 8 9
D0 D1 D2 D3 D4 D5 D6 D7
11 E
1 OE
Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
19 18 17 16 15 14 13 12
LS09050S
'F564
2 3 4 5 6 7 8 9
D0 D1 D2 D3 D4 D5 D6 D7
11 CP
1 OE
Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
19 18 17 16 15 14 13 12
LS09060S

V_{CC} = Pin 20
GND = Pin 10

LOGIC SYMBOL (IEEE/IEC)


'F563
'F564
1 EN1
11 EN2
2 2D 1▽ 19
3 18
4 17
5 16
6 15
7 14
8 13
9 12
LS09071S
1 EN1
11 C2
2 2D 1▽ 19
3 18
4 17
5 16
6 15
7 14
8 13
9 12
LS09083S

Latch/Flip-Flop

FAST 74F563, 74F564

The 'F563 is functionally identical to the 'F533 but has a broadside pinout configuration to facilitate PC board layout and allows easy interface with microprocessors.

The data on the D inputs are transferred to the Latch outputs when the latch Enable (E) input is High. The latch remains transparent to the data inputs while E is High, and stores the data present one setup time before the High-to-Low enable transition.

The 3-State inverting output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active-Low Output Enable ($\overline{OE}$) controls all eight 3-State buffers independently of the latch operation. When $\overline{OE}$ is Low, the latched or transparent data appears at the outputs. When $\overline{OE}$ is High, the outputs are in the High-impedance 'OFF' state, which means they will neither drive nor load the bus.

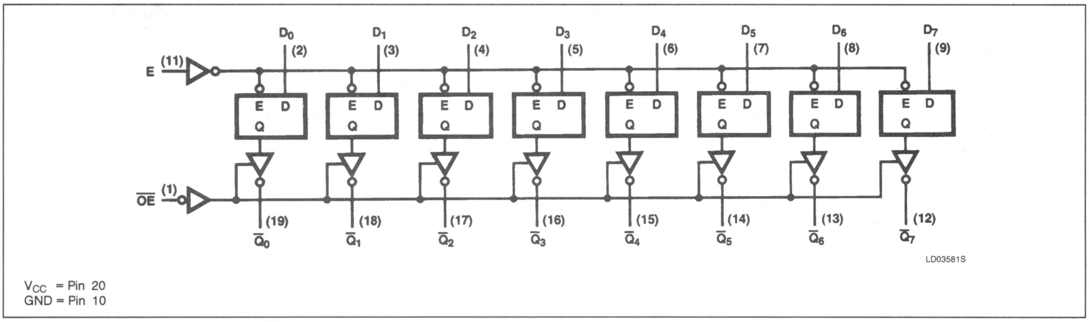
The 'F564 is an 8-bit edge-triggered register coupled to eight 3-State inverting output buffers. The two sections of the device are controlled independently by the Clock (CP) and Output Enable ($\overline{OE}$) control gates.

The F564 is functionally identical to the 'F534 but has a broadside pinout configuration to facilitate PC board layout and allow easy interface with microprocessors.

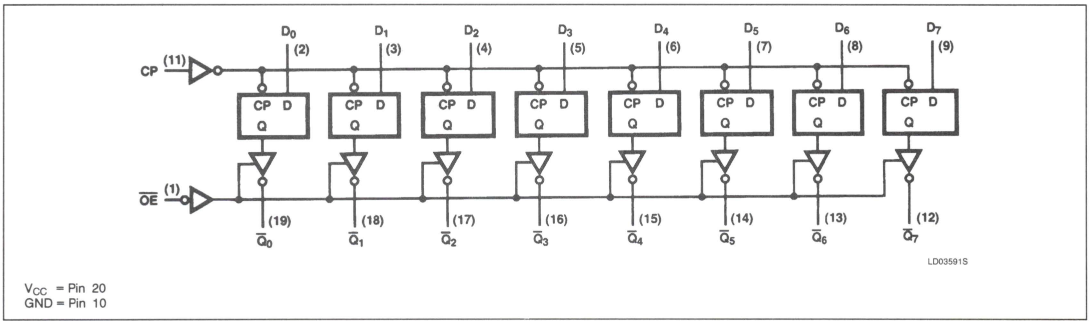
The register is fully edge triggered. The state of each D input, one setup time before the Low-to-High clock transition, transferred to the corresponding flip-flop's $\overline{Q}$ output.

The 3-State inverting output buffers are designed to drive heavily loaded 3-State buses. MOS memories, or MOS microprocessors. The active-Low Output Enable ($\overline{OE}$) controls all eight 3-State buffers independently of the register operation. When $\overline{OE}$ is Low, data in the register appears at the outputs. When $\overline{OE}$ is High, the outputs are in the High-impedance 'OFF' state, which means they will neither drive nor load the bus.

LOGIC DIAGRAM, 'F563



LOGIC DIAGRAM, 'F564



MODE SELECT FUNCTION TABLE for 'F563

OPERATING MODE	INPUTS			INTERNAL REGISTER	OUTPUTS
	$\overline{OE}$	E	D_n		$\overline{Q}_0 - \overline{Q}_7$
Enable and read register	L	H	L	L	H
	L	H	H	H	L
Latch and read register	L	↓	l	L	H
	L	↓	h	H	L
Hold	L	L	X	NC	NC
Disable outputs	H	X	X	X	Z

MODE SELECT FUNCTION TABLE for 'F564

OPERATING MODES	INPUTS			INTERNAL REGISTER	OUTPUTS
	$\overline{OE}$	CP	D_n		$\overline{Q}_0 - \overline{Q}_7$
Load and read register	L L	↑ ↑	l h	L H	H L
Disable outputs	H	X	X	X	Z

H = High voltage level
h = High voltage level one setup time prior to the Low-to-High Clock transition or High-to-Low $\overline{OE}$ transition
L = Low voltage level
X = Don't care
l = Low voltage level one setup time prior to the Low-to-High Clock transition or High-to-Low $\overline{OE}$ transition
Z = High-impedance (OFF) state
↑ = Low-to-High clock transition
NC = No change
↓ = High-to-Low enable transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Operating free-air temperature	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−3	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		74F563, 74F564			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX V_{IH} = MIN,	±10%V_{CC}	2.4			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OL} = MAX V_{IH} = MIN,	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				−0.6	mA
I_{OZH}	OFF-state output current, High-level voltage applied		V_{CC} = MAX, V_O = 2.7V				50	μA
I_{OZL}	OFF-state output current, Low-level voltage applied		V_{CC} = MAX, V_O = 0.5V				−50	μA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current (total)	'F563	V_{CC} = MAX			41	61	mA
		'F564				55	86	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. 'F563 measure I_{CCZ} with $\overline{OE}$ input at 4.5V, D_n and E inputs at ground and all outputs open.
   'F564 measure I_{CCZ} with $\overline{OE}$ inputs at 4.5V and D_n inputs at ground and all outputs open.

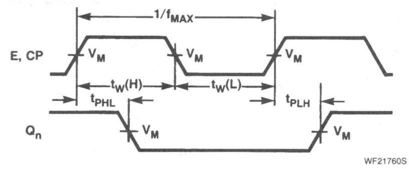
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	74F563, 74F564					UNIT
				$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			T_A, V_{CC} Comp'l $C_L = 50pF$ $R_L = 500\Omega$		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	'F563	Waveform 2	4.0 3.0	6.9 5.2	9.0 7.0	4.0 3.0	10.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay E to Q_n		Waveform 1	5.0 3.0	8.5 5.6	11.0 7.0	5.0 3.0	13.0 8.0	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level		Waveform 4 Waveform 5	2.0 2.0	7.7 5.1	10.0 6.5	2.0 2.0	11.0 7.5	ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level		Waveform 4 Waveform 5	2.0 2.0	4.7 4.1	6.0 5.5	2.0 2.0	7.0 6.5	ns
f_{MAX}	Maximum clock frequency	'F564	Waveform 1	100			70		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n		Waveform 1	4.0 4.0	6.5 6.5	8.5 8.5	4.0 4.0	10.0 10.0	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level		Waveform 4 Waveform 5	2.0 2.0	9.0 5.8	11.5 7.5	2.0 2.0	12.5 8.5	ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level		Waveform 4 Waveform 5	2.0 2.0	5.3 4.3	7.0 5.5	2.0 2.0	8.0 6.5	ns

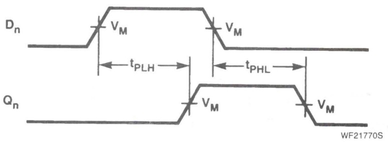
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER		TEST CONDITIONS	74F563, 74F564					UNIT
				$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
				Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time D_n to E	'F563	Waveform 3	2.0 2.0			2.0 2.0		ns
$t_h(H)$ $t_h(L)$	Hold time, D_n to E		Waveform 3	3.0 3.0			3.0 3.0		ns
$t_w(H)$	E Pulse width High High or Low		Waveform 1	6.0			6.0		ns
$t_s(H)$ $t_s(L)$	Setup time D_n to CP	'F564	Waveform 3	2.0 2.0			2.0 2.0		ns
$t_h(H)$ $t_h(L)$	Hold time, D_n to CP		Waveform 3	2.0 2.0			2.0 2.0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low		Waveform 1	5.0 5.0			7.0 6.0		ns

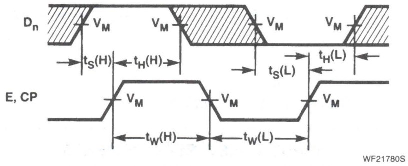
AC WAVEFORMS


1/f_{MAX}
E, CP
V_M
V_M
V_M
$t_W(H)$
$t_W(L)$
t_{PHL}
t_{PLH}
Q_n
V_M
V_M
WF21760S

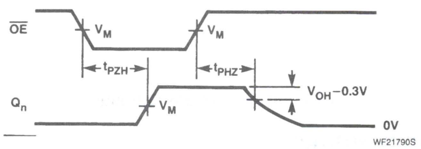
Waveform 1. Propagation Delay, Clock and Enable Inputs to Outputs, Clock and Enable Widths and Maximum Clock Frequency


D_n
V_M
V_M
t_{PLH}
t_{PHL}
Q_n
V_M
V_M
WF21770S

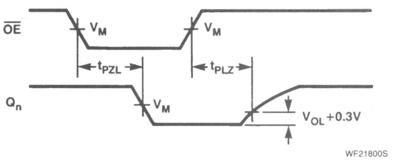
Waveform 2. Propagation Delay for Non-Inverting Output


D_n
V_M
V_M
V_M
V_M
$t_S(H)$
$t_H(H)$
$t_H(L)$
$t_S(L)$
E, CP
V_M
V_M
V_M
$t_W(H)$
$t_W(L)$
WF21780S

Waveform 3. Data Setup and Hold Times


$\overline{OE}$
V_M
V_M
t_{PZH}
t_{PHZ}
$V_{OH}-0.3V$
Q_n
V_M
0V
WF21790S

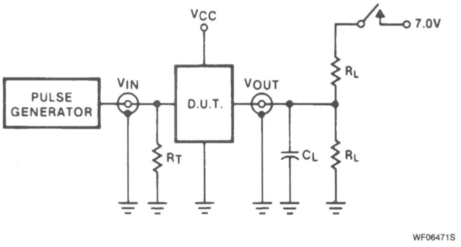
Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time From High Level


$\overline{OE}$
V_M
V_M
t_{PZL}
t_{PLZ}
Q_n
V_M
$V_{OL}+0.3V$
WF21800S

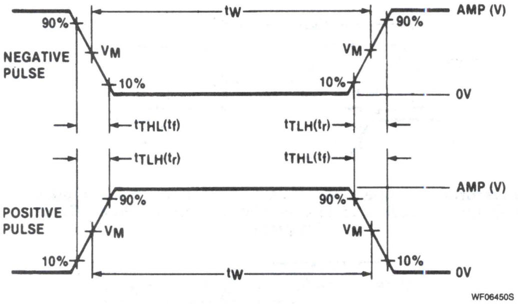
Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time From Low Level

NOTE: V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS


VCC
7.0V
RL
PULSE GENERATOR
VIN
D.U.T.
VOUT
RT
CL
RL
WF06471S

Test Circuit for 3-State Outputs


90%
tW
90%
AMP (V)
NEGATIVE PULSE
VM
VM
10%
10%
0V
tTHL(tf)
tTLH(tr)
tTLH(tr)
tTHL(tf)
AMP (V)
90%
90%
POSITIVE PULSE
VM
VM
10%
10%
0V
tW
WF06450S

$V_M = 1.5V$

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F568, 74F569
Bidirectional Counters

'F568 4-Bit Bidirectional Decade Counter (3-State)
'F569 4-Bit Bidirectional Binary Counter (3-State)
Product Specification

FAST Products

FEATURES

- **4-Bit Bidirectional Counters**
  - **'F568-Decade Counter**
  - **'F569-Binary Counter**
- **Synchronous counting and loading**
- **Look-ahead Carry capability for easy cascading**
- **Preset capability for programmable operation**
- **Master Reset ($\overline{MR}$) overrides all other inputs**
- **Synchronous Reset ($\overline{SR}$) overrides counting and parallel loading**
- **Clocked carry ($\overline{CC}$) output to be used as a clock for flip-flops, registers, and counters**
- **3-State outputs for bus organized systems**

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F568 74F569	115MHz 115MHz	40mA 40mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
20-Pin Plastic DIP	N74F568N, N74F569N
20-Pin Plastic SO	N74F568D, N74F569D

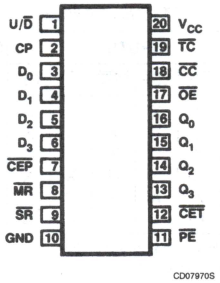
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$D_0 - D_3$	Data inputs	1.0/1.0	20μA/0.6mA
$\overline{CEP}$	Count enable parallel input (active-Low)	1.0/1.0	20μA/0.6mA
$\overline{CET}$	Count enable trickle input (active-Low)	1.0/2.0	20μA/1.2mA
CP	Clock input (active rising edge)	1.0/1.0	20μA/0.6mA
$\overline{PE}$	Parallel enable input (active-Low)	1.0/2.0	20μA/1.2mA
$U/\overline{D}$	Up/Down count control input	1.0/1.0	20μA/0.6mA
$\overline{OE}$	Output enable input (active-Low)	1.0/1.0	20μA/0.6mA
$\overline{MR}$	Master reset input (active-Low)	1.0/1.0	20μA/0.6mA
$\overline{SR}$	Synchronous reset input (active-Low)	1.0/1.0	20μA/0.6mA
$\overline{TC}$	Terminal count output (active-Low)	50/33	1mA/20mA
$\overline{CC}$	Clocked carry output (active-Low)	50/33	1mA/20mA
$Q_0 - Q_3$	Data outputs	150/40	3.0mA/24mA

NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

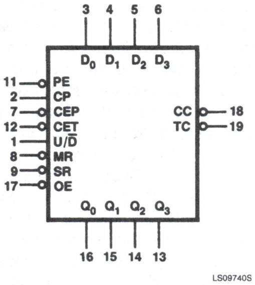
PIN CONFIGURATION

'F568


U/D̄ 1
CP 2
D0 3
D1 4
D2 5
D3 6
CEP 7
MR 8
SR 9
GND 10
20 VCC
19 TC
18 CC
17 OE
16 Q0
15 Q1
14 Q2
13 Q3
12 CET
11 PE
CD07970S

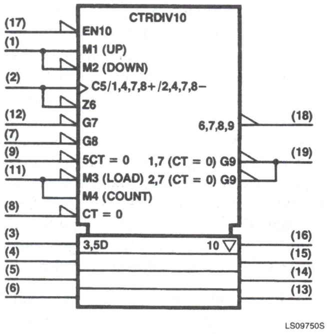
LOGIC SYMBOL

'F568


3 4 5 6
D0 D1 D2 D3
11 PE
2 CP
7 CEP
12 CET
1 U/D
8 MR
9 SR
17 OE
CC 18
TC 19
Q0 Q1 Q2 Q3
16 15 14 13
LS09740S

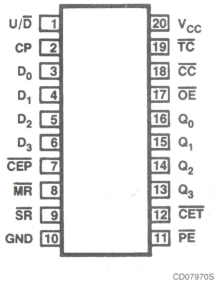
LOGIC SYMBOL (IEEE/IEC)

'F568


CTRDIV10
(17) EN10
(1) M1 (UP)
M2 (DOWN)
(2) C5/1,4,7,8+/2,4,7,8−
Z6
(12) G7
(7) G8
(9) 5CT = 0
(11) M3 (LOAD)
M4 (COUNT)
(8) CT = 0
6,7,8,9 (18)
1,7 (CT = 0) G9 (19)
2,7 (CT = 0) G9
(3) 3,5D
10
(4)
(5)
(6)
(16)
(15)
(14)
(13)
LS09750S

PIN CONFIGURATION

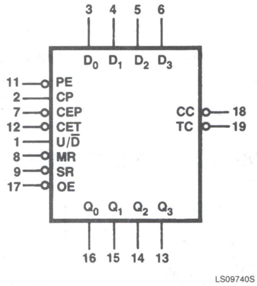
'F569



V_{CC} = Pin 20
GND = Pin 10

LOGIC SYMBOL

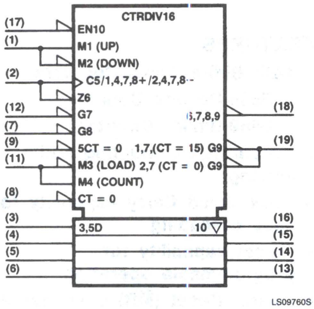
'F569



V_{CC} = Pin 20
GND = Pin 10

LOGIC SYMBOL (IEEE/IEC)

'F569



FUNCTIONAL DESCRIPTION

The "F568 counts modulo-10 in the BCD (8421) sequence. From state 9 (HLLH) it will increment to 0 (LLLL) in the Up mode; in Down mode it will decrement from 0 to 9. The 'F569 counts in the modulo-16 binary sequence. From state 15 it will increment to state 0 in the Up mode; in the Down mode it will decrement from 0 to 15. The clock inputs of all flip-flops are driven in parallel through a clock buffer. All state changes (except those due to Master Reset) occur synchronously with the Low-to-High transition of the Clock Pulse (CP) input signal.

The circuits have five fundamental modes of operation, in order of precedence: asynchronous reset, synchronous reset, parallel load, count and hold. Five control inputs — Master Reset ($\overline{MR}$), Synchronous Reset ($\overline{SR}$), Parallel Enable ($\overline{PE}$), Count Enable Parallel ($\overline{CEP}$), and Count Enable Trickle $\overline{CET}$) — plus the Up/Down ($U/\overline{D}$) input, determine the mode of operation, as shown in the Function Table. A Low signal on $\overline{MR}$ overrides all other inputs and asynchronously forces the flip-flop Q outputs Low. A Low signal on $\overline{SR}$ overrides counting and parallel loading and allows the Q outputs to go Low on the next rising edge of CP. A Low signal on $\overline{PE}$ overrides counting and allows information on the Parallel Data (P_n) inputs to be loaded into the flip-flops on the next rising edge of CP. With $\overline{MR}$, $\overline{SR}$ and $\overline{PE}$ High, $\overline{CEP}$ and $\overline{CET}$ permit counting when both are Low. Conversely, a High signal on either $\overline{CEP}$ or $\overline{CET}$ inhibits counting.

The 'F568 and 'F569 use edge-triggered flip-flops and changing the $\overline{SR}$, $\overline{PE}$, $\overline{CEP}$, $\overline{CET}$ or $U/\overline{D}$ inputs when the CP is in either state does not cause errors, provided that the recommended setup and hold times, (with respect to the rising edge of CP), are observed.

Two types of outputs are provided as overflow/underflow indicators. The Terminal Count ($\overline{TC}$) output is normally High and goes Low providing $\overline{CET}$ is Low, when the counter reaches zero in the Down mode, or reaches maximum (9 for the 'F568, 15 for the 'F569) in the Up mode. $\overline{TC}$ will then remain Low until a state change occurs, whether by counting or presetting, or until $U/\overline{D}$ or $\overline{CET}$ is changed. To implement synchronous multistage counters, the connections between the $\overline{TC}$ output and the $\overline{CEP}$ and $\overline{CET}$ inputs can provide either slow or fast carry propagation. Figure 1 shows the connections for simple ripple carry, in which the clock period must be longer than the CP to $\overline{TC}$ delay of the first stage, plus the cumulative $\overline{CET}$ to $\overline{TC}$ delays of the intermediate stages, plus the $\overline{CET}$ to CP setup time of the last stage. This total delay plus setup time sets the upper limit on clock frequency. For faster clock rates, the carry look-ahead connections shown in Figure 2 are recommended. In this scheme, the ripple delay through the intermediate stages commences with the same clock that causes the first stage to tick over from max to min in the Up mode, (or min to max in the Down mode), to start its final cycle. Since this final cycle takes 10 ('F568) or 16 ('F569) clocks to complete, there is plenty of time for the ripple to progress through the intermediate stages. The critical timing that limits the clock period is the CP to $\overline{TC}$ delay of the first stage plus the $\overline{CEP}$ to CP setup time of the last stage. The $\overline{TC}$ output is subject to decoding spikes due to internal race conditions and is therefore not recommended for use as a clock or asynchronous reset for flip-flops, registers or counters. For such applications, the Clocked Carry ($\overline{CC}$) output is provided. The $\overline{CC}$ output is normally High. When $\overline{CEP}$, $\overline{CET}$, and $\overline{TC}$ are Low, the $\overline{CC}$ output will go Low when the clock next goes Low and will stay Low until the clock goes High again; as shown in the $\overline{CC}$ Function Table. When the Output Enable ($\overline{OE}$) is Low, the parallel data outputs $Q_0 - Q_3$ are active and follow the flip-flop Q outputs. A High signal on $\overline{OE}$ forces $Q_0 - Q_3$ to the Hi-Z state but does not prevent counting, loading or resetting.

LOGIC EQUATIONS:

Count Enable = $\overline{CEP} \bullet \overline{CET} \bullet \overline{PE}$

Up ('F568): $\overline{TC} = Q_0 \bullet \overline{Q}_1 \bullet \overline{Q}_2 \bullet Q_3 \bullet (Up) \bullet \overline{CET}$

('F569): $\overline{TC} = Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3 \bullet (Up) \bullet \overline{CET}$

Down (Both): $\overline{TC} = \overline{Q}_0 \bullet \overline{Q}_1 \bullet \overline{Q}_2 \bullet \overline{Q}_3 \bullet (Down) \bullet \overline{CET}$

$\overline{CC}$ FUNCTION TABLE

INPUTS						OUTPUT
$\overline{SR}$	$\overline{PE}$	$\overline{CEP}$	$\overline{CET}$	$\overline{TC}$*	CP	$\overline{CC}$
L	X	X	X	X	X	H
X	L	X	X	X	X	H
X	X	H	X	X	X	H
X	X	X	H	X	X	H
X	X	X	X	H	X	H
H	H	L	L	L	⊔	⊔

* = $\overline{TC}$ is generated internally
H = High voltage level
L = Low voltage level
X = Don't care

Bidirectional Counters

FAST 74F568, 74F569

FUNCTION TABLE

INPUTS							OPERATING MODE
$\overline{\text{MR}}$	$\overline{\text{SR}}$	$\overline{\text{PE}}$	$\overline{\text{CEP}}$	$\overline{\text{CET}}$	U/$\overline{\text{D}}$	CP	
L	X	X	X	X	X	X	Asynchronous Reset
h	l	X	X	X	X	↑	Synchronous Reset
h	h	l	X	X	X	↑	Parallel Load
h	h	h	l	l	h	↑	Count up (increment)
h	h	h	l	l	l	↑	Count down (decrement)
h	H	H	H	X	X	X	Hold (do nothing)
h	H	H	X	H	X	X	

H = High voltage level
L = Low voltage level
X = Don't care
h = High voltage level one setup prior to the Low-to-High clock transition
l = Low voltage level one setup prior to the Low-to-High clock transition
↑ = Low-to-High clock transition

APPLICATION

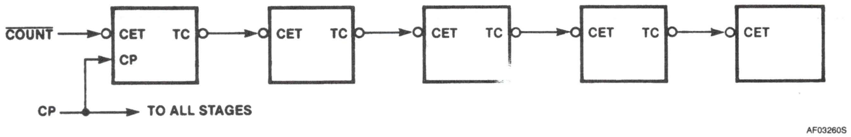

COUNT
CET
TC
CP
CET
TC
CET
TC
CET
TC
CET
CP
TO ALL STAGES
AF03260S

Figure 1. Multistage Counter With Ripple Carry

APPLICATION

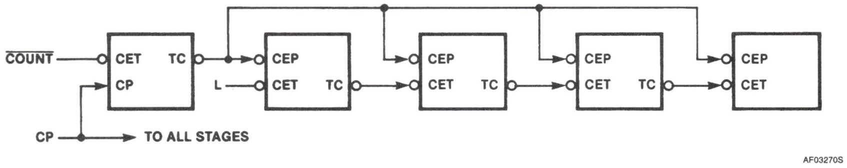
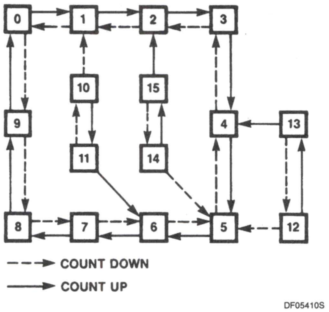

COUNT
CET
TC
CP
CEP
L
CET
TC
CEP
CET
TC
CEP
CET
TC
CEP
CET
CP
TO ALL STAGES
AF03270S

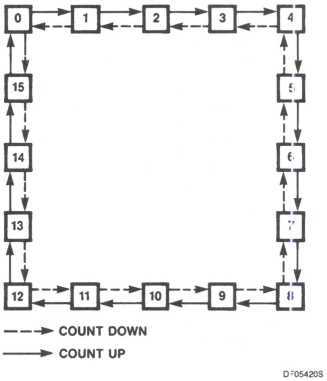
Figure 2. Multistage Counter With Look-ahead Carry

STATE DIAGRAMS

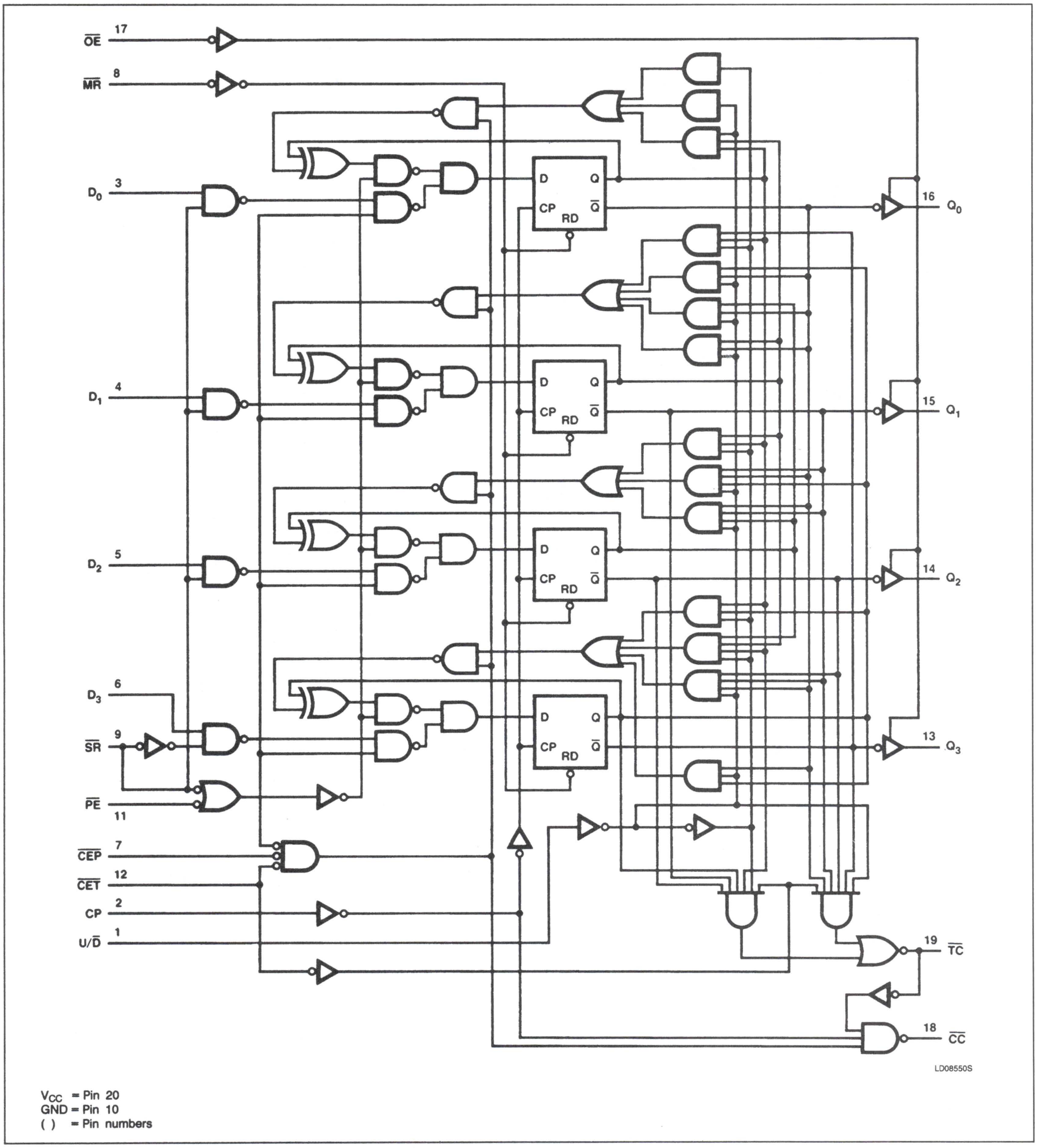
'F568


0
1
2
3
10
15
9
4
13
11
14
8
7
6
5
12
COUNT DOWN
COUNT UP
DF05410S

'F569

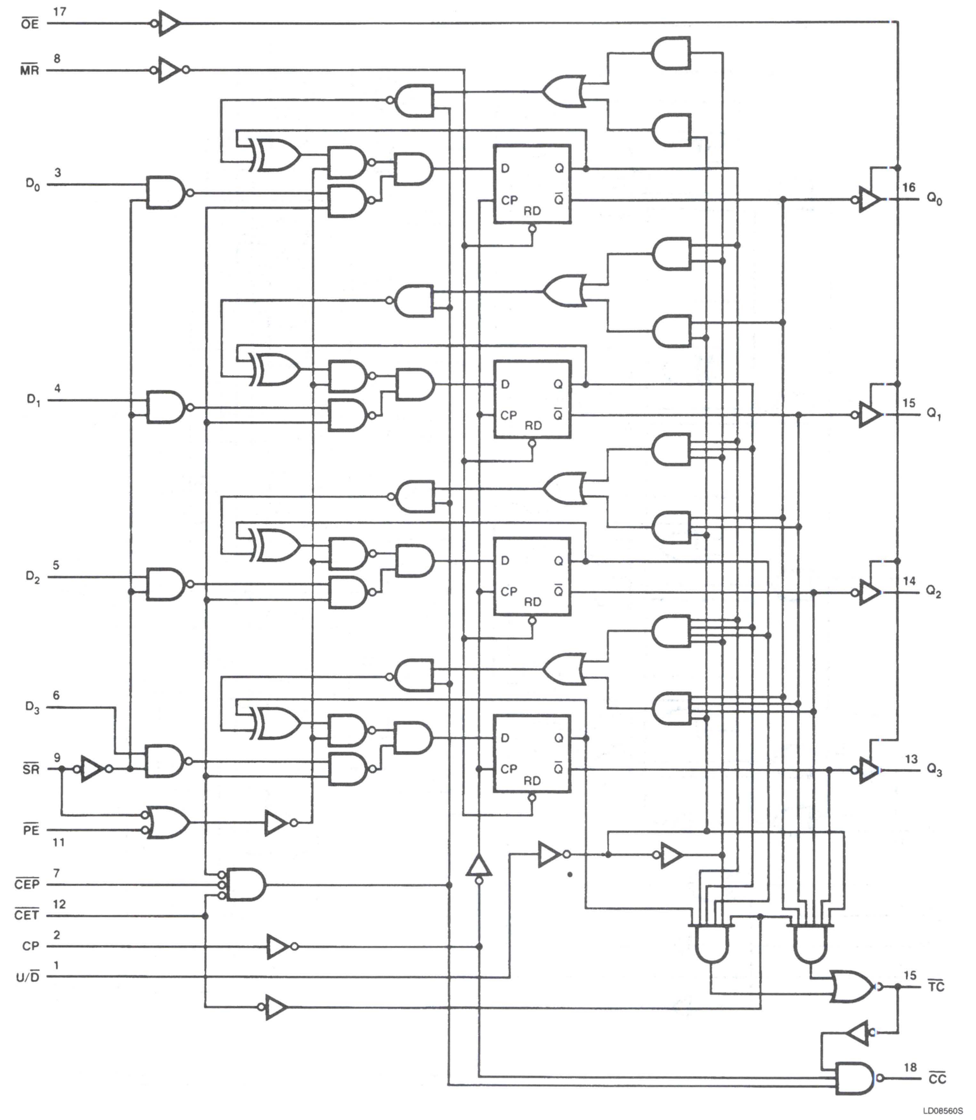

0
1
2
3
4
15
5
14
6
13
7
12
11
10
9
8
COUNT DOWN
COUNT UP
DF05420S

LOGIC DIAGRAM for 'F568


OE 17
MR 8
D0 3
D1 4
D2 5
D3 6
SR 9
PE 11
CEP 7
CET 12
CP 2
U/D 1
D Q
CP RD Q
16 Q0
15 Q1
14 Q2
13 Q3
19 TC
18 CC
LD08550S

V_{CC} = Pin 20
GND = Pin 10
( ) = Pin numbers

LOGIC DIAGRAM FOR 'F569


$\overline{OE}$ 17
$\overline{MR}$ 8
D_0 3
D_1 4
D_2 5
D_3 6
$\overline{SR}$ 9
$\overline{PE}$ 11
$\overline{CEP}$ 7
$\overline{CET}$ 12
CP 2
U/$\overline{D}$ 1
D
Q
CP
RD
$\overline{Q}$
16 Q_0
15 Q_1
14 Q_2
13 Q_3
15 $\overline{TC}$
18 $\overline{CC}$
LD08560S

V_{CC} = Pin 20
GND = Pin 10
( ) = Pin numbers

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		−0.5 to +7.0	V
V_{IN}	Input voltage		−0.5 to +7.0	V
I_{IN}	Input current		−30 to +1	mA
V_{OUT}	Voltage applied to output in High output state		−0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	$\overline{TC}$, $\overline{CC}$	40	mA
		Q_n	48	mA
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	High-level output current	$\overline{TC}$, $\overline{CC}$			−1	mA
		Q_n			−3	mA
I_{OL}	Low-level output current	$\overline{TC}$, $\overline{CC}$			20	mA
		Q_n			24	mA
T_A	Operating free-air temperature		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		74F568, 74F569			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.4			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$			−0.73	−1.2	V
I_I	Input clamp current at maximum input voltage		V_{CC} = MAX V_I = 7.0V				100	μA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current	others	V_{CC} = MAX, V_I = 0.5V				−0.6	μA
		$\overline{CET}$, $\overline{PE}$					−1.2	μA
I_{OZH}	OFF-state output current, High-level voltage applied		V_{CC} = MAX, V_O = 2.7V				50	μA

DC ELECTRICAL CHARACTERISTICS (Continued) (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]	74F568, 74F569			UNIT
				Min	Typ[2]	Max	
I_{OZL}	OFF-state output current, High-level voltage applied		V_{CC} = MAX, V_O = 0.5V			−50	µA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX	−60		−150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX		38	60	mA
		I_{CCL}			43	86	mA
		I_{CCZ}			40	60	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

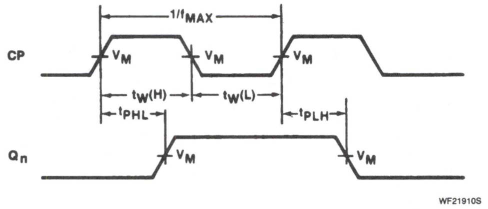
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	74F568, 74F569					UNIT
				T_A = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	to Q	Waveform 1	100	115		90		MHz
		to $\overline{CC}$/$\overline{TC}$	Waveform 2	50	65		45		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n ($\overline{PE}$ = High or Low)		Waveform 1	3.0 4.0	6.0 7.5	9.5 11.0	3.0 4.0	10.0 12.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{TC}$		Waveform 2	5.5 4.0	6.0 7.5	9.5 11.0	5.5 4.0	16.0 12.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CET}$ to $\overline{TC}$		Waveform 3	1.5 2.5	3.0 5.0	6.0 8.0	1.0 2.5	7.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay U/$\overline{D}$ to $\overline{TC}$	'F568	Waveform 4	2.5 5.0	5.0 10.0	9.0 15.0	2.0 5.0	10.0 15.0	ns
t_{PLH} t_{PHL}	Propagation delay U/$\overline{D}$ to $\overline{TC}$	'F569	Waveform 4	4.0 4.0	7.5 6.5	11.0 11.0	4.0 4.0	12.0 12.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{CC}$		Waveform 2	2.5 2.0	4.5 4.0	7.5 6.5	2.0 2.0	6.0 7.0	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{CEP}$, $\overline{CET}$ to $\overline{CC}$		Waveform 2	2.0 3.5	4.0 5.5	7.0 9.0	1.5 3.0	7.5 10.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n		Waveform 5	6.0	8.0	12.0	4.0	13.5	ns
t_{PLH} t_{PHL}	Propagation delay U/$\overline{D}$ to $\overline{CC}$		Waveform 4	4.5 5.0	9.0 11.0	12.0 16.0	4.0 5.0	13.5 17.0	ns
t_{PHL} t_{PZL}	Propagation delay $\overline{MR}$ to $\overline{TC}$		Waveform 5	8.0	11.0	15.0	7.5	16.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to $\overline{CC}$		Waveform 5	10.0	12.0	15.0	9.5	16.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{SR}$ to $\overline{CC}$		Waveform 3	5.5 7.5	8.0 9.5	11.0 12.0	5.0 7.0	12.0 13.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PE}$ to $\overline{CC}$		Waveform 3	3.0 4.0	5.0 5.0	8.0 8.5	2.5 4.0	8.5 9.5	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level $\overline{OE}$ to Q_n		Waveform 10 Waveform 11	2.0 4.5	4.0 6.5	7.0 9.5	2.0 4.0	7.5 10.0	ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level $\overline{OE}$ to Q_n		Waveform 10 Waveform 11	1.5 1.5	3.5 3.5	6.5 6.0	1.5 1.5	7.5 6.5	ns

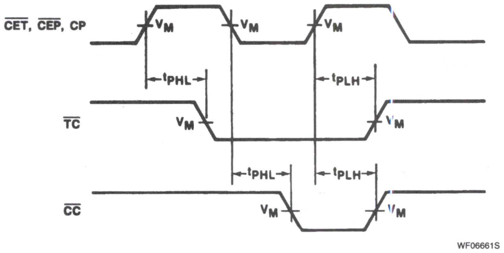
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER		TEST CONDITIONS	74F568, 74F569					UNIT
				$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$, $R_L = 500\Omega$		
				Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to CP		Waveform 6	4.0 4.0			4.5 4.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to CP		Waveform 6	3.0 3.0			3.5 3.5		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{CEP}$, $\overline{CET}$ to CP		Waveform 7	5.0 5.0			6.0 6.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{CEP}$, $\overline{CET}$ to CP		Waveform 7	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{PE}$ to CP		Waveform 6	8.0 8.0			9.0 9.0		ns
$t_h(H$ $t_h(L)$	Hold time, High or Low $\overline{PE}$ to CP		Waveform 6	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low U/$\overline{D}$ to CP ('F568)	'568	Waveform 8	11.0 10.5			12.5 17.5		ns
$t_h(H)$ $t_h(L)$	Setup time, High or Low U/$\overline{D}$ to CP ('F569)	'569	Waveform 8	10.0 8.0			12.5 8.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low U/$\overline{D}$ to CP		Waveform 8	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{SR}$ to CP		Waveform 9	9.5 8.5			10.5 9.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{SR}$ to CP		Waveform 9	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	CP pulse width, High or Low		Waveform 1	4.0 6.0			4.5 6.5		ns
$t_w(L)$	$\overline{MR}$ pulse width, Low		Waveform 5	4.5			5.0		ns
t_{rec}	$\overline{MR}$ recovery time		Waveform 5	6.0			7.0		ns

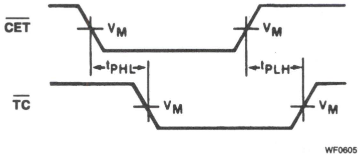
AC WAVEFORMS


1/fMAX
CP
VM
VM
VM
tW(H)
tW(L)
tPHL
tPLH
Qn
VM
VM
WF21910S

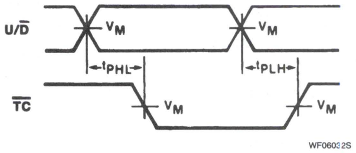
Waveform 1. Clock To Output Delays And Clock Pulse Width


CET, CEP, CP
VM
VM
VM
tPHL
tPLH
TC
VM
VM
tPHL
tPLH
CC
VM
VM
WF06661S

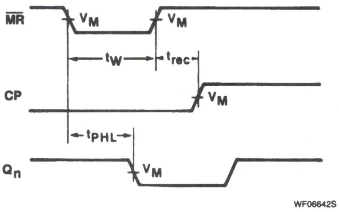
Waveform 2. Propagation Delay, CP, $\overline{CET}$, and $\overline{CET}$ to $\overline{CC}$ and CP to $\overline{TC}$ and Maximum Clock Frequency


CET
VM
VM
tPHL
tPLH
TC
VM
VM
WF06051S

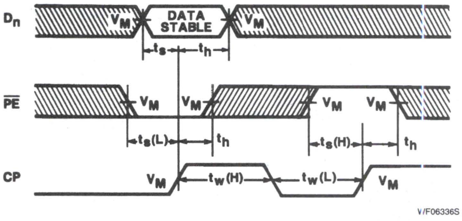
Waveform 3. Propagation Delays $\overline{CET}$ Input to Terminal Count Output


U/D
VM
VM
tPHL
tPLH
TC
VM
VM
WF06032S

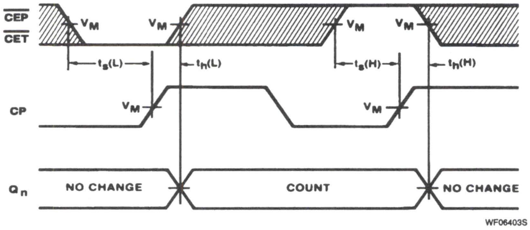
Waveform 4. Propagation Delays U/$\overline{D}$ Control to Terminal Count Output


MR
VM
VM
tW
trec
CP
VM
tPHL
Qn
VM
WF06642S

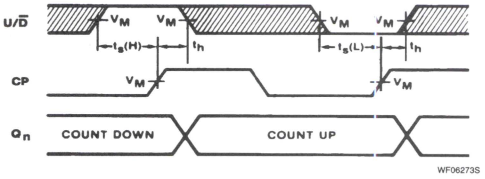
Waveform 5. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time


Dn
VM
DATA STABLE
VM
ts
th
PE
VM
VM
VM
VM
ts(L)
th
ts(H)
th
CP
VM
tw(H)
tw(L)
VM
WF06336S

Waveform 6. Parallel Data and Parallel Enable Setup and Hold Time

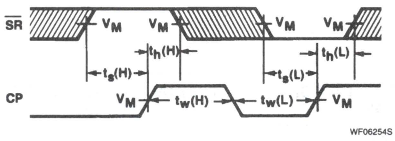

CEP
CET
VM
VM
VM
VM
ts(L)
th(L)
ts(H)
th(H)
CP
VM
VM
Qn
NO CHANGE
COUNT
NO CHANGE
WF06403S

Waveform 7. Count Enables Setup and Hold Times

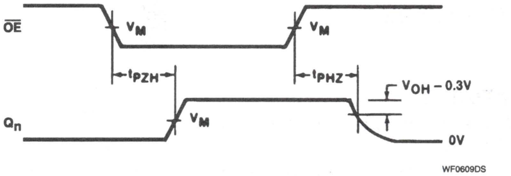

U/D
VM
VM
VM
VM
ts(H)
th
ts(L)
th
CP
VM
VM
Qn
COUNT DOWN
COUNT UP
WF06273S

Waveform 8. Up/Down Control Setup and Hold Times

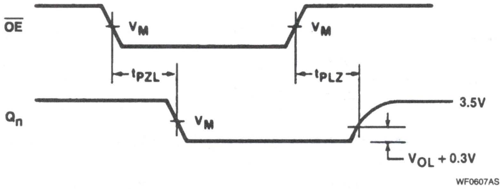
AC WAVEFORMS (Continued)


SR
CP
VM
th(H)
th(L)
ts(H)
ts(L)
tw(H)
tw(L)
WF06254S

Waveform 9. Data and Select Setup and Hold Times


OE
Qn
VM
tPZH
tPHZ
VOH – 0.3V
0V
WF0609DS

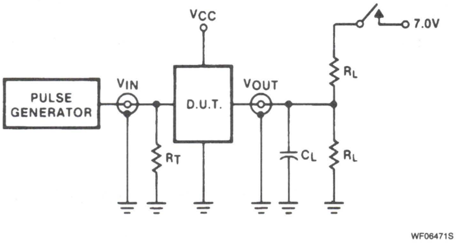
Waveform 10. 3-State Enable Time to High Level and Disable Time From High Level


OE
Qn
VM
tPZL
tPLZ
3.5V
VOL + 0.3V
WF0607AS

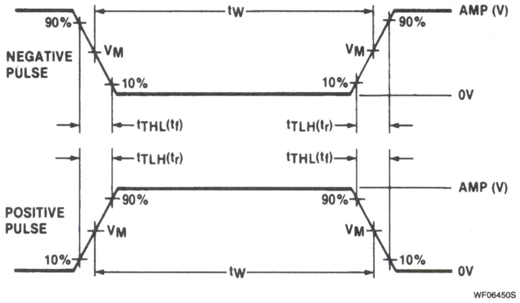
Waveform 11. 3-State Enable Time to Low Level and Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS


VCC
7.0V
RL
PULSE GENERATOR
VIN
D.U.T.
VOUT
RT
CL
RL
WF06471S

Test Circuit for 3-State Outputs


tw
90%
AMP (V)
NEGATIVE PULSE
VM
10%
0V
tTHL(tf)
tTLH(tr)
POSITIVE PULSE
WF06450S

$V_M = 1.5V$
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS
R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST Products

FAST 74F573, 74F574
Latch/Flip-Flops

'F573 Octal Transparent Latch (3-State)
'F574 Octal D Flip-Flop (3-State)
Preliminary Specification

FEATURES

- '573 is broadside pinout version of 'F373
- '574 is broadside pinout version of 'F374
- Inputs and outputs on opposite side of package allow easy interface to microprocessors
- Useful as an input or output port for microprocessors
- 3-State outputs for bus interfacing
- Common Output Enable
- 'F563 and 'F564 are inverting versions of 'F573 and 'F574 respectively
- These are high-speed replacements for N8TS805 and N8TS806

DESCRIPTION

The 'F573 is an octal transparent latch coupled to eight 3-State output buffers. The two sections of the device are controlled independently by Enable (E) and Output Enable ($\overline{OE}$) control gates.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F573	4.5ns	35mA
74F574	6.5ns	55mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
20-Pin Plastic DIP	N74F573N, N74F574N
20-Pin Plastic SOL	N74F573D, N74F574D

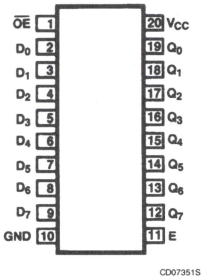
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$D_0 - D_7$	Data inputs	1.0/1.0	20μA/0.6mA
CP ('F574)	Clock Pulse input (active rising edge)	1.0/1.0	20μA/0.6mA
E ('F573)	Latch Enable input (active-High)	1.0/1.0	20μA/0.6mA
$\overline{OE}$	Output Enable input (active-Low)	1.0/1.0	20μA/0.6mA
$Q_0 - Q_7$	3-State outputs	150/40	3mA/24mA

NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION

'F573

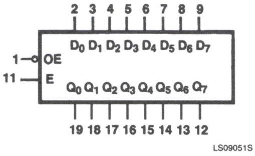


OE 1
D0 2
D1 3
D2 4
D3 5
D4 6
D5 7
D6 8
D7 9
GND 10
20 Vcc
19 Q0
18 Q1
17 Q2
16 Q3
15 Q4
14 Q5
13 Q6
12 Q7
11 E
CD07351S

V_{CC} = Pin 20
GND = Pin 10

LOGIC SYMBOL

'F573

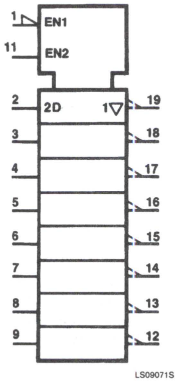


2 3 4 5 6 7 8 9
D0 D1 D2 D3 D4 D5 D6 D7
1 OE
11 E
Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
19 18 17 16 15 14 13 12
LS09051S

V_{CC} = Pin 20
GND = Pin 10

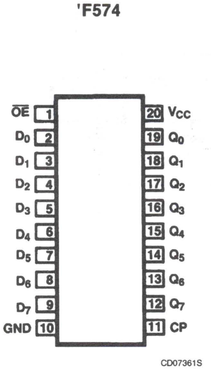
LOGIC SYMBOL (IEEE/IEC)

'F573

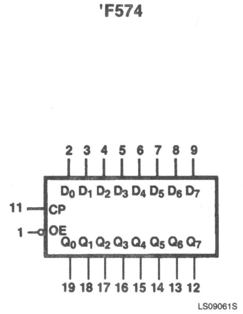


1
EN1
11
EN2
2
2D
1▽
19
3
18
4
17
5
16
6
15
7
14
8
13
9
12
LS09071S

PIN CONFIGURATION

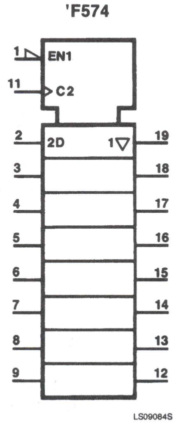

'F574
$\overline{OE}$ 1
D_0 2
D_1 3
D_2 4
D_3 5
D_4 6
D_5 7
D_6 8
D_7 9
GND 10
20 V_{CC}
19 Q_0
18 Q_1
17 Q_2
16 Q_3
15 Q_4
14 Q_5
13 Q_6
12 Q_7
11 CP
CD07361S

LOGIC SYMBOL


'F574
2 3 4 5 6 7 8 9
D_0 D_1 D_2 D_3 D_4 D_5 D_6 D_7
11 CP
1 OE
Q_0 Q_1 Q_2 Q_3 Q_4 Q_5 Q_6 Q_7
19 18 17 16 15 14 13 12
LS09061S

V_{CC} = Pin 20
GND = Pin 10

LOGIC SYMBOL (IEEE/IEC)


'F574
1
EN1
11
C2
2
2D
1▽
19
3
18
4
17
5
16
6
15
7
14
8
13
9
12
LS09084S

The 'F573 is functionally identical to the 'F373 but has a broadside pinout configuration to facilitate PC Board layout and allow easy interface with microprocessors.

The data on the D inputs is transferred to the latch outputs when the Latch Enable (E) input is High. The latch remains transparent to the data inputs while E is High, and stores the data that is present one setup time before the High-to-Low enable transition.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active-Low Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the latch operation. When $\overline{OE}$ is Low, the latched or transparent data appears at the outputs. When $\overline{OE}$ is High, the outputs are in the High-impedance "OFF" state, which means they will neither drive nor load the bus.

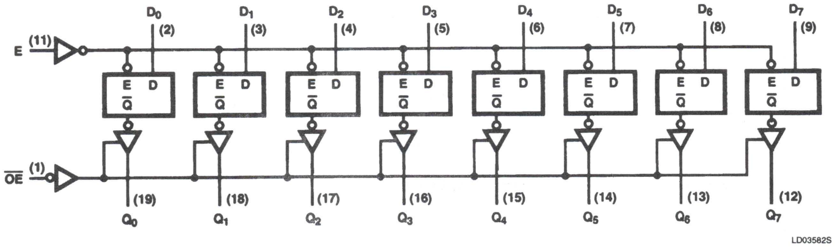
The 'F574 is functionally identical to the 'F374 but has a broadside pinout configuration to facilitate PC board layout and allow easy interface to microprocessors.

It is an 8-bit, edge-triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by the Clock (CP) and Output Enable ($\overline{OE}$) control gates.

The register is fully edge triggered. The state of each D input, one setup time before the Low-to-High clock transition is transferred to the corresponding flip-flop's Q output.

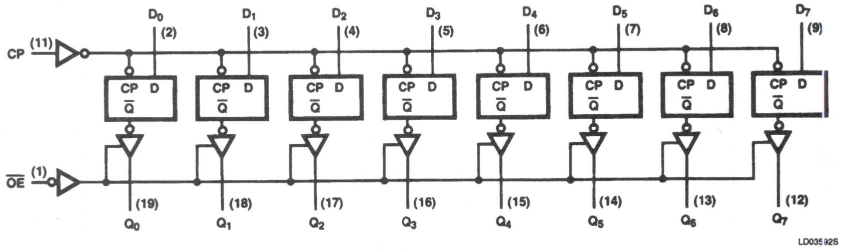
The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active-Low Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the register operation. When $\overline{OE}$ is Low, the data in the register appears at the outputs. When $\overline{OE}$ is High, the outputs are in the High-impedance "OFF" state, which means they will neither drive nor load the bus.

LOGIC DIAGRAM, 'F573


D_0 (2)
D_1 (3)
D_2 (4)
D_3 (5)
D_4 (6)
D_5 (7)
D_6 (8)
D_7 (9)
E (11)
E D
$\overline{Q}$
$\overline{OE}$ (1)
(19) Q_0
(18) Q_1
(17) Q_2
(16) Q_3
(15) Q_4
(14) Q_5
(13) Q_6
(12) Q_7
LD03582S

V_{CC} = Pin 20
GND = Pin 10

LOGIC DIAGRAM, 'F574



V_{CC} = Pin 20
GND = Pin 10

FUNCTION TABLE FOR 'F573

INPUTS			INTERNAL REGISTER	OUTPUTS	OPERATING MODE
$\overline{OE}$	E	D_n		$Q_0 - Q_7$	
L	H	L	L	L	Enable and read register
L	H	H	H	H	
L	↓	l	L	L	Latch and read register
L	↓	h	H	H	
L	L	X	NC	NC	Hold
H	X	X	X	Z	Disable Outputs

H = High voltage level
h = High voltage level one setup time prior to the High-to-Low E transition
L = Low voltage level
l = Low voltage level one setup time prior to the High-to-Low E
NC = No change transition
X = Don't care
Z = High-impedance (OFF) state
↓ = High-to-Low E transition

FUNCTION TABLE FOR 'F574

INPUTS			INTERNAL REGISTER	OUTPUTS	OPERATING MODE
$\overline{OE}$	CP	D_n		$Q_0 - Q_7$	
L	↑	l	L	L	Load and read register
L	↑	h	H	H	
H	X	X	X	Z	Disable outputs

H = High voltage level
h = High voltage level one setup time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one setup time prior to the Low-to-High clock transition
X = Don't care
Z = High-impedance (OFF) state
↑ = Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	74F573	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74F573			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-3	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]		74F573, 74F574			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage			V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7			V
V_{OL}	Low-level output voltage			V_{CC} = MIN, V_{IH} = MIN, I_{OL} = MAX, V_{IL} = MAX	±10%V_{CC}		0.35	0.5	V
					±5%V_{CC}		0.35	0.5	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage			V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	High-level input current			V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current			V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OZH}	OFF-state output current, High-level voltage applied			V_{CC} = MAX, V_O = 2.7V				50	μA
I_{OZL}	OFF-state output current, Low-level voltage applied			V_{CC} = MAX, V_O = 0.5V				-50	μA
I_{OS}	Short-circuit output current[3]			V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CC2}	'F573	V_{CC} = MAX	$\overline{OE}$ = 4.5V D = E = GND		35	55	mA
			'F574		CP = $\overline{OE}$ = 4.5V D_n inputs = GND		57	86	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

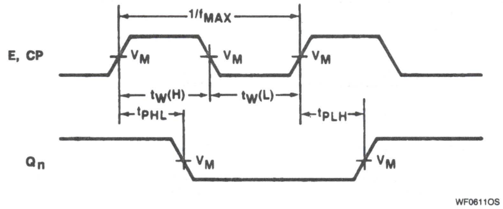
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	74F563, 74F564					UNIT
				$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			T_A, V_{CC} Comp'l $C_L = 50pF$ $R_L = 500\Omega$		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	'F573	Waveform 2	3.0 2.0	5.3 3.7	7.0 5.0	3.0 2.0	8.0 6.0	ns
t_{PLH} t_{PHL}	Propagation delay E to Q_n		Waveform 1	5.0 3.0	9.0 5.2	11.5 7.0	5.0 3.0	13.0 6.0	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level		Waveform 4 Waveform 5	2.0 2.0	5.0 5.6	11.0 7.5	2.0 2.0	12.0 8.5	ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level		Waveform 4 Waveform 5	2.0 2.0	4.5 3.8	6.5 6.0	2.0 2.0	7.5 6.0	ns
f_{MAX}	Maximum clock frequency	'F574	Waveform 1	100			70		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n		Waveform 1	4.0 4.0	6.5 6.5	8.5 8.5	4.0 4.0	10.0 10.0	ns
t_{PZH} t_{PZL}	Output Enable time to High to Low level		Waveform 4 Waveform 5	2.0 2.0	9.0 5.3	11.5 7.5	2.0 2.0	12.5 8.5	ns
t_{PHZ} t_{PLZ}	Output Disable time to High to Low level		Waveform 4 Waveform 5	2.0 2.0	5.3 4.3	7.0 5.5	2.0 2.0	6.0 6.5	ns

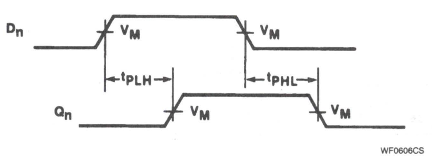
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER		TEST CONDITIONS	74F563, 74F564					UNIT
				$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			T_A, V_{CC} Comp'l $C_L = 50pF$ $R_L = 500\Omega$		
				Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time D_n to E	'F573	Waveform 3	2.0 2.0			2.0 2.0		ns
$t_s(H)$ $t_h(L)$	Hold time, D_n to E		Waveform 3	3.0 3.0			3.0 3.0		ns
$t_w(H)$ $t_w(L)$	E Pulse width, High or Low		Waveform 1	6.0 6.0			6.0 6.0		ns
$t_s(H)$ $t_s(L)$	Setup time D_n to CP	'F574	Waveform 3	2.0 2.0			2.0 2.0		ns
$t_s(H)$ $t_h(L)$	Hold time, D_n to CP		Waveform 3	2.0 2.0			2.0 2.0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low		Waveform 1	7.0 6.0			7.0 6.0		ns

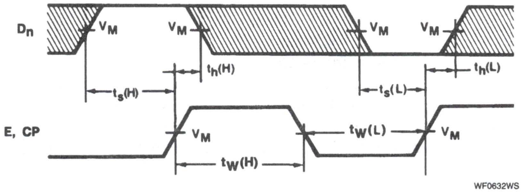
AC WAVEFORMS


1/fMAX
E, CP
VM
VM
VM
tW(H)
tW(L)
tPHL
tPLH
Qn
VM
VM
WF0611OS

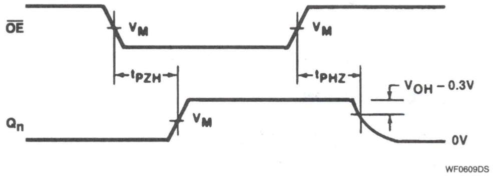
Waveform 1. Propagation Delay, Clock and Enable Inputs to Outputs, Clock and Enable Widths and Maximum Clock Frequency


Dn
VM
VM
tPLH
tPHL
Qn
VM
VM
WF0606CS

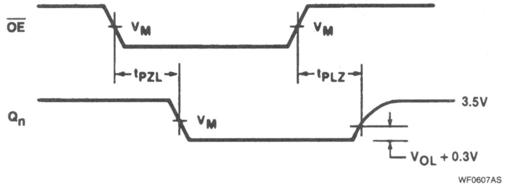
Waveform 2. Propagation Delay for Non-Inverting Output


Dn
VM
VM
VM
VM
th(H)
th(L)
ts(H)
ts(L)
E, CP
VM
tW(L)
VM
tW(H)
WF0632WS

Waveform 3. Data setup and Hold Times


OE
VM
VM
tPZH
tPHZ
VOH − 0.3V
Qn
VM
0V
WF0609DS

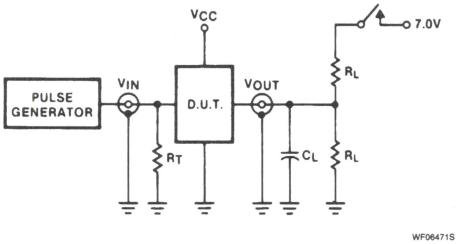
Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time From High Level


OE
VM
VM
tPZL
tPLZ
Qn
VM
3.5V
VOL + 0.3V
WF0607AS

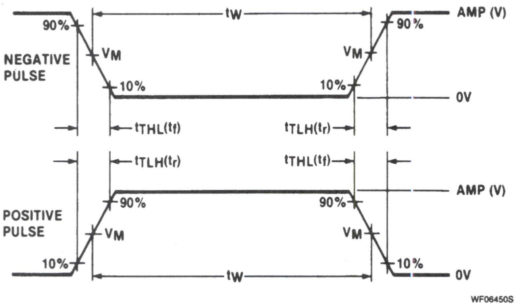
Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS


VCC
7.0V
RL
PULSE GENERATOR
VIN
D.U.T.
VOUT
RT
CL
RL
WF06471S

Test Circuit for 3-State Outputs


90%
tW
90%
AMP (V)
NEGATIVE PULSE
VM
VM
10%
10%
0V
tTHL(tf)
tTLH(tr)
tTLH(tr)
tTHL(tf)
AMP (V)
90%
90%
POSITIVE PULSE
VM
VM
10%
10%
0V
tW
WF06450S

$V_M = 1.5V$

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F579
Counter

8-Bit Bidirectional Binary Counter (3-State)
Product Specification

FAST Products

FEATURES

- **Multiplexed 3-State I/O ports for bus-oriented applications**
- **Built-in cascading carry capability**
- **Count frequency 115MHz typ**
- **Supply current 100mA typ**
- **Fully synchronous operation**
- **U/$\overline{D}$ pin to control direction of counting**
- **Separate pins for Master Reset and Synchronous Reset**
- **Center power pins to reduce effects of package inductance**
- **See 'F269 for 24-pin separate I/O port version**
- **See 'F779 for 16-pin version**

DESCRIPTION

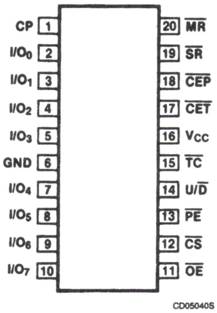
The 'F579 is a fully synchronous 8-stage up/down counter with multiplexed 3-State I/O ports for bus-oriented applications. It features a preset capability for programmable operation, carry look-ahead for easy cascading and a U/$\overline{D}$ input to control the direction of counting. All state changes, except for the case of asynchronous reset, are initiated by the rising edge of the clock.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F579	115MHz	100mA

ORDERING INFORMATION

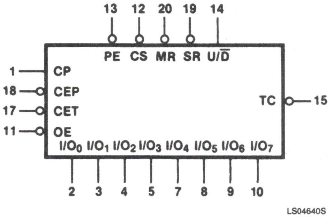
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V± 10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F579N
20-Pin Plastic SOL	N74F579D

PIN CONFIGURATION



CP 1
I/O0 2
I/O1 3
I/O2 4
I/O3 5
GND 6
I/O4 7
I/O5 8
I/O6 9
I/O7 10
20 MR
19 SR
18 CEP
17 CET
16 Vcc
15 TC
14 U/D
13 PE
12 CS
11 OE
CD05040S

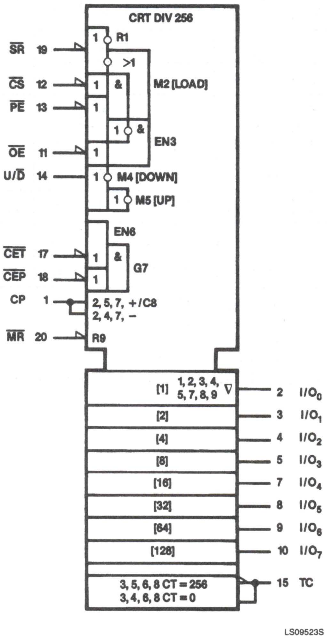
LOGIC SYMBOL



13 12 20 19 14
PE CS MR SR U/D
1 CP
18 CEP
17 CET
11 OE
TC 15
I/O0 I/O1 I/O2 I/O3 I/O4 I/O5 I/O6 I/O7
2 3 4 5 7 8 9 10
LS04640S

V_{CC} = Pin 16
GND = Pin 6

LOGIC SYMBOL (IEEE/IEC)



CRT DIV 256
SR 19
CS 12
PE 13
OE 11
U/D 14
CET 17
CEP 18
CP 1
MR 20
1 R1
>1
1 & M2 [LOAD]
1
1 & EN3
1
1 M4 [DOWN]
1 M5 [UP]
EN6
1 & G7
1
2, 5, 7, +/C8
2, 4, 7, −
R9
[1] 1, 2, 3, 4, 5, 7, 8, 9 ∇
[2]
[4]
[8]
[16]
[32]
[64]
[128]
3, 5, 6, 8 CT = 256
3, 4, 6, 8 CT = 0
2 I/O0
3 I/O1
4 I/O2
5 I/O3
7 I/O4
8 I/O5
9 I/O6
10 I/O7
15 TC
LS09523S

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$I/O_0 - I/O_7$	Data inputs	3.5/1.0	70μA/0.6mA
	Data outputs	150/40	3mA/24mA
$\overline{PE}$	Parallel Enable input (active-Low)	1.0/1.0	20μA/0.6mA
$U/\overline{D}$	Up-down count control input	1.0/1.0	20μA/0.6mA
$\overline{MR}$	Master Reset input (active-Low)	1.0/1.0	20μA/0.6mA
$\overline{SR}$	Synchronous reset input (active-Low)	1.0/1.0	20μA/0.6mA
$\overline{CEP}$	Count Enable parallel input (active-Low)	1.0/1.0	20μA/0.6mA
$\overline{CET}$	Count Enable trickle input (active-Low)	1.0/1.0	20μA/0.6mA
$\overline{CS}$	Chip Select input (active-Low)	1.0/1.0	20μA/0.6mA
$\overline{OE}$	Output Enable input (active-Low)	1.0/1.0	20μA/0.6mA
CP	Clock Pulse input (active rising edge)	1.0/1.0	20μA/0.6mA
$\overline{TC}$	Terminal Count output (active-Low)	50/33	1.0mA/20mA

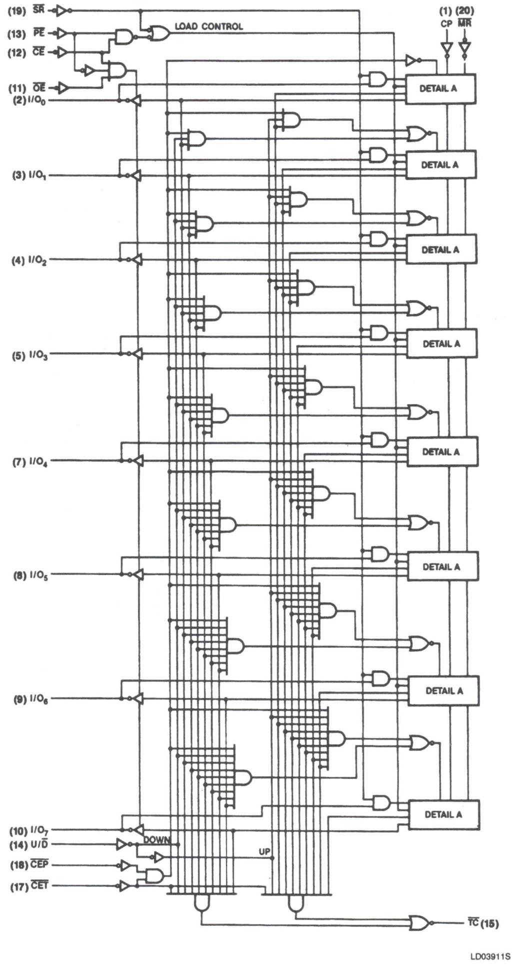
NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

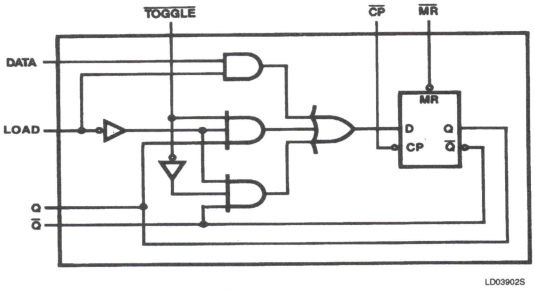
FUNCTION TABLE

$\overline{MR}$	$\overline{SR}$	$\overline{CS}$	$\overline{PE}$	$\overline{CEP}$	$\overline{CET}$	$U/\overline{D}$	$\overline{OE}$	CP	FUNCTION
X	X	H	X	X	X	X	X	X	I/O_0 to I/O_7 in Hi-Z ($\overline{PE}$ disabled)
X	X	L	H	X	X	X	H	X	I/O_0 to I/O_7 in Hi-Z
X	X	L	H	X	X	X	L	X	Flip-flop outputs appear on I/O lines
L	X	X	X	X	X	X	X	X	Asynchronous reset for all flip-flops
H	L	X	X	X	X	X	X	↑	Synchronous reset for all flip-flops
H	H	L	L	X	X	X	X	↑	Parallel load all flip-flops
H	H	(not LL)		H	X	X	X	↑	Hold
H	H	(not LL)		X	H	X	X	↑	Hold ($\overline{TC}$ held high)
H	H	(not LL)		L	L	H	X	↑	Count up
H	H	(not LL)		L	L	L	X	↑	Count down

H = High voltage level
L = Low voltage level
X = Don't Care
↑ = Low-to-High clock transition
(not LL) = $\overline{CS}$ and $\overline{PE}$ should never both be Low voltage level at the same time

LOGIC DIAGRAM


(19) $\overline{SR}$
(13) $\overline{PE}$
(12) $\overline{CE}$
(11) $\overline{OE}$
(2) I/O$_0$
LOAD CONTROL
(1) (20)
CP $\overline{MR}$
DETAIL A
(3) I/O$_1$
(4) I/O$_2$
(5) I/O$_3$
(7) I/O$_4$
(8) I/O$_5$
(9) I/O$_6$
(10) I/O$_7$
(14) U/$\overline{D}$
(18) $\overline{CEP}$
(17) $\overline{CET}$
DOWN
UP
$\overline{TC}$ (15)
LD03911S


$\overline{TOGGLE}$
$\overline{CP}$
$\overline{MR}$
DATA
LOAD
Q
$\overline{Q}$
MR
D
Q
CP
$\overline{Q}$
LD03902S

Detail A

V_{CC} = Pin 16
GND = Pin 6
( ) = Pin numbers

Counter

FAST 74F579

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		−0.5 to +7.0	V
V_{IN}	Input voltage		−0.5 to +7.0	V
I_{IN}	Input current		−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		−0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	$\overline{TC}$	40	mA
		I/O_n	48	mA
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		−65 to 150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	High-level output current	$\overline{TC}$			−1	mA
		I/O_n			−3	mA
I_{OL}	Low-level output current	$\overline{TC}$			20	mA
		I/O_n			24	mA
T_A	Operating free-air temperature		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			74F579			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage	$\overline{TC}$	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN (V_{IL} = 0.0V V_{IH} = 4.5V for $\overline{MR}$, CP inputs)	I_{OH} = −1mA	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7	3.4		V
		I/O_n		I_{OH} = −3mA	±10%V_{CC}	2.4	3.3		V
					±5%V_{CC}	2.7	3.3		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX		±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$				−0.73	−1.2	V
I_I	Input current at maximum input voltage	I/O_n	V_{CC} = MAX, V_I = 5.5V					1.0	mA
		Others	V_{CC} = MAX, V_I = 7.0V					100	μA
I_{IH}	High-level input current	All inputs except I/O_n	V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					−0.6	mA
I_{OZH} $+I_{IH}$	OFF-state current High-level voltage applied	I/O_n	V_{CC} = MAX, V_I = 2.7V					70	μA
I_{OZL} $+I_{IL}$	OFF-state current Low-level voltage applied		V_{CC} = MAX, V_I = 0.5V					−600	μA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX			−60	−80	−150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				95	135	mA
		I_{CCL}					105	145	mA
		I_{CCZ}					105	150	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

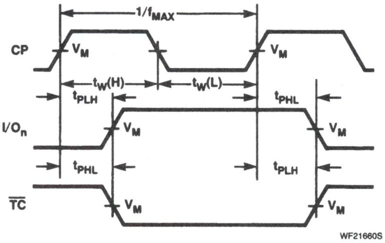
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F579					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	100	115		80		MHz
t_{PLH} t_{PHL}	Propagation Delay CP to I/O_n	Waveform 1	5.0 5.0	7.5 7.5	10.5 10.5	5.0 5.0	11.5 11.5	ns
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{TC}$	Waveform 1	5.5 5.5	7.5 7.5	10.0 10.0	5.0 5.0	11.0 11.0	ns
t_{PLH} t_{PHL}	Propagation Delay U/$\overline{D}$ to $\overline{TC}$	Waveform 4	3.5 4.5	5.5 6.5	8.0 8.0	3.5 4.5	9.0 9.0	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{CET}$ to $\overline{TC}$	Waveform 3	3.5 3.5	5.5 6.0	7.0 8.0	3.5 3.5	8.5 8.5	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to I/O_n	Waveform 2	5.0	7.0	9.0	5.0	10.0	ns
t_{PHZ} t_{PLZ}	Output Enable Time to High or Low level $\overline{CS}$,$\overline{PE}$ to I/O_n	Waveform 6 Waveform 7	6.0 6.5	8.0 9.0	10.5 10.5	6.0 6.0	11.5 11.5	ns
t_{PZH} t_{PZL}	Output Disable Time from High or Low level $\overline{CS}$, $\overline{PE}$ to I/O_n	Waveform 6 Waveform 7	3.0 6.5	6.0 8.5	7.5 9.5	3.0 6.0	9.0 11.0	ns
t_{PHZ} t_{PLZ}	Output Enable Time to High or Low level $\overline{OE}$ to I/O_n	Waveform 6 Waveform 7	4.0 6.5	6.5 8.5	8.5 9.5	4.0 5.0	9.5 10.5	ns
t_{PZH} t_{PZL}	Output Disable Time from High or Low level $\overline{OE}$ to I/O_n	Waveform 6 Waveform 7	1.0 2.5	2.5 5.0	4.0 7.0	1.0 2.5	5.5 8.0	ns

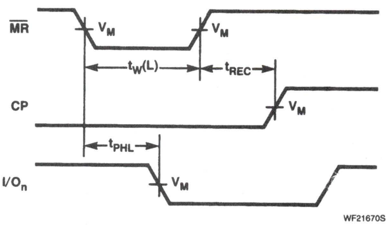
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	74F579					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low I/O_n to CP	Waveform 5	3.0 3.0			4.0 4.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low I/O_n to CP	Waveform 5	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{PE}$,$\overline{SR}$ or $\overline{CS}$ to CP	Waveform 5	9.5 9.5			10.0 10.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{PE}$, $\overline{SR}$ or $\overline{CS}$ to CP	Waveform 5	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{CET}$ or $\overline{CEP}$ to CP	Waveform 5	5.0 9.0			5.5 10.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{CET}$ or $\overline{CEP}$ to CP	Waveform 5	0 0			0 0		ns
t_W	Clock pulse width	Waveform 1	4.5			6.0		ns
$t_w(L)$	$\overline{MR}$ Pulse Width	Waveform 2	3.0			3.0		ns
t_{rec}	$\overline{MR}$ Recovery Time	Waveform 2	4.0			4.5		ns

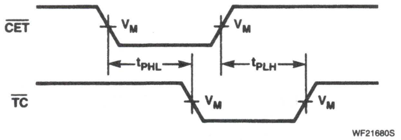
AC WAVEFORMS


1/fMAX
CP
VM
VM
tW(H)
tW(L)
tPLH
tPHL
I/On
VM
VM
tPHL
tPLH
TC
VM
VM
WF21660S

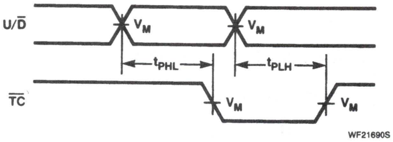
Waveform 1. Propagation Delay, Clock Input to Output, Clock Widths and Maximum Clock Fequency


MR
VM
VM
tW(L)
tREC
CP
VM
tPHL
I/On
VM
WF21670S

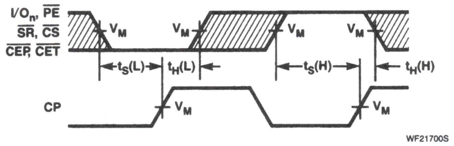
Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time


CET
VM
VM
tPHL
tPLH
TC
VM
VM
WF21680S

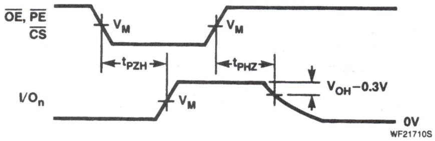
Waveform 3. Propagation Delay, $\overline{CET}$ input to Terminal Count Output


U/D
VM
VM
tPHL
tPLH
TC
VM
VM
WF21690S

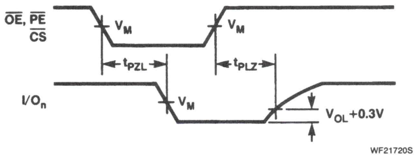
Waveform 4. Propagation Delay, U/$\overline{D}$ to Terminal Count Output


I/On, PE
SR, CS
CEP, CET
VM
VM
VM
VM
tS(L)
tH(L)
tS(H)
tH(H)
CP
VM
VM
WF21700S

Waveform 5. Setup And Hold Times


OE, PE
CS
VM
VM
tPZH
tPHZ
VOH−0.3V
I/On
VM
0V
WF21710S

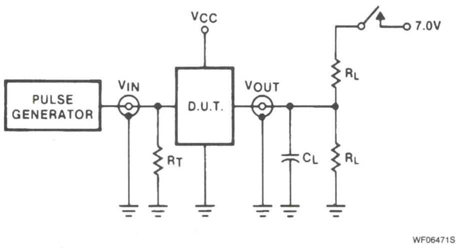
Waveform 6. 3-State Output Enable Time to High Level and Output Disable Time From High Level


OE, PE
CS
VM
VM
tPZL
tPLZ
I/On
VM
VOL+0.3V
WF21720S

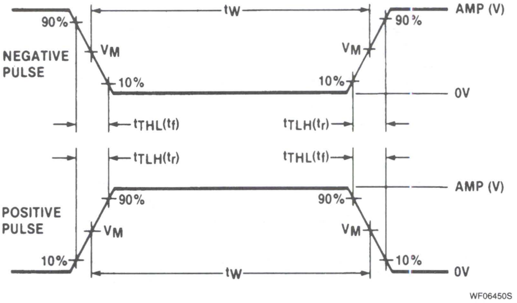
Waveform 7. 3-State Output Enable Time to Low Level and Output Disable Time From Low Level

NOTE: $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS


VCC
7.0V
RL
PULSE GENERATOR
VIN
D.U.T.
VOUT
RT
CL
RL
WF06471S

Test Circuit for 3-State Outputs


tW
AMP (V)
90%
NEGATIVE PULSE
VM
10%
0V
tTHL(tf)
tTLH(tr)
POSITIVE PULSE
AMP (V)
90%
VM
10%
0V
tW
WF06450S

$V_M = 1.5V$

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F582
4-Bit BCD Arithmetic Logic Unit

Product Specification

Logic Products

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F582	12ns	55mA

FEATURES

- **Performs four BCD functions**
- **$\overline{P}$ and $\overline{G}$ outputs for high-speed expansion**
- **Add/Subtract delay 28ns max**
- **Look-ahead delay 22.5ns max**
- **Supply current 85mA max**
- **24-pin 300mil Slim DIP package**

DESCRIPTION

The 'F582 Binary Coded Decimal (BCD) Arithmetic Logic Unit (ALU) is a 24-pin expandable unit that performs addition, subtraction, comparison of two numbers, and binary to BCD conversion.

The 'F582 input and output logic includes a Carry/$\overline{\text{Borrow}}$ which is generated internally in the look-ahead mode, allowing BCD arithmetic to be computed directly. For more than one BCD decade, the Carry/$\overline{\text{Borrow}}$ term may ripple between 'F582s.

When $\overline{A}$/S is Low, BCD addition is performed (A + B + C/$\overline{B}$ = F). If an input is greater than 9, binary to BCD conversion results at the output.

When A/$\overline{S}$ is High, subtraction is performed. If the C/$\overline{B}$ is Low, then the subtraction is accomplished by internally computing the nine's complement addition of two BCD numbers (A – B – 1 = F). When C/$\overline{B}$ is High, the difference of the two numbers is figured as A – F = F. If: A is greater than or equal to B, the BCD difference appears at the output F in its true form. If: A is less than B and C/$\overline{B}$ is Low, the nine's complement of the true form appears at the output F.

As long as A is less than B, an active-Low borrow is also generated. The 'F582 also performs binary to BCD conversion. For inputs between 10 and 15, binary to BCD conversion occurs by grounding one set of inputs, A_n or B_n, and applying the binary number to the other set of inputs. This will generate a carry term to the next decade.

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V± 5%; T_A = 0°C to +70°C
24-Pin Plastic Slim DIP (300mil)	N74F582N
24-Pin Plastic SOL	N74F582D

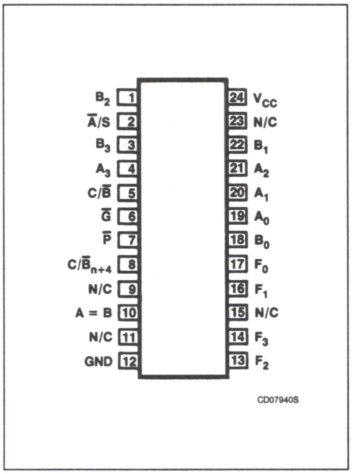
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$A_0 - A_3$	A operand inputs	1.0/2.0	20μA/1.2mA
B_0	B operand input	1.0/1.0	20μA/0.6mA
B_1	B operand input	1.0/4.0	20μA/2.4mA
B_2	B operand input	1.0/3.0	20μA/1.8mA
B_3	B operand input	1.0/2.0	20μA/1.2mA
$\overline{A}$/S	Add/subtract input	1.0/3.0	20μA/1.8mA
C/$\overline{B}$	Carry/borrow input	1.0/1.0	20μA/0.6mA
C/$\overline{B}_{n+4}$	Carry/borrow output	50/33	1.0mA/20mA
$\overline{P}$	Carry propagate output	50/33	1.0mA/20mA
$\overline{G}$	Carry generate output	50/33	1.0mA/20mA
A = B	Comparator output	OC*/33	OC*/20mA
$F_0 - F_3$	Outputs	50/33	1.0mA/20mA

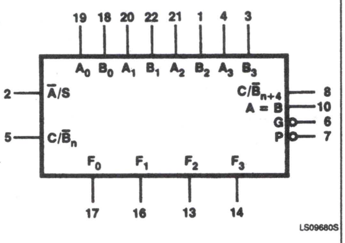
NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

4-Bit BCD Arithmetic Logic Unit **FAST 74F582**

PIN CONFIGURATION

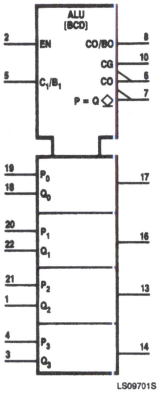

B_2 1
$\overline{A}/S$ 2
B_3 3
A_3 4
$C/\overline{B}$ 5
$\overline{G}$ 6
$\overline{P}$ 7
$C/\overline{B}_{n+4}$ 8
N/C 9
A = B 10
N/C 11
GND 12
24 V_{CC}
23 N/C
22 B_1
21 A_2
20 A_1
19 A_0
18 B_0
17 F_0
16 F_1
15 N/C
14 F_3
13 F_2
CD07940S

LOGIC SYMBOL


19 18 20 22 21 1 4 3
A_0 B_0 A_1 B_1 A_2 B_2 A_3 B_3
2 $\overline{A}/S$
5 $C/\overline{B}_n$
$C/\overline{B}_{n+4}$ 8
A = B 10
G 6
P 7
F_0 F_1 F_2 F_3
17 16 13 14
LS09680S

V_{CC} = Pin 24
GND = Pin 12

LOGIC SYMBOL (IEEE/IEC)


ALU
[BCD]
2 EN
5 C_1/B_1
CO/BO 8
CG 10
CO 6
P = Q 7
19 P_0
18 Q_0
20 P_1
22 Q_1
21 P_2
1 Q_2
4 P_3
3 Q_3
17
16
13
14
LS09701S

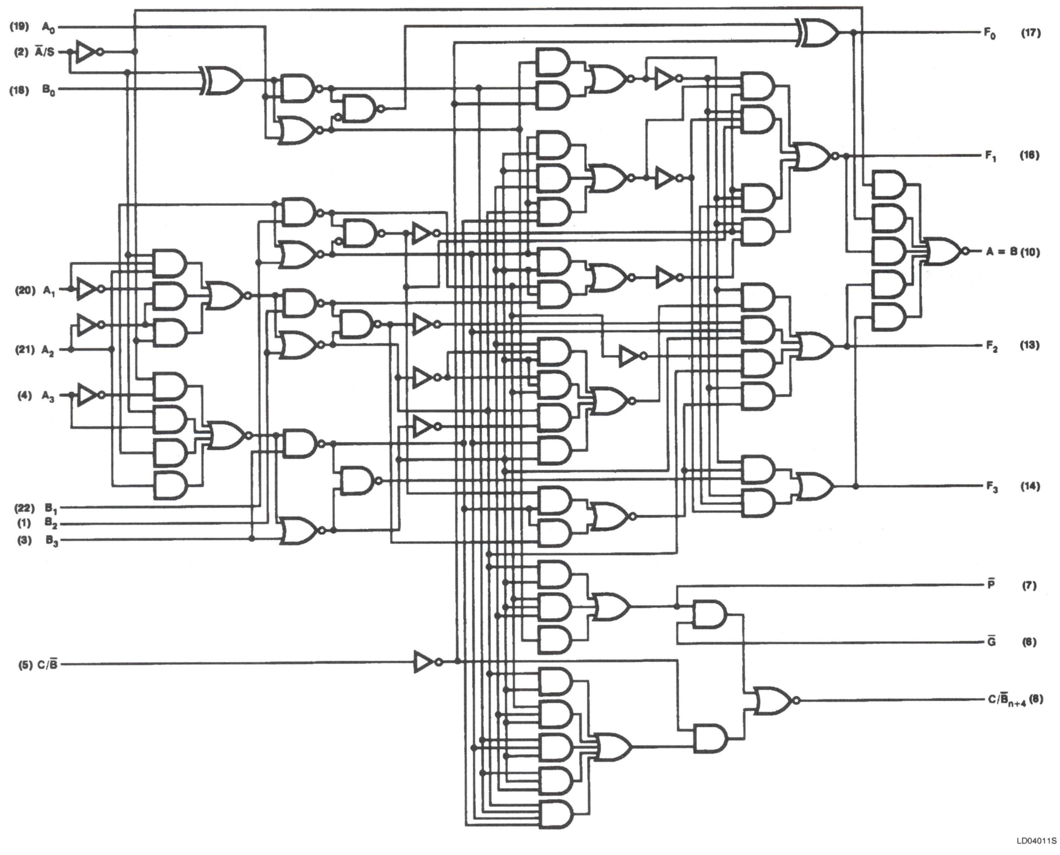
FUNCTION TABLE

OPERATING MODE	INPUTS				OUTPUTS		
	$\overline{A}/S$	A_n	B_n	$C/\overline{B}$	F_n	$C/\overline{B}_{n+4}$	(Compare) A = B
Add	L	BCD Augend	BCD Addend	H = Carry L = No Carry	IF $C/\overline{B}$ = H F = A+B+1 IF $C/\overline{B}$ = L F = A+B	F≤9 $C/\overline{B}_{n+4}$ = L F>9 $C/\overline{B}_{n+4}$ = H	X
Subtract	H	BCD Minuend	BCD Subtrahend	L = Borrow H = No Borrow	IF $C/\overline{B}$ = L F = A−B−1 IF $C/\overline{B}$ = H F = A−B	A>B $C/\overline{B}_{n+4}$ = H A≤B $C/\overline{B}_{n+4}$ = L A<B $C/\overline{B}_{n+4}$ = L A≥B $C/\overline{B}_{n+4}$ = H	X
Compare	H	BCD Word A	BCD Word B	H	A−B	A<B $C/\overline{B}_{n+4}$ = L A>B $C/\overline{B}_{N+4}$ = H	IF A = B Compare = H IF A ≠ B Compare = L
Binary to BCD Conversion	L	0<A<15	B = 0	X	BCD	A≤9 $C/\overline{B}_{n+4}$ = L A>9 $C/\overline{B}_{n+4}$ = H	X

4-Bit BCD Arithmetic Logic Unit

FAST 74F582

LOGIC DIAGRAM


(19) A_0
(2) $\overline{A}/S$
(18) B_0
(20) A_1
(21) A_2
(4) A_3
(22) B_1
(1) B_2
(3) B_3
(5) $C/\overline{B}$
F_0 (17)
F_1 (16)
A = B (10)
F_2 (13)
F_3 (14)
$\overline{P}$ (7)
$\overline{G}$ (6)
$C/\overline{B}_{n+4}$ (8)
LD04011S

V_{CC} = Pin 24
GND = Pin 12
( ) = Pin numbers

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5.0	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
V_{OH}	High-level output voltage	A = B only			4.5	V
I_{OH}	High-level output current	except A = B			−1	mA
I_{OL}	Low-level output current				20	mA
T_A	Operating free-air temperature		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		74F582			UNIT
					Min	Typ[2]	Max	
I_{OH}	High-level output current	A = B only	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, V_{OH} = MAX				250	μA
V_{OH}	High-level output voltage	Any output except A = B	V_{CC} = MIN V_{IL} = MAX I_{OH} = MAX V_{IH} = MIN	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN V_{IL} = MAX I_{OL} = MAX V_{IH} = MIN	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current	B_0, $C/\overline{B}$	V_{CC} = MAX, V_I = 0.5V				−0.6	mA
		A_n, B_3					−1.2	mA
		B_2, $\overline{A}/S$					−1.8	mA
		B_1					−2.4	mA
I_{OS}	Short-circuit output current[3]	Any output except A = B	V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current (total)		V_{CC} = MAX			55	85	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of High-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

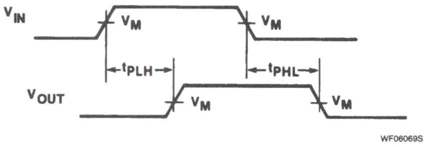
4-Bit BCD Arithmetic Logic Unit

FAST 74F582

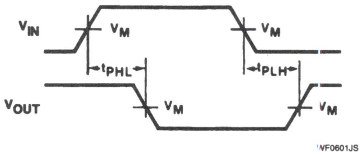
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F582					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n or B_n to F_n	Waveform 1, 2	5.0 4.0	17.5 14.0	23.0 19.0	5.0 4.0	25.0 20.0	ns
t_{PLH} t_{PHL}	Propagation delay A_n or B_n to $C/\overline{B}_{n+4}$	Waveform 1, 2	7.0 4.0	16.0 10.0	20.0 14.0	6.0 4.0	22.5 16.0	ns
t_{PLH} t_{PHL}	Propagation delay $C/\overline{B}_n$ to $C/\overline{B}_{n+4}$	Waveform 1, 2	3.5 2.5	5.5 5.0	8.0 7.0	3.0 2.5	8.5 7.5	ns
t_{PLH} t_{PHL}	Propagation delay A_n or B_n to $A = B$	Waveform 1, 2	8.0 6.0	18.0 14.0	24.0 18.0	8.0 5.5	27.0 21.5	ns
t_{PLH} t_{PHL}	Propagation delay A_n or B_n to $\overline{G}$ or $\overline{P}$	Waveform 1, 2	4.0 4.0	11.0 11.0	14.0 14.0	4.0 4.0	16.5 16.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}/S$ to F_n	Waveform 1, 2	8.0 8.0	15.0 14.0	20.0 18.0	7.0 7.0	25.0 19.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}/S$ to $A = B$	Waveform 1, 2	10.0 4.0	18.0 6.0	24.0 9.0	10.0 3.5	28.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}/S$ to $\overline{G}$ or $\overline{P}$	Waveform 1, 2	6.0 6.0	11.0 11.0	14.5 14.5	6.0 6.0	16.0 16.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}/S$ to $C/\overline{B}_{n+4}$	Waveform 1, 2	8.0 7.0	14.0 12.0	19.0 15.0	8.0 7.0	20.5 16.5	ns
t_{PLH} t_{PHL}	Propagation delay $C/\overline{B}_n$ to F_n	Waveform 1, 2	4.0 3.0	13.0 9.0	17.5 13.0	4.0 3.0	18.5 14.0	ns
t_{PLH} t_{PHL}	Propagation delay $C/\overline{B}_n$ to $A = B$	Waveform 1, 2	8.0 4.0	15.0 8.0	20.0 12.0	8.0 3.5	22.5 13.0	ns

AC WAVEFORMS



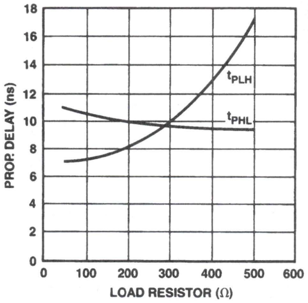
Waveform 1. Propagation Delay for Non-Inverting Outputs



Waveform 2. Propagation Delay for Inverting Outputs

NOTE: $V_M = 1.5V$.

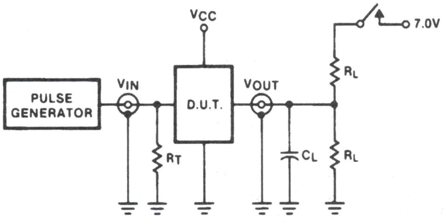
TYPICAL PROPAGATION DELAYS VERSUS LOAD RESISTOR FOR OPEN-COLLECTOR OUTPUTS



OP19810S

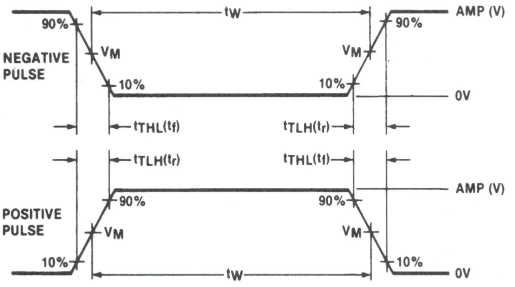
NOTE:
When using Open-Collector parts, the value of the pull-up resistor greatly affects the value of the t_{PLH}. For example, changing the specified pull-up resistor value from 500Ω to 100Ω will improve the t_{PLH} up to 50% with only a slight increase in the t_{PHL}. However, if the value of the pull-up resistor is changed, the user must make certain that the total I_{OL} current through the resistor and the total I_{IL}s of the receivers does not exceed the I_{OL} maximum specification.

TEST CIRCUIT AND WAVEFORMS


VCC
7.0V
PULSE GENERATOR
VIN
D.U.T.
VOUT
RL
RT
CL
RL

WF06471S

Test Circuit for Totem-Pole Outputs


tW
AMP (V)
90%
90%
NEGATIVE PULSE
VM
VM
10%
10%
0V
tTHL(tf)
tTLH(tr)
tTLH(tr)
tTHL(tf)
AMP (V)
90%
90%
POSITIVE PULSE
VM
VM
10%
10%
0V
tW

WF06450S

$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS
R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

FAST 74F583
4-Bit BCD Adder

Product Specification

FAST Products

FEATURES
- Adds two decimal numbers
- Full internal look-ahead
- Fast ripple carry for economical expansion
- Sum output delay 19.5ns max
- Ripple carry delay 8.5ns max
- Input to ripple delay 13.0ns max
- Supply current 60mA max

DESCRIPTION
The 'F583 4-bit coded (BCD) full adder performs the addition of two decimal numbers (A_0–A_3, B_0–B_3). The look-ahead generates BCD carry terms internally, allowing the 'F583 to then do BCD addition correctly. For BCD numbers 0 through 9 at A and B inputs, the BCD sum forms at the output.

In addition of two BCD numbers totalling a number greater than 9, a valid BCD number and a carry will result. For input values larger than 9, the number is converted from binary to BCD. Binary to BCD conversion occurs by grounding one set of inputs, A_n or B_n, and applying a 4-bit binary number to the other set of inputs. If the input is between 0 and 9, a BCD number occurs at the output. If the binary input falls between 10 and 15, a carry term is generated. Both the carry term and the sum are the BCD equivalent of the binary input. Converting binary numbers greater than 16 may be achieved by cascading 'F583s.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F583	9.0ns	45mA

ORDERING INFORMATION

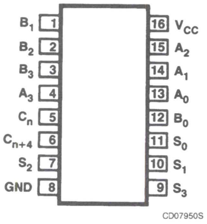
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ± 5%; T_A = 0°C to +70°C
16-Pin Plastic Slim DIP	74F583N
16-Pin Plastic SO	74F583D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$A_0 - A_3$	A operand inputs	1.0/2.0	20μA/1.2mA
$B_0 - B_3$	B operand inputs	1.0/2.0	20μA/1.2mA
C_n	Carry input	1.0/1.0	20μA/0.6mA
S_0–S_3	Sum outputs	50/33	1.0μA/20mA
C_{n+4}	Carry output	50/33	1.0μA/20mA

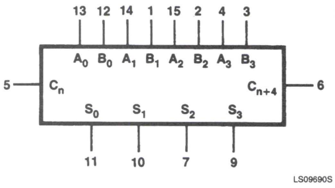
NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



B1 1
B2 2
B3 3
A3 4
Cn 5
Cn+4 6
S2 7
GND 8
16 VCC
15 A2
14 A1
13 A0
12 B0
11 S0
10 S1
9 S3
CD07950S

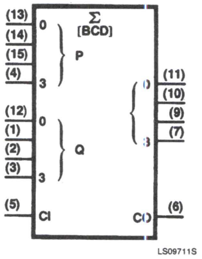
LOGIC SYMBOL



13
12
14
1
15
2
4
3
A0
B0
A1
B1
A2
B2
A3
B3
5
Cn
Cn+4
6
S0
S1
S2
S3
11
10
7
9
LS09690S

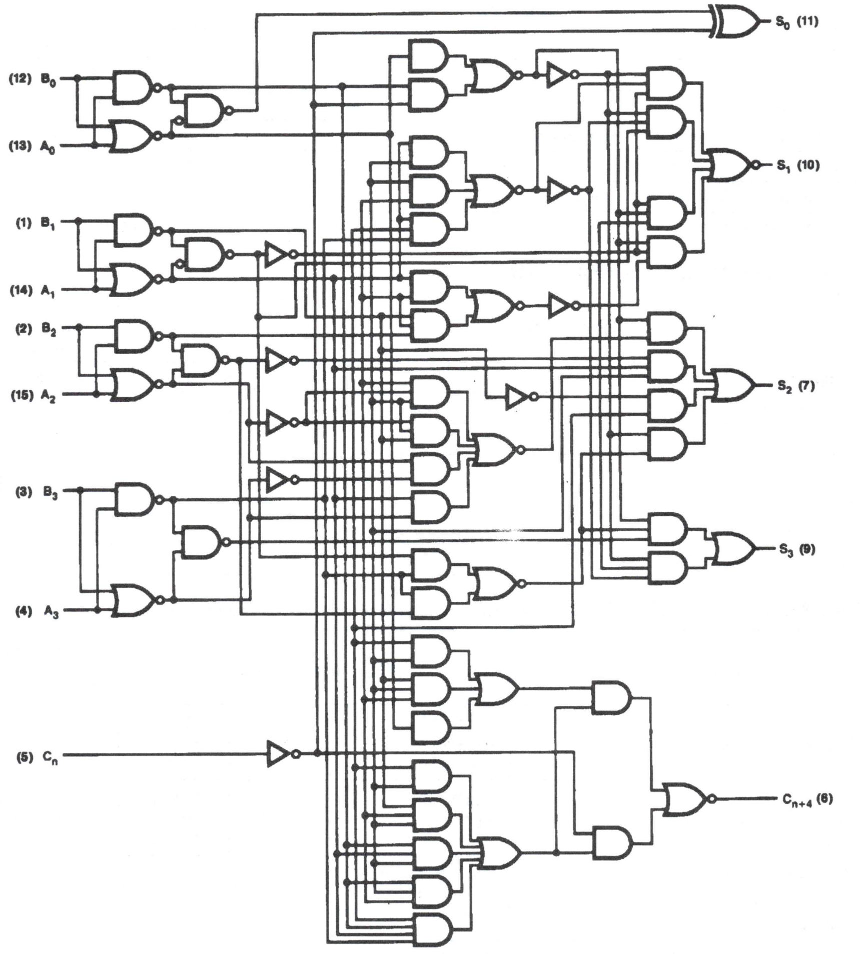
V_{CC} = Pin 16
GND = Pin 8

LOGIC SYMBOL (IEEE/IEC)



Σ
[BCD]
(13)
(14)
(15)
(4)
0
3
P
(12)
(1)
(2)
(3)
0
3
Q
(5)
CI
0
3
(11)
(10)
(9)
(7)
CO
(6)
LS09711S

LOGIC DIAGRAM


(12) B0
(13) A0
(1) B1
(14) A1
(2) B2
(15) A2
(3) B3
(4) A3
(5) Cn
S0 (11)
S1 (10)
S2 (7)
S3 (9)
Cn+4 (6)
LD04021S

V_{CC} = Pin 16
GND = Pin 8
( ) = Pin numbers

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	74F583	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5.0	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74F583			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			74F582, 74F583			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = MAX	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = MAX	±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$				−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V					100	μA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	Low-level input current	C_n only	V_{CC} = MAX, V_I = 0.5V					−0.6	mA
		A_n & B_n						−1.2	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX			−60		−150	mA
I_{CC}	Supply current (total)		V_{CC} = MAX				45	60	mA

NOTES:

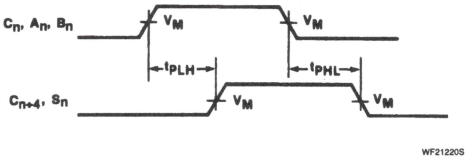
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

4-Bit BCD Adder FAST 74F583

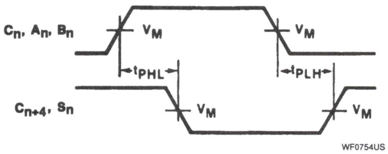
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F582					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n or B_n to S_n	Waveform 1	5.0 5.0	13.0 10.5	17.0 14.0	5.0 5.0	18.0 15.0	ns
t_{PLH} t_{PHL}	Propagation delay A_n or B_n to S_n (INV)	Waveform 2	6.0 4.0	11.0 8.0	18.0 12.0	5.0 4.0	19.5 12.5	ns
t_{PLH} t_{PHL}	Propagation delay C_n to C_{n+4}	Waveform 1, 2	3.5 2.5	5.0 4.0	8.0 7.0	3.0 2.0	8.5 7.0	ns
t_{PLH} t_{PHL}	Propagation delay A_n or B_n to C_{n+4}	Waveform 1, 2	5.0 5.0	8.0 7.5	11.5 10.5	4.5 4.5	13.0 11.5	ns
t_{PLH} t_{PHL}	Propagation delay C_n to S_n	Waveform 1	4.0 3.5	12.0 8.0	15.5 12.5	3.5 3.0	17.0 13.5	ns
t_{PLH} t_{PHL}	Propagation delay C_n to S_n (INV)	Waveform 2	6.0 3.5	9.5 8.0	13.0 11.5	5.0 3.0	14.5 12.0	ns

AC WAVEFORMS



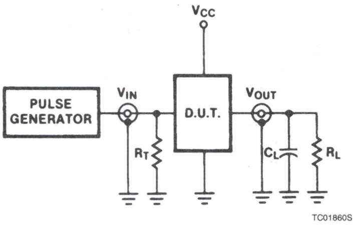
Waveform 1. Propagation Delay for Non-Inverting Outputs



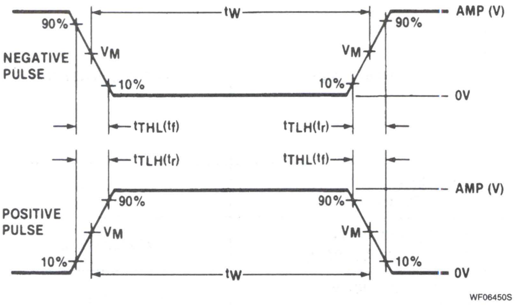
Waveform 2. Propagation Delay for Inverting Outputs

NOTE: $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORMS


V_{CC}
PULSE GENERATOR
V_{IN}
D.U.T.
V_{OUT}
R_T
C_L
R_L
TC01860S

Test Circuit for Totem-Pole Outputs


tW
90%
AMP (V)
NEGATIVE PULSE
VM
10%
0V
tTHL(tf)
tTLH(tr)
POSITIVE PULSE
WF06450S

$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST Products

FAST 74F588
Transceiver

Octal Bidirectional Transceiver With IEEE-488 Termination Resistors (3-State Inputs and Outputs)
Product Specification

FEATURES
- **High-impedance NPN base input for reduced loading (70μA in High and Low states)**
- **Non-inverting buffers**
- **Bidirectional data path**
- **B outputs sink 48mA, source 15mA**

DESCRIPTION
The 'F588 contains eight non-inverting bidirectional buffers with 3-State outputs and is intended for bus-oriented applications. The B ports have termination resistors as specified in the IEEE-488 specifications. Current sinking capability is 20mA at the A ports and 48mA at the B ports. The Transmit/Receive (T/$\overline{R}$) input determines the direction of data flow through the bidirectional transceiver. Transmit (active-High) enables data from A ports to B ports and Receive (active-Low) enables data from B ports to A ports. The Output Enable input, when High, disables both A and B ports by placing them in a high-impedance condition.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F588	4.0ns	96mA

ORDERING INFORMATION

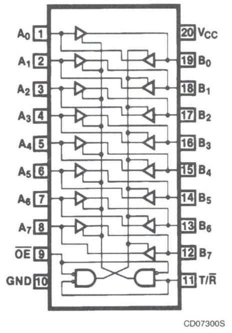
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F588N
20-Pin Plastic SOL	N74F588D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

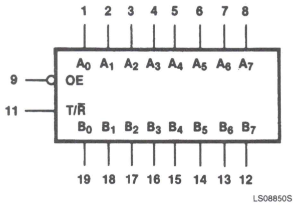
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$A_0 - A_7$	Port A data inputs	3.5/0.115	70μA/70μA
$B_0 - B_7$	Port B data inputs	*T/5.33	*T/3.2mA
T/$\overline{R}$	Transmit/receive input	2.0/0.067	40μA/40μA
$\overline{OE}$	Output enable input (active-Low)	2.0/0.067	40μA/40μA
$A_0 - A_7$	Port A data outputs	150/40	3mA/24mA
$B_0 - B_7$	Port B data outputs	750/106.7	15mA/64mA

NOTES:
1. One (1.0) FAST unit load is defined as: 20μA in the High state and 0.6mA in the Low state.
2. *T = Resistance Termination per IEEE-488 Standard.

PIN CONFIGURATION

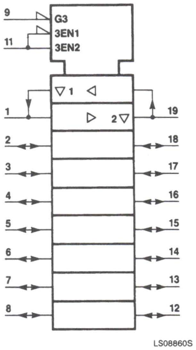

A0 1
A1 2
A2 3
A3 4
A4 5
A5 6
A6 7
A7 8
$\overline{OE}$ 9
GND 10
20 VCC
19 B0
18 B1
17 B2
16 B3
15 B4
14 B5
13 B6
12 B7
11 T/$\overline{R}$
CD07300S

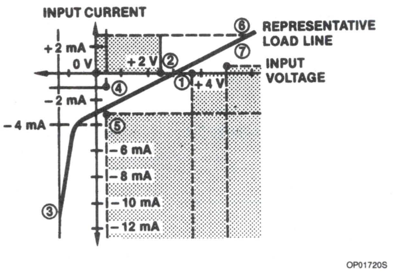
LOGIC SYMBOL


1 2 3 4 5 6 7 8
A0 A1 A2 A3 A4 A5 A6 A7
9 OE
11 T/$\overline{R}$
B0 B1 B2 B3 B4 B5 B6 B7
19 18 17 16 15 14 13 12
LS08850S

V_{CC} = Pin 20
GND = Pin 10

LOGIC SYMBOL (IEEE/IEC)


9
11
G3
3EN1
3EN2
▽1 ◁
▷ 2▽
1
2
3
4
5
6
7
8
19
18
17
16
15
14
13
12
LS08860S



①, ② No-load voltage
③ Clamp diode
④, ⑤ I_{IL}
⑥, ⑦ I_{IH}

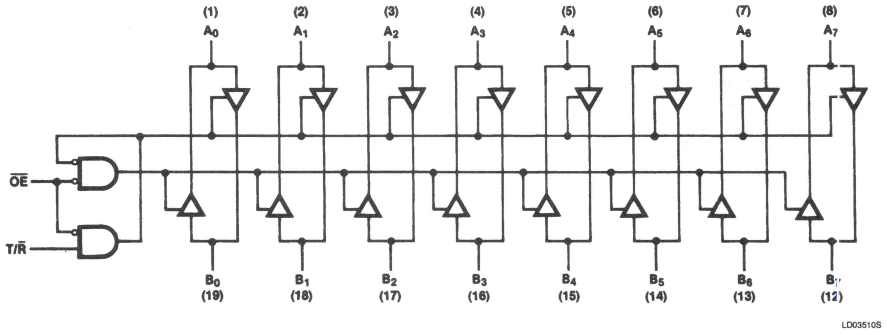
B Port Input Characteristics with $T/\overline{R}$ Low

FUNCTION TABLE

INPUTS		OUTPUTS
$\overline{OE}$	$T/\overline{R}$	
L	L	Bus B data to bus A
L	H	Bus A data to bus B
H	X	High impedance

H = High voltage level
L = Low voltage level
X = Don't care

LOGIC DIAGRAM


(1) A_0
(2) A_1
(3) A_2
(4) A_3
(5) A_4
(6) A_5
(7) A_6
(8) A_7
$\overline{OE}$
$T/\overline{R}$
B_0 (19)
B_1 (18)
B_2 (17)
B_3 (16)
B_4 (15)
B_5 (14)
B_6 (13)
B_7 (12)
LD03510S

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		−0.5 to +7.0	V
V_{IN}	Input voltage		−0.5 to +7.0	V
I_{IN}	Input current		−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		−0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	$A_0 - A_7$	48	mA
		$B_0 - B_7$	128	mA
T_A	Operating free-air temperature range		0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	High-level output current	$A_0 - A_7$			−3	mA
		$B_0 - B_7$			−15	mA
I_{OL}	Low-level output current	$A_0 - A_7$			24	mA
		$B_0 - B_7$			64	mA
T_A	Operating free-air temperature		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS^1			74F588			UNIT
						Min	Typ^2	Max	
V_{OH}	High-level output voltage	$A_0 - A_7$ $B_0 - B_7$	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, $\overline{OE}$ = 0.0V	I_{OH} = −3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.4		V
		$B_0 - B_7$		I_{OH} = −15mA	±10%V_{CC}	2.0			V
					±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage	$A_0 - A_7$	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, $\overline{OE}$ = 0.0V	I_{OL} = 24mA	±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
		$B_0 - B_7$		I_{OL} = 48mA	±10%V_{CC}		0.40	0.55	V
				I_{OL} = 64mA	±5%V_{CC}		0.40	0.55	V
V_{NL}	No load voltage	$B_0 - B_7$	I_{OUT} = 0mA, T/$\overline{R}$ = 0.0V			2.5		3.7	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$				−0.73	−1.2	V
I_I	Input current at maximum input voltage	$A_0 - A_7$	V_{CC} = 5.5V, V_I = 5.5V					1.0	mA
		$\overline{OE}$, T/$\overline{R}$	V_{CC} = 0.0V, V_I = 7.0V					100	μA
I_{IH}	High-level input current	$\overline{OE}$, T/$\overline{R}$	V_{CC} = MAX, V_I = 2.7V					40	μA
I_{IL}	Low-level input current	$\overline{OE}$, T/$\overline{R}$	V_{CC} = MAX, V_I = 0.5V					−40	μA
I_{OZH} + I_{IH}	OFF-state current, High-level voltage applied	$A_0 - A_7$	V_{CC} = MAX, V_I = 2.7V, T/$\overline{R}$ = 4.5V					70	μA
I_{OZL} + I_{IL}	OFF-state current, Low-level voltage applied	$A_0 - A_7$	V_{CC} = MAX, V_I = 0.5V, T/$\overline{R}$ = 4.5V					−70	μA
I_{OZH} + I_{IH}	OFF-state current, High-level voltage applied	$B_0 - B_7$	V_{CC} = MAX, V_I = 5.0V, T/$\overline{R}$ = 0.0V			0.7			mA
			V_{CC} = MAX, V_I = 5.5V, T/$\overline{R}$ = 0.0V					2.5	mA
I_{OZL} + I_{IL}	OFF-state current Low-level voltage applied	$B_0 - B_7$	V_{CC} = MAX, V_I = 0.4V, T/$\overline{R}$ = 0.0V			−1.3		−3.2	mA
I_{OS}	Short-circuit output current^3	$A_0 - A_7$	V_{CC} = MAX			−60		−150	mA
		$B_0 - B_7$				−100		−225	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	A_n = T/$\overline{R}$ = 4.5V; $\overline{OE}$ = 0.0V			82	100	mA
		I_{CCL}		A_n = $\overline{OE}$ = 0.0V; T/$\overline{R}$ = 4.5V			110	135	mA
		I_{CCZ}		$\overline{OE}$ = 4.5V			95	125	mA

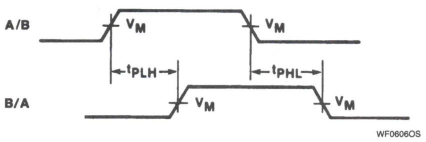
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

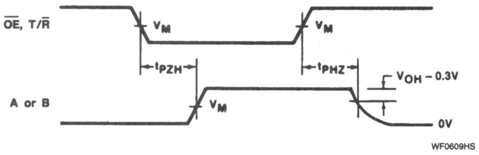
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F588					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH}	Propagation delay A_n to B_n, B_n to A_n	Waveform 1	2.0	3.5	6.0	2.0	7.0	ns
t_{PHL}			2.5	4.5	7.0	2.0	7.5	
t_{PZH}	Output enable time to High or Low level	Waveform 2	5.5	7.5	10.0	5.5	11.0	ns
t_{PZL}		Waveform 3	5.0	7.5	9.5	5.0	10.0	
t_{PHZ}	Output disable time from High or Low level	Waveform 2	2.5	4.5	7.0	2.5	8.0	ns
t_{PLZ}		Waveform 3	2.5	4.0	7.0	2.5	7.5	

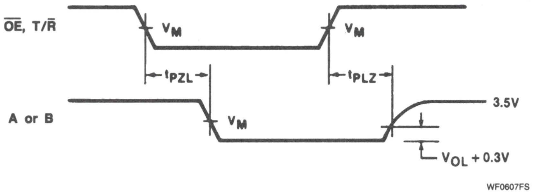
AC WAVEFORMS


A/B
V_M
V_M
t_{PLH}
t_{PHL}
B/A
V_M
V_M
WF06060S

Waveform 1. For Non-Inverting Outputs


$\overline{OE}$, T/$\overline{R}$
V_M
V_M
t_{PZH}
t_{PHZ}
$V_{OH} - 0.3V$
A or B
V_M
0V
WF0609HS

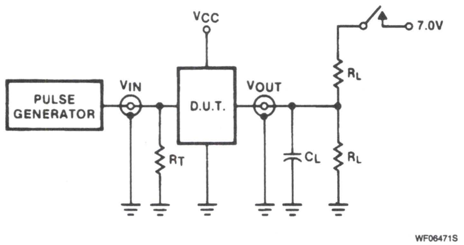
Waveform 2. 3-State Output Enable Time to High Level and Output Disable Time From High Level

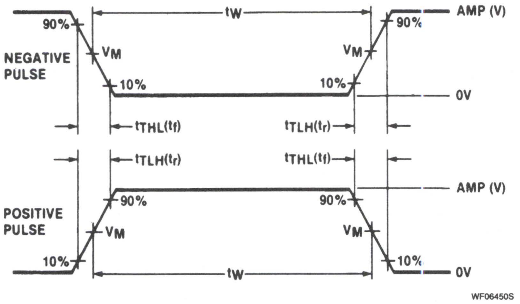

$\overline{OE}$, T/$\overline{R}$
V_M
V_M
t_{PZL}
t_{PLZ}
A or B
V_M
3.5V
$V_{OL} + 0.3V$
WF0607FS

Waveform 3. 3-State Output Enable Time to Low Level and Output Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORMS


VCC
PULSE GENERATOR
VIN
D.U.T.
VOUT
7.0V
RL
RT
CL
RL
WF06471S


tW
AMP (V)
90%
90%
NEGATIVE PULSE
VM
VM
10%
10%
0V
tTHL(tf)
tTLH(tr)
tTLH(tr)
tTHL(tf)
AMP (V)
90%
90%
POSITIVE PULSE
VM
VM
10%
10%
0V
tW
WF06450S

Test Circuit for 3-State Outputs

$V_M = 1.5V$

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F595
8-Bit Shift Register

8-Bit Shift Register with Output Latches (3-State)
Preliminary Specification

FAST Products

FEATURES

- **High-impedance NPN base input for reduced loading (20μA in High and Low states)**
- **8-bit serial-in, parallel-out shift-register with storage**
- **3-State outputs**
- **Shift-register has direct clear**
- **Guaranteed shift frequency – DC to 120MHz**

DESCRIPTION

This device contains an 8-bit serial-in, parallel-out shift-register that feeds an 8-bit D-type storage register. The storage register has parallel 3-State outputs. Separate clocks are provided for both the shift-register and the storage register. The shift-register has a direct overriding clear, Serial input, and Serial output pins for cascading.

Both the shift-register and storage register clocks are positive edge-triggered. If the user wishes to connect both clocks together, the shift-register state will always be one clock pulse ahead of the storage register.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F595	120MHz	75mA

ORDERING INFORMATION

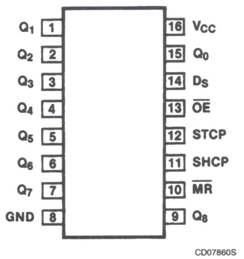
PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
16-Pin Plastic DIP	N74F595N
16-Pin Plastic SO	N74F595D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_S	Serial data input	1.0/0.033	20μA/20μA
SHCP	Shift register clock pulse input	1.0/0.033	20μA/20μA
STCP	Storage register clock pulse input	1.0/0.033	20μA/20μA
$\overline{MR}$	Master reset input (active-Low)	1.0/1.0	20μA/0.6mA
$\overline{OE}$	Output Enable input (active-Low)	1.0/1.0	20μA/0.6mA
Q_8	Serial expansion output	50/33	1.0mA/20mA
$Q_0 - Q_7$	Data outputs	150/40	3.0mA/24mA

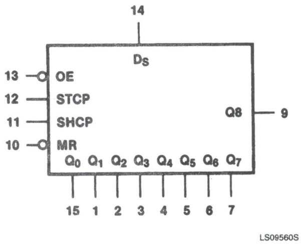
NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



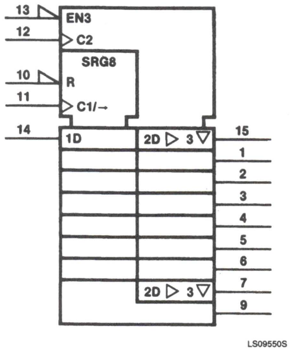
Q1 1
Q2 2
Q3 3
Q4 4
Q5 5
Q6 6
Q7 7
GND 8
16 Vcc
15 Q0
14 Ds
13 OE
12 STCP
11 SHCP
10 MR
9 Q8
CD07860S

LOGIC SYMBOL



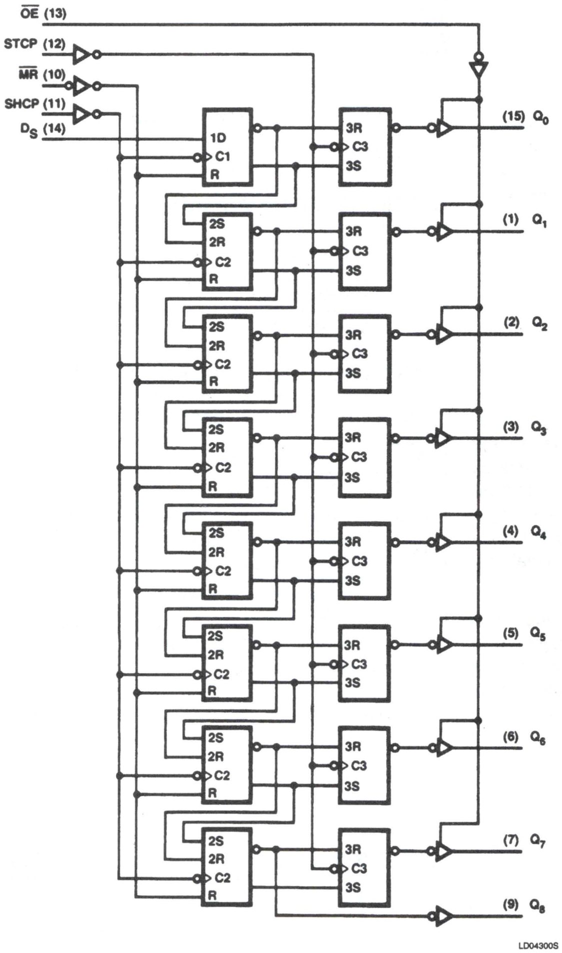
14
Ds
13 OE
12 STCP
11 SHCP
10 MR
Q8 9
Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
15 1 2 3 4 5 6 7
LS09560S

LOGIC SYMBOL (IEEE/IEC)



13
12
10
11
14
EN3
C2
SRG8
R
C1/→
1D
2D ▷ 3▽
2D ▷ 3▽
15
1
2
3
4
5
6
7
9
LS09550S

LOGIC DIAGRAM



$\overline{OE}$ (13)
STCP (12)
$\overline{MR}$ (10)
SHCP (11)
D_S (14)
1D
C1
R
2S
2R
C2
3R
C3
3S
(15) Q_0
(1) Q_1
(2) Q_2
(3) Q_3
(4) Q_4
(5) Q_5
(6) Q_6
(7) Q_7
(9) Q_8
LD04300S

8-Bit Shift Register FAST 74F595

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		74F595	UNIT
V_{CC}	Supply voltage		−0.5 to +7.0	V
V_{IN}	Input voltage		−0.5 to +7.0	V
I_{IN}	Input current		−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		−0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	Q_8	40	mA
		$Q_0 - Q_7$	48	mA
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		74F595			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	High-level output current	Q_8			−1	mA
		$Q_0 - Q_7$			−3	mA
I_{OL}	Low-level output current	Q_8			20	mA
		$Q_0 - Q_7$			24	mA
T_A	Operating free-air temperature		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			74F595			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage	Q_8	V_{CC} = MIN V_{IL} = MAX V_{IH} = MIN	I_{OH} = −1mA	±10% V_{CC}	2.5			V
					±5% V_{CC}	2.7	3.4		V
		$Q_0 - Q_7$		I_{OH} = −3mA	±10% V_{CC}	2.4			V
					±5% V_{CC}	2.7	3.3		V
V_{OL}	Low-level output voltage		V_{CC} = MIN V_{IL} = MIN I_{OL} = MAX, V_{IH} = MIN		±10% V_{CC}		0.35	0.50	V
					±5% V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$				−0.73	−1.2	V
I_I	Input current at maximum input voltage	others	V_{CC} = 0.0V, V_I = 7.0V					100	μA
		$Q_0 - Q_7$	V_{CC} = 5.5V, V_I = 5.5V					1.0	μA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	Low-level input current	others	V_{CC} = MAX, V_I = 0.5V					−20	μA
		$\overline{MR}$, $\overline{OE}$						−0.6	mA
I_{OZH}	OFF-state output current, High-level voltage applied	$Q_0 - Q_7$ only	V_{CC} = MAX, V_O = 2.7V					50	μA
I_{OZL}	OFF-state output current, Low-level voltage applied	$Q_0 - Q_7$ only	V_{CC} = MAX, V_O = 0.5V					50	μA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX			−60		−150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				60	75	mA
		I_{CCL}					70	85	mA
		I_{CCZ}					80	95	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

8-Bit Shift Register FAST 74F595

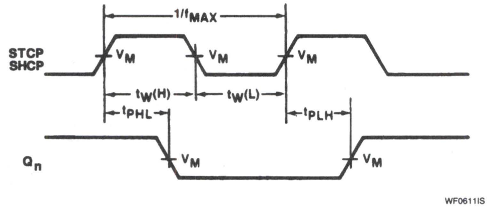
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F595					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$, $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	100	120		80		MHz
t_{PLH} t_{PHL}	Propagation delay SHCP to Q_8	Waveform 1	4.0 4.0	6.5 7.0	8.5 9.0	4.0 4.0	9.5 10.5	ns
t_{PLH} t_{PHL}	Propagation delay STCP to $Q_0 - Q_7$	Waveform 1	4.0 4.0	6.5 7.0	9.0 9.0	4.0 4.0	9.5 10.5	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_8	Waveform 2	4.0	7.0	9.0	4.0	10.5	ns
t_{PZH} t_{PZL}	Output enable time to High or Low level	Waveform 5 Waveform 6	2.0 2.0	6.5 5.5	8.0 7.0	2.0 2.0	9.5 8.0	ns
t_{PHZ} t_{PLZ}	Output disable time from High or Low level	Waveform 5 Waveform 6	2.0 2.0	6.5 5.5	7.0 7.0	2.0 2.0	9.5 8.0	ns

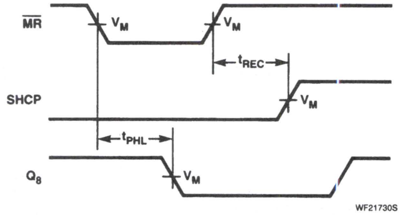
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	74F595					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$, $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_s to SHCP	Waveform 3	3.0 3.0			3.0 3.0		ns ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_s to SHCP	Waveform 3	1.0 1.0			1.0 1.0		ns ns
$t_s(L)$	Setup time, $\overline{MR}$ to STCP	Waveform 3	5.0			6.0		ns
$t_s(H)$	Setup time SHCP to STCP	Waveform 4	6.0			6.0		ns
$t_w(H)$ $t_w(L)$	SHCP Pulse width, High or Low	Waveform 1	4.0 5.0			4.0 5.0		ns
$t_w(H)$ $t_w(L)$	STCP Pulse width, High or Low	Waveform 1	4.0 5.0			4.0 5.0		ns
t_{rec}	Recovery time $\overline{MR}$ to SHCP	Waveform 2	6.0			7.0		ns

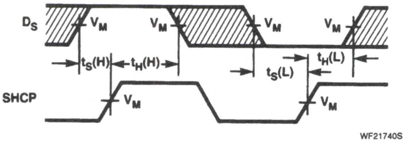
AC WAVEFORMS


$1/f_{MAX}$
STCP
SHCP
V_M
V_M
V_M
$t_W(H)$
$t_W(L)$
t_{PHL}
t_{PLH}
Q_n
V_M
V_M
WF06111S

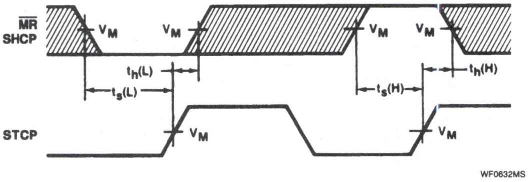
Waveform 1. Clock to Output Delays, Clock Pulse Width, and Maximum Clock Frequency


$\overline{MR}$
V_M
V_M
t_{REC}
SHCP
V_M
t_{PHL}
Q_8
V_M
WF21730S

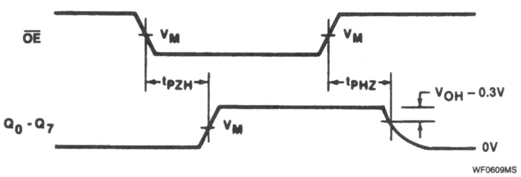
Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time


D_S
V_M
V_M
V_M
V_M
$t_S(H)$
$t_H(H)$
$t_S(L)$
$t_H(L)$
SHCP
V_M
V_M
WF21740S

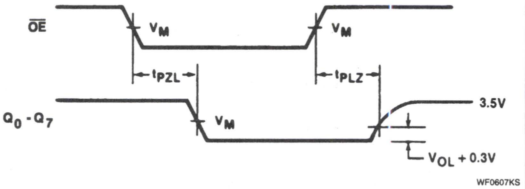
Waveform 3. Data Setup and Hold Times


$\overline{MR}$
SHCP
V_M
V_M
V_M
V_M
$t_h(L)$
$t_s(L)$
$t_s(H)$
$t_h(H)$
STCP
V_M
V_M
WF0632MS

Waveform 4. Data Setup and Hold Times


$\overline{OE}$
V_M
V_M
t_{PZH}
t_{PHZ}
$V_{OH} - 0.3V$
$Q_0 - Q_7$
V_M
0V
WF0609MS

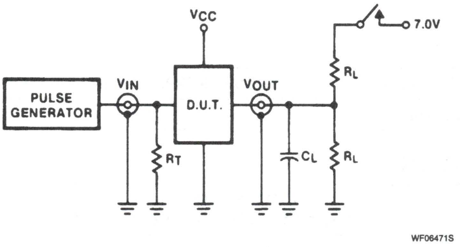
Waveform 5. 3-State Output Enable Time to High Level and Output Disable Time From High Level


$\overline{OE}$
V_M
V_M
t_{PZL}
t_{PLZ}
3.5V
$Q_0 - Q_7$
V_M
$V_{OL} + 0.3V$
WF0607KS

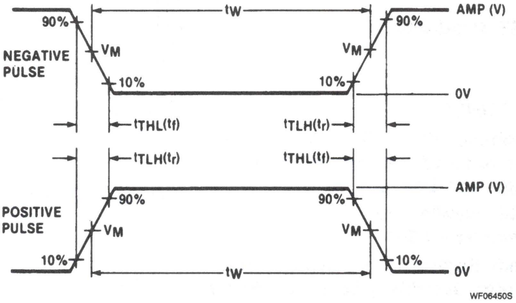
Waveform 6. 3-State Output Enable Time to Low Level and Output Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMSS


VCC
7.0V
RL
PULSE GENERATOR
VIN
D.U.T.
VOUT
RT
CL
RL
WF06471S

Test Circuit for 3-State Outputs


tW
AMP (V)
90%
NEGATIVE PULSE
VM
10%
0V
tTHL(tf)
tTLH(tr)
tTLH(tr)
tTHL(tf)
AMP (V)
90%
POSITIVE PULSE
VM
10%
0V
tW
WF06450S

$V_M = 1.5V$

Input Pulse Definitions

SWITCH POSITION

TEST	SWITCH
t_{PLZ} t_{PZL} All other	closed closed open

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Signetics

FAST 74F597, 74F598
8-Bit Shift Register

8-Bit Shift Register with Input Latches (3-State)
Preliminary Specification

FAST Products

FEATURES

- **High-impedance NPN Base input for reduced loading (20μA in High and Low states)**
- **8-bit Parallel Storage Register – 'F597**
- **Shift Register has Asynchronous Direct Overriding Load and Reset**
- **Guaranteed Shift Frequency DC to 120MHz**
- **Parallel 3-State I/O, Storage Register inputs**
- **Shift Register outputs – 'F598**

DESCRIPTION

The 'F597 consists of an 8-bit storage register feeding a parallel-in, serial-out 8-bit shift register. The storage register and shift register have separate positive-edge triggered clocks. The shift register also has asynchronous direct load (from storage) and reset inputs.

The 'F598 consists of an 8-bit storage latch feeding a parallel/serial-in, parallel/serial-out 8-bit shift register. Both the storage register and shift register have positive edge triggered clocks. The shift register also has asynchronous direct load (from storage) and reset inputs. The 'F598 has 3-State I/O ports that provide parallel shift register outputs and also has multiplexed serial data input.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F597	120MHz	75mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V± 10%; T_A = 0°C to +70°C
Plastic DIP	N74F597N, N74F598D
16-Pin Plastic SO	N74F597D
20-Pin Plastic SO	N74F598D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

TYPE	PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
'F597	D_S	Serial data input	1.0/0.033	20μA/20μA
	$D_0 - D_7$	Parallel data inputs	1.0/0.033	20μA/20μA
	SHCP	Shift register clock pulse input	1.0/0.033	20μA/20μA
	STCP	Store register clock pulse input	1.0/0.033	20μA/20μA
	$\overline{SHL}$	Shift register load input (active-Low)	1.0/0.033	20μA/20μA
	$\overline{SHR}$	Shift register reset input (active-Low)	1.0/0.033	20μA/20μA
	Q_S	Serial data output	50/33	1.0mA/20mA
'F598	I/O_n	Parallel data inputs	1.0/0.033	20μA/20μA
	D_{S0}, D_{S1}	Serial data inputs	1.0/0.033	20μA/20μA
	$\overline{SHCP}$	Shift register clock pulse input	1.0/0.033	20μA/20μA
	$\overline{STCP}$	Store register clock pulse input	1.0/0.033	20μA/20μA
	$\overline{SHCPEN}$	Shift register clock pulse enable input	1.0/0.033	20μA/20μA
	$\overline{SHL}$	Shift register load input (active-Low)	1.0/0.033	20μA/20μA
	$\overline{SHR}$	Shift register reset input (active-Low)	1.0/0.033	20μA/20μA
	S	Serial data selector input	1.0/0.033	20μA/20μA
	$\overline{OE}$	Output Enable input	1.0/0.033	20μA/20μA
	Q_S	Serial data output	50/33	1.0mA/20mA
	I/O_n	Parallel data output	150/33	3.0mA/20mA

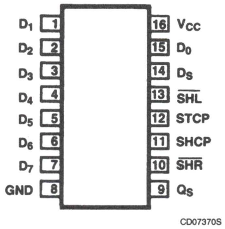
NOTE:
1. One (1.0) FAST unit load is defined as: 20μA in the High state and 0.6mA in the Low state.

8-Bit Shift Register

FAST 74F597, 74F598

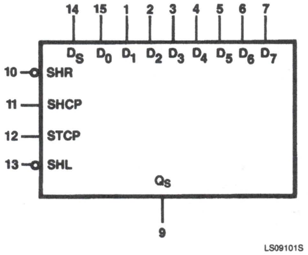
PIN CONFIGURATION

'F597


D1 1
D2 2
D3 3
D4 4
D5 5
D6 6
D7 7
GND 8
16 VCC
15 D0
14 DS
13 SHL
12 STCP
11 SHCP
10 SHR
9 QS
CD07370S

LOGIC SYMBOL

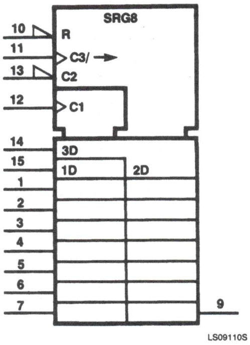
'F597


14 15 1 2 3 4 5 6 7
DS D0 D1 D2 D3 D4 D5 D6 D7
10 SHR
11 SHCP
12 STCP
13 SHL
QS
9
LS09101S

V_{CC} = Pin 16
GND = Pin 8

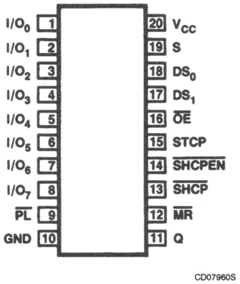
LOGIC SYMBOL (IEEE/IEC)

'F597


SRG8
10 R
11 C3/ →
13 C2
12 C1
14 3D
15 1D 2D
1
2
3
4
5
6
7
9
LS09110S

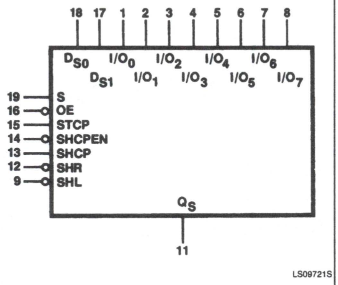
PIN CONFIGURATION

'F598


I/O0 1
I/O1 2
I/O2 3
I/O3 4
I/O4 5
I/O5 6
I/O6 7
I/O7 8
PL 9
GND 10
20 VCC
19 S
18 DS0
17 DS1
16 OE
15 STCP
14 SHCPEN
13 SHCP
12 MR
11 Q
CD07960S

LOGIC SYMBOL

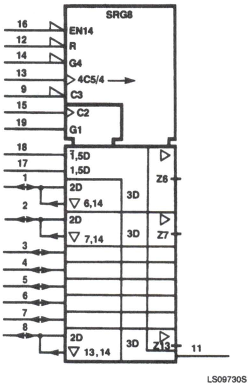
'F598


18 17 1 2 3 4 5 6 7 8
DS0 I/O0 I/O2 I/O4 I/O6
DS1 I/O1 I/O3 I/O5 I/O7
19 S
16 OE
15 STCP
14 SHCPEN
13 SHCP
12 SHR
9 SHL
QS
11
LS09721S

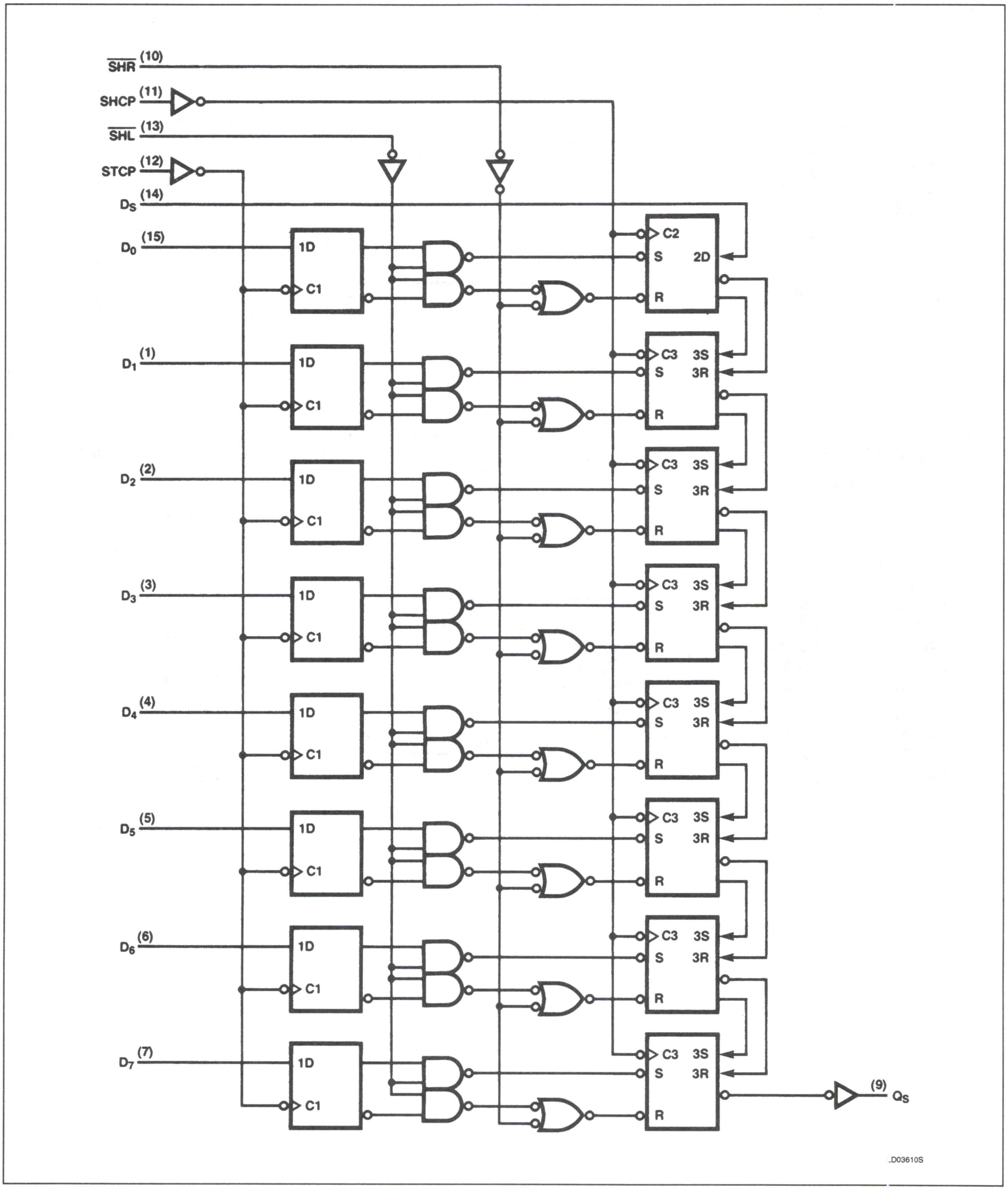
V_{CC} = Pin 20
GND = Pin 10

LOGIC SYMBOL (IEEE/IEC)

'F598

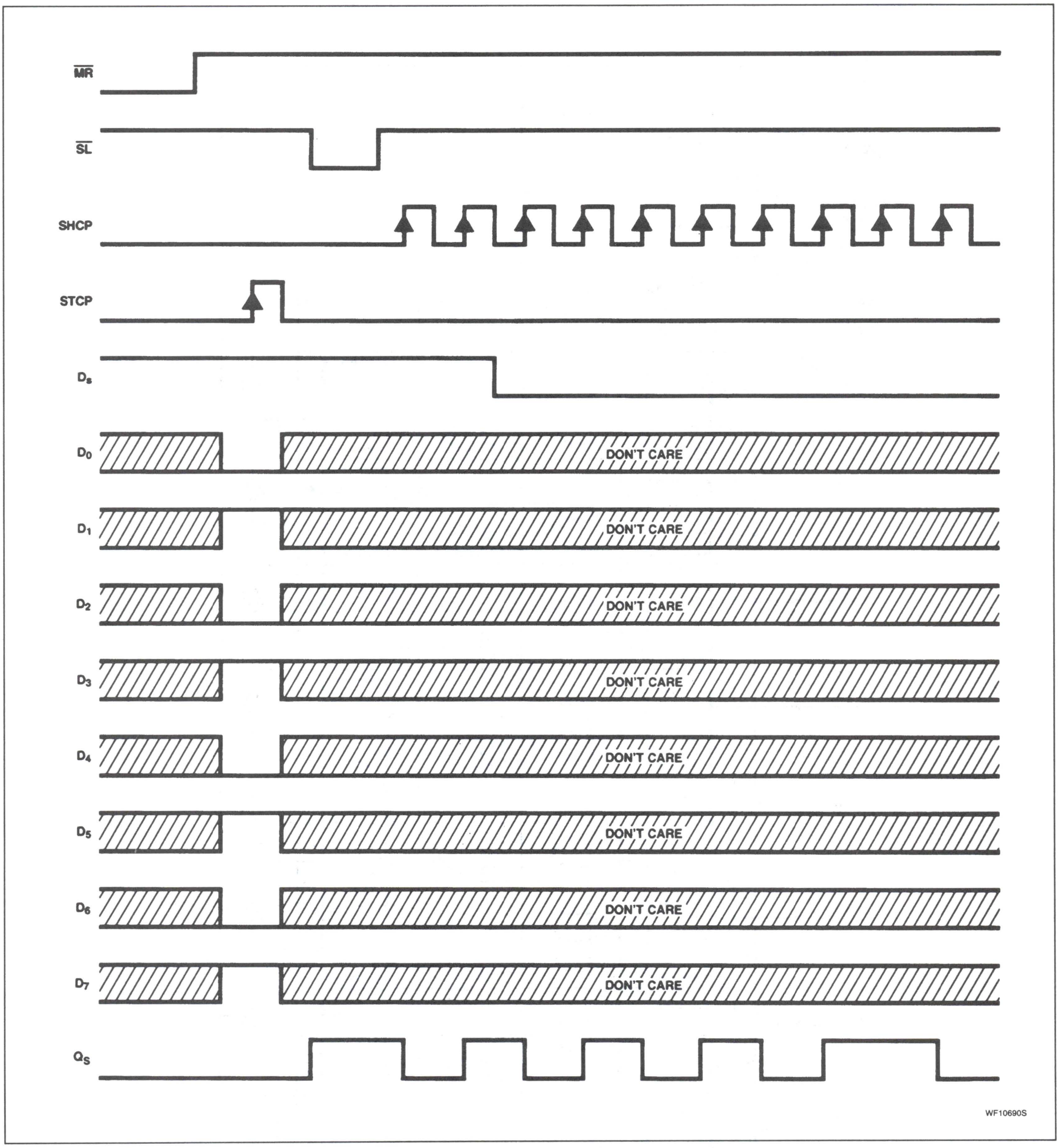

SRG8
16 EN14
12 R
14 G4
13 4C5/4 →
9 C3
15 C2
19 G1
18 1,5D
17 1,5D
1 2D
6,14
3D
Z6
2 2D
7,14
3D
Z7
3
4
5
6
7
8 2D
13, 14
3D
Z13
11
LS09730S

LOGIC DIAGRAM for 74F597

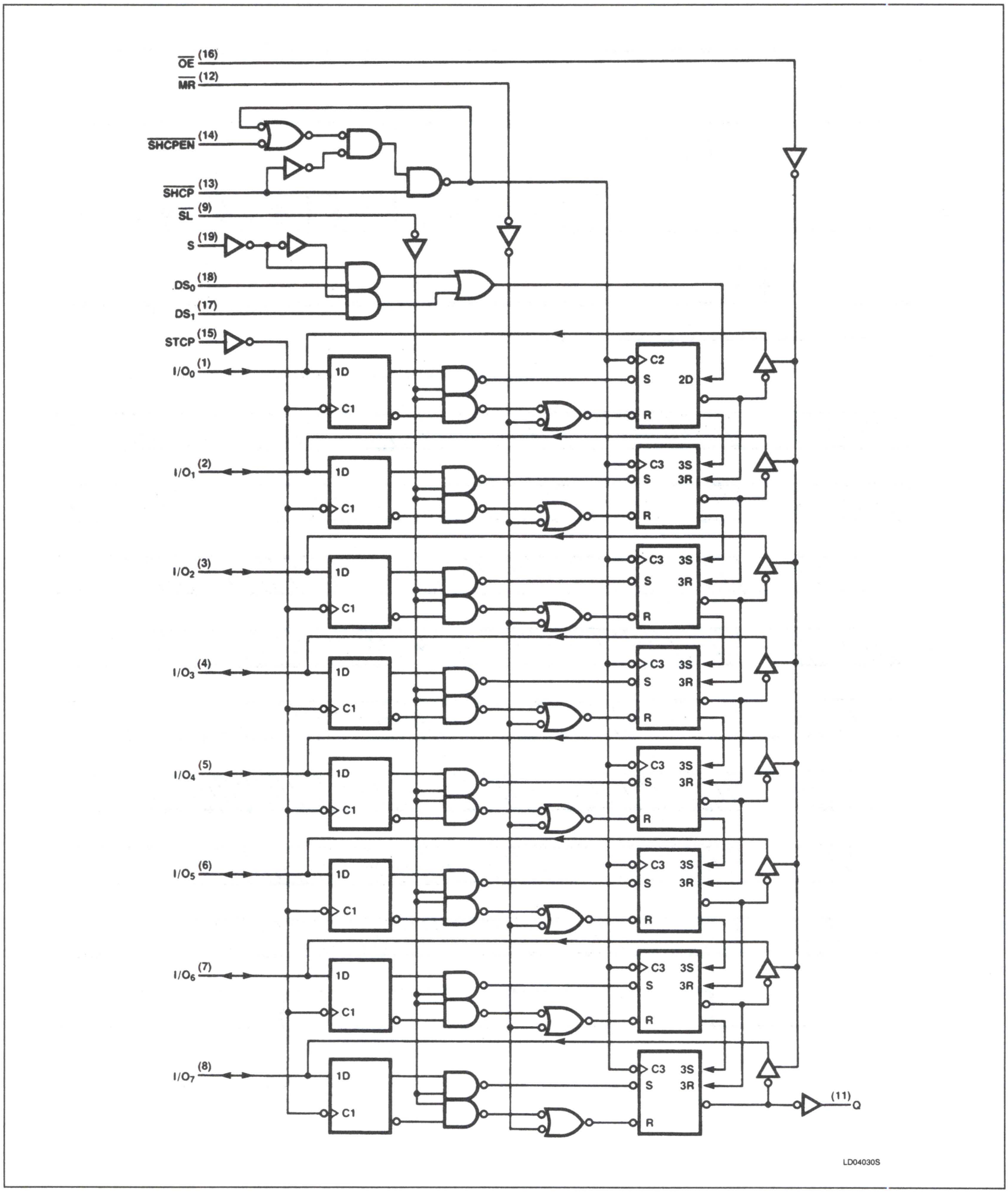


$\overline{SHR}$ (10)
SHCP (11)
$\overline{SHL}$ (13)
STCP (12)
D_S (14)
D_0 (15)
D_1 (1)
D_2 (2)
D_3 (3)
D_4 (4)
D_5 (5)
D_6 (6)
D_7 (7)
1D
C1
C2
S
2D
R
C3
3S
3R
(9) Q_S
D03610S

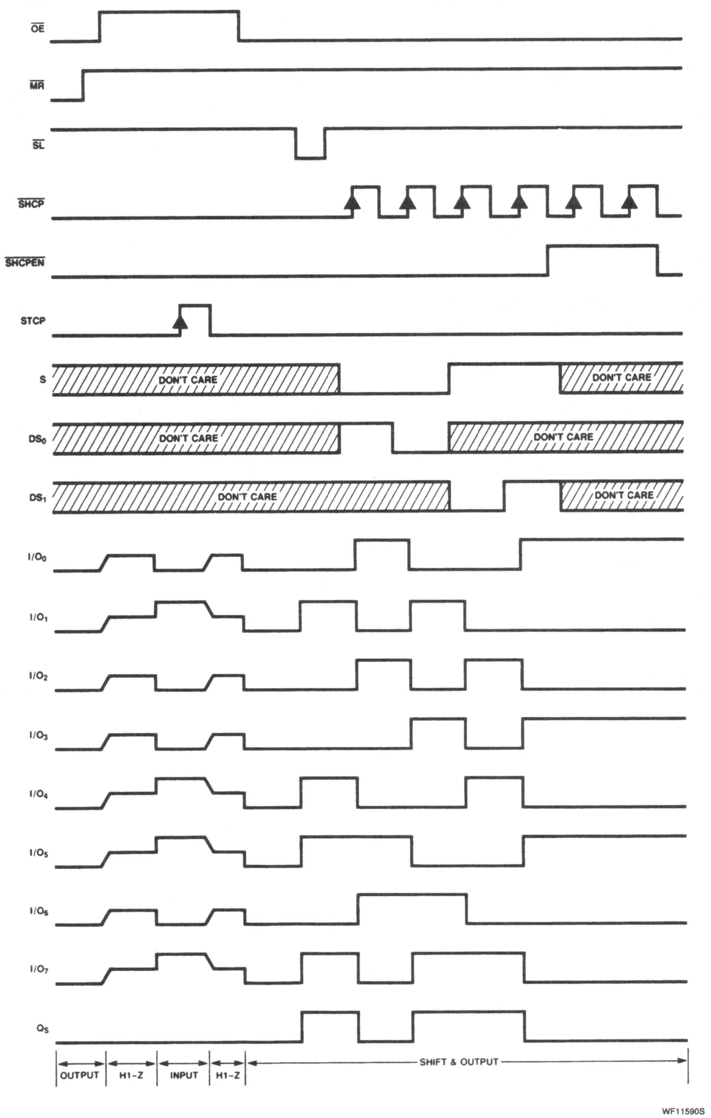
TYPICAL TIMING DIAGRAM for 'F597


$\overline{MR}$
$\overline{SL}$
SHCP
STCP
D_s
D_0
D_1
D_2
D_3
D_4
D_5
D_6
D_7
Q_S
DON'T CARE
WF10690S

LOGIC DIAGRAM for 74F598


OE (16)
MR (12)
SHCPEN (14)
SHCP (13)
SL (9)
S (19)
DS0 (18)
DS1 (17)
STCP (15)
I/O0 (1)
I/O1 (2)
I/O2 (3)
I/O3 (4)
I/O4 (5)
I/O5 (6)
I/O6 (7)
I/O7 (8)
1D
C1
C2
S
2D
R
C3
3S
3R
(11) Q
LD04030S

TYPICAL TIMING DIAGRAM for 'F598


OE
MR
SL
SHCP
SHCPEN
STCP
S
DON'T CARE
DON'T CARE
DS0
DON'T CARE
DON'T CARE
DS1
DON'T CARE
DON'T CARE
I/O0
I/O1
I/O2
I/O3
I/O4
I/O5
I/O6
I/O7
QS
OUTPUT
HI-Z
INPUT
HI-Z
SHIFT & OUTPUT
WF11590S

8-Bit Shift Register

FAST 74F597, 74F598

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		−0.5 to +7.0	V
V_{IN}	Input voltage		−0.5 to +7.0	V
I_{IN}	Input current		−30 to +1	mA
V_{OUT}	Voltage applied to output in High output state		−0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	Q_S	40	mA
		I/O_n	48	mA
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	High-level output current	Q_S			−1	mA
		I/O_n			−3	mA
I_{OL}	Low-level output current	Q_S			20	mA
		I/O_n			24	mA
T_A	Operating free-air temperature		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]			74F597			UNIT
							Min	Typ[2]	Max	
V_{OH}	High-level output voltage		Q_S	V_{CC} = MIN V_{IL} = MAX V_{IH} = MIN	I_{OH} = −1mA	±10%V_{CC}	2.5			V
						±5%V_{CC}	2.7	3.4		V
			I/O_n		I_{OH} = −3mA	±10%V_{CC}	2.4			V
						±5%V_{CC}	2.7	3.3		V
V_{OL}	Low-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX		±10%V_{CC}		0.35	0.50	V
						±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, $I_I = I_{IK}$				−0.73	−1.2	V
I_I	Input current at maximum input voltage		Others	V_{CC} = 0.0V, V_I = 7.0V					100	μA
			I/O_n	V_{CC} = 5.5V, V_I = 5.5V					1.0	mA
I_{IH}	High-level input current			V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	Low-level input current			V_{CC} = MAX, V_I = 0.5V					−20	μA
I_{OZH}	OFF-state current, High-level voltage applied		I/O_n only	V_{CC} = MAX, V_O = 2.7V					70	μA
I_{OZL}	OFF-state current, Low-level voltage applied		I/O_n only	V_{CC} = MAX, V_O = 0.5V					−70	μA
I_{OS}	Short-circuit output current[3]			V_{CC} = MAX			−60		−150	mA
I_{CC}	Supply current (total)	'F597	I_{CCH}	V_{CC} = MAX				45	70	mA
			I_{CCL}					48	75	mA
		'F598	I_{CCH}					75	90	mA
			I_{CCL}					78	95	mA
			I_{CCZ}					85	100	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of High-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F597					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_L = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	100	120		80		MHz
t_{PLH} t_{PHL}	Propagation delay SHCP to Q_S	Waveform 1	4.0 4.0	6.5 7.0	8.5 9.0	4.0 4.0	9.5 10.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{SHL}$ to Q_S	Waveform 1	4.0 4.0	7.5 8.0	9.5 10.0	4.0 4.0	10.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay STCP to Q_S	Waveform 1	4.0 4.0	7.5 8.0	9.5 10.0	4.0 4.0	10.0 11.0	ns
t_{PHL}	Propagation delay $\overline{SHR}$ to Q_S	Waveform 3	4.0	8.0	10.0	4.0	11.0	ns

AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	74F597					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_S to SHCP	Waveform 3	3.0 3.0			3.0 3.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_S to SHCP	Waveform 3	1.0 1.0			1.0 1.0		ns
$t_s(H)$ $t_s(L)$	Setup time STCP to $\overline{SHL}$	Waveform 4	3.0 3.0			3.0 3.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low STCP to $\overline{SHL}$	Waveform 4	1.0 1.0			1.0 1.0		ns
$t_w(H)$ $t_w(L)$	SHCP pulse width, High or Low	Waveform 1	4.0 5.0			4.0 5.0		ns
$t_w(H)$ $t_w(L)$	STCP pulse width, High or Low	Waveform 1	4.0 5.0			4.0 5.0		ns
$t_w(L)$	$\overline{SHR}$ pulse width, Low	Waveform 1	4.0			4.0		ns
$t_w(L)$	$\overline{SHL}$ pulse width, Low	Waveform 1	4.0			4.0		ns
t_{rec}	Recovery time, $\overline{SHR}$ to SHCP	Waveform 2	6.0			7.0		ns
t_{rec}	Recovery time, $\overline{SHL}$ to SHCP	Waveform 2	6.0			7.0		ns

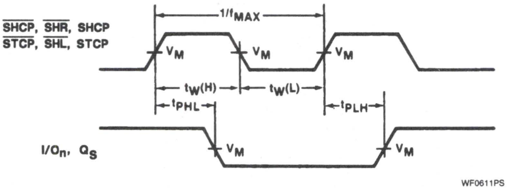
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F598					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_L = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	100	120		80		MHz
t_{PLH} t_{PHL}	Propagation delay $\overline{\text{SHCP}}$ to Q_S	Waveform 1	4.0 4.0	6.5 7.0	8.5 9.0	4.0 4.0	9.5 10.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{\text{STCP}}$ to Q_S ($\overline{\text{SHL}}$ = Low)	Waveform 1	4.0 4.0	7.5 8.0	9.5 10.0	4.0 4.0	10.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{\text{SHL}}$ to Q_S	Waveform 1	4.0 4.0	7.5 8.0	9.0 9.0	4.0 4.0	10.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{\text{SHCP}}$ to I/O_n	Waveform 1	4.0 4.0	7.0 7.0	9.0 9.0	4.0 4.0	10.5 10.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{\text{SHL}}$ to I/O_n	Waveform 1	4.0 4.0	7.0 7.0	9.0 9.0	4.0 4.0	10.0 10.0	ns
t_{PHL}	Propagation delay $\overline{\text{SHR}}$ to I/O_n	Waveform 2	4.0	8.0	10.0	4.0	11.0	ns
t_{PHL}	Propagation delay $\overline{\text{SHR}}$ to Q_S	Waveform 2	4.0	8.0	10.0	4.0	11.5	ns
t_{PZH} t_{PZL}	Output enable time to High or Low level	Waveform 5 Waveform 6	4.0 4.0	7.5 7.5	9.0 9.0	4.0 4.0	10.5 10.5	ns
t_{PHZ} t_{PLZ}	Output disable time from High or Low level	Waveform 5 Waveform 6	3.0 3.0	6.0 6.0	8.0 8.0	3.0 3.0	9.0 9.0	ns

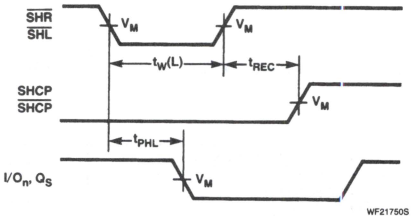
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	74F598					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_{Sn} to $\overline{\text{SHCP}}$	Waveform 3	3.0 3.0			3.0 3.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_{Sn} to $\overline{\text{SHCP}}$	Waveform 3	1.0 1.0			1.0 1.0		ns
$t_s(H)$ $t_s(L)$	Setup time $\overline{\text{STCP}}$ to $\overline{\text{SHL}}$	Waveform 4	3.0 3.0			3.0 3.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{\text{STCP}}$ to $\overline{\text{SHL}}$	Waveform 4	1.0 1.0			1.0 1.0		ns
$t_s(H)$ $t_s(L)$	Setup time $\overline{\text{SHCPEN}}$ to SHCP	Waveform 3	6.0			6.0		ns
$t_w(H)$ $t_w(L)$	$\overline{\text{SHCP}}$ pulse width, High or Low	Waveform 1	4.0 5.0			4.0 5.0		ns
$t_w(H)$ $t_w(L)$	$\overline{\text{STCP}}$ pulse width, High or Low	Waveform 1	4.0 5.0			4.0 5.0		ns
$t_w(L)$	$\overline{\text{SHR}}$ pulse width, Low	Waveform 1	4.0			4.0		ns
$t_w(L)$	$\overline{\text{SHL}}$ pulse width, Low	Waveform 1	4.0			4.0		ns
t_{rec}	Recovery time, $\overline{\text{SHR}}$ to SHCP	Waveform 2	6.0			7.0		ns
t_{rec}	Recovery time, $\overline{\text{SHL}}$ to SHCP	Waveform 2	6.0			6.0		ns

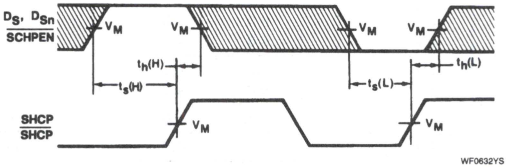
AC WAVEFORMS


SHCP, SHR, SHCP
STCP, SHL, STCP
1/fMAX
VM
VM
VM
tW(H)
tW(L)
tPHL
tPLH
I/On, QS
VM
VM
WF0611PS

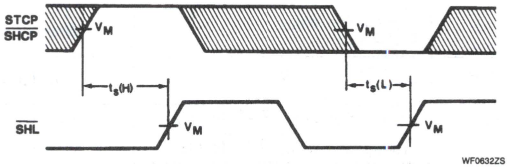
Waveform 1. Propagation Delay, Clock Inputs to Output, Clock Widths and Maximum Clock Frequency and Shift Register Reset and Load Inputs to Serial Data Output


SHR
SHL
VM
VM
tW(L)
tREC
SHCP
SHCP
VM
tPHL
I/On, QS
VM
WF21750S

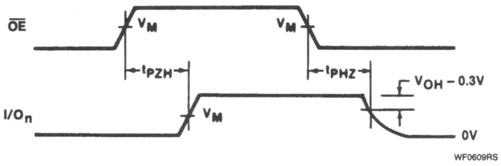
Waveform 2. Propagation Delay, Shift Register Reset and Load Inputs to Serial Data Output, Shift Register Reset and Load Inputs to Shift Register Clock Pulse Input Recovery Time


DS, DSn
SCHPEN
VM
VM
VM
VM
th(H)
th(L)
ts(H)
ts(L)
SHCP
SHCP
VM
VM
WF0632YS

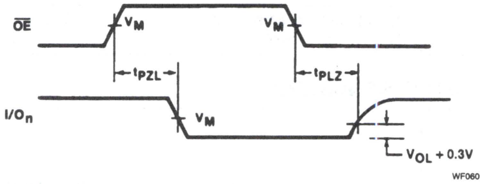
Waveform 3. Data Setup and Hold Times


STCP
SHCP
VM
VM
ts(H)
ts(L)
SHL
VM
VM
WF0632ZS

Waveform 4. Data Setup and Hold Times


OE
VM
VM
tPZH
tPHZ
VOH – 0.3V
I/On
VM
0V
WF0609RS

Waveform 5. 3-State Output Enable Time to High Level and Output Disable Time From High Level

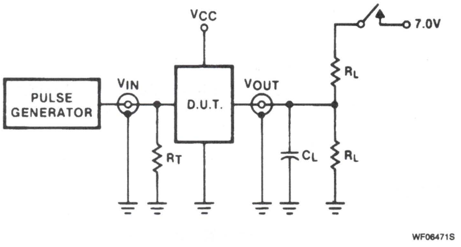

OE
VM
VM
tPZL
tPLZ
I/On
VM
VOL + 0.3V
WF0607PS

Waveform 6. 3-State Output Enable Time to Low Level and Output Disable Time From Low Level

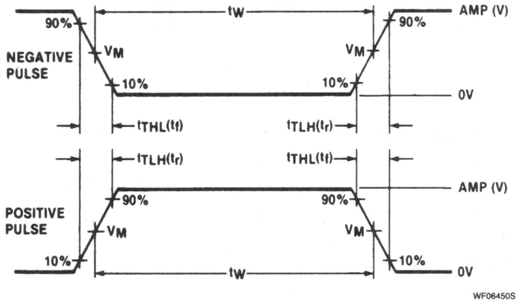
NOTE: $V_M = 1.5V$.

The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS


VCC
7.0V
RL
PULSE GENERATOR
VIN
D.U.T.
VOUT
RT
CL
RL
WF06471S

Test Circuit for 3-State Outputs


tW
90%
AMP (V)
90%
NEGATIVE PULSE
VM
VM
10%
10%
0V
tTHL(tf)
tTLH(tr)
tTLH(tr)
tTHL(tf)
AMP (V)
90%
90%
POSITIVE PULSE
VM
VM
10%
10%
0V
tW
WF06450S

$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F604
Register

Dual Octal Register (3-State)
Product Specification

FAST Products

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F604	105MHz	75mA

FEATURES

- **High-impedance NPN base inputs for reduced loading (20μA in High and Low states)**
- **Stores 16-bit-wide Data inputs, multiplexed 8-bit outputs**
- **3-State outputs**
- **Typical shift frequency of 105 MHz**
- **Power supply current 75mA typical**

DESCRIPTION

The 'F604 contains 16 D-type edge-triggered data inputs. Organized as 8-bit A and B registers, the flip-flop outputs are connected by pairs to eight 2-input multiplexers. A SELECT (SELECT A/$\overline{B}$) input determines whether the A or B register contents are multiplexed to the eight 3-State outputs. Data entered from the B inputs are selected when SELECT A/$\overline{B}$ is Low: data from the A inputs are selected when SELECT A/$\overline{B}$ is High. Data enters the flip-flops on the rising edge of the Clock (CP) input, which also controls the 3-State outputs. The outputs are enabled when CP is High and disabled when CP is Low.

ORDERING INFORMATION

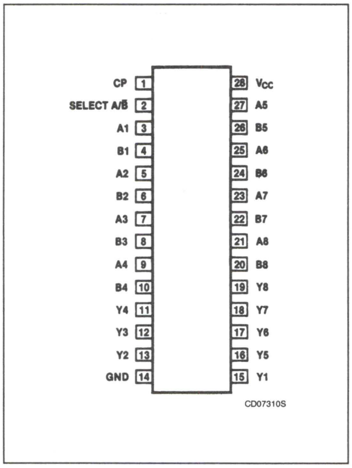
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C
28-Pin Plastic DIP	N74F604N
28-Pin Plastic SOL	N74F604D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

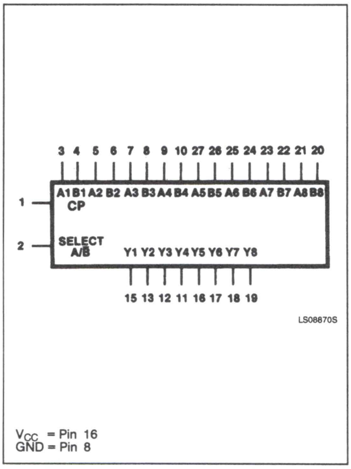
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$A_1 - A_8$	Inputs A	1.0/0.033	20μA/20μA
$B_1 - B_8$	Inputs B	1.0/0.033	20μA/20μA
SELECT A/$\overline{B}$	Select inputs	1.0/0.033	20μA/20μA
CP	Clock Pulse input (active rising edge)	1.0/0.033	20μA/20μA
$Y_1 - Y_8$	Outputs	150/40	3.0mA/24mA

NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION

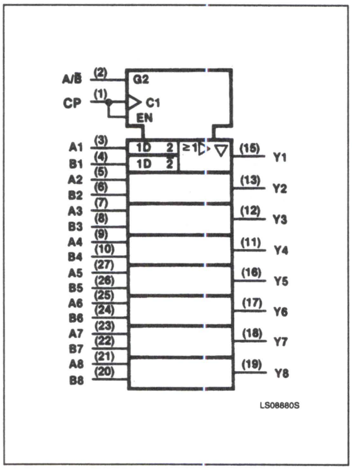

CP 1
SELECT A/B̄ 2
A1 3
B1 4
A2 5
B2 6
A3 7
B3 8
A4 9
B4 10
Y4 11
Y3 12
Y2 13
GND 14
28 Vcc
27 A5
26 B5
25 A6
24 B6
23 A7
22 B7
21 A8
20 B8
19 Y8
18 Y7
17 Y6
16 Y5
15 Y1
CD07310S

LOGIC SYMBOL


3 4 5 6 7 8 9 10 27 26 25 24 23 22 21 20
A1 B1 A2 B2 A3 B3 A4 B4 A5 B5 A6 B6 A7 B7 A8 B8
1
CP
2
SELECT A/B̄
Y1 Y2 Y3 Y4 Y5 Y6 Y7 Y8
15 13 12 11 16 17 18 19
LS08870S

V_{CC} = Pin 16
GND = Pin 8

LOGIC SYMBOL (IEEE/IEC)


A/B̄ (2)
CP (1)
G2
C1
EN
1D 2
1D 2̄
≥1
▽
A1 (3)
B1 (4)
A2 (5)
B2 (6)
A3 (7)
B3 (8)
A4 (9)
B4 (10)
A5 (27)
B5 (26)
A6 (25)
B6 (24)
A7 (23)
B7 (22)
A8 (21)
B8 (20)
(15) Y1
(13) Y2
(12) Y3
(11) Y4
(16) Y5
(17) Y6
(18) Y7
(19) Y8
LS08880S

Register

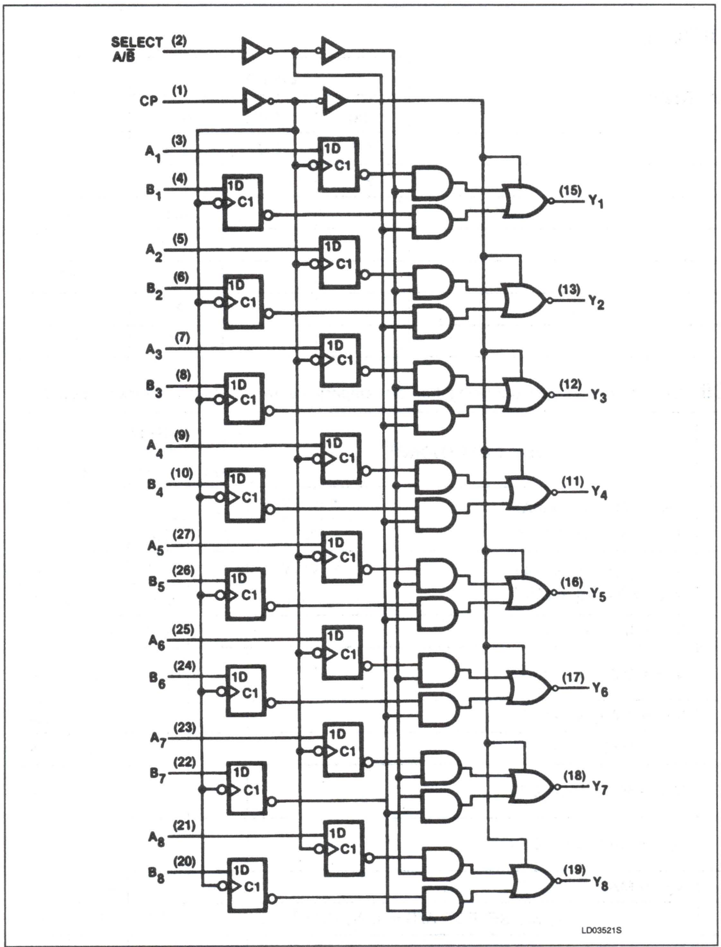
FAST 74F604

FUNCTION TABLE

INPUTS				OUTPUTS
$A_1 - A_8$	$B_1 - B_8$	SELECT A/$\overline{B}$	CP	$Y_1 - Y_8$
A data	B data	L	I	B data
A data	B data	H	I	A data
X	X	X	L	Z
X	X	L	H	B register stored data
X	X	H	H	A register stored data

H = High level (steady state)
L = Low level (steady state)
X = Don't care
Z = High-impedance state
I = Transition from Low-to-High level

LOGIC DIAGRAM


SELECT A/B̄ (2)
CP (1)
A1 (3)
B1 (4)
1D
C1
(15) Y1
A2 (5)
B2 (6)
(13) Y2
A3 (7)
B3 (8)
(12) Y3
A4 (9)
B4 (10)
(11) Y4
A5 (27)
B5 (26)
(16) Y5
A6 (25)
B6 (24)
(17) Y6
A7 (23)
B7 (22)
(18) Y7
A8 (21)
B8 (20)
(19) Y8
LD03521S

Register

FAST 74F604

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to +5.5	
I_{OUT}	Current applied to output in Low output state	48	mA
T_A	Operating free-air temperature range	0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−3	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		74F604			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.4			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = 0.0V, V_I = 7.0V				100	μA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				−20	μA
I_{OZH}	OFF-state output current, High-level voltage applied		V_{CC} = MAX, V_O = 2.7V				50	μA
I_{OZL}	OFF-state output current, Low-level voltage applied		V_{CC} = MAX, V_O = 0.5V				−50	μA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	A_n, B_n, SELECT A/$\overline{B}$ = 4.5V, CP = ↑		60	82	mA
		I_{CCL}		A_n, B_n, SELECT A/$\overline{B}$ = GND, CP = ↑		75	100	mA
		I_{CCZ}		A_n, B_n, SELECT A/$\overline{B}$ = GND, CP = GND		75	100	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

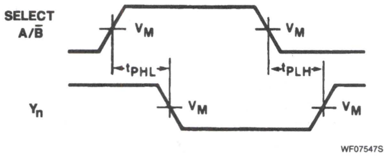
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F604					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 5	95	105		80		MHz
t_{PLH} t_{PHL}	Propagation delay SELECT A/$\overline{B}$ to Y_n	Waveform 2	5.0 6.0	7.0 8.5	9.0 10.5	4.5 5.5	10.0 11.5	ns
t_{PLH} t_{PHL}	Propagation delay SELECT A/$\overline{B}$ to Y_n	Waveform 1	6.0 4.0	8.0 6.5	10.0 8.5	5.5 3.5	11.5 9.0	ns
t_{PZH} t_{PZL}	Output enable time to High or Low level	Waveform 4, 5	5.0 6.5	7.5 9.0	9.5 11.0	4.5 6.0	10.5 12.0	ns
t_{PHZ} t_{PLZ}	Output disable time from High or Low level	Waveform 4, 5	5.0 5.0	7.0 7.0	9.5 9.5	4.5 4.5	11.0 11.0	ns

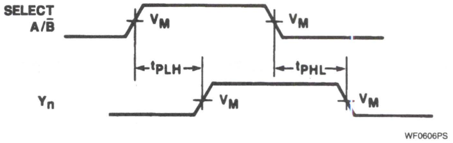
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	74F604					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low A_n, B_n, SELECT A/$\overline{B}$ to CP	Waveform 4	1 2			2 3		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low A_n, B_n, SELECT A/$\overline{B}$ to CP	Waveform 4	0 1			0 1.5		ns
$t_w(H)$	Clock pulse width, High	Waveform 4	5			6		ns

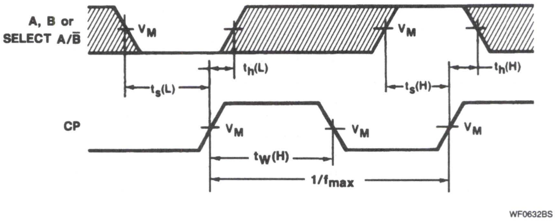
AC WAVEFORMS


SELECT
A/B̄
VM
VM
tPHL
tPLH
Yn
VM
VM
WF07547S

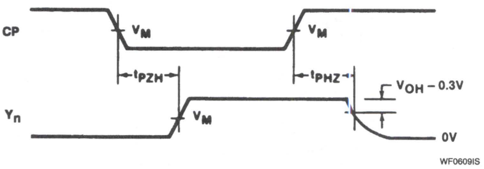
Waveform 1. Propagation Delay Select A/B̄ to Output (Y_n)
(A Register Stored Data = L, CP = H)


SELECT
A/B̄
VM
VM
tPLH
tPHL
Yn
VM
VM
WF0606PS

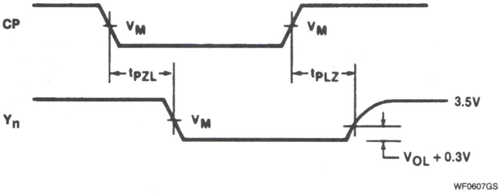
Waveform 2. Propagation Delay Select A/B̄ to Output (Y_n)
(B Register Stored Data = L, CP = H)


A, B or
SELECT A/B̄
VM
VM
th(L)
th(H)
ts(L)
ts(H)
CP
VM
VM
VM
tW(H)
1/fmax
WF0632BS

Waveform 3. Data and Select Setup and Hold Times


CP
VM
VM
tPZH
tPHZ
VOH − 0.3V
Yn
VM
0V
WF0609IS

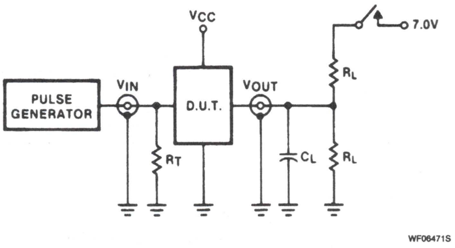
Waveform 4. 3-State Output Enable Time to High Level
and Output Disable Time From High Level


CP
VM
VM
tPZL
tPLZ
3.5V
Yn
VM
VOL + 0.3V
WF0607GS

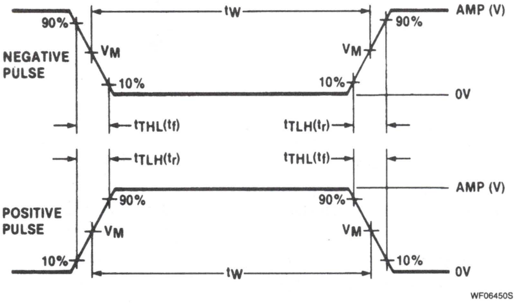
Waveform 5. 3-State Output Enable Time to Low Level
and Output Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS


VCC
7.0V
RL
PULSE GENERATOR
VIN
D.U.T.
VOUT
RT
CL
RL
WF06471S

Test Circuit for 3-State Outputs


NEGATIVE PULSE
90%
VM
10%
tW
VM
10%
90%
AMP (V)
0V
tTHL(tf)
tTLH(tr)
tTLH(tr)
tTHL(tf)
AMP (V)
POSITIVE PULSE
90%
VM
10%
90%
VM
10%
tW
0V
WF06450S

$V_M = 1.5V$

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor to GND; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F605
Register

Dual Octal Register (Open-Collector)
Product Specification

FAST Products

FEATURES
- **High-impedance NPN base inputs for reduced loading (20μA in High and Low states)**
- **Stores 16-bit-wide data inputs, multiplexed 8-bit outputs**
- **Open-Collector outputs**
- **Propagation delay 10ns typical**
- **Power supply current 85mA typical**

DESCRIPTION
The 'F605 contains 16 D-type edge-triggered flip-flops with common Clock and individual data inputs. Organized as 8-bit A and B registers, the flip-flop outputs are connected by pairs to eight 2-input multiplexers. A SELECT (SELECT A/$\overline{B}$) input determines whether the A or B register contents are multiplexed to the eight Open-Collector outputs. Data entered from the B inputs are selected when SELECT A/$\overline{B}$ is Low; data from the A inputs are selected when SELECT A/$\overline{B}$ is High. Data enters the flip-flops on the rising edge of the Clock (CP) input, which also controls the Open-Collector outputs. The outputs are enabled when CP is High and disabled when CP is Low.

These functions are well-suited for receiving 16-bit simultaneous data and transmitting it as two sequential 8-bit words.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F605	105MHz	85mA

ORDERING INFORMATION

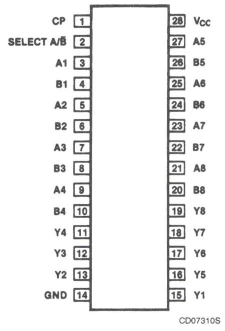
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ± 10%; T_A = 0°C to +70°C
28-Pin Plastic DIP	N74F605N
28-Pin Plastic SOL	N74F605D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

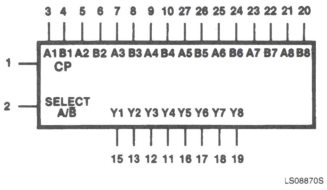
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$A_1 - A_8$	Inputs A	1.0/0.033	20μA/20μA
$B_1 - B_8$	Inputs B	1.0/0.033	20μA/20μA
SELECT A/$\overline{B}$	Select input	1.0/0.033	20μA/20μA
CP	Clock Pulse input (active rising edge)	1.0/0.033	20μA/20μA
$Y_1 - Y_8$	Outputs	*OC /33.3	*OC /20mA

NOTES:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.
2. *OC = Open-Collector.

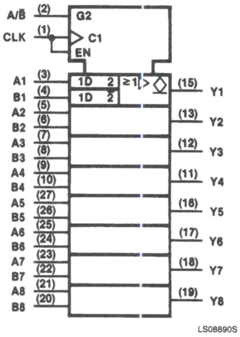
PIN CONFIGURATION


CP 1
SELECT A/B̄ 2
A1 3
B1 4
A2 5
B2 6
A3 7
B3 8
A4 9
B4 10
Y4 11
Y3 12
Y2 13
GND 14
28 VCC
27 A5
26 B5
25 A6
24 B6
23 A7
22 B7
21 A8
20 B8
19 Y8
18 Y7
17 Y6
16 Y5
15 Y1
CD07310S

LOGIC SYMBOL


3 4 5 6 7 8 9 10 27 26 25 24 23 22 21 20
A1 B1 A2 B2 A3 B3 A4 B4 A5 B5 A6 B6 A7 B7 A8 B8
1
CP
2
SELECT A/B̄
Y1 Y2 Y3 Y4 Y5 Y6 Y7 Y8
15 13 12 11 16 17 18 19
LS08870S

LOGIC SYMBOL (IEEE/IEC)

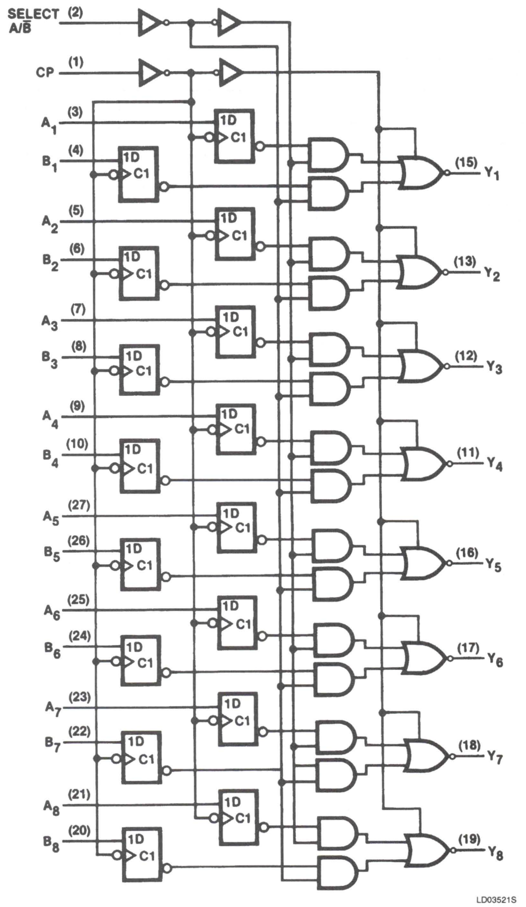

A/B̄ (2)
CLK (1)
G2
C1
EN
1D 2
1D 2̄
≥1
A1 (3)
B1 (4)
A2 (5)
B2 (6)
A3 (7)
B3 (8)
A4 (9)
B4 (10)
A5 (27)
B5 (26)
A6 (25)
B6 (24)
A7 (23)
B7 (22)
A8 (21)
B8 (20)
(15) Y1
(13) Y2
(12) Y3
(11) Y4
(16) Y5
(17) Y6
(18) Y7
(19) Y8
LS08890S

FUNCTION TABLE

INPUTS				OUTPUTS
$A_1 - A_8$	$B_1 - B_8$	SELECT $A/\overline{B}$	CP	$Y_1 - Y_8$
A data	B data	L	↑	B data
A data	B data	H	↑	A data
X	X	X	L	Z or Off
X	X	L	H	B register stored data
X	X	H	H	A register stored data

H = High level (steady state)
L = Low level (steady state)
Off = H if pull-up resistor is connected to Open-Collector output
X = Don't care
Z = High-impedance state
↑ = Transition from Low-to-High level

LOGIC DIAGRAM


SELECT A/B̄ (2)
CP (1)
A1 (3)
B1 (4)
A2 (5)
B2 (6)
A3 (7)
B3 (8)
A4 (9)
B4 (10)
A5 (27)
B5 (26)
A6 (25)
B6 (24)
A7 (23)
B7 (22)
A8 (21)
B8 (20)
1D
C1
(15) Y1
(13) Y2
(12) Y3
(11) Y4
(16) Y5
(17) Y6
(18) Y7
(19) Y8
LD03521S

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
V_{OH}	High-level output voltage			4.5	V
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

Register

FAST 74F605

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		74F605			UNIT
					Min	Typ[2]	Max	
I_{OH}	High-level output current		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, V_{OH} = 4.5V				250	μA
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OL} = MAX, V_{IH} = MIN	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = 0.0V, V_I = 7.0V				100	μA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-20	μA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	$A_n = B_n$ = SELECT A/$\overline{B}$ = 4.5V, CP = ↑		80	100	mA
		I_{CCL}		$A_n = B_n$ = SELECT A/$\overline{B}$ = GND, CP = ↑		85	105	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.

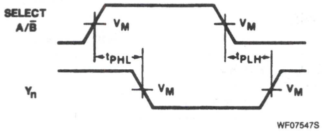
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F605					UNIT
			T_A = +25°C V_{CC} = +5.0V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 4	95	105		80		MHz
t_{PLH} t_{PHL}	Propagation delay SELECT A/$\overline{B}$ to Y_n	Waveform 2	7.5 7.5	9.5 10.0	11.5 12.0	7.0 7.0	12.0 13.5	ns
t_{PLH} t_{PHL}	Propagation delay SELECT A/$\overline{B}$ to Y_n	Waveform 1	8.5 6.5	11.0 8.5	13.0 11.0	8.0 6.0	14.5 11.5	ns
t_{PLH} t_{PHL}	Propagation delay CP to Y_n	Waveform 3	8.5 6.5	11.0 9.0	13.0 11.0	8.0 6.0	14.5 12.0	ns

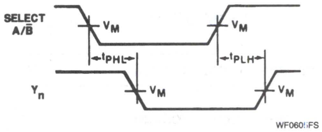
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	74F605					UNIT
			T_A = +25°C V_{CC} = +5.0V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low A_n, B_n, Select A/$\overline{B}$ to CP	Waveform 4	1 3			2 4		ns ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low A_n, B_n, Select A/$\overline{B}$ to CP	Waveform 4	1 2			2 3		ns ns
t_w	Clock Pulse width	Waveform 4	5			6		ns

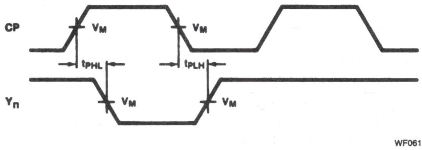
AC WAVEFORMS


SELECT A/B̄
VM
VM
tPHL
tPLH
Yn
VM
VM
WF07547S

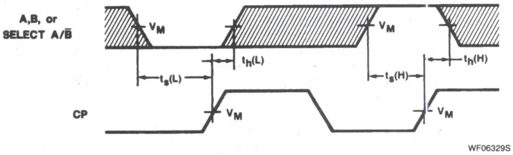
Waveform 1. Propagation Delay SELECT $A/\overline{B}$ to Output (Y_n) (A Register stored data = L, CP = H)


SELECT A/B̄
VM
VM
tPHL
tPLH
Yn
VM
VM

Waveform 2. Propagation Delay SELECT $A/\overline{B}$ to Output (Y_n) (B Register stored data = L, CP = H)


CP
VM
VM
tPHL
tPLH
Yn
VM
VM
WF06141S

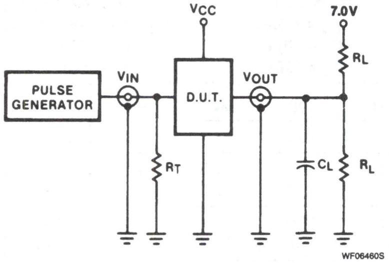
Waveform 3. Clock to Output Delays (SELECT $A/\overline{B}$ = H)


A,B, or SELECT A/B̄
VM
th(L)
VM
ts(L)
ts(H)
th(H)
CP
VM
VM
WF06329S

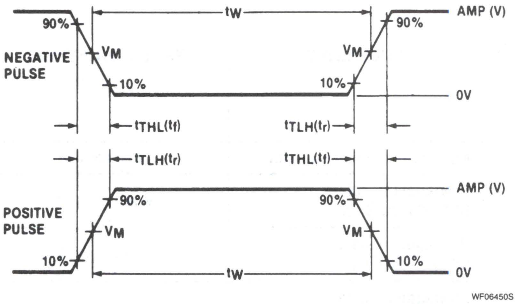
Waveform 4. Data and SELECT Setup and Hold Times

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORM


VCC
7.0V
RL
PULSE GENERATOR
VIN
D.U.T.
VOUT
RT
CL
RL
WF06460S

Test Circuit for Open-Collector Outputs


tW
90%
90%
AMP (V)
NEGATIVE PULSE
VM
VM
10%
10%
0V
tTHL(tf)
tTLH(tr)
tTLH(tr)
tTHL(tf)
AMP (V)
90%
90%
POSITIVE PULSE
VM
VM
10%
10%
tW
0V
WF06450S

V_M = 1.5V

Input Pulse Definition

DEFINITIONS
R_L = Load resistor to GND; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F620, F623
Transceivers

Octal Bus Transceiver
('F620 — Inverting 3-State)
('F623 — Non-Inverting 3-State)
Product Specification

FAST Products

FEATURES

- High-impedance NPN base inputs for reduced loading (70μA in High and Low states)
- Ideal for applications which require high output drive and minimal bus loading
- Octal bidirectional bus interface
- 3-State buffer outputs sink 64mA and source 15mA
  - 'F620, inverting
  - 'F623, non-inverting

DESCRIPTION

The 'F623 is an octal transceiver featuring non-inverting 3-State bus-compatible outputs in both send and receive directions. The outputs are capable of sinking 64mA and sourcing up to 15mA, providing very good capacitive drive characteristics. The 'F620 is an inverting version of the 'F623.

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F620	3.5ns	75mA
74F623	4.5ns	105mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
20-Pin Plastic DIP	N74F620N, N74F623N
20-Pin Plastic SOL[1]	N74F620D

NOTE:
1. Thermal mounting techniques are recommended. See App Note AN SMD-100 for a discussion of thermal considerations for surface mounted device.

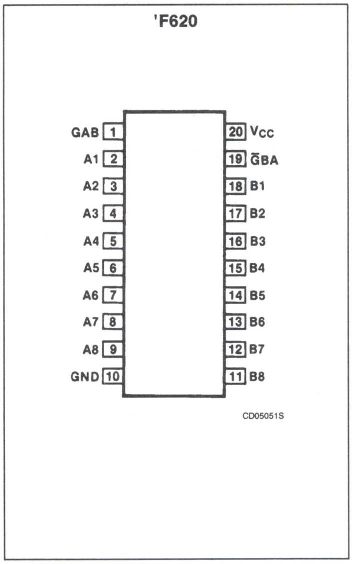
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$A_1 - A_8$, $B_1 - B_8$	Data inputs	3.5/0.116	70μA/70μA
$\overline{G}$BA, GAB	3-State output enable inputs (active-Low)	1.0/0.033	20μA/20μA
$A_1 - A_8$	Data outputs	150/40	3mA/24mA
$B_1 - B_8$	Data outputs	750/106.7	15mA/64mA

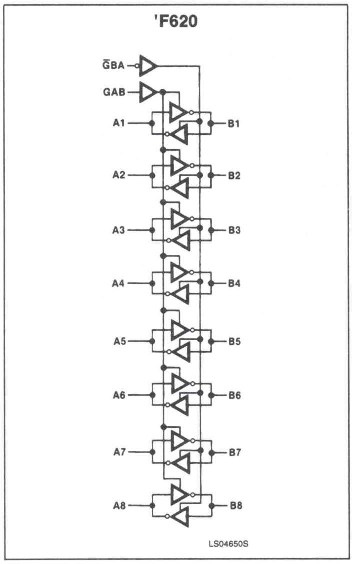
NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

6

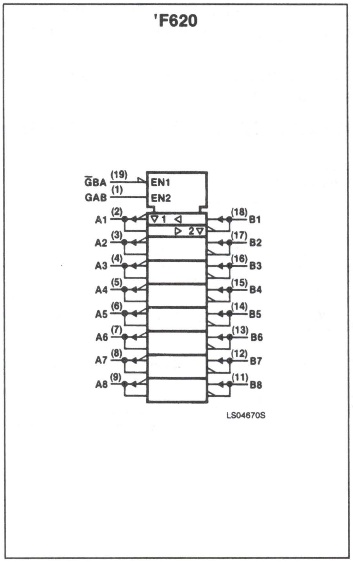
PIN CONFIGURATION


'F620
GAB 1
A1 2
A2 3
A3 4
A4 5
A5 6
A6 7
A7 8
A8 9
GND 10
20 Vcc
19 ḠBA
18 B1
17 B2
16 B3
15 B4
14 B5
13 B6
12 B7
11 B8
CD05051S

LOGIC SYMBOL


'F620
ḠBA
GAB
A1
A2
A3
A4
A5
A6
A7
A8
B1
B2
B3
B4
B5
B6
B7
B8
LS04650S

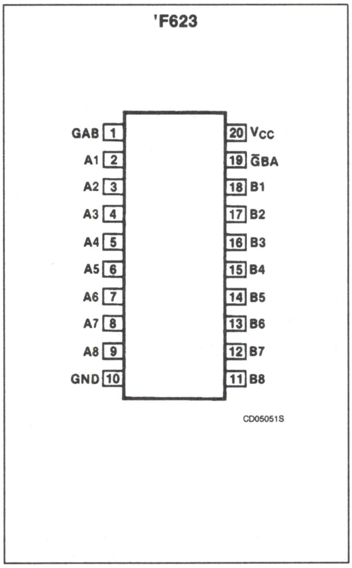
LOGIC SYMBOL (IEEE)


'F620
ḠBA (19)
GAB (1)
EN1
EN2
∇1 ◁
▷ 2∇
A1 (2)
A2 (3)
A3 (4)
A4 (5)
A5 (6)
A6 (7)
A7 (8)
A8 (9)
(18) B1
(17) B2
(16) B3
(15) B4
(14) B5
(13) B6
(12) B7
(11) B8
LS04670S

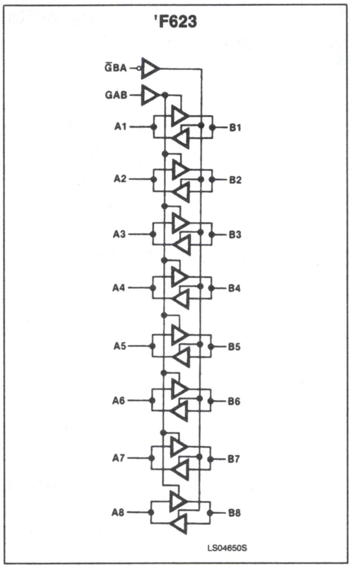
Transceivers

FAST 74F620, F623

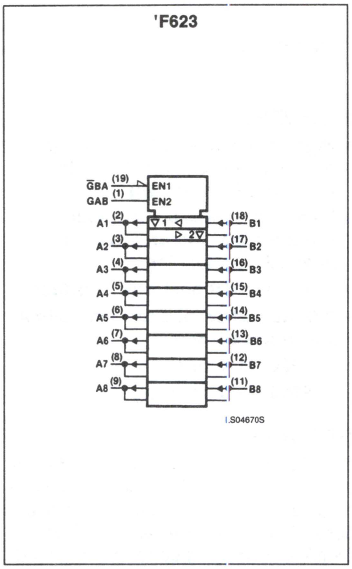
PIN CONFIGURATION


'F623
GAB 1
A1 2
A2 3
A3 4
A4 5
A5 6
A6 7
A7 8
A8 9
GND 10
20 V_{CC}
19 $\overline{G}$BA
18 B1
17 B2
16 B3
15 B4
14 B5
13 B6
12 B7
11 B8
CD05051S

LOGIC SYMBOL


'F623
$\overline{G}$BA
GAB
A1
A2
A3
A4
A5
A6
A7
A8
B1
B2
B3
B4
B5
B6
B7
B8
LS04650S

LOGIC SYMBOL (IEEE)


'F623
$\overline{G}$BA (19)
GAB (1)
EN1
EN2
∇1 ◁
▷ 2∇
A1 (2)
A2 (3)
A3 (4)
A4 (5)
A5 (6)
A6 (7)
A7 (8)
A8 (9)
(18) B1
(17) B2
(16) B3
(15) B4
(14) B5
(13) B6
(12) B7
(11) B8
LS04670S

These devices allow data transmisstion from the A bus to the B bus or from the B bus to the A bus, depending upon the logic levels at the Enable inputs ($\overline{G}$BA and GAB). The Enable inputs can be used to disable the device so that the buses are effectively isolated.

The dual-enable configuration gives the 'F620 and 'F623 the capability to store data by the simultaneous enabling of $\overline{G}$BA and GAB. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of the bus lines are at high impedance, both sets of bus lines (16 in all) will remain at their last states.

FUNCTION TABLE

ENABLE INPUTS		OPERATION	
$\overline{G}$BA	GAB	'F620	'F623
L	L	$\overline{B}$ data to A bus	B data to A bus
H	H	$\overline{A}$ data to B bus	A data to B bus
H	L	Z	Z
L	H	$\overline{B}$ data to A bus, $\overline{A}$ data to B bus	B data to A bus, A data to B bus

H = High voltage level
L = Low voltage level
Z = High-impedance (OFF) state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		−0.5 to +7.0	V
V_{IN}	Input voltage		−0.5 to +7.0	V
I_{IN}	Input current		−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		−0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	$A_1 - A_8$	48	mA
		$B_1 - B_8$	128	mA
T_A	Operating free-air temperature range		0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS Min	LIMITS Nom	LIMITS Max	UNIT
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	High-level output current	$A_1 - A_8$			−3	mA
		$B_1 - B_8$			−15	mA
I_{OL}	Low-level output current	$A_1 - A_8$			24	mA
		$B_1 - B_8$			64	mA
T_A	Operating free-air temperature		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]			LIMITS Min	LIMITS Typ[2]	LIMITS Max	UNIT
V_{OH}	High-level output voltage		$A_1 - A_8$ $B_1 - B_8$	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = −3mA	±10%V_{CC}	2.4			V
						±5%V_{CC}	2.7	3.4		V
			$B_1 - B_8$		I_{OH} = −15mA	±10%V_{CC}	2.0			V
						±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage		$A_1 - A_8$	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 24mA	±10%V_{CC}		0.35	0.50	V
						±5%V_{CC}		0.35	0.50	V
			$B_1 - B_8$		I_{OL} = 48mA	±10%V_{CC}		0.40	0.55	V
					I_{OL} = 64mA	±5%V_{CC}		0.40	0.55	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, $I_I = I_{IK}$				−0.73	−1.2	V
I_I	Input current at maximum input voltage		$\overline{GBA}$, GAB	V_{CC} = 0.0V, V_I = 7.0V					100	µA
			Others	V_{CC} = 5.5V, V_I = 5.5V					1	mA
I_{IH}	High-level input current		$\overline{GBA}$, GAB only	V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current			V_{CC} = MAX, V_I = 0.5V					−20	µA
I_{OZH} + I_{IH}	OFF-state current High-level voltage applied		$A_1 - A_8$ $B_1 - B_8$	V_{CC} = MAX, V_O = 2.7V					70	µA
I_{OZL} + I_{IL}	OFF-state current Low-level voltage applied			V_{CC} = MAX, V_O = 0.5V					−70	µA
I_{OS}	Short-circuit output current[3]		$A_1 - A_8$	V_{CC} = MAX			−60		−150	mA
			$B_1 - B_8$				−100		−225	mA
I_{CC}	Supply current (total)	'F620	I_{CCH}	V_{CC} = MAX	$\overline{GBA}$ = GAB = 4.5V; $A_1 - A_8$ = GND			70	92	mA
			I_{CCL}		$\overline{GBA}$ = GAB = 4.5V; $A_1 - A_8$ = 4.5V			84	110	mA
			I_{CCZ}		GAB = GND; $\overline{GBA}$ = $A_1 - A_8$ = 4.5V			70	92	mA
		'F623	I_{CCH}		$\overline{GBA}$ = GAB = 4.5V; $A_1 - A_8$ = 4.5V			110	140	mA
			I_{CCL}		$\overline{GBA}$=GAB = 4.5V; $A_1 - A_8$ = GND			110	140	mA
			I_{CCZ}		GAB = GND; $\overline{GBA}$ = $A_1 - A_8$ = 4.5V			99	130	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Measure I_{CC} with outputs open.

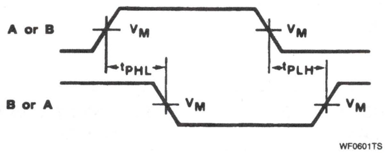
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F620					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n	Waveform 1	2.5 1.0	4.5 2.5	6.5 4.5	2.0 1.0	7.5 5.0	ns
t_{PLH} t_{PHL}	Propagation delay B_n to A_n	Waveform 1	2.5 1.0	4.5 2.5	6.5 4.5	2.0 1.0	7.5 5.0	ns
t_{PZH} t_{PZL}	Output enable to High or Low level $\overline{G}$BA to A_n	Waveform 3 Waveform 4	3.0 4.0	7.5 7.5	10.5 10.5	2.5 3.5	11.5 11.5	ns
t_{PHZ} t_{PLZ}	Output disable from High or Low level $\overline{G}$BA to A_n	Waveform 3 Waveform 4	2.5 2.0	4.5 4.5	7.5 7.0	2.0 1.5	8.0 7.5	ns
t_{PZH} t_{PZL}	Output enable to High or Low level GAB to B_n	Waveform 3 Waveform 4	4.5 4.5	7.5 7.5	10.5 10.0	4.0 4.0	11.5 11.0	ns
t_{PHZ} t_{PLZ}	Output disable from High or Low level GAB to B_n	Waveform 3 Waveform 4	3.0 4.0	6.5 6.5	9.5 9.5	2.5 3.5	10.5 10.5	ns

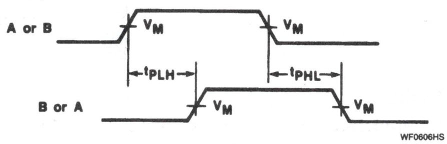
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F623					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n	Waveform 1	2.0 3.0	4.0 5.0	5.5 7.0	2.0 2.5	6.5 7.5	ns
t_{PLH} t_{PHL}	Propagation delay B_n to A_n	Waveform 1	2.0 2.5	4.0 4.5	5.5 6.5	2.0 2.5	6.5 7.5	ns
t_{PZH} t_{PZL}	Output enable to High or Low level $\overline{G}$BA to A_n	Waveform 3 Waveform 4	5.0 5.0	8.5 7.5	10.5 9.5	5.0 5.0	12.0 10.0	ns
t_{PHZ} t_{PLZ}	Output disable from High or Low level $\overline{G}$BA to A_n	Waveform 3 Waveform 4	2.5 2.5	4.5 4.5	6.5 6.5	2.5 2.5	7.5 7.0	ns
t_{PZH} t_{PZL}	Output enable to High or Low level GAB to B_n	Waveform 3 Waveform 4	5.0 4.5	8.0 7.0	10.0 9.0	5.0 4.5	11.5 9.5	ns
t_{PHZ} t_{PLZ}	Output disable from High or Low level GAB to B_n	Waveform 3 Waveform 4	3.0 4.0	6.0 7.0	8.5 9.0	3.0 4.0	10.0 10.0	ns

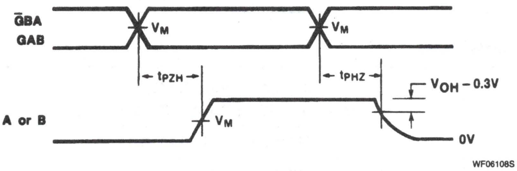
AC WAVEFORMS


A or B
V_M
V_M
t_{PHL}
t_{PLH}
B or A
V_M
V_M
WF0601TS

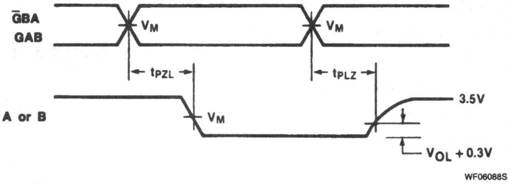
Waveform 1. For Inverting Outputs


A or B
V_M
V_M
t_{PLH}
t_{PHL}
B or A
V_M
V_M
WF0606HS

Waveform 2. For Non-Inverting Outputs


$\overline{G}BA$
GAB
V_M
V_M
t_{PZH}
t_{PHZ}
$V_{OH}-0.3V$
A or B
V_M
0V
WF06108S

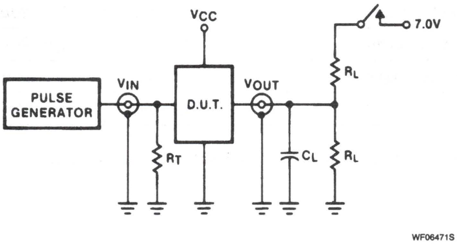
Waveform 3. 3-State Output Enable Time to High Level
Output Disable Time From High Level


$\overline{G}BA$
GAB
V_M
V_M
t_{PZL}
t_{PLZ}
3.5V
A or B
V_M
$V_{OL}+0.3V$
WF06088S

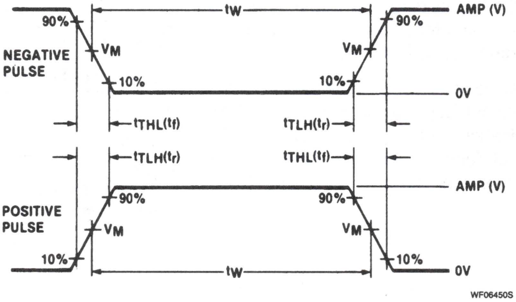
Waveform 4. 3-State Output Enable Time to Low Level
Output Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORMS


V_{CC}
7.0V
R_L
PULSE GENERATOR
V_{IN}
D.U.T.
V_{OUT}
R_T
C_L
R_L
WF06471S

Test Circuit for 3-State Outputs


90%
t_W
AMP (V)
90%
NEGATIVE PULSE
V_M
V_M
10%
10%
0V
$t_{THL}(t_f)$
$t_{TLH}(t_r)$
$t_{TLH}(t_r)$
$t_{THL}(t_f)$
AMP (V)
90%
90%
POSITIVE PULSE
V_M
V_M
10%
10%
t_W
0V
WF06450S

$V_M = 1.5V$
Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS
R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Signetics

FAST Products

FAST 74F621, F622
Transceivers

Octal Bus Transceiver
'F621 — Non-Inverting (Open-Collector)
'F622 — Inverting (Open-Collector)
Product Specification

FEATURES

- **High-impedance NPN base inputs for reduced loading (20μA in High and Low states)**
- **Octal bidirectional bus interface**
- **Open-Collector outputs sink 64mA**
  - **'F621, non-inverting**
  - **'F622, inverting**
- **15mA source current**

DESCRIPTION

The 'F621 is an octal transceiver featuring non-inverting Open-Collector bus-compatible outputs in both send and receive directions. The outputs are capable of sinking 64mA and sourcing up to 15mA, providing very good capacitive drive characteristics. The 'F622 is an inverting version of the 'F621.

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F621	8.0ns	105mA
74F622	8.5ns	53mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
20-Pin Plastic DIP	N74F621N, N74F622N
20-Pin Plastic SOL[1]	N74F621D, N74F622D

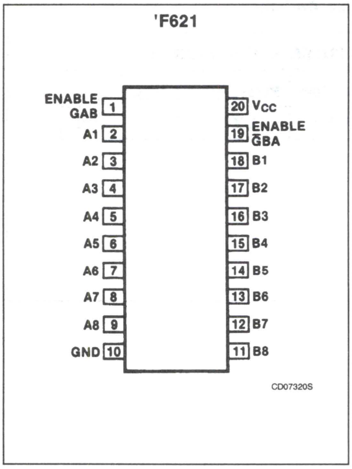
NOTE:
1. Thermal mounting techniques are recommended. See App Note AN SMD-100 for a discussion of thermal considerations for surface mounted devices.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

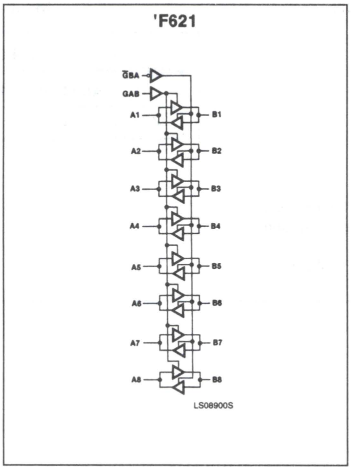
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$\overline{G}$BA, GAB	Enable inputs	1.0/0.033	20μA/20μA
$A_1 - A_8$, $B_1 - B_8$	3-State inputs	1.0/0.033	20μA/20μA
$A_1 - A_8$	3-State outputs	*OC/40	*OC/24mA
$B_1 - B_8$	3-State outputs	*OC/106.7	*OC/64mA

NOTES:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.
2. *OC = Open-Collector

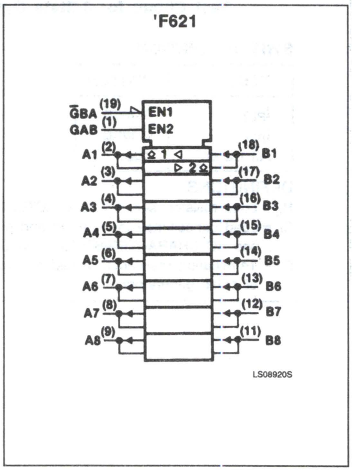
PIN CONFIGURATION


'F621
ENABLE GAB 1
A1 2
A2 3
A3 4
A4 5
A5 6
A6 7
A7 8
A8 9
GND 10
20 VCC
19 ENABLE GBA
18 B1
17 B2
16 B3
15 B4
14 B5
13 B6
12 B7
11 B8
CD07320S

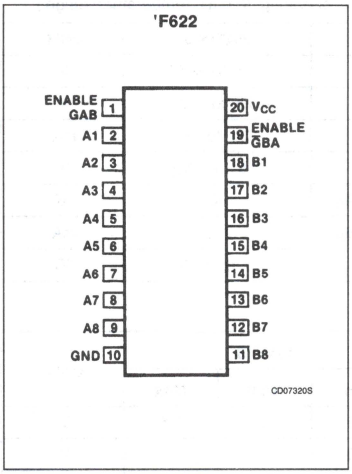
LOGIC SYMBOL


'F621
GBA
GAB
A1
A2
A3
A4
A5
A6
A7
A8
B1
B2
B3
B4
B5
B6
B7
B8
LS08900S

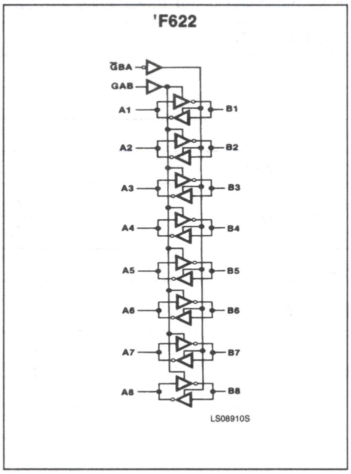
LOGIC SYMBOL (IEEE/IEC)


'F621
GBA (19)
GAB (1)
EN1
EN2
1
2
A1 (2)
A2 (3)
A3 (4)
A4 (5)
A5 (6)
A6 (7)
A7 (8)
A8 (9)
(18) B1
(17) B2
(16) B3
(15) B4
(14) B5
(13) B6
(12) B7
(11) B8
LS08920S

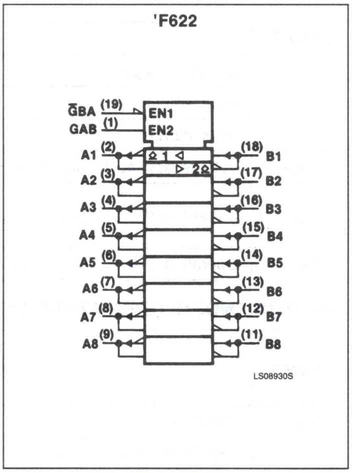
PIN CONFIGURATION


'F622
ENABLE GAB 1
A1 2
A2 3
A3 4
A4 5
A5 6
A6 7
A7 8
A8 9
GND 10
20 VCC
19 ENABLE $\overline{G}$BA
18 B1
17 B2
16 B3
15 B4
14 B5
13 B6
12 B7
11 B8
CD07320S

LOGIC SYMBOL


'F622
$\overline{G}$BA
GAB
A1
A2
A3
A4
A5
A6
A7
A8
B1
B2
B3
B4
B5
B6
B7
B8
LS08910S

LOGIC SYMBOL (IEEE/IEC)


'F622
$\overline{G}$BA (19)
GAB (1)
EN1
EN2
1
2
A1 (2)
A2 (3)
A3 (4)
A4 (5)
A5 (6)
A6 (7)
A7 (8)
A8 (9)
(18) B1
(17) B2
(16) B3
(15) B4
(14) B5
(13) B6
(12) B7
(11) B8
LS08930S

These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic levels at the Enable inputs ($\overline{G}$BA and GAB). The Enable inputs can be used to disable the device so that the buses are effectively isolated.

The dual-enable configuration gives the 'F621 and 'F622 the capability to store data by the simultaneous enabling of $\overline{G}$BA and GAB. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of the bus lines are at high-impedance, both sets of bus lines (16 in all) will remain at their last states.

FUNCTION TABLE

ENABLE INPUTS		MODE OF OPERATION	
$\overline{G}$BA	**GAB**	**'F621**	**'F622**
L	L	B data to A bus	$\overline{B}$ data to A bus
H	H	A data to B bus	$\overline{A}$ data to B bus
H	L	Z or OFF	Z or OFF
L	H	B data to A bus, A data to B bus	$\overline{B}$ data to A bus, $\overline{A}$ data to B bus

H = High voltage level
L = Low voltage level
Z = High-impedance (OFF) state
OFF = High if pull-up resistor is connected to Open-Collector output

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		−0.5 to +7.0	V
V_{IN}	Input voltage		−0.5 to +7.0	V
I_{IN}	Input current		−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		−0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	$A_1 - A_8$	40	mA
		$B_1 - B_8$	128	mA
T_A	Operating free-air temperature range		0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
V_{OH}	High-level output voltage				4.5	V
I_{OL}	Low-level output current	$A_1 - A_8$			20	mA
		$B_1 - B_8$			64	mA
T_A	Operating free-air temperature		0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			74F621, 74F622			UNIT
						Min	Typ[2]	Max	
I_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, V_{OH} = MAX					250	μA
V_{OL}	Low-level output voltage	$A_1 - A_8$	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 20mA	±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
		$B_1 - B_8$		I_{OL} = 48mA	±10%V_{CC}		0.40	0.55	V
				I_{OL} = 64mA	±5%V_{CC}		0.40	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$				−0.73	−1.2	V
I_I	Input current at maximum input voltage	$\overline{G}$BA, GAB	V_{CC} = 0.0V, V_I = 7.0V					100	μA
		Others	V_{CC} = 5.5V, V_I = 5.5V					1	mA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					−20	μA
I_{CC}	Supply current (total)	'F621 I_{CCH}	V_{CC} = MAX	$\overline{G}$BA = GAB = 4.5V; $A_1 - A_8$ = 4.5V			105	140	mA
		'F621 I_{CCL}		$\overline{G}$BA = GAB = 4.5V; $A_1 - A_8$ = GND			105	140	mA
		'F622 I_{CCH}		$\overline{G}$BA = GAB = 4.5V; $A_1 - A_8$ = GND			37	48	mA
		'F622 I_{CCL}		$\overline{G}$BA = GAB = 4.5V; $A_1 - A_8$ = 4.5V			68	90	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.

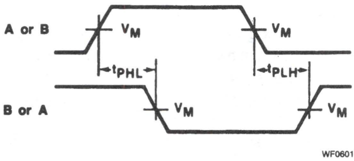
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F621					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A to B	Waveform 2	6.0 4.0	9.5 6.0	12.0 8.0	5.5 3.5	13.0 8.5	ns
t_{PLH} t_{PHL}	Propagation delay B to A	Waveform 2	6.0 3.5	9.0 5.5	12.0 7.5	5.5 3.0	12.5 8.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{G}$BA to A	Waveform 3	6.0 3.5	10.0 6.5	13.5 10.5	5.5 3.0	14.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay GAB to B	Waveform 4	7.0 3.5	12.0 6.5	15.0 9.5	6.0 3.0	17.0 10.0	ns

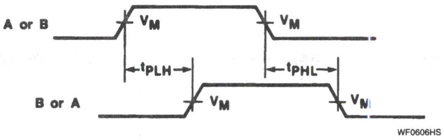
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F622					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A to B	Waveform 1	8.0 1.5	11.0 4.0	12.5 5.5	8.0 1.5	13.5 6.0	ns
t_{PLH} t_{PHL}	Propagation delay B to A	Waveform 1	7.5 1.5	10.0 3.5	12.0 5.0	7.5 1.5	12.5 5.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{G}$BA to A	Waveform 3	8.0 6.0	10.5 8.0	12.0 10.0	8.0 6.0	12.5 10.5	ns
t_{PLH} t_{PHL}	Propagation delay GAB to B	Waveform 4	10.0 5.0	12.5 7.5	14.5 9.0	10.0 5.0	15.5 9.5	ns

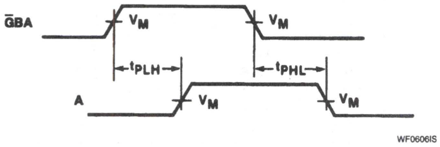
AC WAVEFORMS


A or B
VM
VM
tPHL
tPLH
B or A
VM
VM
WF0601TS

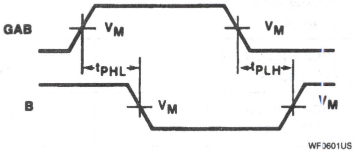
Waveform 1. Propagation Delay for A to B or B to A (F622)


A or B
VM
VM
tPLH
tPHL
B or A
VM
VM
WF0606HS

Waveform 2. Propagation Delay for A to B or B to A (F621)


GBA
VM
VM
tPLH
tPHL
A
VM
VM
WF0606IS

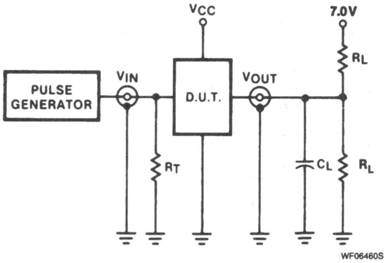
Waveform 3. Propagation Delay for GBA to A


GAB
VM
VM
tPHL
tPLH
B
VM
VM
WF0601US

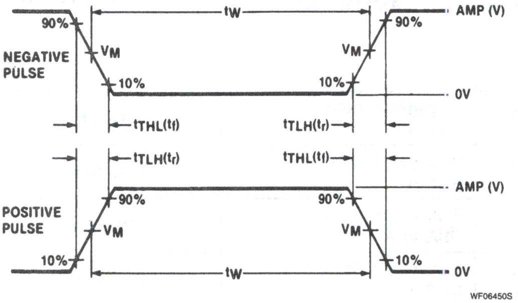
Waveform 4. Propagation Delay for GAB to B

NOTE: For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORMS


VCC
7.0V
RL
PULSE GENERATOR
VIN
D.U.T.
VOUT
RT
CL
RL
WF06460S

Test Circuit for Open-Collector Outputs


NEGATIVE PULSE
90%
VM
10%
tW
90%
VM
10%
AMP (V)
0V
tTHL(tf)
tTLH(tr)
tTLH(tr)
tTHL(tf)
POSITIVE PULSE
90%
VM
10%
90%
VM
10%
tW
AMP (V)
0V
WF06450S

$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST Products

FAST 74F630, 74F631
Error Detection Correction

16-Bit Parallel Error Detection and Correction
('F630 — 3-State)
('F631 — Open-Collector)
Preliminary Specification

FEATURES

- **High-impedance NPN base input for reduced loading (20µA in High and Low states)**
- **Detects and corrects single-bit errors**
- **Detects and flags dual-bit errors**
- **Fast processing times:**
  - **Write cycle: Generates check word in 20ns typical**
  - **Read cycle: Flags errors in 25ns typical**
- **Power dissipation 600mW (typical)**
- **Choice of output configurations**
  - **'F630: 3-State**
  - **'F631: Open-Collector**

DESCRIPTION

The 'F630 and 'F631 devices are 16-bit parallel error detection and correction circuits (EDACs) in 28-pin, 600-mil packages. They use a modified Hamming code to generate a 6-bit check word from a 16-bit data word.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F630	17ns	120mA
74F631	17ns	120mA

ORDERING INFORMATION

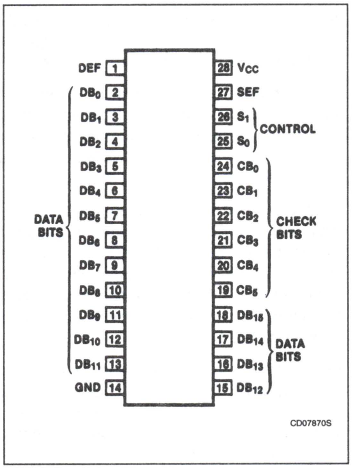
PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
28-Pin Plastic DIP	N74F630N, N74F631N
28-Pin Plastic SOL	N74F630D, N74F631D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
S_0, S_1	Control	1.0/0.033	20µA/20µA
$CB_0 - CB_{15}$	Check bits, input	1.0/0.033	20µA/20µA
$DB_0 - DB_{15}$	Data bits, input	1.0/0.033	20µA/20µA
$CB_0 - CB_5$	Check bits, output for 'F630	150/33.3	3mA/20mA
$CB_0 - CB_5$	Check bits, output for 'F631	*OC/33.3	*OC/20mA
$DB_0 - DB_{15}$	Data bits, outputs for 'F630	150/33.3	3mA/20mA
$DB_0 - DB_{15}$	Data bits, outputs for 'F631	*OC/33.3	*OC/20mA
SEF, DEF	Error flags outputs for 'F630	150/33.3	3mA/20mA
SEF, DEF	Error flags outputs for 'F631	*OC/33.3	*OC/20mA

NOTES:
1. One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.
2. *OC = Open-Collector

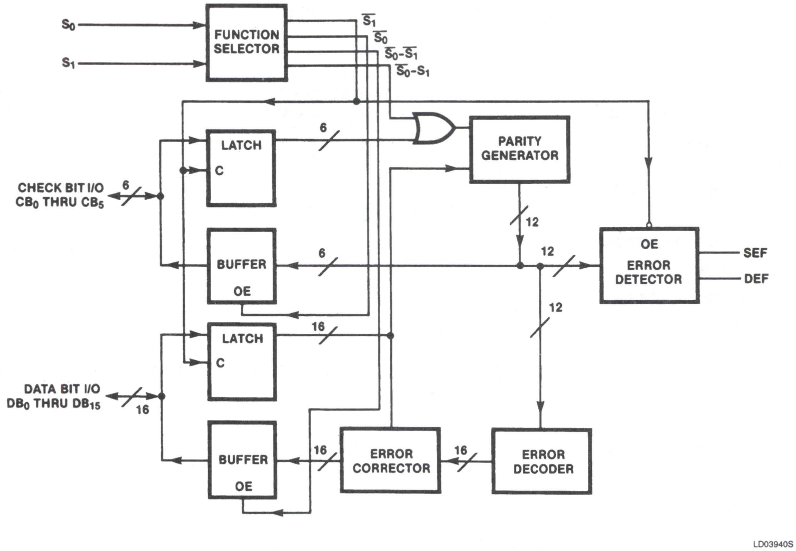
PIN CONFIGURATION


DEF 1
DB0 2
DB1 3
DB2 4
DB3 5
DB4 6
DB5 7
DB6 8
DB7 9
DB8 10
DB9 11
DB10 12
DB11 13
GND 14
DATA BITS
28 Vcc
27 SEF
26 S1
25 S0
CONTROL
24 CB0
23 CB1
22 CB2
21 CB3
20 CB4
19 CB5
CHECK BITS
18 DB15
17 DB14
16 DB13
15 DB12
DATA BITS
CD07870S

Error Detection Correction

FAST 74F630, 74F631

LOGIC DIAGRAM



This check word is stored along with the data word during the memory write cycle. During the memory read cycle, the 22-bit words from memory are processed by the EDACs to determine if errors have occurred in memory.

Single-bit errors in the 16-bit data word are flagged and corrected. Single-bit errors in the 6-bit check word are flagged, and the CPU sends the EDAC through the correction cycle even though the 16-bit word is not in error. The correction cycle will simply pass along the original 16-bit word in this case and produce error syndrome bits to pinpoint the error-generating location.

Dual-bit errors are flagged but not corrected. These dual errors may occur in any 2 bits of the 22-bit word from memory (two errors in the 16-bit data word, two errors in the 6-bit check word, or one error in each word).

The gross-error condition of all Lows or all Highs from memory will be detected. Otherwise, errors in three or more bits of the 22-bit word are beyond the capabilities of these devices to detect.

In order to be able to determine whether the data from the memory is acceptable to use as presented to the bus, the EDAC must be strobed to enable the error flags, and the flags will have to be tested for the zero condition.

The first case in the error function table represents the normal, no-error condition. The CPU sees Lows on both flags. The next two cases of single-bit errors require data correction. Although the EDAC can discern the single check bit error and ignore it, the error flags are identical to the single error in the 16-bit data word. The CPU will ask for data correction in both cases. An interrupt condition to the CPU results in each of the last three cases, where dual errors occur.

ERROR DETECTION AND CORRECTION DETAILS

During a memory write cycle, six check bits ($CB_0 - CB_5$) are generated by eight-input parity generators using the data bits as defined below. During a memory read cycle, the 6-bit check word is retrieved along with the actual data.

Error detection is accomplished as the 6-bit check word and the 16-bit data word from memory are applied to internal parity generators/checkers. If the parity of all six groupings of data and check bits is correct, it is assumed that no error has occurred and both error flags will be Low. (It should be noted that the sense of two of the check bits, CB_0 and CB_1, is inverted to ensure that the gross-error condition of all Lows and all Highs is detected.)

If the parity of one or more of the check groups is incorrect, an error has occurred and the proper error flag or flags will be set High. Any single error in the 16-bit data word will change the sense of exactly 3 bits of the 6-bit check word. Any single error in the 6-bit check word changes the sense of only that one bit. In either case, the single-error flag will be set High while the dual-error flag will remain Low.

Any 2-bit error will change the sense of an even number of check bits. The 2-bit error is not correctable, since the parity tree can only identify single-bit errors. Both error flags are set High when any 2-bit error is detected.

Three or more simultaneous bit errors can fool the EDAC into believing that no error, a correctable error, or an uncorrectable error has occurred and produce erroneous results in all three cases.

Error correction is accomplished by identifying the bad bit and inverting it. Identification of the erroneous bit is achieved by comparing the 16-bit data word and 6-bit check word from memory with the new check word with one (check word error) or three (data word error) inverted bits.

As the corrected word is made available on the data word I/O port, the check word I/O port presents a 6-bit syndrome error code. This syndrome code can be used to identify the bad memory chip.

Error Detection Correction FAST 74F630, 74F631

FUNCTION TABLE

TOTAL NUMBER OF ERRORS		ERROR FLAGS		DATA CORRECTION
16-Bit Data	6-Bit Check Word	SEF	DEF	
0	0	L	L	Not Applicable
1	0	H	L	Correction
0	1	H	L	Correction
1	1	H	H	Interrupt
2	0	H	H	Interrupt
0	2	H	H	Interrupt

H = High voltage level, L = Low voltage level

CHECK WORD BIT	16-BIT DATA WORD															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CB_0	X	X		X	X				X	X	X			X		
CB_1	X		X	X		X	X		X			X			X	
CB_2		X	X		X	X		X		X			X			X
CB_3	X	X	X				X	X			X	X	X			
CB_4				X	X	X	X	X						X	X	X
CB_5									X	X	X	X	X	X	X	X

NOTE:

1. The six check bits are parity bits derived from the matrix of data bits as indicated by "X" for each bit.

ERROR SYNDROME TABLE

ERROR LOCATION	SYNDROME ERROR CODE					
	CB_0	CB_1	CB_2	CB_3	CB_4	CB_5
DB_0	L	L	H	L	H	H
DB_1	L	H	L	L	H	H
DB_2	H	L	L	L	H	H
DB_3	L	L	H	H	L	H
DB_4	L	H	L	H	L	H
DB_5	H	L	L	H	L	H
DB_6	H	L	H	L	L	H
DB_7	H	H	L	L	L	H
DB_8	L	L	H	H	H	L
DB_9	L	H	L	H	H	L
DB_{10}	L	H	H	L	H	L
DB_{11}	H	L	H	L	H	L
DB_{12}	H	H	L	L	H	L
DB_{13}	L	H	H	H	L	L
DB_{14}	H	L	H	H	L	L
DB_{15}	H	H	L	H	L	L
CB_0	L	H	H	H	H	H
CB_1	H	L	H	H	H	H
CB_2	H	H	L	H	H	H
CB_3	H	H	H	L	H	H
CB_4	H	H	H	H	L	H
CB_5	H	H	H	H	H	L
No Error	H	H	H	H	H	H

H = High voltage level
L = Low voltage level

Error Detection Correction

FAST 74F630, 74F631

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
V_{OH}	High-level output voltage	'F631			4.5	V
I_{OH}	High-level output current	'F630			−3	mA
I_{OL}	Low-level output current				20	mA
T_A	Operating free-air temperature		0		70	°C

Error Detection Correction

FAST 74F630, 74F631

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		74F630			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.4			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = 0.0V, V_I = 7.0V				100	μA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				−20	μA
I_{OZH}	OFF-state output current, High-level voltage applied		V_{CC} = MAX, V_O = 2.7V				50	μA
I_{OZL}	OFF-state output current, Low-level voltage applied		V_{CC} = MAX, V_O = 0.5V				−50	μA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX					mA
		I_{CCL}						mA
		I_{CCZ}						mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		74F631			UNIT
					Min	Typ[2]	Max	
I_{OH}	High-level output current		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, V_{OH} = MAX				250	μA
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				−20	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX					mA
		I_{CCL}						mA
		I_{CCZ}						mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F630					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay DB to CB	Waveform 1			22 20			ns
t_{PLH} t_{PHL}	Propagation delay SI to DEF, SEF	Waveform 1			13 12			ns
t_{PZH} t_{PZL}	Output enable time to High level, SO to CB, DB	Waveform 3 & 4			12 12			ns
t_{PHZ} t_{PLZ}	Output disable time from High level, SO to CB, DB	Waveform 3 & 4			15 15			ns

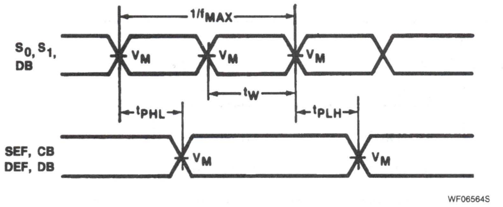
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F631					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay DB to CB	Waveform 1			25 18			ns
t_{PLH} t_{PHL}	Propagation delay SI to DEF, SEF	Waveform 1			16 11			ns
t_{PHL} t_{PLH}	Propagation delay time, High-to-Low level output, SO to CB, DB	Waveform 1			12 16			ns

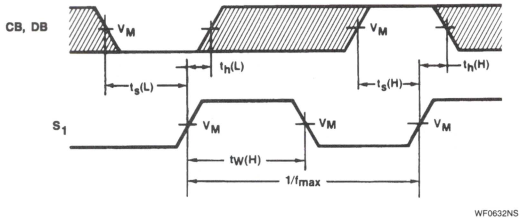
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	74F630, 'F631					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_s	Setup time, CB or DB to SI	Waveform 2	4					ns
t_h	Hold time, CB or DB to SI	Waveform 2	4					ns

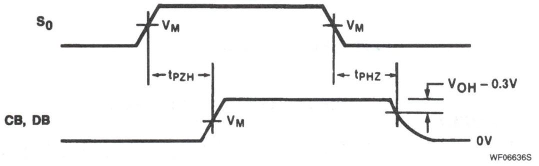
AC WAVEFORMS


1/fMAX
S0, S1, DB
VM
VM
VM
tW
tPHL
tPLH
SEF, CB
DEF, DB
VM
VM
WF06564S

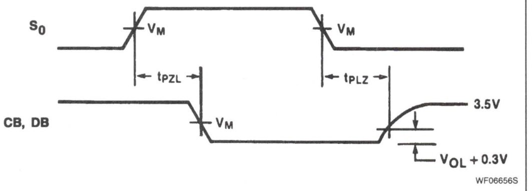
Waveform 1.
DB To CB
SI To DEF, SEF
SO To CB, DB
Delays


CB, DB
VM
VM
th(L)
th(H)
ts(L)
ts(H)
S1
VM
VM
VM
tW(H)
1/fmax
WF0632NS

Waveform 2. Data Setup and Hold Times


S0
VM
VM
tPZH
tPHZ
VOH − 0.3V
CB, DB
VM
0V
WF06636S

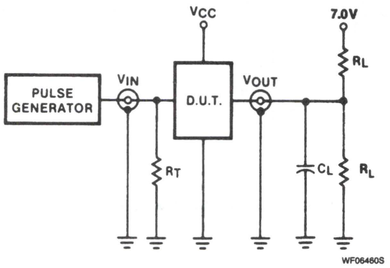
Waveform 3. 3-State Enable Time to High Level and Disable Time From High Level


S0
VM
VM
tPZL
tPLZ
3.5V
CB, DB
VM
VOL + 0.3V
WF06656S

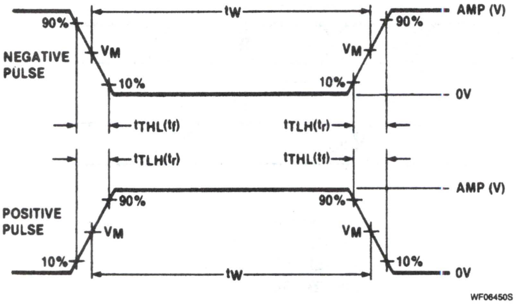
Waveform 4. 3-State Enable Time to Low Level and Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS


VCC
7.0V
RL
PULSE GENERATOR
VIN
D.U.T.
VOUT
RT
CL
RL
WF06460S

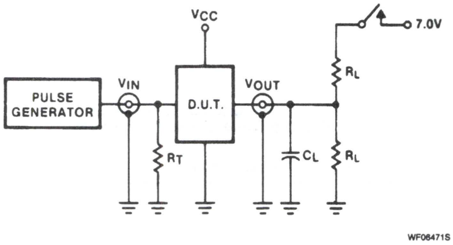
Test Circuit for Open-Collector Outputs ('F631)


NEGATIVE PULSE
90%
VM
10%
tW
AMP (V)
0V
tTHL(tf)
tTLH(tr)
POSITIVE PULSE
90%
VM
10%
tTLH(tr)
tTHL(tf)
AMP (V)
0V
WF06450S

$V_M = 1.5V$

Input Pulse Definition

<table>
<tr><th rowspan="2">FAMILY</th><th colspan="5">INPUT PULSE REQUIREMENTS</th></tr>
<tr><th>Amplitude</th><th>Rep. Rate</th><th>Pulse Width</th><th>t_{TLH}</th><th>t_{THL}</th></tr>
<tr><td>74F</td><td>3.0V</td><td>1MHz</td><td>500ns</td><td>2.5ns</td><td>2.5ns</td></tr>
</table>


VCC
7.0V
RL
PULSE GENERATOR
VIN
D.U.T.
VOUT
RT
CL
RL
WF06471S

Test Circuit for 3-State Outputs ('F630)

SWITCH POSITION

TEST	SWITCH
t_{PZH}	open
t_{PZL}	closed
t_{PHZ}	open
t_{PLZ}	closed

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Signetics

FAST 74F640

Transceiver

Octal Bus Transceiver, Inverting (3-State)

Product Specification

FAST Products

FEATURES

- **High-impedance NPN base inputs for reduced loading (70μA in High and Low states)**
- **Ideal for applications which require high-output drive and minimal bus loading**
- **Inverting version of 'F245**
- **Octal bidirectional bus interface**
- **3-State buffer outputs sink 64mA and source 15mA**

DESCRIPTION

The 'F640 is an octal transceiver featuring inverting 3-State bus-compatible outputs in both send and receive directions.

The $B_1 - B_8$ outputs are capable of sinking 64mA and sourcing 15mA, providing very good capacitive drive characteristics.

These octal bus transceivers are designed for asynchronous two-way communication between data busses.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F640	3.5ns	78mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
20-Pin Plastic DIP	N74F640N
20-Pin Plastic SOL	N74F640D

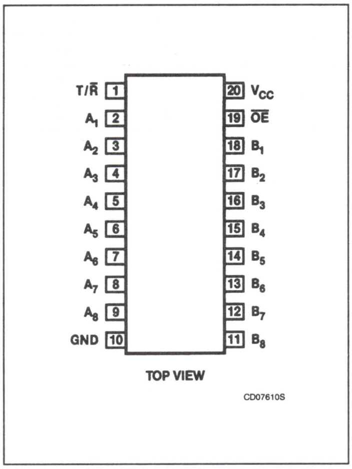
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$A_1 - A_8$, $B_1 - B_8$	Data inputs	3.5/0.115	70uA/70μA
$T/\overline{R}$	Transmit/receive input	2.0/0.067	40uA/40μA
$\overline{OE}$	Output enable inputs (active-Low)	2.0/0.067	40uA/40μA
$A_1 - A_8$	Data outputs	150/40	3mA/24mA
$B_1 - B_8$	Data outputs	750/106.7	15mA/64mA

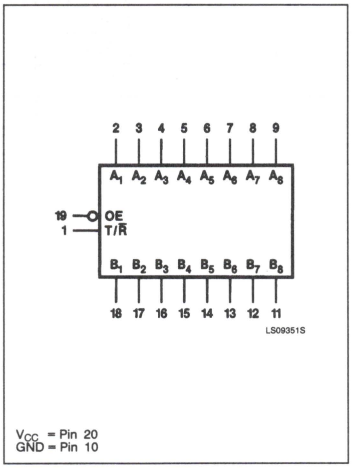
NOTE:

1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION

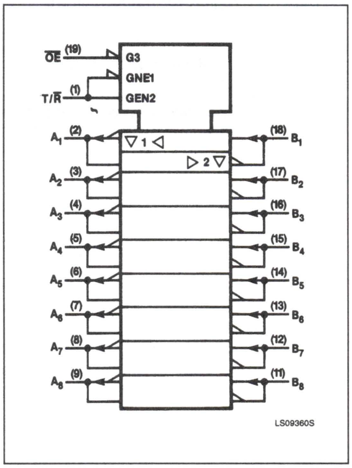

T/R̄ 1
A1 2
A2 3
A3 4
A4 5
A5 6
A6 7
A7 8
A8 9
GND 10
20 VCC
19 OE̅
18 B1
17 B2
16 B3
15 B4
14 B5
13 B6
12 B7
11 B8
TOP VIEW
CD07610S

LOGIC SYMBOL


2 3 4 5 6 7 8 9
A1 A2 A3 A4 A5 A6 A7 A8
19 OE
1 T/R̄
B1 B2 B3 B4 B5 B6 B7 B8
18 17 16 15 14 13 12 11
LS09351S

V_{CC} = Pin 20
GND = Pin 10

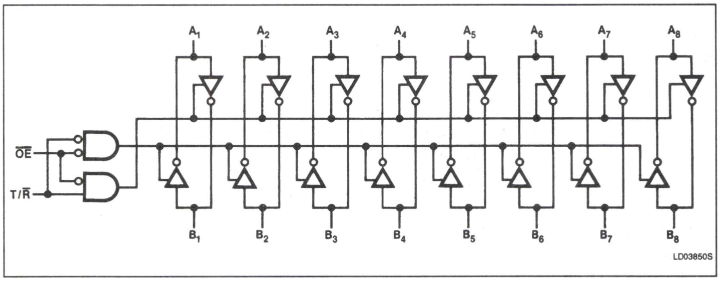
LOGIC SYMBOL (IEEE/IEC)


OE̅ (19)
T/R̄ (1)
G3
GNE1
GEN2
▽1◁
▷2▽
A1 (2)
A2 (3)
A3 (4)
A4 (5)
A5 (6)
A6 (7)
A7 (8)
A8 (9)
(18) B1
(17) B2
(16) B3
(15) B4
(14) B5
(13) B6
(12) B7
(11) B8
LS09360S

Transceiver

FAST 74F640

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS		OUTPUTS
$\overline{OE}$	T/$\overline{R}$	
L	L	Bus $\overline{B}$ data to Bus A
L	H	Bus $\overline{A}$ data to Bus B
H	X	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High-impedance state

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		−0.5 to +7.0	V
V_{IN}	Input voltage		−0.5 to +7.0	V
I_{IN}	Input current		−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	$A_1 - A_8$	48	mA
		$B_1 - B_8$	128	mA
T_A	Operating free-air temperature range		0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.50	5.0	5.50	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	High-level output current	$A_1 - A_8$			−3	mA
		$B_1 - B_8$			−15	mA
I_{OL}	Low-level output current	$A_1 - A_8$			24	mA
		$B_1 - B_8$			64	mA
T_A	Operating free-air temperature		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			74F640			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage	$A_1 - A_8$ $B_1 - B_8$	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = −3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.4		V
		$B_1 - B_8$		I_{OH} = −15mA	±10%V_{CC}	2.0			V
					±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage	$A_1 - A_8$	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 24mA	±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
		$B_1 - B_8$		I_{OL} = 48mA	±10%V_{CC}		0.40	0.55	V
				I_{OL} = 64mA	±5%V_{CC}		0.40	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$				−0.73	−1.2	V
I_I	Input current at maximum input voltage	$A_1 - A_8$ $B_1 - B_8$	V_{CC} = 5.5V, V_I = 5.5V					1.0	mA
		$\overline{OE}$, T/$\overline{R}$	V_{CC} = 0.0V, V_I = 7.0V					100	μA
I_{IH}	High-level input current	$\overline{OE}$, T/$\overline{R}$ only	V_{CC} = MAX, V_I = 2.7V					40	μA
I_{IL}	Low-level input current	$\overline{OE}$, T/$\overline{R}$ only	V_{CC} = MAX, V_I = 0.5V					−40	μA
I_{IH}+ I_{OZH}	OFF-state current, High-level voltage applied		V_{CC} = MAX, V_O = 2.7V					70	μA
I_{IL}+ I_{OZL}	OFF-state current, Low-level voltage applied		V_{CC} = MAX, V_O = 0.5V					−70	μA
I_{OS}	Short-circuit output current[3]	$A_1 - A_8$	V_{CC} = MAX			−60		−150	mA
		$B_1 - B_8$				−100		−225	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	T/$\overline{R}$ = $A_1 - A_8$ = 4.5V; $\overline{OE}$ = GND			66	85	mA
		I_{CCL}		$\overline{OE}$ = T/$\overline{R}$ = $B_1 - B_8$ = GND			91	120	mA
		I_{CCZ}		$\overline{OE}$ = 4.5V; T/$\overline{R}$ = $B_1 - B_8$ = GND			78	102	mA

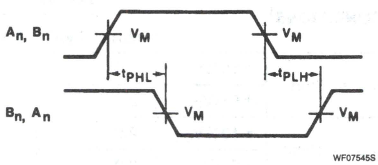
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

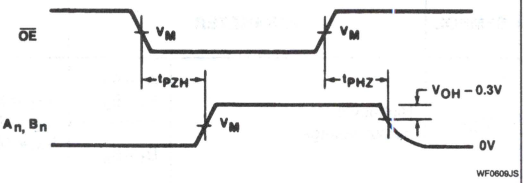
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F640					UNIT
			T_A = +25°C V_{CC} = +5.0V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH}	Propagation delay	Waveform 1	2.0	4.5	7.0	2.0	8.0	ns
t_{PHL}	A_n to B_n, B_n to A_n		1.0	2.5	5.0	1.0	5.5	
t_{PZH}	Output enable time	Waveform 2	6.0	9.0	11.0	6.0	13.0	ns
t_{PZL}	to High or Low level	Waveform 3	6.0	9.0	11.0	6.0	11.5	
t_{PHZ}	Output disable time	Waveform 2	2.5	5.5	8.0	2.5	9.0	ns
t_{PLZ}	from High or Low level	Waveform 3	2.0	4.5	7.0	2.0	7.5	

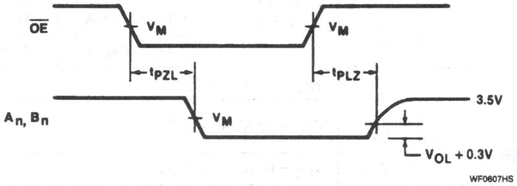
AC WAVEFORMS


An, Bn
VM
VM
tPHL
tPLH
Bn, An
VM
VM
WF07545S

Waveform 1. Propagation Delays for A_n to B_n or B_n to A_n


OE
VM
VM
tPZH
tPHZ
VOH – 0.3V
An, Bn
VM
0V
WF0609JS

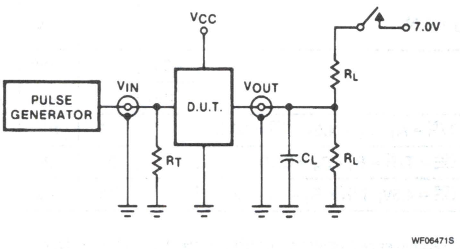
Waveform 2. 3-State Output Enable Time to High Level and Output Disable Time From High Level


OE
VM
VM
tPZL
tPLZ
An, Bn
VM
3.5V
VOL + 0.3V
WF0607HS

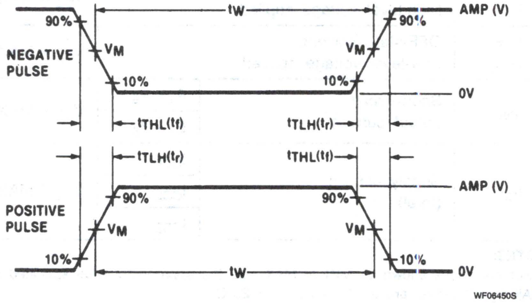
Waveform 3. 3-State Output Enable Time to Low Level and Output Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORMS


VCC
7.0V
PULSE GENERATOR
VIN
D.U.T.
VOUT
RL
RT
CL
RL
WF06471S

Test Circuit for 3-State Outputs


tW
AMP (V)
90%
90%
NEGATIVE PULSE
VM
VM
10%
10%
0V
tTHL(tf)
tTLH(tr)
tTLH(tr)
tTHL(tf)
AMP (V)
90%
90%
POSITIVE PULSE
VM
VM
10%
10%
0V
tW
WF06450S

$V_M = 1.5V$

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F641, 74F642

Transceivers

'F641 – Octal Bus Transceiver with Common Output Enable, Non-Inverting (Open-Collector)
'F642 – Octal Bus Transceiver with Common Output Enable, Inverting (Open-Collector)
Product Specification

FAST Products

FEATURES

- **High-impedance NPN base inputs for reduced loading (20μA in High and Low states)**
- **Octal bidirectional bus interface**
- **Common Output Enable for both Transmit and Receive modes**
- **Open-Collector outputs sink 64mA**
- **'F641 Non-inverting**
  'F642 Inverting

FUNCTION TABLE 'F641

INPUTS		INPUTS/OUTPUTS	
$\overline{OE}$	T/$\overline{R}$	A_n	B_n
L	L	A = B	INPUTS
L	H	INPUTS	B = A
H	X	Z	Z

FUNCTION TABLE 'F642

INPUTS		INPUTS/OUTPUTS	
$\overline{OE}$	T/$\overline{R}$	A_n	B_n
L	L	A = $\overline{B}$	INPUTS
L	H	INPUTS	B = $\overline{A}$
H	X	Z	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High-impedance state

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F641	8.0ns	69mA
74F642	8.5ns	52mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F641N, N74F642N
20-Pin Plastic SOL	N74F641D, N74F642D

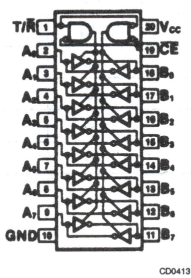
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$A_0 - A_7$, $B_0 - B_7$	Data inputs	1.0/0.033	20μA/20μA
T/$\overline{R}$	Transmit/receive input	2.0/0.067	40μA/40μA
$\overline{OE}$	Common output enable input (active-Low)	2.0/0.067	40μA/40μA
$A_0 - A_7$	Data outputs	*OC/33	*OC/20mA
$B_0 - B_7$	Data outputs	*OC/106.7	*OC/64mA

NOTES:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.
2. *OC = Open-Collector

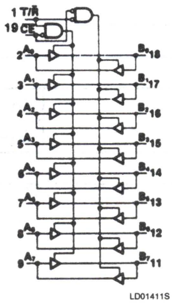
PIN CONFIGURATION

'F641


T/R̄ 1
A0 2
A1 3
A2 4
A3 5
A4 6
A5 7
A6 8
A7 9
GND 10
20 Vcc
19 CE
18 B0
17 B1
16 B2
15 B3
14 B4
13 B5
12 B6
11 B7
CD04131S

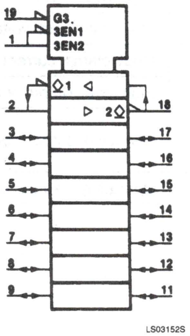
LOGIC SYMBOL

'F641


1 T/R̄
19 CE
2 A0
3 A1
4 A2
5 A3
6 A4
7 A5
8 A6
9 A7
B0 18
B1 17
B2 16
B3 15
B4 14
B5 13
B6 12
B7 11
LD01411S

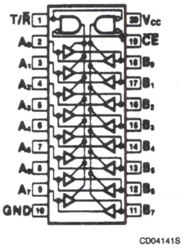
LOGIC SYMBOL (IEEE/IEC)

'F641


19
1
G3
3EN1
3EN2
1
2
18
3
4
5
6
7
8
9
17
16
15
14
13
12
11
LS03152S

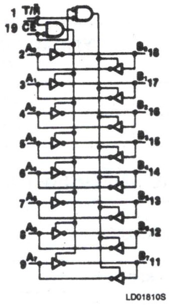
PIN CONFIGURATION

'F642


T/R̄ 1
A0 2
A1 3
A2 4
A3 5
A4 6
A5 7
A6 8
A7 9
GND 10
20 Vcc
19 CE
18 B0
17 B1
16 B2
15 B3
14 B4
13 B5
12 B6
11 B7
CD04141S

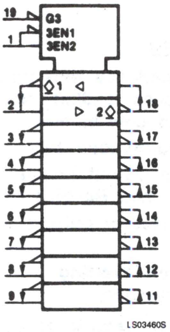
LOGIC SYMBOL

'F642


1 T/R̄
19 CE
2 A0
3 A1
4 A2
5 A3
6 A4
7 A5
8 A6
9 A7
B0 18
B1 17
B2 16
B3 15
B4 14
B5 13
B6 12
B7 11
LD01810S

LOGIC SYMBOL (IEEE/IEC)

'F642


19
1
G3
3EN1
3EN2
1
2
2
3
4
5
6
7
8
9
18
17
16
15
14
13
12
11
LS03460S

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		−0.5 to +7.0	V
V_{IN}	Input voltage		−0.5 to +7.0	V
I_{IN}	Input current		−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		−0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	$A_0 - A_7$	40	mA
		$B_0 - B_7$	128	mA
T_A	Operating free-air temperature range		0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
V_{OH}	High-level output voltage				4.5	mA
I_{OL}	Low-level output current	$A_0 - A_7$			20	mA
		$B_0 - B_7$			64	mA
T_A	Operating free-air temperature		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]			74F641/74F642			UNIT
							Min	Typ[2]	Max	
V_{OH}	High-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, V_{OH} = MAX					250	μA
V_{OL}	Low-level output voltage	$A_0 - A_7$		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 20mA	±10%V_{CC}		0.35	0.50	V
						±5%V_{CC}		0.35	0.50	V
		$B_0 - B_7$			I_{OL} = 48mA	±10%V_{CC}		0.40	0.55	V
					I_{OL} = 64mA	±5%V_{CC}		0.40	0.55	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, $I_I = I_{IK}$				−0.73	−1.2	V
I_I	Input current at maximum input voltage	$T/\overline{R}$, $\overline{OE}$		V_{CC} = 0.0V, V_I = 7.0V					100	μA
		$A_0 - A_7$, $B_0 - B_7$		V_{CC} = 5.5V, V_i = 5.5V					1.0	mA
I_{IH}	High-level input current	$T/\overline{R}$, $\overline{OE}$		V_{CC} = MAX, V_I = 2.7V					40	μA
		$A_0 - A_7$, $B_0 - B_7$							20	μA
I_{IL}	Low-level input current	$T/\overline{R}$, $\overline{OE}$		V_{CC} = MAX, V_I = 0.5V					−40	μA
		$A_0 - A_7$, $B_0 - B_7$							−20	μA
I_{CC}	Supply current (total)	'F641	I_{CCH}	V_{CC} = MAX	$A_n = T/\overline{R}$ = 4.5V; $\overline{OE}$ = GND			60	90	mA
			I_{CCL}		$T/\overline{R}$ = 4.5V; $A_n = \overline{OE}$ = GND			78	120	mA
		'F642	I_{CCH}		$A_n = T/\overline{R} = \overline{OE}$ = 4.5V			37	55	mA
			I_{CCL}		$A_n = T/\overline{R}$ = 4.5V; $\overline{OE}$ = GND			67	98	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

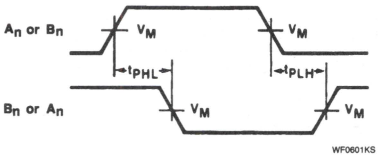
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F641					UNIT
			T_A = +25°C V_{CC} = +5.0V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = +5.0V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n	Waveform 2	7.5 4.0	10.0 6.0	12.5 9.5	7.5 4.0	13.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay B_n to A_n	Waveform 2	6.0 3.5	9.5 5.5	12.0 7.5	6.0 3.5	12.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{OE}$ to A_n	Waveform 3	7.0 5.0	10.5 7.0	12.5 9.0	7.0 5.0	13.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{OE}$ to B_n	Waveform 4	9.0 5.5	10.5 7.5	12.5 9.5	9.0 5.5	13.5 10.5	ns

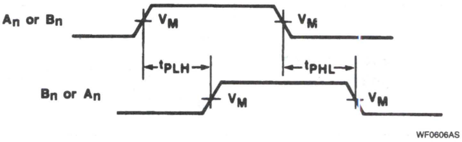
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F642					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n	Waveform 1	9.0 2.0	11.5 4.5	13.5 6.5	9.0 2.0	14.5 7.0	ns
t_{PLH} t_{PHL}	Propagation delay B_n to A_n	Waveform 1	8.5 1.5	10.5 4.0	12.5 6.0	8.5 1.5	13.0 6.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{OE}$ to A_n	Waveform 3	8.5 6.0	10.5 8.0	12.5 10.5	8.5 6.0	13.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{OE}$ to B_n	Waveform 4	9.0 6.5	11.5 9.0	13.5 11.0	9.0 6.5	14.0 11.5	ns

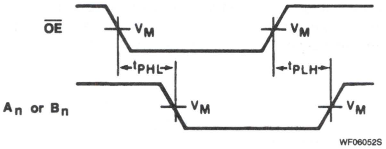
AC WAVEFORM


An or Bn
VM
VM
tPHL
tPLH
Bn or An
VM
VM
WF0601KS

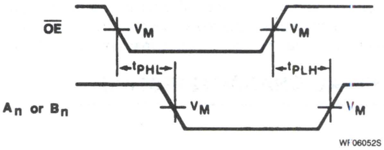
Waveform 1. Propagation Delay for A_n to B_n or B_n to A_n (F642)


An or Bn
VM
VM
tPLH
tPHL
Bn or An
VM
VM
WF0606AS

Waveform 2. Propagation Delays for A_n to B_n or B_n to A_n (F641)


OE
VM
VM
tPHL
tPLH
An or Bn
VM
VM
WF06052S

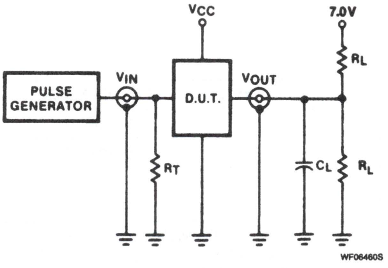
Waveform 3. Propagation Delay for $\overline{OE}$ to A_n or B_n Outputs ('F642) (B_n or A_n Inputs in High State)


OE
VM
VM
tPHL
tPLH
An or Bn
VM
VM
WF06052S

Waveform 4. Propagation Delays for $\overline{OE}$ to A_n or B_n Outputs ('F641) (B_n or A_n Inputs in Low State)

NOTE: For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORMS


VCC
7.0V
RL
PULSE GENERATOR
VIN
D.U.T.
VOUT
RT
CL
RL
WF06460S

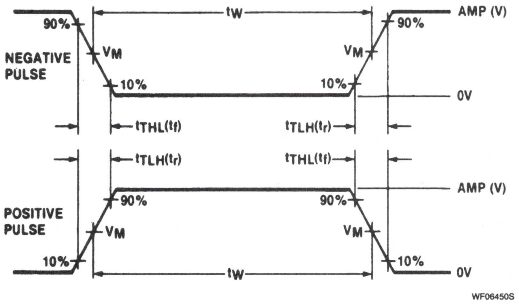
Test Circuit for Open-Collector Outputs

DEFINITIONS

R_L = Load resistor to GND; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.


tW
90%
AMP (V)
NEGATIVE PULSE
VM
VM
10%
10%
0V
tTHL(tf)
tTLH(tr)
tTLH(tr)
tTHL(tf)
AMP (V)
90%
90%
POSITIVE PULSE
VM
VM
10%
10%
0V
tW
WF06450S

$V_M = 1.5V$

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST Products

FAST 74F646, 74F648

Transceivers/Registers

'F646 — Octal Transceiver/Register, Non-Inverting (3-State)
'F648 — Octal Transceiver/Register, Inverting (3-State)
Product Specification

FEATURES

- **Combines 'F245 and 'F374 type functions in one chip**
- **High-impedance NPN base inputs for reduced loading (70μA in High and Low states)**
- **Independent registers for A and B buses**
- **Multiplexed real-time and stored data**
- **Choice of non-inverting and inverting data paths**
- **3-State outputs**
- **300mil wide 24-pin Slim DIP package**

DESCRIPTION

These devices consist of bus transceiver circuits with 3-State outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to a High logic level. Enable $\overline{G}$ and DIR pins are provided to control the transceiver function. In the transceiver mode, data present at the High-impedance port may be stored in either the A or B register or both.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F646	115MHz	140mA
74F648	115MHz	140mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
24-Pin Plastic Slim DIP (300mil)	N74F646N, N74F648N
24-Pin Plastic SOL[1]	N74F646D, N74F648D

NOTE:
1. Thermal mounting techniques are recommeded. See App Note AN SMD-100 for a discussion of thermal considerations for surface mounted devices.

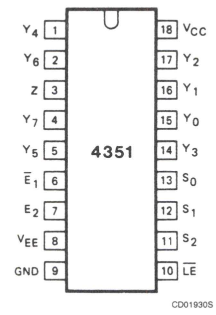
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$A_0 - A_7$	A inputs	3.5/0.0116	70μA/70μA
$B_0 - B_7$	B inputs	3.5/0.0116	70μA/70μA
CPAB	A-to-B Clock input	1.0/0.033	20μA/20μA
CPBA	B-to-A Clock input	1.0/0.033	20μA/20μA
SAB	A-to-B Select input	1.0/0.033	20μA/20μA
SBA	B-to-A Select input	1.0/0.033	20μA/20μA
DIR	Data flow Directional control Enable input	1.0/0.033	20μA/20μA
$\overline{OE}$	Output Enable Input	1.0/0.033	20μA/20μA
$A_0 - A_7$	A outputs	750/106.7	15mA/64mA
$B_0 - B_7$	B outputs	750/106.7	15mA/64mA

NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

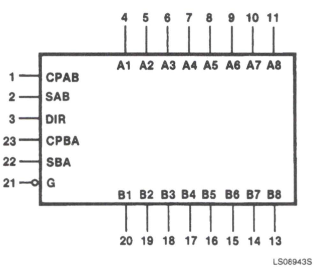
PIN CONFIGURATION

'F646


Y4 1
Y6 2
Z 3
Y7 4
Y5 5
Ē1 6
E2 7
VEE 8
GND 9
18 VCC
17 Y2
16 Y1
15 Y0
14 Y3
13 S0
12 S1
11 S2
10 L̄Ē
4351
CD01930S

LOGIC SYMBOL

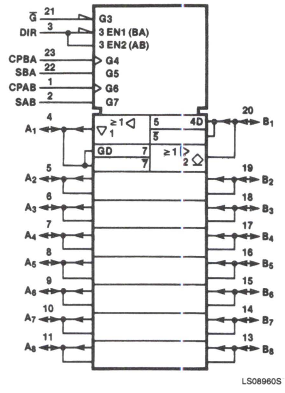
'F646


4 5 6 7 8 9 10 11
A1 A2 A3 A4 A5 A6 A7 A8
1 CPAB
2 SAB
3 DIR
23 CPBA
22 SBA
21 G
B1 B2 B3 B4 B5 B6 B7 B8
20 19 18 17 16 15 14 13
LS08943S

V_{CC} = Pin 24
GND = Pin 12

LOGIC SYMBOL (IEEE/IEC)

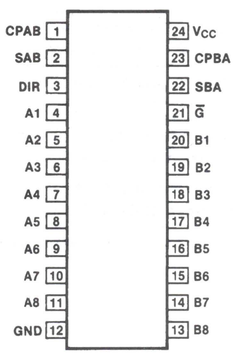
'F646


Ḡ 21
DIR 3
G3
3 EN1 (BA)
3 EN2 (AB)
CPBA 23
SBA 22
CPAB 1
SAB 2
G4
G5
G6
G7
≥1
1
5
4D
5̄
GD
7
7̄
≥1
2
A1 4
A2 5
A3 6
A4 7
A5 8
A6 9
A7 10
A8 11
20 B1
19 B2
18 B3
17 B4
16 B5
15 B6
14 B7
13 B8
LS08960S

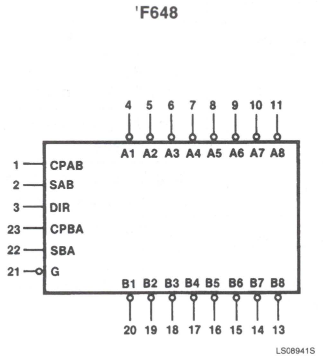
Transceivers/Registers

FAST 74F646, 74F648

PIN CONFIGURATION

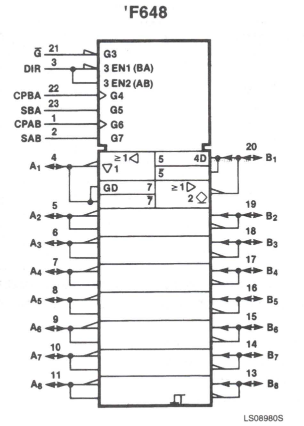

'F648
CPAB 1
SAB 2
DIR 3
A1 4
A2 5
A3 6
A4 7
A5 8
A6 9
A7 10
A8 11
GND 12
24 V_{CC}
23 CPBA
22 SBA
21 $\overline{G}$
20 B1
19 B2
18 B3
17 B4
16 B5
15 B6
14 B7
13 B8
CD07330S

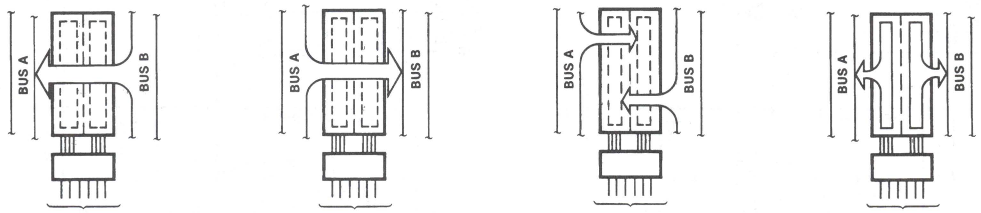
LOGIC SYMBOL


'F648
4 5 6 7 8 9 10 11
A1 A2 A3 A4 A5 A6 A7 A8
1 CPAB
2 SAB
3 DIR
23 CPBA
22 SBA
21 G
B1 B2 B3 B4 B5 B6 B7 B8
20 19 18 17 16 15 14 13
LS08941S

V_{CC} = Pin 24
GND = Pin 12

LOGIC SYMBOL (IEEE/IEC)


'F648
$\overline{G}$ 21
DIR 3
CPBA 22
SBA 23
CPAB 1
SAB 2
G3
3 EN1 (BA)
3 EN2 (AB)
G4
G5
G6
G7
≥1
▽1
5
4D
5
GD
7
7
≥1
2
A_1 4
A_2 5
A_3 6
A_4 7
A_5 8
A_6 9
A_7 10
A_8 11
20 B_1
19 B_2
18 B_3
17 B_4
16 B_5
15 B_6
14 B_7
13 B_8
LS08980S


BUS A
BUS B
BUS A
BUS B
BUS A
BUS B
BUS A
BUS B

REAL-TIME TRANSFER BUS B TO BUS A

(3) $\overline{\text{OE}}$	(21) DIR	(1) CPAB	(23) CPBA	(2) SAB	(22) SBA
L	L	X	X	X	L

REAL-TIME TRANSFER BUS A TO BUS B

(3) $\overline{\text{OE}}$	(21) DIR	(1) CPAB	(23) CPBA	(2) SAB	(22) SBA
L	H	X	X	L	X

STORAGE FROM A, B or A and B

(3) $\overline{\text{OE}}$	(21) DIR	(1) CPAB	(23) CPBA	(2) SAB	(22) SBA
X	H	↑	X	X	X
X	X	X	↑	X	X
H	X	↑	↑	X	X

TRANSFER STORAGE DATA TO A OR B

(3) $\overline{\text{OE}}$	(21) DIR	(1) CPAB	(23) CPBA	(2) SAB	(22) SBA
L	L	X	H or L	X	H
L	H	H or L	X	H	X

Figure 1

The Select (S) controls can multiplex stored and real-time (transparent mode) data. The DIR determines which bus will receive data when the Enable $\overline{G}$ is active (Low). In the isolation mode (Enable G, High), A data may be stored in the B register and/or B data may be stored in the A register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time. Figure 1 demonstrates the four fundamental bus-management functions that can be performed with the 'F646 and 'F648.

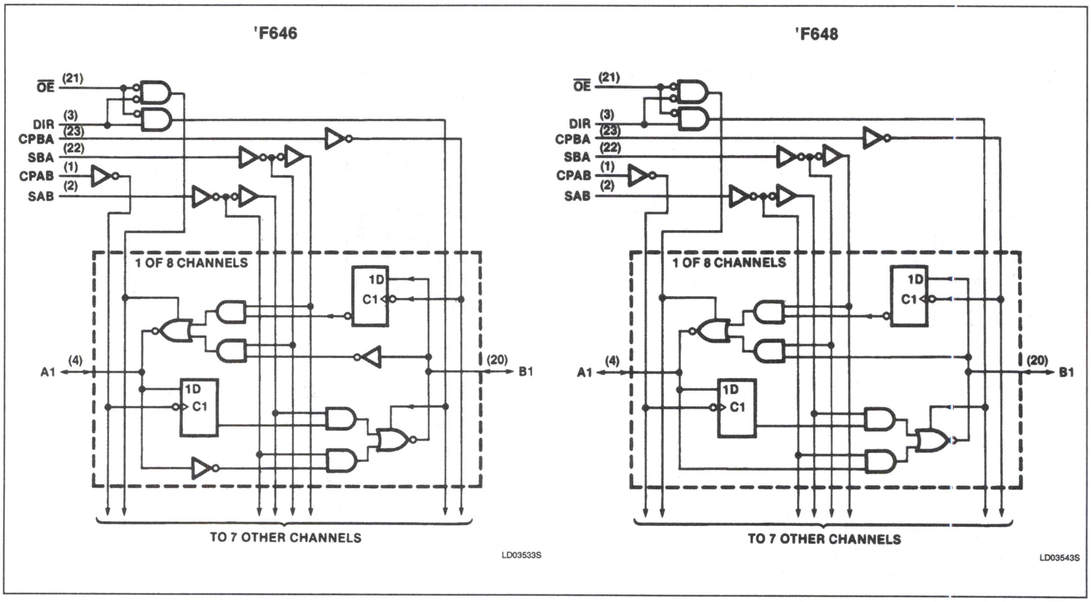
FUNCTION TABLE

INPUTS						DATA I/O*		OPERATING MODE	
$\overline{OE}$	DIR	CPAB	CPBA	SAB	SBA	$A_0 - A_7$	$B_0 - B_7$	'F646	'F648
X	X	↑	X	X	X	Input	un*	Store A, B unspecified*	Store A, B unspecified*
X	X	X	↑	X	X	un*	Input	Store B, A unspecified*	Store B, A unspecified*
H	X	↑	↑	X	X	Input	Input	Store A and B Data Isolation, hold storage	Store A and B Data Isolation, hold storage
H	X	H or L	H or L	X	X				
L	L	X	X	X	L	Output	Input	Real Time B Data to A Bus	Real time $\overline{B}$ Data to A bus
L	L	X	H or L	X	H			Stored B Data to A Bus	Stored $\overline{B}$ data to A bus
L	H	X	X	L	X	Input	Output	Real Time A Data to B Bus	Real Time $\overline{A}$ Data to B Bus
L	H	H or L	X	H	X			Stored A Data to B Bus	Stored $\overline{A}$ Data to B Bus

*The data output functions may be enabled or disabled by various signals at the $\overline{OE}$ and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every Low-to-High transition of the clock.

un = unspecified
H = High voltage level
L = Low voltage level
X = Don't Care
↑ = Low-to-High clock transition

LOGIC DIAGRAM


'F646
$\overline{OE}$ (21)
DIR (3)
CPBA (23)
SBA (22)
CPAB (1)
SAB (2)
1 OF 8 CHANNELS
1D
C1
1D
C1
A1 (4)
(20) B1
TO 7 OTHER CHANNELS
LD03533S
'F648
$\overline{OE}$ (21)
DIR (3)
CPBA (23)
SBA (22)
CPAB (1)
SAB (2)
1 OF 8 CHANNELS
1D
C1
1D
C1
A1 (4)
(20) B1
TO 7 OTHER CHANNELS
LD03543S

Transceivers/Registers

FAST 74F646, 74F648

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	74F646	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	128	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage Temperature range	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		74F646			UNIT
			Min	Typ	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	High-level output current	V_{OH} = 2.4V or 2.7V			−3	mA
		V_{OH} = 2.0V			−15	
I_{OL}	Low-level output current				64	mA
T_A	Operating free-air temperature		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			74F646, 74F648			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = −3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.3		V
				I_{OH} = −15mA	±10%V_{CC}	2.0			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OL} = MAX V_{IH} = MIN,		±10%V_{CC}		4.0	0.55	V
					±5%V_{CC}		4.0	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				−0.73	−1.2	V
I_I	Input current at maximum input voltage	Others	V_{CC} = 0.0V, V_I = 7.0V					100	μA
		A_0–A_7, B_0–B_7	V_{CC} = 5.5V, V_I = 5.5V					1.0	μA
I_{IH}	High-level input current	CPAB, CPBA SAB, SBA $\overline{OE}$, DIR	V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					−20	μA
I_{OZH} + I_{IH}	High-level input current	A_0–A_7 B_0–B_7	V_{CC} = MAX, V_O = 2.7V					70	μA
I_{OZL} + I_{IL}	Low-level input current		V_{CC} = MAX, V_O = 0.5V					−70	μA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX			−100		−225	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				125	165	mA
		I_{CCL}					160	210	mA
		I_{CCZ}					135	180	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of High-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F646					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	100	115		90		MHz
t_{PLH} t_{PHL}	Propagation delay CPAB or CPBA to A_n to B_n	Waveform 1	5.5 5.5	7.5 8.0	10.0 10.0	5.0 5.0	11.5 11.0	ns
t_{PLH} t_{PHL}	Propagation delay A_n or B_n to B_n or A_n	Waveform 2, 3	4.0 4.0	6.0 6.5	9.0 9.0	4.0 4.0	10.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay SBA or SAB to A_n or B_n	Waveform 2, 3	5.0 5.0	7.0 6.5	8.5 8.5	4.5 4.5	10.5 9.5	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}$ to A_n or B_n	Waveform 5 Waveform 6	5.0 6.5	7.0 8.5	10.0 11.0	4.5 6.0	11.0 12.5	ns
t_{PZH} t_{PZL}	Output Enable Time DIR to A_n or B_n	Waveform 5 Waveform 6	4.0 6.0	6.5 8.5	9.0 11.0	4.0 5.5	10.0 12.5	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}$ to A_n or B_n	Waveform 5 Waveform 6	6.5 6.5	9.0 9.0	11.5 11.5	6.0 6.0	12.5 13.5	ns
t_{PHZ} t_{PLZ}	Output Disable time DIR to A_n or B_n	Waveform 5 Waveform 6	5.5 5.5	8.5 8.5	11.0 11.0	4.5 5.0	13.0 12.5	ns

AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	74F646					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_S(H)$ $t_S(L)$	Setup time, High or Low A_n or B_n to CPAB or CPBA	Waveform 4	4.5 4.5			5.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low A_n or B_n to CPAB or CPBA	Waveform 4	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	Pulse width, High or Low CPAB or CPBA	Waveform 1	4.0 6.0			4.0 6.0		ns

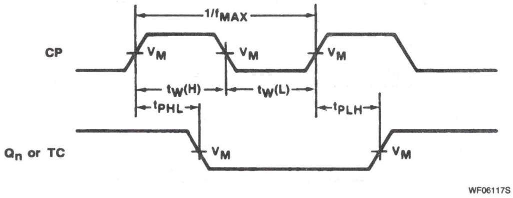
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F648					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	100	115		90		MHz
t_{PLH} t_{PHL}	Propagation delay CPAB or CPBA to A_n to B_n	Waveform 1	5.0 5.0	7.0 7.5	9.5 9.5	4.5 4.5	11.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay A_n or B_n to B_n or A_n	Waveform 2, 3	3.0 4.0	6.0 6.0	8.5 8.5	2.5 3.5	9.5 9.5	ns
t_{PLH} t_{PHL}	Propagation delay SBA or SAB to A_n or B_n	Waveform 2, 3	4.5 4.5	7.0 6.5	8.5 8.5	4.5 4.5	10.5 9.5	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}$ to A_n or B_n	Waveform 5 Waveform 6	4.5 6.0	7.0 8.5	10.0 11.0	4.0 5.5	11.0 12.5	ns
t_{PZH} t_{PZL}	Output Enable Time DIR to A_n or B_n	Waveform 5 Waveform 6	4.5 6.0	7.0 8.5	10.0 11.0	4.0 5.5	11.0 12.5	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}$ to A_n or B_n	Waveform 5 Waveform 6	6.0 6.0	9.0 8.5	11.5 12.0	6.0 6.0	12.5 13.5	ns
t_{PHZ} t_{PLZ}	Output Disable time DIR to A_n or B_n	Waveform 5 Waveform 6	5.0 6.0	9.0 9.0	12.5 12.5	4.5 5.0	14.0 14.0	ns

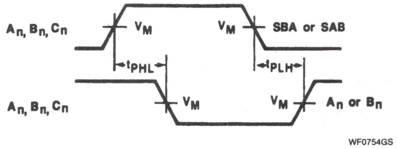
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	74F648					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low A_n or B_n to CPAB or CPBA	Waveform 4	4.0 4.0			5.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low A_n or B_n to CPAB or CPBA	Waveform 4	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	Pulse width, High or Low CPAB or CPBA	Waveform 1	3.5 6.5			4.0 7.0		ns

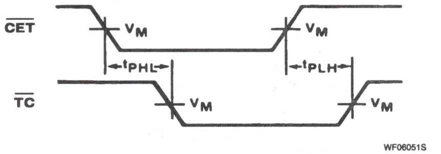
AC WAVEFORMS


1/fMAX
CP
VM
VM
VM
tW(H)
tW(L)
tPHL
tPLH
Qn or TC
VM
VM
WF06117S

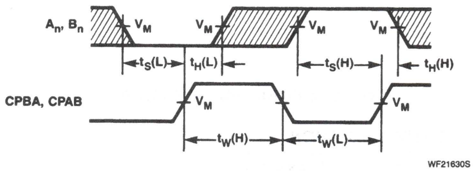
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width and Maximum Clock Frequency


An, Bn, Cn
VM
VM
SBA or SAB
tPHL
tPLH
An, Bn, Cn
VM
VM
An or Bn
WF0754GS

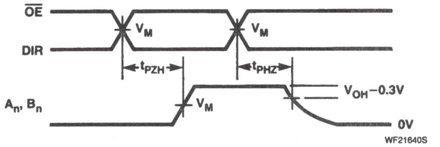
Waveform 2. Propagation Delay, A_n or B_n to B_n or A_n and SBA or SAB to A_n or B_n


CET
VM
VM
tPHL
tPLH
TC
VM
VM
WF06051S

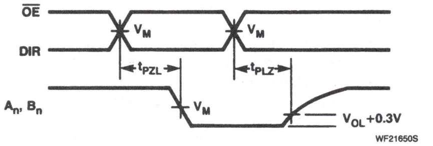
Waveform 3. Propagation Delay, A_n or B_n to B_n or A_n and SBA or SAB to A_n or B_n (Y_n) (B Register Stored Data = L, $\overline{CP}$ = H)


An, Bn
VM
VM
VM
VM
tS(L)
tH(L)
tS(H)
tH(H)
CPBA, CPAB
VM
VM
tW(H)
tW(L)
WF21630S

Waveform 4. Data Setup and Hold Times


OE
DIR
VM
VM
tPZH
tPHZ
An, Bn
VM
VOH−0.3V
0V
WF21640S

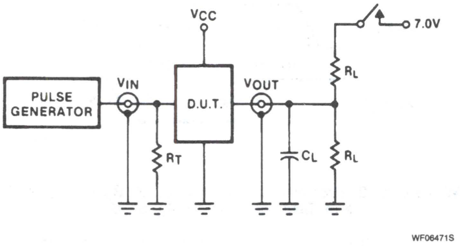
Waveform 5. 3-State Output Enable Time to High Level and Output Disable Time From High Level


OE
DIR
VM
VM
tPZL
tPLZ
An, Bn
VM
VOL+0.3V
WF21650S

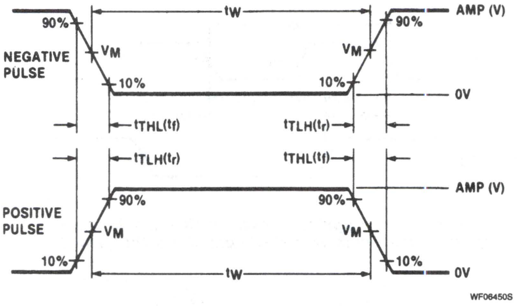
Waveform 6. 3-State Output Enable Time to Low Level and Output Disable Time From Low Level

NOTE: V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS


VCC
7.0V
RL
PULSE GENERATOR
VIN
D.U.T.
VOUT
RT
CL
RL
WF06471S

Test Circuit for 3-State Outputs


NEGATIVE PULSE
90%
VM
10%
tW
AMP (V)
0V
tTHL(tf)
tTLH(tr)
POSITIVE PULSE
tTLH(tr)
tTHL(tf)
90%
VM
10%
tW
AMP (V)
0V
WF06450S

$V_M = 1.5V$

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F647, 74F649

Transceivers/Registers

'F647 — Octal Transceiver/Register, Non-Inverting (Open-Collector)
'F649 — Octal Transceiver/Register, Inverting (Open-Collector)
Product Specification

FAST Products

FEATURES

- High-impedance NPN base inputs for reduced loading (20μA in High and Low states)
- Independent registers for A and B buses
- Multiplexed real-time and stored data
- Choice of non-inverting and inverting data paths
- Open-Collector outputs
- Available in 300mil-wide 24-pin Slim DIP package

DESCRIPTION

These devices consist of bus transceiver circuits with Open-Collector outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to High logic level. Enable $\overline{OE}$ and DIR pins are provided to control the transceiver function. In the transceiver mode, data present at the High-impedance port may be stored in either the A or B register or both.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F647	65MHz	125mA
74F649	65MHz	125mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ± 10%; T_A = 0°C to +70°C
24-Pin Plastic Slim DIP (300mil)	N74F647N, N74F649N
24-Pin Plastic SOL[1]	N74F647D, N74F649D

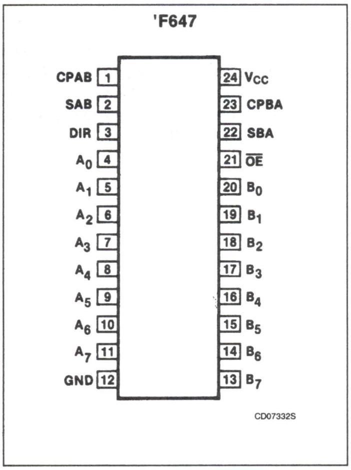
NOTE:
1. Thermal mounting techniques are recommended. See App Note AN SMD-100 for a discussion of thermal considerations for surface mounted devices.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

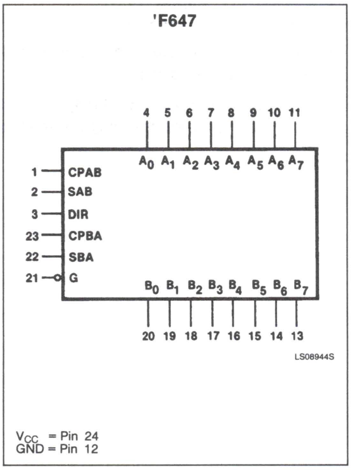
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$A_0 - A_7$	A inputs	1.0/0.033	20μA/20μA
$B_0 - B_7$	B inputs	1.0/0.033	20μA/20μA
CPAB	A-to-B Clock input	1.0/0.033	20μA/20μA
CPBA	B-to-A Clock input	1.0/0.033	20μA/20μA
SAB	A-to-B Select input	1.0/0.033	20μA/20μA
SBA	B-to-A Select input	1.0/0.033	20μA/20μA
DIR	Data flow directional control enable input	1.0/0.033	20μA/20μA
$\overline{OE}$	Output Enable input	1.0/0.033	20μA/20μA
$A_0 - A_7$	A outputs	*OC/106.7	OC/64mA
$B_0 - B_7$	B outputs	*OC/106.7	OC/64mA

NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.
2. *OC = Open-Collector

PIN CONFIGURATION

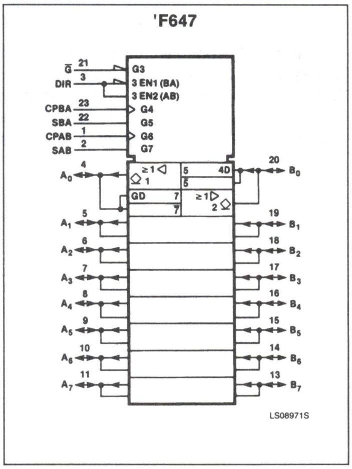

'F647
CPAB 1
SAB 2
DIR 3
A0 4
A1 5
A2 6
A3 7
A4 8
A5 9
A6 10
A7 11
GND 12
24 Vcc
23 CPBA
22 SBA
21 OE
20 B0
19 B1
18 B2
17 B3
16 B4
15 B5
14 B6
13 B7
CD07332S

LOGIC SYMBOL

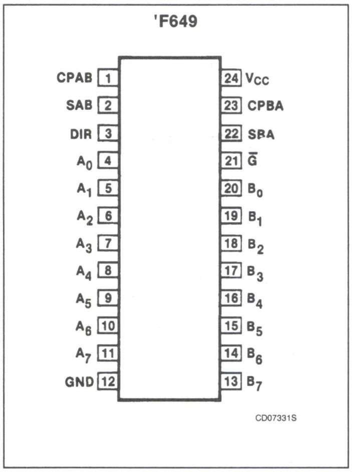

'F647
4 5 6 7 8 9 10 11
A0 A1 A2 A3 A4 A5 A6 A7
1 CPAB
2 SAB
3 DIR
23 CPBA
22 SBA
21 G
B0 B1 B2 B3 B4 B5 B6 B7
20 19 18 17 16 15 14 13
LS08944S

V_{CC} = Pin 24
GND = Pin 12

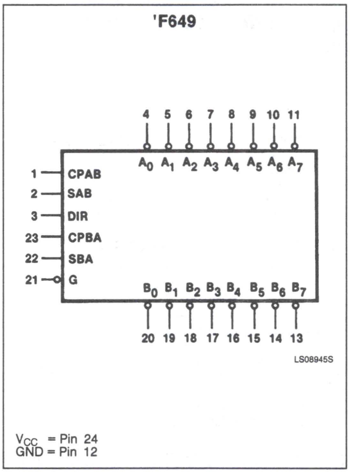
LOGIC SYMBOL (IEEE/IEC)


'F647
G 21 G3
DIR 3 3 EN1 (BA)
3 EN2 (AB)
CPBA 23 G4
SBA 22 G5
CPAB 1 G6
SAB 2 G7
≥1
1
5
4D
5
GD
7
7
≥1
2
A0 4
A1 5
A2 6
A3 7
A4 8
A5 9
A6 10
A7 11
20 B0
19 B1
18 B2
17 B3
16 B4
15 B5
14 B6
13 B7
LS08971S

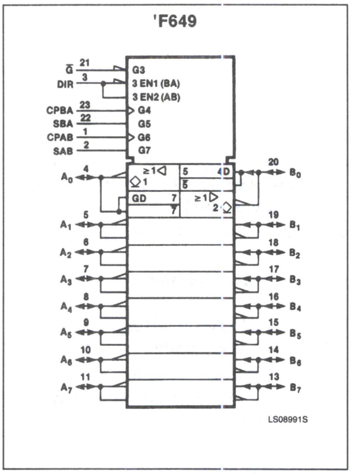
PIN CONFIGURATION

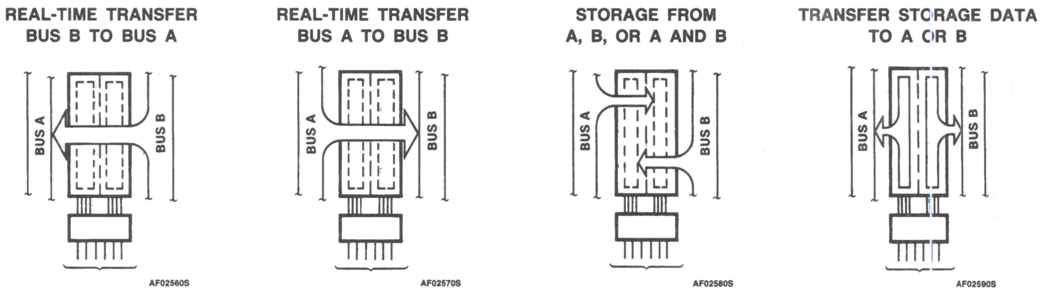

'F649
CPAB 1
SAB 2
DIR 3
A0 4
A1 5
A2 6
A3 7
A4 8
A5 9
A6 10
A7 11
GND 12
24 VCC
23 CPBA
22 SBA
21 G̅
20 B0
19 B1
18 B2
17 B3
16 B4
15 B5
14 B6
13 B7
CD07331S

LOGIC SYMBOL


'F649
4 5 6 7 8 9 10 11
A0 A1 A2 A3 A4 A5 A6 A7
1 CPAB
2 SAB
3 DIR
23 CPBA
22 SBA
21 G
B0 B1 B2 B3 B4 B5 B6 B7
20 19 18 17 16 15 14 13
LS08945S
VCC = Pin 24
GND = Pin 12

LOGIC SYMBOL (IEEE/IEC)


'F649
G̅ 21
DIR 3
G3
3 EN1 (BA)
3 EN2 (AB)
CPBA 23
SBA 22
CPAB 1
SAB 2
G4
G5
G6
G7
A0 4
≥1
1
5
4D
GD
7
≥1
2
20 B0
A1 5
A2 6
A3 7
A4 8
A5 9
A6 10
A7 11
19 B1
18 B2
17 B3
16 B4
15 B5
14 B6
13 B7
LS08991S


BUS A
BUS B
BUS A
BUS B
BUS A
BUS B
BUS A
BUS B
AF02560S
AF02570S
AF02580S
AF02590S

REAL-TIME TRANSFER BUS B TO BUS A

(3) $\overline{OE}$	(21) DIR	(1) CPAB	(23) CPBA	(2) SAB	(22) SBA
L	L	X	X	X	L

REAL-TIME TRANSFER BUS A TO BUS B

(3) $\overline{OE}$	(21) DIR	(1) CPAB	(23) CPBA	(2) SAB	(22) SBA
L	H	X	X	L	X

STORAGE FROM A, B, OR A AND B

(3) $\overline{OE}$	(21) DIR	(1) CPAB	(23) CPBA	(2) SAB	(22) SBA
X	X	↑	X	X	X
X	X	X	↑	X	X
H	X	↑	↑	X	X

TRANSFER STORAGE DATA TO A OR B

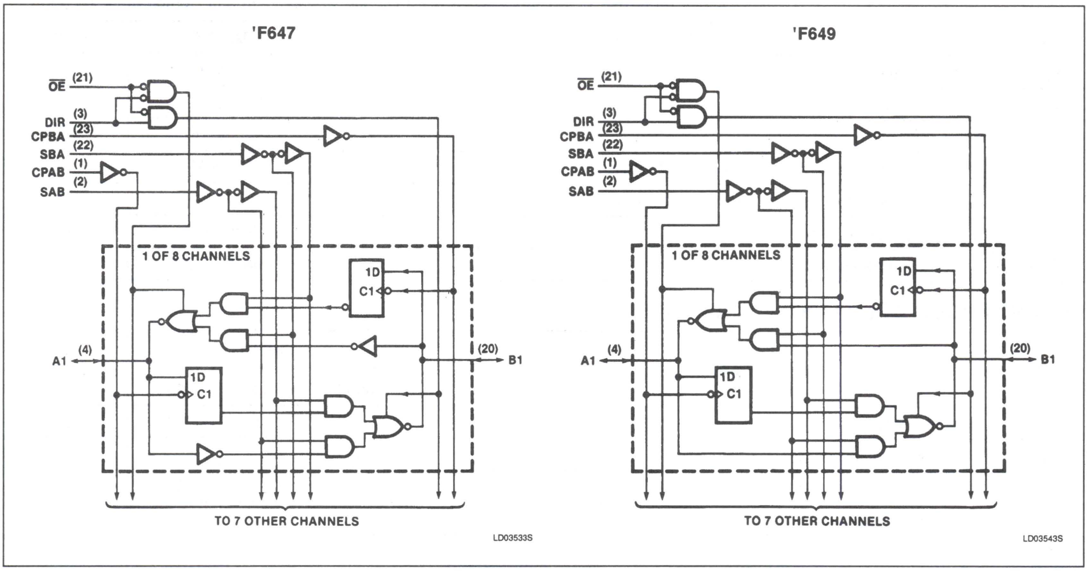
(3) $\overline{OE}$	(21) DIR	(1) CPAB	(23) CPBA	(2) SAB	(22) SBA
L	L	X	H or L	X	H
L	H	H or L	X	H	X

Figure 1

The Select (S) controls can multiplex stored and real-time (transparent mode) data. The DIR determines which bus will receive data when the Enable $\overline{OE}$ is active-Low. In the isolation mode (Enable $\overline{G}$, High), A data may be stored in the B register and/or B data may be stored in the A register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time. Figure 1 demonstrates the four fundamental bus-management functions that can be performed with the 'F647, and 'F649.

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS						DATA I/O		OPERATING MODE	
$\overline{OE}$	DIR	CPAB	CPBA	SAB	SBA	$A_0 - A_7$	$B_0 - B_7$	'F647	'F649
X	X	↑	X	X	X	Input	un*	Store A, B unspecified*	Store A, B unspecified*
X	X	X	↑	X	X	un*	Input	Store B, A unspecified*	Store B, A unspecified*
H	X	↑	↑	X	X	Input	Input	Store A and B Data	Store A and B Data
H	X	Hor L	Hor L	X	X			Isolation, hold storage	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real Time B Data to A Bus	Real Time $\overline{B}$ Data to A Bus
L	L	X	Hor L	X	H			Stored B Data to A Bus	Stored $\overline{B}$ Data to A Bus
L	H	Hor L	X	L	X	Input	Output	Real Time A Data to B Bus	Real Time $\overline{A}$ Data to B Bus
L	H	X	X	H	X			Stored A Data to B Bus	Stored $\overline{A}$ Data to B Bus

*The data output function may be enabled or disabled by various signals at the $\overline{OE}$ and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every Low-to-High transition of the clock.

un = unspecified
H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	128	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
V_{OH}	High-level output voltage			4.5	V
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		74F647, 'F649			UNIT
					Min	Typ[2]	Max	
I_{OH}	High-level output current		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, V_{OH} = MAX				250	µA
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = 0.0V, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				−20	µA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			105	145	mA
		I_{CCL}				145	200	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.

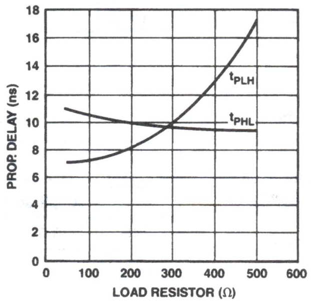
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F647, 'F649					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	50	65		40		MHz
t_{PLH} t_{PHL}	Propagation delay CPBA or CPAB to A_n or B_n	Waveform 1	10.0 5.5	15.0 8.5	18.0 11.0	10.0 5.5	19.5 12.0	ns
t_{PLH} t_{PHL}	Propagation delay A_n or B_n to B_n or A_n	Waveform 2, 3	10.5 4.0	13.5 7.0	16.5 9.5	10.5 4.0	19.0 10.5	ns
t_{PLH} t_{PHL}	Propagation delay SBA or SAB to A_n or B_n	Waveform 2, 3	10.5 4.0	14.5 7.0	17.5 9.5	10.5 4.0	20.0 10.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{OE}$ to A_n or B_n	Waveform 2, 3	13.0 6.5	17.0 10.0	20.0 12.5	13.0 6.5	22.5 13.5	ns
t_{PLH} t_{PHL}	Propagation delay DIR to A_n or B_n	Waveform 2, 3	13.0 7.0	17.0 15.0	20.0 18.0	13.0 7.0	22.5 20.0	ns

AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	74F647, 'F649					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low A_n or B_n to CPBA or CPAB	Waveform 4	4.0 4.0			5.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low A_n or B_n to CPBA or CPAB	Waveform 4	0 0			0 0		ns
t_w	Pulse width, High or Low CPAB or CPBA	Waveform 1	4.5 6.0			4.5 6.5		ns

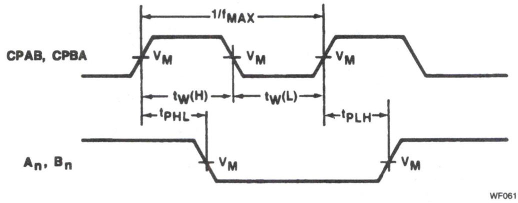
TYPICAL PROPAGATION DELAYS VERSUS LOAD RESISTOR FOR OPEN-COLLECTOR OUTPUTS



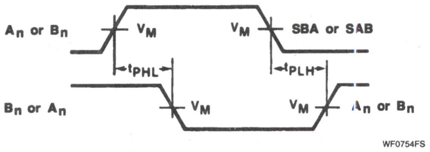
OP19810S

NOTES:
When using Open-Collector parts, the value of the pull-up resistor greatly affects the value of the t_{PLH}. For example, changing the specified pull-up resistor value from 500Ω to 100Ω will improve the t_{PLH} up to 50% with only a slight increase in the t_{PHL}. However, if the value of the pull-up resistor is changed, the user must make certain that the total I_{OL} current through the resistor and the total I_{IL}'s of the receivers does not exceed the I_{OL} maximum specification.

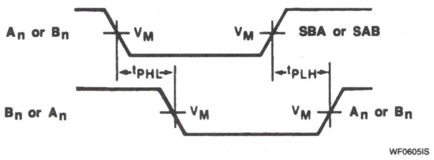
AC WAVEFORMS


1/fMAX
CPAB, CPBA
VM
VM
VM
tW(H)
tW(L)
tPHL
tPLH
An, Bn
VM
VM
WF06110S

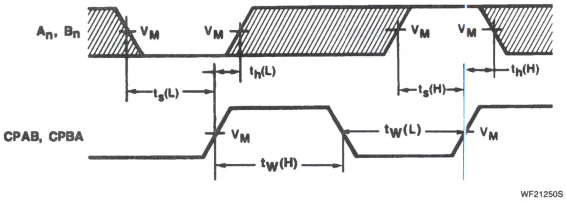
Waveform 1. Clock to Bus Delays, Clock Pulse Width


An or Bn
VM
VM
SBA or SAB
tPHL
tPLH
Bn or An
VM
VM
An or Bn
WF0754FS

Waveform 2. Propagation Delay, A_n or B_n to B_n or A_n and SBA or SAB to A_n or B_n


An or Bn
VM
VM
SBA or SAB
tPHL
tPLH
Bn or An
VM
VM
An or Bn
WF0605IS

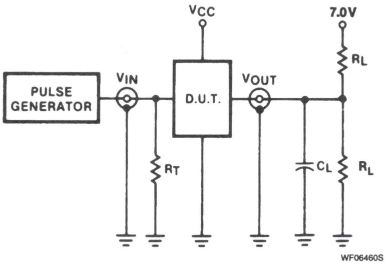
Waveform 3. Propagation Delay, A_n or B_n to B_n or A_n and SBA or SAB to A_n or B_n


An, Bn
VM
VM
VM
VM
th(L)
th(H)
ts(L)
ts(H)
CPAB, CPBA
VM
tW(L)
VM
tW(H)
WF21250S

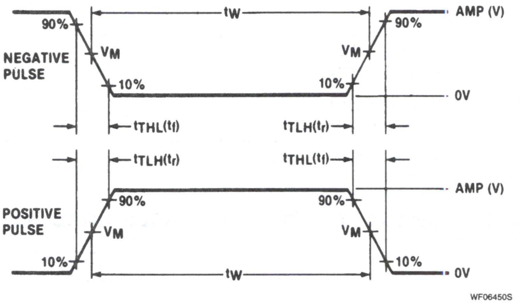
Waveform 4. Data and Select Setup and Hold Times

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS


VCC
7.0V
RL
PULSE GENERATOR
VIN
D.U.T.
VOUT
RT
CL
RL
WF06460S

Test Circuit for Open-Collector Outputs


NEGATIVE PULSE
90%
VM
10%
tW
90%
VM
10%
AMP (V)
0V
tTHL(tf)
tTLH(tr)
tTLH(tr)
tTHL(tf)
POSITIVE PULSE
90%
VM
10%
90%
VM
10%
tW
AMP (V)
0V
WF06450S

$V_M = 1.5V$
Input Pulse Definition

DEFINITIONS
R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

FAST 74F651, 74F652
Transceivers/Registers

'F651 Octal Transceiver/Register, Inverting (3-State)
'F652 Octal Transceiver/Register, Non-Inverting (3-State)
Product Specification

FAST Products

FEATURES

- **High-impedance NPN base inputs for reduced loading (70μA in High and Low states)**
- **Independent registers for A and B buses**
- **Multiplexed real-time and stored data**
- **Choice of non-inverting and inverting data paths**
- **3-State outputs**

DESCRIPTION

These devices consist of bus transceiver circuits with 3-State outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes High. Output Enable (OEAB, $\overline{OEBA}$) and Select (SAB, SBA) pins are provided for bus management.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F651	115MHz	140mA
74F652	115MHz	140mA

ORDERING INFORMATION

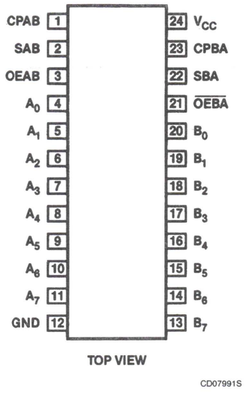
PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
Cerdip (300mil)	N74F651F, N74F652F

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

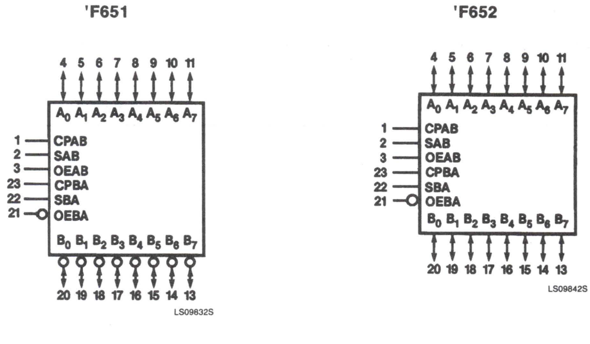
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$A_0 - A_7$	A inputs	3.5/0.116	70μA/70μA
$B_0 - B_7$	B inputs	3.5/0.116	70μA/70μA
CPAB	A-to-B clock input	1.0/0.033	20μA/20μA
CPBA	B-to-A clock input	1.0/0.033	20μA/20μA
SAB	A-to-B select input	1.0/0.033	20μA/20μA
SBA	B-to-A select input	1.0/0.033	20μA/20μA
OEAB	Output Enable input	1.0/0.033	20μA/20μA
$\overline{OEBA}$	Output Enable input	1.0/0.033	20μA/20μA
$A_0 - A_7$	A outputs	750/106.7	15mA/64mA
$B_0 - B_7$	B outputs	750/106.7	15mA/64mA

NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION


CPAB 1
SAB 2
OEAB 3
A_0 4
A_1 5
A_2 6
A_3 7
A_4 8
A_5 9
A_6 10
A_7 11
GND 12
24 V_{CC}
23 CPBA
22 SBA
21 $\overline{OEBA}$
20 B_0
19 B_1
18 B_2
17 B_3
16 B_4
15 B_5
14 B_6
13 B_7
TOP VIEW
CD07991S

LOGIC SYMBOL


'F651
4 5 6 7 8 9 10 11
A_0 A_1 A_2 A_3 A_4 A_5 A_6 A_7
1 CPAB
2 SAB
3 OEAB
23 CPBA
22 SBA
21 OEBA
B_0 B_1 B_2 B_3 B_4 B_5 B_6 B_7
20 19 18 17 16 15 14 13
LS09832S
'F652
4 5 6 7 8 9 10 11
A_0 A_1 A_2 A_3 A_4 A_5 A_6 A_7
1 CPAB
2 SAB
3 OEAB
23 CPBA
22 SBA
21 OEBA
B_0 B_1 B_2 B_3 B_4 B_5 B_6 B_7
20 19 18 17 16 15 14 13
LS09842S

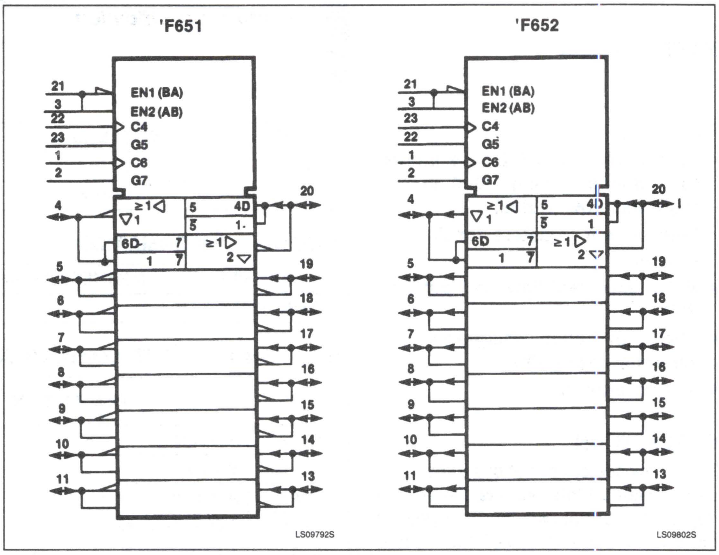
V_{CC} = Pin 24
GND = Pin 12

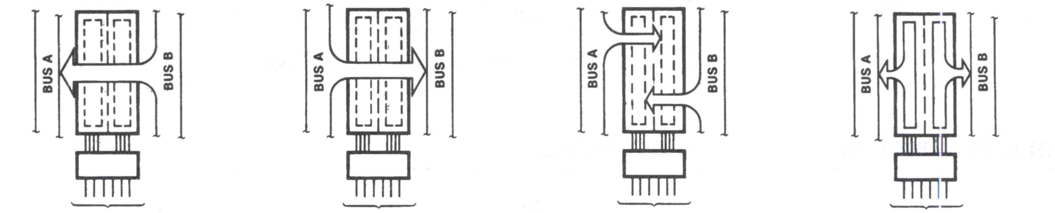
The following examples demonstrate the four fundamental bus-management functions that can be performed with the 'F651 and 'F652.

The select pins determine whether data is stored or transferred through the device in real-time.

The Output Enable pins determine the direction of the data flow.

SYMBOL (IEEE/IEC)


'F651
'F652
EN1 (BA)
EN2 (AB)
C4
G5
C6
G7
≥1
1
5
4D
6D
7
≥1
2
21
3
22
23
1
2
4
20
5
19
6
18
7
17
8
16
9
15
10
14
11
13
LS09792S
LS09802S



REAL-TIME TRANSFER BUS B TO BUS A

OEAB	$\overline{\text{OEBA}}$	CPAB	CPBA	SAB	SBA
L	L	X	X	X	L

REAL-TIME TRANSFER BUS A TO BUS B

OEAB	$\overline{\text{OEBA}}$	CPAB	CPBA	SAB	SBA
H	H	X	X	L	X

STORAGE FROM A, B, OR A AND B

OEAB	$\overline{\text{OEBA}}$	CPAB	CPBA	SAB	SBA
X	H	↑	X	X	X
L	X	X	↑	X	X
L	H	↑	↑	X	X

TRANSFER STORAGE DATA TO A OR B

OEAB	$\overline{\text{OEBA}}$	CPAB	CPBA	SAB	SBA
H	L	H or L	H or L	H	H

Figure 1

FUNCTION TABLE

OPERATING MODE		INPUTS						DATA I/O	
'F651	'F652	$\overline{\text{OEBA}}$	OEAB	CPAB	CPBA	SAB	SBA	A_n	B_n
Isolation Store A and B data	Isolation Store A and B data	L L	H H	H or L ↑	H or L ↑	X X	X X	Input	Input
Store A, Hold B Store A in both registers	Store A, Hold B Store A in both registers	X H	H H	↑ ↑	H or L ↑	X L	X X	Input Input	un* Output
Hold A, Store B Store B in both registers	Hold A, Store B Store B in both registers	L L	X L	H or L ↑	↑ ↑	X X	X L	un* Output	Input Input
Real time $\overline{B}$ data to A bus Stored $\overline{B}$ data to A bus	Real time B data to A bus Stored B data to A bus	L L	L L	X X	X H or L	X X	L H	Output	Input
Real time $\overline{A}$ data to B bus Stored $\overline{A}$ data to B bus	Real time A data to B bus Stored A data to B bus	H H	H H	X H or L	X X	L H	X X	Input	Output
Stored $\overline{A}$ data to B bus Stored $\overline{B}$ data to A bus	Stored A data to B bus Stored B data to A bus	H	L	H or L	H or L	H	H	Output	Output

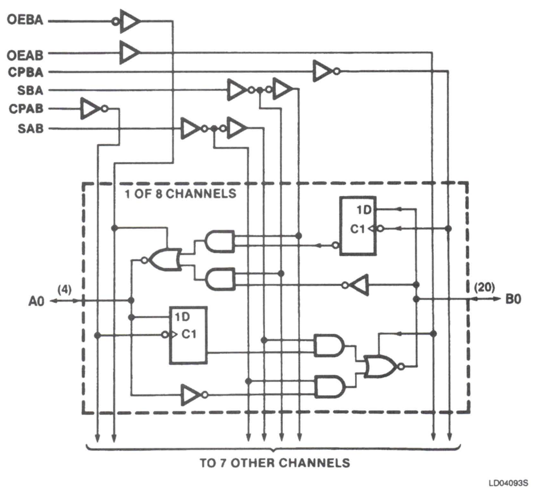
NOTES:

* The data output function may be enabled or disabled by various signals at OEBA and OEAB inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every Low-to-High transition of the clock.

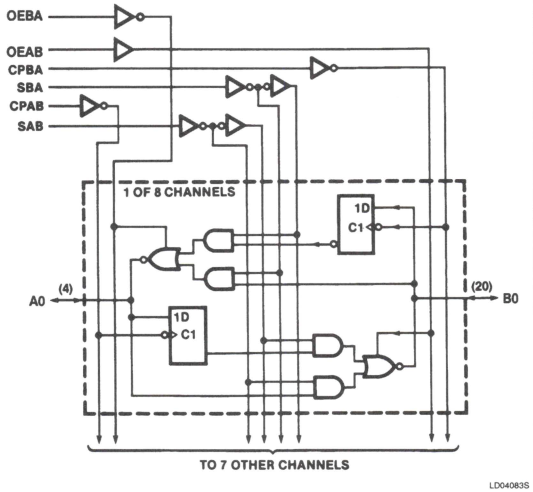
H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-to-High clock transition

LOGIC DIAGRAM

'F651


OEBA
OEAB
CPBA
SBA
CPAB
SAB
1 OF 8 CHANNELS
1D
C1
A0
(4)
(20)
B0
1D
C1
TO 7 OTHER CHANNELS
LD04093S

'F652


OEBA
OEAB
CPBA
SBA
CPAB
SAB
1 OF 8 CHANNELS
1D
C1
A0
(4)
(20)
B0
1D
C1
TO 7 OTHER CHANNELS
LD04083S

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	128	V
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	High-level output current	V_{OH} = 2.4V or 2.7V			−3	mA
		V_{OH} = 2.0V			−15	mA
I_{OL}	Low-level output current				64	mA
T_A	Operating free-air temperature		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			74F651, 74F652			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN V_{IL} = MAX V_{IH} = MIN	I_{OH} = −3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.3		V
				I_{OH} = −15mA	±10%V_{CC}	2.0			V
V_{OL}	Low-level output voltage		V_{CC} = MIN V_{IL} = MAX V_{IH} = MIN	I_{OL} = 48mA	±10%V_{CC}		0.35	0.50	V
				I_{OL} = 64mA	±5%V_{CC}		0.40	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$				−0.73	−1.2	V
I_I	Input current at maximum input voltage	Others	V_{CC} = 0.0V, V_I = 7.0V					100	µA
		$A_0 - A_7$, $B_0 - B_7$	V_{CC} = 5.5V, V_I = 5.5V					1.0	mA
I_{IH}	High-level input current	CPAB, CPBA SAB, SBA OEAB, $\overline{\text{OEBA}}$	V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					−20	µA
$I_{IH} + I_{OZH}$	High-level input current	$A_0 - A_7$ $B_0 - B_7$	V_{CC} = MAX, V_O = 2.7V					70	µA
$I_{IL} + I_{OZL}$	Low-level input current		V_{CC} = MAX, V_O = 0.5V					−70	µA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX			−100		−225	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				110 140[4]	155 185[4]	mA
		I_{CCL}					155 165[4]	200 240[4]	mA
		I_{CCZ}					130	175	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of High-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. These values are for worst case only. Worst case is defined as all (16) I/O pins selected as outputs. Thermal mounting is required when using worst case conditions.

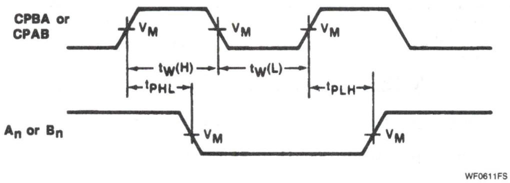
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F651, 74F652					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	90	110		80		MHz
t_{PLH} t_{PHL}	Propagation delay CPAB or CPBA to A_n or B_n	Waveform 1	5.0 5.5	7.0 7.5	10.5 11.0	4.5 5.0	12.5 12.0	ns
t_{PLH} t_{PHL}	Propagation delay A_n or B_n to B_n or A_n	Waveform 2, 3	3.0 3.0	6.0 6.0	10.0 9.0	2.5 3.0	12.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay SBA or SAB to A_n or B_n	Waveform 2, 3	4.0 4.0	7.0 6.5	10.0 9.5	4.0 4.0	12.5 10.0	ns
t_{PZH} t_{PZL}	Output Enable time OEAB or $\overline{OEBA}$ to A_n or B_n	Waveform 6 Waveform 7	4.0 6.0	7.0 10.5	10.0 12.0	3.5 5.5	11.0 13.0	ns
t_{PHZ} t_{PLZ}	Output Enable time OEAB or $\overline{OEBA}$ to A_n or B_n	Waveform 6 Waveform 7	4.5 4.5	9.5 9.0	13.0 13.0	4.0 4.0	14.5 15.5	ns

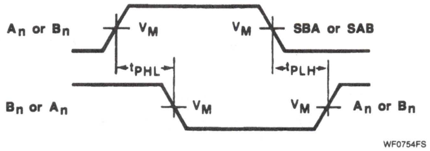
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	74F651, 74F652					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low A_n or B_n to CPAB or CPBA	Waveform 4	4.0 4.0			5.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low A_n or B_n to CPAB or CPBA	Waveform 4	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{OEBA}$ to OEAB	Waveform 5	5.0 5.0			5.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{OEBA}$ to OEAB	Waveform 5	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	Pulse width, High or Low CPAB or CPBA	Waveform 1	4.5 6.5			4.5 6.5		ns

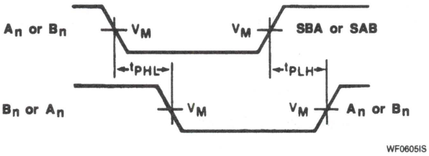
AC WAVEFORMS


CPBA or CPAB
V_M
V_M
V_M
$t_W(H)$
$t_W(L)$
t_{PHL}
t_{PLH}
A_n or B_n
V_M
V_M
WF0611FS

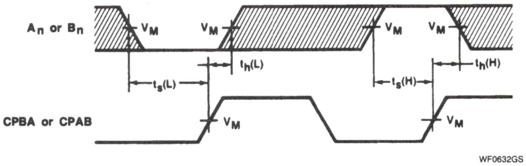
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width and Maximum Clock Frequency


A_n or B_n
V_M
V_M
SBA or SAB
t_{PHL}
t_{PLH}
B_n or A_n
V_M
V_M
A_n or B_n
WF0754FS

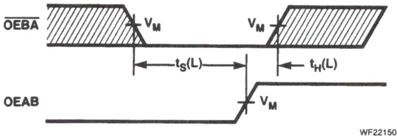
Waveform 2. Propagation Delay, A_n or B_n to B_n or A_n and SBA or SAB to A_n or B_n


A_n or B_n
V_M
V_M
SBA or SAB
t_{PHL}
t_{PLH}
B_n or A_n
V_M
V_M
A_n or B_n
WF0605IS

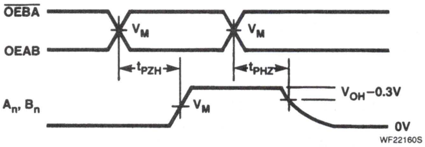
Waveform 3. Propagation Delay, A_n or B_n to B_n or A_n and SBA or SAB to A_n or B_n


A_n or B_n
V_M
V_M
V_M
V_M
$t_h(L)$
$t_h(H)$
$t_s(L)$
$t_s(H)$
CPBA or CPAB
V_M
V_M
WF0632GS

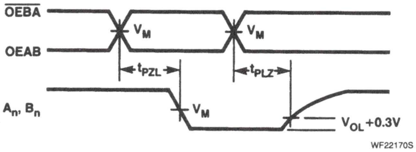
Waveform 4. Data Setup and Hold Times, and Clock Width


$\overline{OEBA}$
V_M
V_M
$t_S(L)$
$t_H(L)$
OEAB
V_M
WF22150S

Waveform 5. OEBA to OEAB Setup and Hold Time


$\overline{OEBA}$
OEAB
V_M
V_M
t_{PZH}
t_{PHZ}
A_n, B_n
V_M
V_{OH}−0.3V
0V
WF22160S

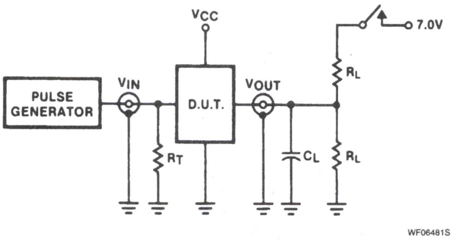
Waveform 6. 3-State Output Enable Time to High Level and Output Disable Time From High Level


$\overline{OEBA}$
OEAB
V_M
V_M
t_{PZL}
t_{PLZ}
A_n, B_n
V_M
V_{OL}+0.3V
WF22170S

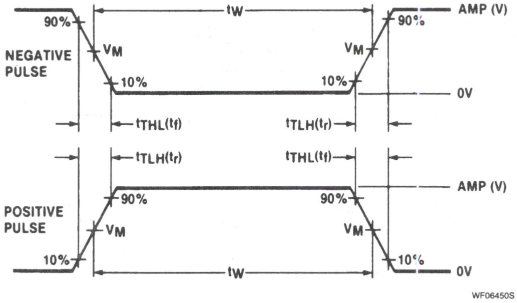
Waveform 7. 3-State Output Enable Time to Low Level and Output Disable Time From Low Level

NOTE: V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output.

TEST CIRCUIT AND WAVEFORMS


VCC
7.0V
RL
PULSE GENERATOR
VIN
D.U.T.
VOUT
RT
CL
RL
WF06481S

Test Circuit for 3-State Outputs


tW
AMP (V)
90%
90%
NEGATIVE PULSE
VM
VM
10%
10%
0V
tTHL(tf)
tTLH(tr)
tTLH(tr)
tTHL(tf)
AMP (V)
90%
90%
POSITIVE PULSE
VM
VM
10%
10%
0V
tW
WF06450S

$V_M = 1.5V$

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
OC	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F653, 74F654

FAST Products

'F653 Octal Transceiver/Register, Inverting (3-State + Open-Collector)
'F654 Octal Transceiver/Register, Inverting (3-State + Open-Collector)
Product Specification

FEATURES

- **High-impedance NPN base inputs for reduced loading**
- **Independent registers for A and B buses**
- **Multiplexed real-time and stored data**
- **Choice of non-inverting and inverting data paths**
- **3-State outputs ($B_0 - B_7$) or Open-Collector outputs ($A_0 - A_7$)**

DESCRIPTION

These devices consist of bus transceiver circuits with 3-State ($B_0 - B_7$) or Open-Collector ($A_0 - A_7$) outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes High. Output Enable (OEAB, $\overline{\text{OEBA}}$) pins are provided for bus management.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F653	90MHz	140mA
74F654	90MHz	140mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
Cerdip (300mil)	74F653F, 74F654F

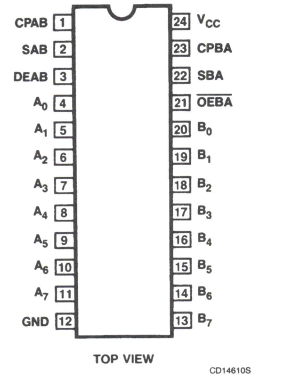
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$A_0 - A_7$	A inputs	1.0/0.033	20μA/20μA
$B_0 - B_7$	B inputs	3.5/0.116	70μA/70μA
CPAB	A-to-B clock input	1.0/0.033	20μA/20μA
CPBA	B-to-A clock input	1.0/0.033	20μA/20μA
SAB	A-to-B select input	1.0/0.033	20μA/20μA
SBA	B-to-A select input	1.0/0.033	20μA/20μA
OEAB	Output enable input	1.0/0.033	20μA/20μA
$\overline{\text{OEBA}}$	Output enable input	1.0/0.033	20μA/20μA
$A_0 - A_7$	A outputs	OC/106.7	OC/64mA
$B_0 - B_7$	B outputs	750/106.7	15mA/64mA

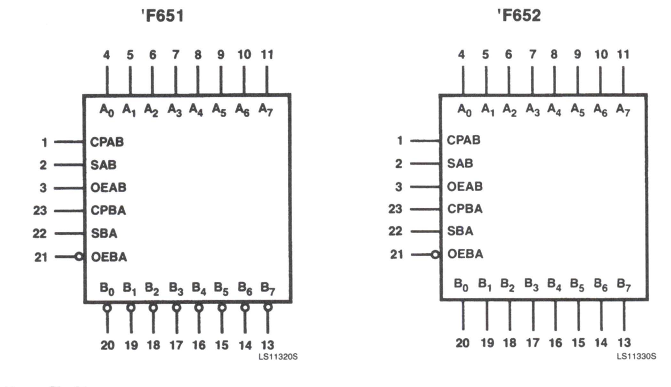
NOTE:

1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION


CPAB 1
SAB 2
DEAB 3
A0 4
A1 5
A2 6
A3 7
A4 8
A5 9
A6 10
A7 11
GND 12
24 VCC
23 CPBA
22 SBA
21 OEBA
20 B0
19 B1
18 B2
17 B3
16 B4
15 B5
14 B6
13 B7
TOP VIEW
CD14610S

LOGIC SYMBOL


'F651
'F652
4 5 6 7 8 9 10 11
A0 A1 A2 A3 A4 A5 A6 A7
1 CPAB
2 SAB
3 OEAB
23 CPBA
22 SBA
21 OEBA
B0 B1 B2 B3 B4 B5 B6 B7
20 19 18 17 16 15 14 13
LS11320S
LS11330S

V_{CC} = Pin 24
GND = Pin 12

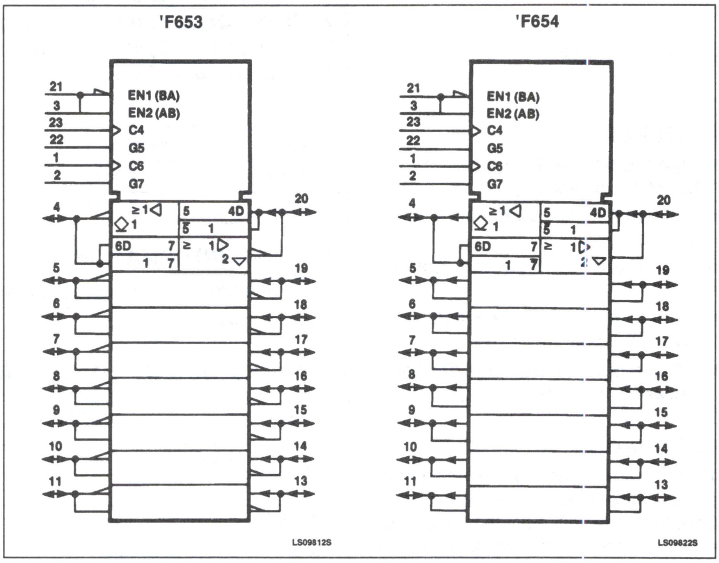
FAST 74F653, 74F654

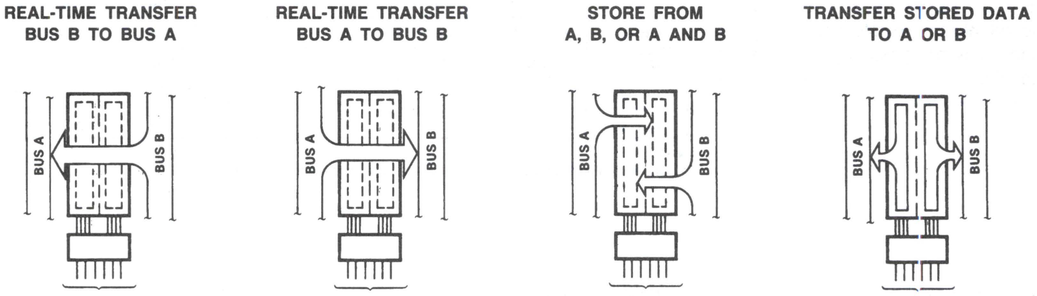
The following examples demonstrate the four fundamental bus-management functions that can be performed with the 'F653 and 'F654.

The Select pins determine whether data is stored or transferred through the device in real-time.

The Output Enable pins determine the direction of the data flow.

SYMBOL (IEEE/IEC)


'F653
'F654
EN1 (BA)
EN2 (AB)
C4
G5
C6
G7
≥1
1
5
4D
6D
7
2
21
3
23
22
1
2
4
5
6
7
8
9
10
11
20
19
18
17
16
15
14
13
LS09812S
LS09822S



REAL-TIME TRANSFER BUS B TO BUS A

OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA
L	L	X	X	X	L

REAL-TIME TRANSFER BUS A TO BUS B

OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA
H	H	X	X	L	X

STORE FROM A, B, OR A AND B

OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA
X	H	↑	X	X	X
L	X	X	↑	X	X
L	H	↑	↑	X	X

TRANSFER STORED DATA TO A OR B

OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA
H	L	H or L	H or L	H	H

Figure 1

FUNCTION TABLE

OPERATING MODE		INPUTS						DATA I/O	
'F651	'F652	$\overline{\text{OEBA}}$	OEAB	CPAB	CPBA	SAB	SBA	A_n	B_n
Isolation	Isolation	L	H	H or L	H or L	X	X	Input	Input
Store A and B data	Store A and B data	L	H	↑	↑	X	X		
Store A, Hold B	Store A, Hold B	X	H	↑	H or L	X	X	Input	un*
Store A in both registers	Store A in both registers	H	H	↑	↑	L	X	Input	Output
Hold A, Store B	Hold A, Store B	L	X	H or L	↑	X	X	un*	Input
Store B in both registers	Store B in both registers	L	L	↑	↑	X	L	Output	Input
Real-time $\overline{\text{B}}$ data to A bus	Real-time B data to A bus	L	L	X	X	X	L	Output	Input
Stored $\overline{\text{B}}$ data to A bus	Stored B data to A bus	L	L	X	H or L	X	H		
Real-time $\overline{\text{A}}$ data to B bus	Real-time A data to B bus	H	H	X	X	L	X	Input	Output
Stored $\overline{\text{A}}$ data to B bus	Stored A data to B bus	H	H	H or L	X	H	X		
Stored $\overline{\text{A}}$ data to B bus	Stored A data to B bus	H	L	H or L	H or L	H	H	Output	Output
Stored $\overline{\text{B}}$ data to A bus	Stored B data to A bus								

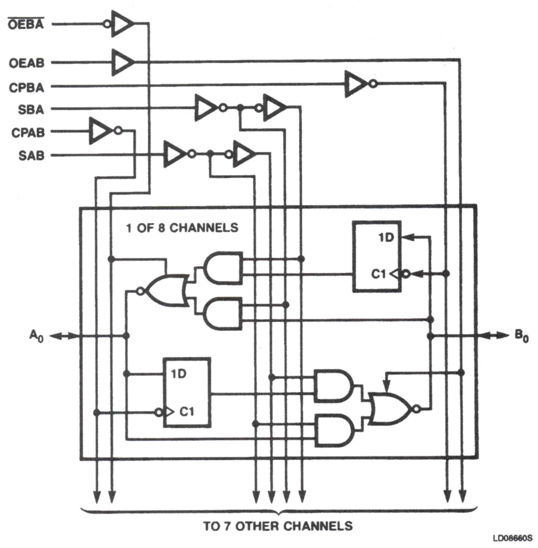
NOTES:

* The data output function may be enabled or disabled by various signals at OEBA and OEAB inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every Low-to-High transition of the clock.

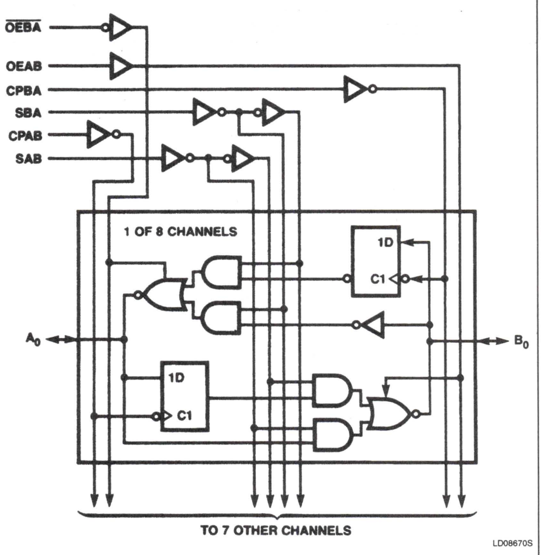
H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-to-High clock transition

LOGIC DIAGRAM

'F653


$\overline{\text{OEBA}}$
OEAB
CPBA
SBA
CPAB
SAB
1 OF 8 CHANNELS
1D
C1
1D
C1
A_0
B_0
TO 7 OTHER CHANNELS
LD08660S

'F654


$\overline{\text{OEBA}}$
OEAB
CPBA
SBA
CPAB
SAB
1 OF 8 CHANNELS
1D
C1
1D
C1
A_0
B_0
TO 7 OTHER CHANNELS
LD08670S

FAST 74F653, 74F654

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	–0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	128	V
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

<table>
<tr><th rowspan="2">SYMBOL</th><th rowspan="2" colspan="3">PARAMETER</th><th colspan="3">LIMITS</th><th rowspan="2">UNIT</th></tr>
<tr><th>Min</th><th>Nom</th><th>Max</th></tr>
<tr><td>V_{CC}</td><td colspan="3">Supply voltage</td><td>4.5</td><td>5.0</td><td>5.5</td><td>V</td></tr>
<tr><td>V_{IH}</td><td colspan="3">High-level input voltage</td><td>2.0</td><td></td><td></td><td>V</td></tr>
<tr><td>V_{IL}</td><td colspan="3">Low-level input voltage</td><td></td><td></td><td>0.8</td><td>V</td></tr>
<tr><td>I_{IK}</td><td colspan="3">Input clamp current</td><td></td><td></td><td>–18</td><td>mA</td></tr>
<tr><td>V_{OH}</td><td colspan="2">High-level output voltage</td><td>$A_0 - A_7$</td><td></td><td></td><td>4.5</td><td>V</td></tr>
<tr><td rowspan="2">I_{OH}</td><td rowspan="2">High-level output current</td><td>V_{OH} = 2.4V or 2.7V</td><td rowspan="2">$B_0 - B_7$</td><td></td><td></td><td>-3</td><td rowspan="2">mA</td></tr>
<tr><td>V_{OH} = 2.0V</td><td></td><td></td><td>–15</td></tr>
<tr><td>I_{OL}</td><td colspan="3">Low-level output current</td><td></td><td></td><td>64</td><td>mA</td></tr>
<tr><td>T_A</td><td colspan="3">Operating free-air temperature</td><td>0</td><td></td><td>70</td><td>°C</td></tr>
</table>

FAST 74F653, 74F654

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output current	$A_0 - A_7$	V_{CC} = MIN, V_{IH} = MIN V_{IL} = MAX, V_{OH} = MAX					250	μA
V_{OH}	High-level output voltage	$B_0 - B_7$	V_{CC} = MIN V_{IL} = MAX V_{IH} = MIN	$I_{OH} = -3mA$	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.4		V
				$I_{OH} = -15mA$	±10%V_{CC}	2.0			V
V_{OL}	Low-level output voltage		V_{CC} = MIN V_{IL} = MAX V_{IH} = MIN	$I_{OL} = 48mA$	±10%V_{CC}		0.35	0.50	V
				$I_{OL} = 64mA$	±5%V_{CC}		0.40	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$				-0.73	-1.2	V
I_I	Input current at maximum input voltage	Others	V_{CC} = 0.0V, V_I = 7.0V					100	μA
		$A_0 - A_7$, $B_0 - B_7$	V_{CC} = 5.5V, V_I = 5.5V					1.0	mA
I_{IH}	High-level input current	CPAB, CPBA SAB, SBA OEAB, $\overline{OEBA}$ $A_0 - A_7$	V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					-20	μA
$I_{OZH} + I_{IH}$	High-level input current	$B_0 - B_7$	V_{CC} = MAX, V_O = 2.7V					70	μA
$I_{OZL} + I_{IL}$	Low-level input current		V_{CC} = MAX, V_O = 0.5V					-70	μA
I_{OS}	Short-circuit output current[3]	$B_0 - B_7$	V_{CC} = MAX			-100		-225	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				110 140[4]	160 185[4]	mA
		I_{CCL}					140 160[4]	210 240[4]	mA
		I_{CCZ}					130	175	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of High-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. These values are for worst case only. Worst case is defined as all (16) I/O pins selected as outputs. Thermal mounting is required when using worst case conditions.

FAST 74F653, 74F654

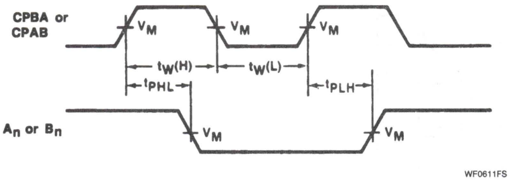
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS					UNIT
				$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
				Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	$A_0 - A_7$	Waveform 1	55	70		45		MHz
		$B_0 - B_7$	Waveform 1	100	115		85		MHz
t_{PLH} t_{PHL}	Propagation delay CPBA to A_n		Waveform 1	6.0 6.0	14.5 8.0	19.0 11.0	5.5 5.5	21.0 11.5	ns
t_{PLH} t_{PHL}	Propagation delay CPAB to B_n		Waveform 1	5.5 5.5	7.5 8.0	10.5 10.5	5.0 5.5	12.0 12.0	ns
t_{PLH} t_{PHL}	Propagation delay B_n to A_n		Waveform 3, 4	4.5 4.5	14.0 7.0	18.5 10.0	4.0 4.0	20.0 10.5	ns
t_{PLH} t_{PHL}	Propagation delay A_n to B_n		Waveform 3, 4	4.0 4.0	6.0 6.5	9.5 9.5	3.5 4.0	11.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay SBA to A_n		Waveform 3, 4	5.0 5.0	15.0 7.5	18.5 10.5	4.5 4.5	21.5 11.5	ns
t_{PLH} t_{PHL}	Propagation delay SAB to B_n		Waveform 3, 4	5.0 5.0	7.0 7.0	10.0 10.0	4.5 4.5	12.0 10.5	ns
t_{PLH} t_{PHL}	Output enable time $\overline{OEBA}$ to A_n		Waveform 2	6.5 6.5	16.0 10.0	20.0 12.5	6.0 6.0	23.0 14.0	ns
t_{PZH} t_{PZL}	Output enable time OEAB to B_n		Waveform 7 Waveform 8	4.5 6.0	6.5 8.0	9.5 11.0	4.0 5.5	10.0 11.5	ns
t_{PHZ} t_{PLZ}	Output enable time OEAB to B_n		Waveform 7 Waveform 8	6.5 6.0	9.5 9.0	13.0 12.0	6.0 5.5	14.5 14.5	ns

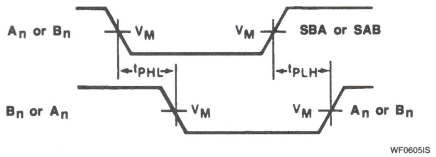
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low A_n or B_n to CPAB or CPBA	Waveform 4	4.5 4.5			5.5 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low A_n or B_n to CPAB or CPBA	Waveform 4	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{OEBA}$ to OEAB	Waveform 5	5.0 5.0			5.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{OEBA}$ to OEAB	Waveform 5	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	Pulse width, High or Low CPAB or CPBA	Waveform 1	4.5 6.5			4.5 6.5		ns

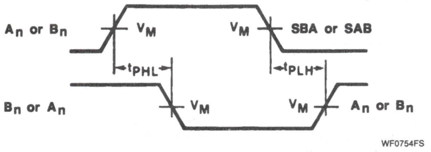
AC WAVEFORMS


CPBA or CPAB
V_M
V_M
V_M
$t_W(H)$
$t_W(L)$
t_{PHL}
t_{PLH}
A_n or B_n
V_M
V_M
WF0611FS

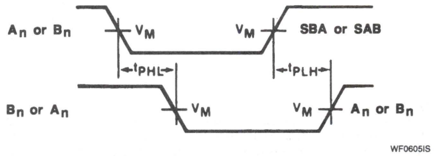
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width and Maximum Clock Frequency


A_n or B_n
V_M
V_M
SBA or SAB
t_{PHL}
t_{PLH}
B_n or A_n
V_M
V_M
A_n or B_n
WF0605IS

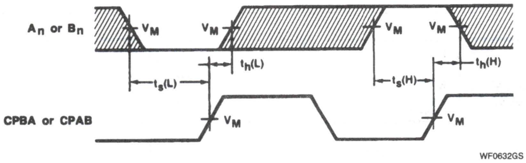
Waveform 2. Enable and Disable Times for Open-Collector Outputs


A_n or B_n
V_M
V_M
SBA or SAB
t_{PHL}
t_{PLH}
B_n or A_n
V_M
V_M
A_n or B_n
WF0754FS

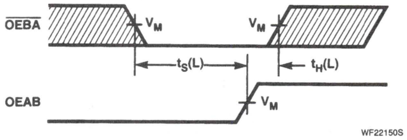
Waveform 3. Propagation Delay, A_n or B_n to B_n or A_n and SBA or SAB to A_n or B_n


A_n or B_n
V_M
V_M
SBA or SAB
t_{PHL}
t_{PLH}
B_n or A_n
V_M
V_M
A_n or B_n
WF0605IS

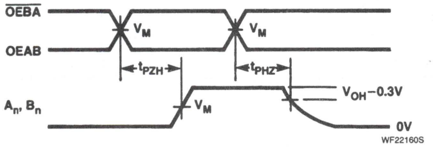
Waveform 4. Propagation Delay, A_n or B_n to B_n or A_n and SBA or SAB to A_n or B_n


A_n or B_n
V_M
V_M
V_M
V_M
$t_h(L)$
$t_h(H)$
$t_s(L)$
$t_s(H)$
CPBA or CPAB
V_M
V_M
WF0632GS

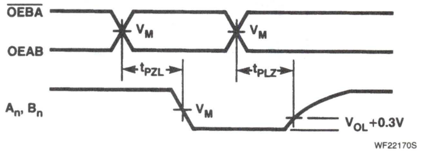
Waveform 5. Data Setup and Hold Times, and Clock Width


$\overline{OEBA}$
V_M
V_M
$t_S(L)$
$t_H(L)$
OEAB
V_M
WF22150S

Waveform 6. OEBA to OEAB Setup and Hold Time


$\overline{OEBA}$
OEAB
V_M
V_M
t_{PZH}
t_{PHZ}
A_n, B_n
V_M
$V_{OH}-0.3V$
0V
WF22160S

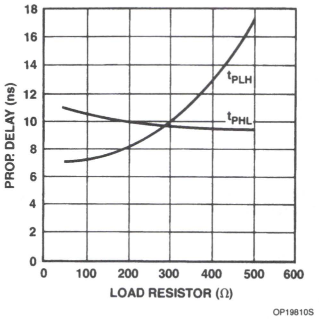
Waveform 7. 3-State Output Enable Time to High Level and Output Disable Time From High Level


$\overline{OEBA}$
OEAB
V_M
V_M
t_{PZL}
t_{PLZ}
A_n, B_n
V_M
$V_{OL}+0.3V$
WF22170S

Waveform 8. 3-State Output Enable Time to Low Level and Output Disable Time From Low Level

NOTE: $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

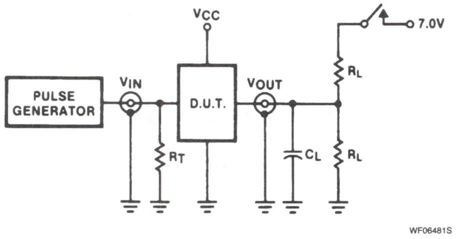
TYPICAL PROPAGATION DELAYS VERSUS LOAD FOR OPEN-COLLECTOR OUTPUTS



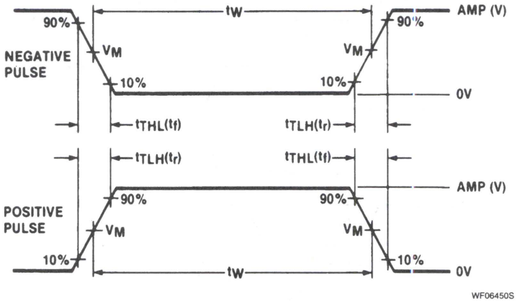
NOTES:

When using Open-Collector parts, the value of the pull-up resistor greatly affects the value of the t_{PLH}. For example, changing the specified pull-up resistor value from 500Ω to 100Ω will improve the t_{PLH} up to 50% with only a slight increase in the t_{PHL}. However, if the value of the pull-up resistor is changed, the user must make certain that the total I_{OL} current through the resistor and the total I_{IL}'s of the receivers does not exceed the I_{OL} maximum specification.

TEST CIRCUIT AND WAVEFORMS


VCC
7.0V
RL
PULSE GENERATOR
VIN
D.U.T.
VOUT
RT
CL
RL
WF06481S

Test Circuit for 3-State and Open-Collector (OC) Outputs


tw
90%
AMP (V)
NEGATIVE PULSE
VM
VM
10%
10%
0V
tTHL(tf)
tTLH(tr)
tTLH(tr)
tTHL(tf)
AMP (V)
90%
90%
POSITIVE PULSE
VM
VM
10%
10%
0V
tw
WF06450S

$V_M = 1.5V$

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
OC	closed
All other	open

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Signetics

FAST 74F655A, 74F656A
Buffers/Drivers

Octal Buffers/Line Drivers with Parity
('F655A – Inverting 3-State)
('F656A – Non-Inverting 3-State)
Product Specification

FAST Products

FEATURES

- **Significantly improved AC performance over 'F655 and 'F656**
- **High-impedance NPN base input for reduced loading (20μA in High and Low states)**
- **Ideal in applications where high output drive and light bus loading are required (I_{IL} is 20μA vs FAST std of 600μA)**
- **'F655A combines 'F240 and 'F280 functions in one package**
- **'F656A combines 'F244 and 'F280A functions in one package**
- **'F655A Inverting**
  'F656A Non-inverting
- **3-State outputs sink 64mA**
- **Inputs source 15mA**
- **24-pin plastic Slim DIP (300mil) package**
- **Inputs on one side and outputs on the other side simplify PC board layout**
- **Combined functions reduce part count and enhance system performance**

DESCRIPTION

The 'F655A and 'F656A are octal buffers and line drivers with parity generation/checking designed to be employed as memory address drivers, clock drivers, and bus-oriented transmitters/receivers. These parts include parity generator/checker to improve PC board density.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F655A	6.5ns	64mA
74F656A	6.5ns	64mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
24-Pin Plastic Slim DIP	N74F655AN, N74F656AN
24-Pin Plastic SOL	N74F655AD, N74F656AD

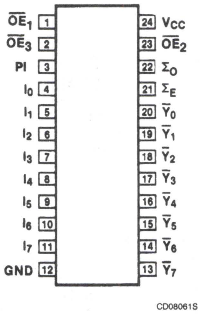
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I_n	Data inputs	2.0/0.066	40μA/40μA
PI	Parity input	1.0/0.033	20μA/20μA
$\overline{OE}_1$, $\overline{OE}_2$ $\overline{OE}_3$	3-State output enable inputs (active-Low)	1.0/0.033	20μA/20μA
$\overline{Y}_n$	Data outputs ('F655A)	750/106.7	15mA/64mA
Y_n	Data outputs ('F656A)	750/106.7	15mA/64mA
Σ_E, Σ_O	Parity outputs	750/106.7	15mA/64mA

NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

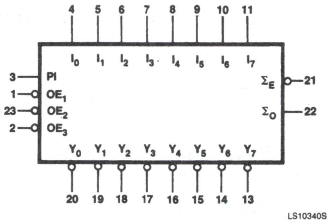
PIN CONFIGURATION

'F655A


$\overline{OE}_1$ 1
$\overline{OE}_3$ 2
PI 3
I_0 4
I_1 5
I_2 6
I_3 7
I_4 8
I_5 9
I_6 10
I_7 11
GND 12
24 V_{CC}
23 $\overline{OE}_2$
22 Σ_O
21 Σ_E
20 $\overline{Y}_0$
19 $\overline{Y}_1$
18 $\overline{Y}_2$
17 $\overline{Y}_3$
16 $\overline{Y}_4$
15 $\overline{Y}_5$
14 $\overline{Y}_6$
13 $\overline{Y}_7$
CD08061S

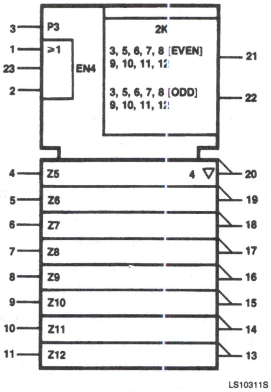
LOGIC SYMBOL

'F655A


4 5 6 7 8 9 10 11
I_0 I_1 I_2 I_3 I_4 I_5 I_6 I_7
3 PI
1 OE_1
23 OE_2
2 OE_3
Σ_E 21
Σ_O 22
Y_0 Y_1 Y_2 Y_3 Y_4 Y_5 Y_6 Y_7
20 19 18 17 16 15 14 13
LS10340S

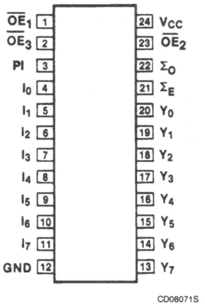
LOGIC SYMBOL (IEEE/IEC)

'F655A


3 P3
1 ≥1
23 EN4
2
2K
3, 5, 6, 7, 8 [EVEN] 9, 10, 11, 12 21
3, 5, 6, 7, 8 [ODD] 9, 10, 11, 12 22
4 Z5 4 ▽ 20
5 Z6 19
6 Z7 18
7 Z8 17
8 Z9 16
9 Z10 15
10 Z11 14
11 Z12 13
LS10311S

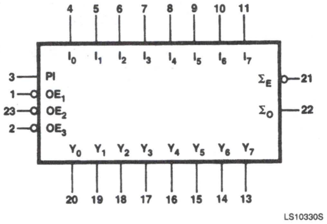
PIN CONFIGURATION

'F656A


$\overline{OE}_1$ 1
$\overline{OE}_3$ 2
PI 3
I_0 4
I_1 5
I_2 6
I_3 7
I_4 8
I_5 9
I_6 10
I_7 11
GND 12
24 V_{CC}
23 $\overline{OE}_2$
22 Σ_O
21 Σ_E
20 Y_0
19 Y_1
18 Y_2
17 Y_3
16 Y_4
15 Y_5
14 Y_6
13 Y_7
CD08071S

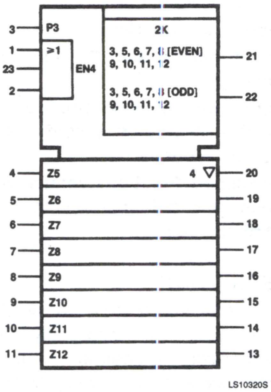
LOGIC SYMBOL

'F656A

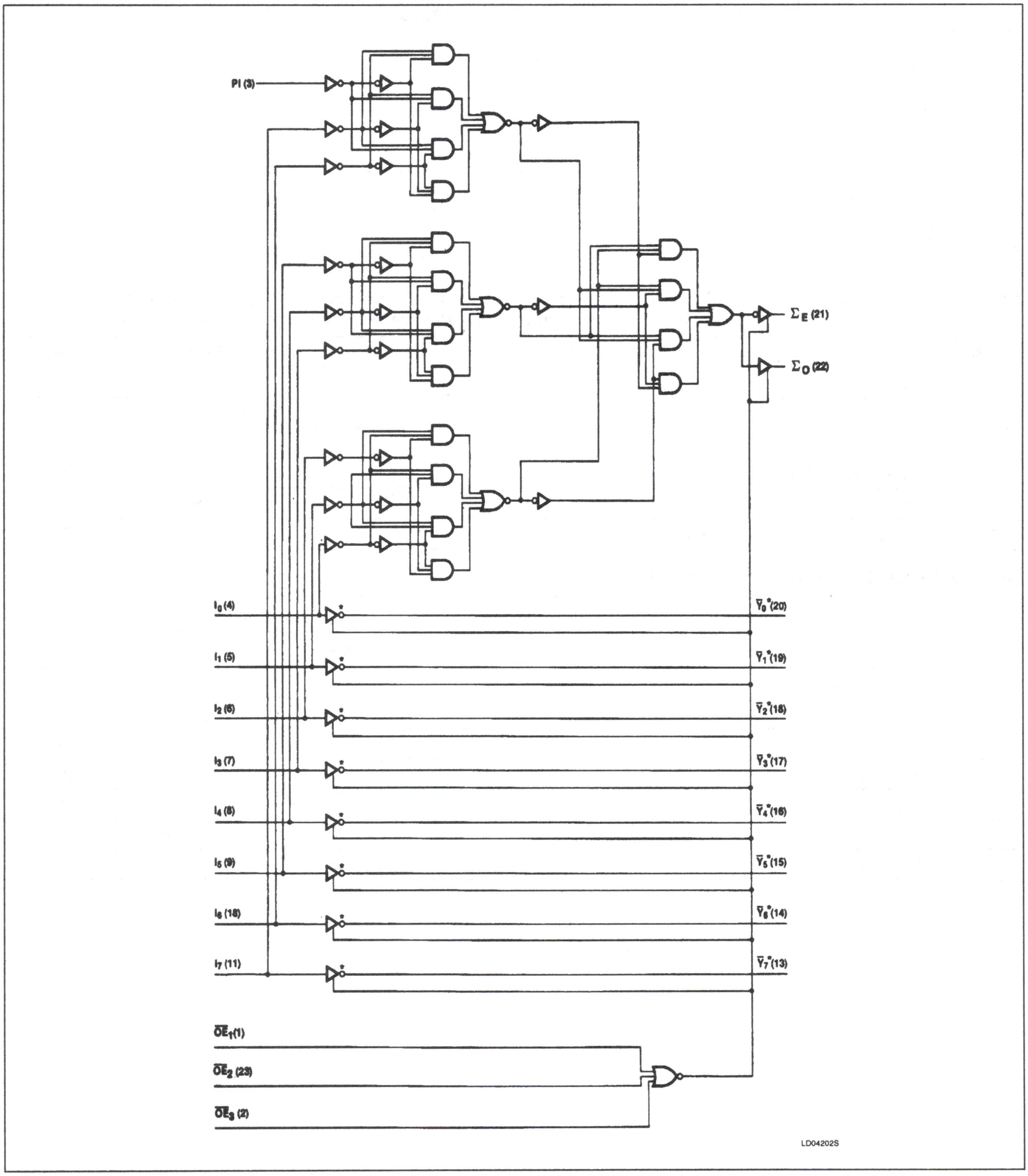

4 5 6 7 8 9 10 11
I_0 I_1 I_2 I_3 I_4 I_5 I_6 I_7
3 PI
1 OE_1
23 OE_2
2 OE_3
Σ_E 21
Σ_O 22
Y_0 Y_1 Y_2 Y_3 Y_4 Y_5 Y_6 Y_7
20 19 18 17 16 15 14 13
LS10330S

LOGIC SYMBOL (IEEE/IEC)

'F656A


3 P3
1 ≥1
23 EN4
2
2K
3, 5, 6, 7, 8 [EVEN] 9, 10, 11, 12 21
3, 5, 6, 7, 8 [ODD] 9, 10, 11, 12 22
4 Z5 4 ▽ 20
5 Z6 19
6 Z7 18
7 Z8 17
8 Z9 16
9 Z10 15
10 Z11 14
11 Z12 13
LS10320S

LOGIC DIAGRAM FOR 'F655A
(Non-inverting for 'F656A Indicated by Symbol *)


PI (3)
ΣE (21)
ΣO (22)
I0 (4)
I1 (5)
I2 (6)
I3 (7)
I4 (8)
I5 (9)
I6 (10)
I7 (11)
Y̅0*(20)
Y̅1*(19)
Y̅2*(18)
Y̅3*(17)
Y̅4*(16)
Y̅5*(15)
Y̅6*(14)
Y̅7*(13)
O̅E̅1(1)
O̅E̅2 (23)
O̅E̅3 (2)
LD04202S

FUNCTION TABLE

INPUTS				DATA OUTPUTS	
$\overline{OE}_1$	$\overline{OE}_2$	$\overline{OE}_3$	I_n	'F655A	'F656A
L	L	L	L	H	L
L	L	L	H	L	H
H	X	X	X	Z	Z
X	H	X	X	Z	Z
X	X	H	X	Z	Z

INPUTS	PARITY OUTPUTS	
Number of inputs High (PI, $I_0 - I_7$)	Σ_E	Σ_0
EVEN – 0, 2, 4, 6, 8	H	L
ODD – 1, 3, 5, 7, 9	L	H
Any $\overline{OE}$ = High	Z	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High-impedance state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	–0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	128	mA
T_A	Operating free-air temperature range	0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			–18	mA
I_{OH}	High-level output current			–15	mA
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			74F655A, 'F655A			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = −3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.4		V
				I_{OH} = −15mA	±10%V_{CC}	2.0			V
					±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 48mA	±10%V_{CC}		0.35	0.50	V
				I_{OL} = 64mA	±5%V_{CC}		0.40	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$				−0.73	−1.2	V
I_I	Input clamp current at maximum input voltage		V_{CC} = 0.0V, V_I = 7.0V					100	μA
I_{IH}	High-level input current	I_n	V_{CC} = MAX, V_I = 2.7V					40	μA
		PI, $\overline{OE}_n$						20	μA
I_{IL}	Low-level input current	I_n	V_{CC} = MAX, V_I = 0.5V					−40	μA
		PI, $\overline{OE}_n$						−20	μA
I_{OZH}	OFF-state output current, High-level voltage applied		V_{CC} = MAX, V_O = 2.7V					50	μA
I_{OZL}	OFF-state output current Low-level voltage applied		V_{CC} = MAX, V_O = 0.5V					−50	μA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX, V_O = 0.0V			−100		−225	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				50	80	mA
		I_{CCL}					78	110	mA
		I_{CCZ}					63	90	mA

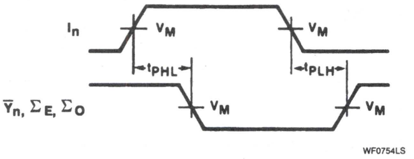
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

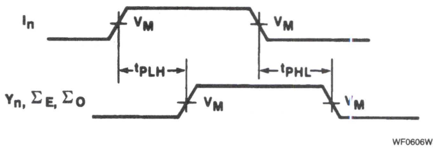
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	74F655A, 656A					UNIT
				T_A = +25°C V_{CC} = +5.0V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = +5.0V ±10% C_L = 50pF R_L = 500Ω		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_n to $\overline{Y}_n$	'F655A	Waveform 1	2.0 1.0	4.5 2.5	6.5 4.0	2.0 1.0	7.5 4.5	ns
t_{PLH} t_{PHL}	Propagation delay I_n to Y_n	'F656A	Waveform 2	2.0 2.5	4.0 5.5	6.5 7.0	2.0 2.5	7.0 7.5	ns
t_{PLH} t_{PHL}	Propagation delay I_n to Σ_E, Σ_O		Waveform 1, 2	5.5 5.5	10.0 11.0	13.0 14.5	5.5 5.5	14.0 16.5	ns
t_{PZH} t_{PZL}	Output enable time to High or Low level		Waveform 3 Waveform 4	4.0 4.0	7.0 8.0	10.5 11.0	4.0 4.0	11.5 12.0	ns
t_{PHZ} t_{PLZ}	Output disable time from High or Low level		Waveform 3 Waveform 4	1.5 2.0	4.5 5.0	8.0 8.0	1.5 2.0	9.0 9.0	ns

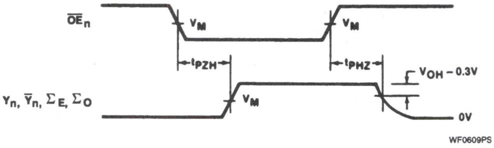
AC WAVEFORMS


In
VM
VM
tPHL
tPLH
Ȳn, ΣE, ΣO
VM
VM
WF0754LS

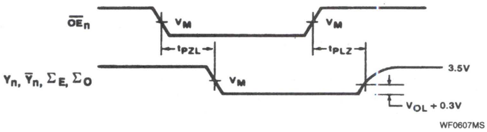
Waveform 1. Clock to Output Delays and Clock Pulse Width


In
VM
VM
tPLH
tPHL
Yn, ΣE, ΣO
VM
VM
WF0606WS

Waveform 2. Propagation Delay for I_n to Y_n, Σ_E, Σ_0


OEn
VM
VM
tPZH
tPHZ
VOH − 0.3V
Yn, Ȳn, ΣE, ΣO
VM
0V
WF0609PS

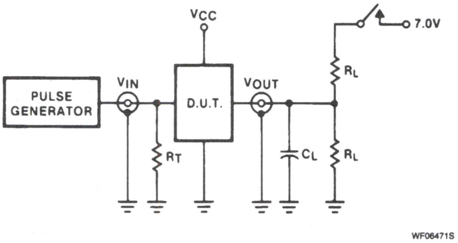
Waveform 3. 3-State Output Enable Time to Low Level and Output Disable Time From Low Level


OEn
VM
VM
tPZL
tPLZ
3.5V
Yn, Ȳn, ΣE, ΣO
VM
VOL + 0.3V
WF0607MS

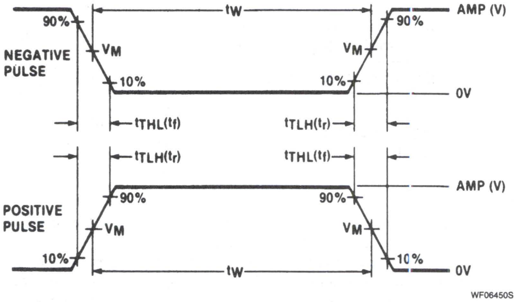
Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORMS


VCC
7.0V
RL
PULSE GENERATOR
VIN
D.U.T.
VOUT
RT
CL
RL
WF06471S

Test Circuit for 3-State Outputs


tW
AMP (V)
90%
90%
NEGATIVE PULSE
VM
VM
10%
10%
0V
tTHL(tf)
tTLH(tr)
tTLH(tr)
tTHL(tf)
AMP (V)
90%
90%
POSITIVE PULSE
VM
VM
10%
10%
tW
0V
WF06450S

$V_M = 1.5V$.

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F657
Transceiver

Octal Bidirectional Transceiver With 8-Bit Parity Generator/Checker (3-State Outputs)
Product Specification

FAST Products

FEATURES

- **High-impedance NPN base input for reduced loading (70μA in High and Low states)**
- **Ideal in applications where High output drive and light bus loading are required (I_{IL} is 70μA vs FAST std of 600μA)**
- **24-pin plastic Slim dip (300-mil) package**
- **Combines 'F245 and 'F280A functions in one package**
- **3-State outputs**
- **Outputs sink 64mA**
- **15mA source current**
- **Input diodes for termination effects**

DESCRIPTION

The 'F657 contains eight non-inverting buffers with 3-State outputs and an 8-bit parity generator/checker, and is intended for bus-oriented applications. The buffers have a guaranteed current sinking capability of 24mA at the A ports and 64mA at the B ports. The Transmit/Receive (T/$\overline{R}$) input determines the direction of the data flow through the bidirectional transceivers. Transmit (active-High) enables data from A ports to B ports; Receive (active-Low) enables data from B ports to A ports.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F657	8.0ns	100mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
24-Pin Plastic Slim DIP (300mil)	N74F657N
24-Pin Plastic SOL	N74F657D

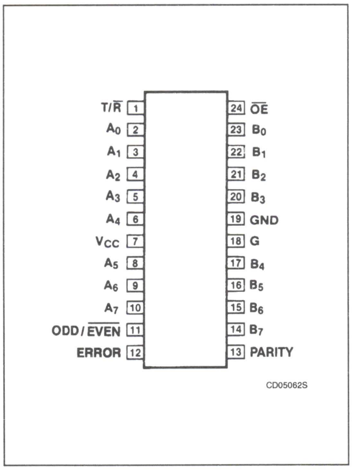
NOTE:
1. Thermal mounting techniques are recommended. See App Note AN SMD-100 for a discussion of thermal considerations for surface mounted devices.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$A_0 - A_7$	A ports 3-State inputs	3.5/0.117	70μA/70μA
$B_0 - B_7$	B ports 3-State inputs	3.5/0.117	70μA/70μA
PARITY	Parity input	3.5/0.117	70μA/70μA
T/$\overline{R}$	Transmit/receive input	2.0/0.066	40μA/40μA
ODD/$\overline{EVEN}$	Parity select	1.0/0.033	20μA/20μA
$\overline{OE}$	Output enable input (active-Low)	2.0/0.066	40μA/40μA
$A_0 - A_7$	A ports 3-State outputs	150/40	3mA/24mA
$B_0 - B_7$	B ports 3-State outputs	750/106.7	15mA/64mA
PARITY	Parity output	750/106.7	15mA/64mA
$\overline{ERROR}$	Error output	750/106.7	15mA/64mA

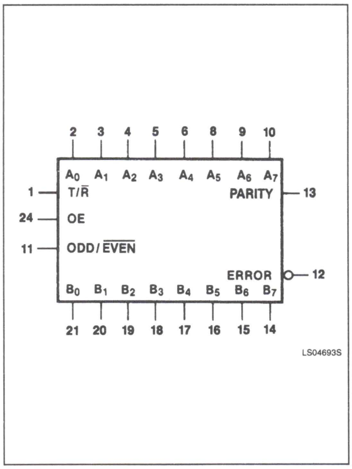
NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



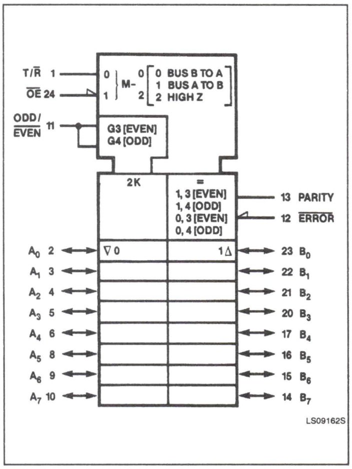
T/R̄ 1
A0 2
A1 3
A2 4
A3 5
A4 6
VCC 7
A5 8
A6 9
A7 10
ODD/EVEN 11
ERROR 12
24 OE
23 B0
22 B1
21 B2
20 B3
19 GND
18 G
17 B4
16 B5
15 B6
14 B7
13 PARITY
CD05062S

LOGIC SYMBOL



2 3 4 5 6 8 9 10
A0 A1 A2 A3 A4 A5 A6 A7
1 T/R̄
24 OE
11 ODD/EVEN
PARITY 13
ERROR 12
B0 B1 B2 B3 B4 B5 B6 B7
21 20 19 18 17 16 15 14
LS04693S

LOGIC SYMBOL (IEEE/IEC)



T/R̄ 1
OE 24
0
1
M-
0
2
0 BUS B TO A
1 BUS A TO B
2 HIGH Z
ODD/EVEN 11
G3 [EVEN]
G4 [ODD]
2K
=
1, 3 [EVEN]
1, 4 [ODD]
0, 3 [EVEN]
0, 4 [ODD]
13 PARITY
12 ERROR
∇0
1Δ
A0 2
A1 3
A2 4
A3 5
A4 6
A5 8
A6 9
A7 10
23 B0
22 B1
21 B2
20 B3
17 B4
16 B5
15 B6
14 B7
LS09162S

Transceiver

FAST 74F657

The Output Enable (OE) input disables both the A and B ports by placing them in a Hi-Z condition when the $\overline{\text{OE}}$ input is High.

The parity select (ODD/$\overline{\text{EVEN}}$) input gives the user the option of odd or even parity systems.

The parity (PARITY) pin is an output from the generator/checker when transmitting from port A to B (T/$\overline{\text{R}}$ = High) and an input when receiving from port B to A (T/$\overline{\text{R}}$ = Low).

When transmitting (T/$\overline{\text{R}}$ = High) the parity select (ODD/$\overline{\text{EVEN}}$) input is set, then the A port data is polled to determine the number of High bits. The parity (PARITY) output then goes to the logic state determined by the parity select (ODD/$\overline{\text{EVEN}}$) setting and by the number of High bits on port A. For example, if the parity select (ODD/$\overline{\text{EVEN}}$) is set Low (even parity), and the number of High bits on port A is odd, then the parity (PARITY) output will be High, transmitting even parity. If the number of High bits on port A is even, then the parity (PARITY) output will be Low, keeping even parity. When in receive mode (T/$\overline{\text{R}}$ = Low) the B port is polled to determine the number of High bits.

If parity select (ODD/$\overline{\text{EVEN}}$) is Low (even parity) and the number of Highs on port B is:

(1) odd and the parity (PARITY) input is High, then $\overline{\text{ERROR}}$ will be High, signifying no error.

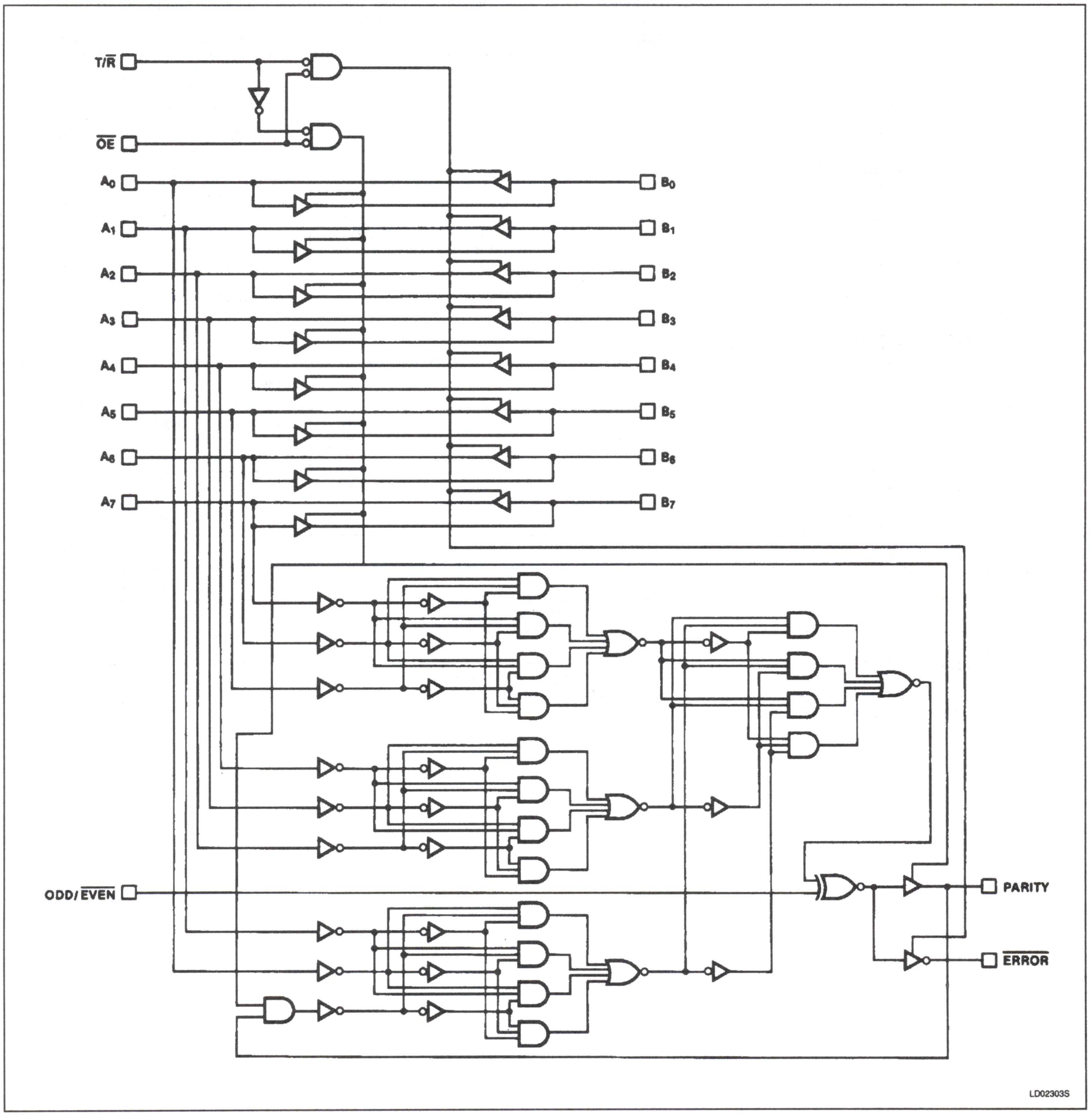
(2) even and the parity (PARITY) input is Low, then $\overline{\text{ERROR}}$ will be asserted Low, indicating an error.

FUNCTION TABLE

NUMBER OF INPUTS THAT ARE HIGH	INPUTS			INPUT/ OUTPUT	OUTPUTS	
	$\overline{\text{OE}}$	T/$\overline{\text{R}}$	ODD/$\overline{\text{EVEN}}$	PARITY	$\overline{\text{ERROR}}$	OUTPUTS MODE
0, 2, 4, 6, 8	L	H	H	H	Z	Transmit
	L	H	L	L	Z	Transmit
	L	L	H	H	H	Receive
	L	L	H	L	L	Receive
	L	L	L	H	L	Receive
	L	L	L	L	H	Receive
1, 3, 5, 7	L	H	H	L	Z	Transmit
	L	H	L	H	Z	Transmit
	L	L	H	H	L	Receive
	L	L	H	L	H	Receive
	L	L	L	H	H	Receive
	L	L	L	L	L	Receive
Don't care	H	X	X	Z	Z	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High-impedance state

LOGIC DIAGRAM


T/R̄
ŌĒ
A₀
A₁
A₂
A₃
A₄
A₅
A₆
A₇
B₀
B₁
B₂
B₃
B₄
B₅
B₆
B₇
ODD/ĒVĒN̄
PARITY
ĒR̄R̄ŌR̄
LD02303S

6

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		−0.5 to +7.0	V
V_{IN}	Input voltage		−0.5 to +7.0	V
I_{IN}	Input current		−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		−0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	$A_0 - A_7$	48	mA
		$B_0 - B_7$, PARITY, $\overline{\text{ERROR}}$	128	mA
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	High-level output current	$A_0 - A_7$			−3	mA
		$B_0 - B_7$, PARITY, $\overline{\text{ERROR}}$			−15	mA
I_{OL}	Low-level output current	$A_0 - A_7$			24	mA
		$B_0 - B_7$, PARITY, $\overline{\text{ERROR}}$			64	mA
T_A	Operating free-air temperature		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage	All Outputs	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = −3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.4		V
		$B_0 - B_7$, PARITY, $\overline{ERROR}$		I_{OH} = −15mA	±10%V_{CC}	2.0			V
					±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage	$A_0 - A_7$	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 24mA	±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
		$B_0 - B_7$, PARITY, $\overline{ERROR}$		I_{OL} = 48mA	±10%V_{CC}		0.40	0.55	V
				I_{OL} = 64mA	±5%V_{CC}		0.40	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$				−0.73	−1.2	V
I_I	Input current at maximum input voltage	T/$\overline{R}$, $\overline{OE}$, ODD/$\overline{EVEN}$	V_{CC} = 0.0V, V_I = 7.0V					100	μA
		$A_0 - A_7$	V_{CC} = MAX, V_I = 5.5V					2	mA
		$B_0 - B_7$						1	mA
I_{IH}	High-level input current	ODD/$\overline{EVEN}$	V_{CC} = MAX, V_I = 2.7V					20	μA
		T/$\overline{R}$,$\overline{OE}$						40	μA
I_{IL}	Low-level input current	ODD/$\overline{EVEN}$	V_{CC} = MAX, V_I = 0.5V					−20	μA
		T/$\overline{R}$,$\overline{OE}$						−40	μA
$I_{IH} + I_{OZH}$	OFF-state current High level voltage applied	$A_0 - A_7$, $B_0 - B_7$, PARITY	V_{CC} = MAX, V_O = 2.7V					70	μA
$I_{IL} + I_{OZL}$	OFF-state current Low level voltage applied		V_{CC} = MAX, V_O = 0.5V					−70	μA
I_{OZH}	OFF-state current High level voltage applied	$\overline{ERROR}$	V_{CC} = MAX, V_{IH} = MIN, V_O = 2.7V					50	μA
I_{OZL}	OFF-state current Low level voltage applied		V_{CC} = MAX, V_{IH} = MIN, V_O = 0.5V					−50	μA
I_{OS}	Short-circuit output current[3]	$A_0 - A_7$	V_{CC} = MAX			−60		−150	mA
		$B_0 - B_7$				−100		−225	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				90	125	mA
		I_{CCL}					106	150	mA
		I_{CCZ}					98	145	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of High-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Transceiver FAST 74F657

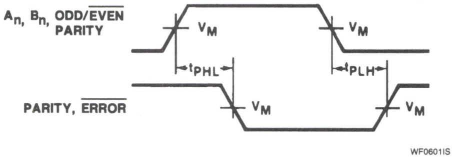
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS $T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50pF$, $R_L = 500\Omega$			LIMITS $T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		UNIT
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n or B_n to A_n	Waveform 2	2.5 3.0	5.5 6.0	7.5 7.5	2.5 3.0	8.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay A_n to PARITY	Waveform 1, 2	7.0 7.0	10.0 10.0	14.0 15.0	7.0 7.0	16.0 16.0	ns
t_{PLH} t_{PHL}	Propagation delay ODD/$\overline{\text{EVEN}}$ to PARITY, $\overline{\text{ERROR}}$	Waveform 1, 2	4.5 4.5	7.5 8.0	11.0 11.5	4.5 4.5	12.0 12.5	ns
t_{PLH} t_{PHL}	Propagation delay B_n to $\overline{\text{ERROR}}$	Waveform 1, 2	8.0 8.0	14.0 14.0	20.5 20.5	7.5 7.5	22.5 22.5	ns
t_{PLH} t_{PHL}	Propagation delay PARITY to $\overline{\text{ERROR}}$	Waveform 1, 2	8.0 8.0	11.5 12.0	15.5 15.5	7.5 8.0	16.5 17.0	ns
t_{PZH} t_{PZL}	Output enable time^2 to High or Low level	Waveform 3 Waveform 4	3.0 4.0	5.5 7.0	8.0 9.5	3.0 4.0	9.0 11.0	ns
t_{PHZ} t_{PLZ}	Output disable time from High or Low level	Waveform 3 Waveform 4	2.0 2.0	4.5 4.0	7.5 6.0	2.0 2.0	8.0 6.5	ns

NOTE:

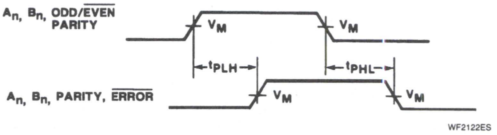
1. These delay times reflect the 3-state recovery time only and not the signal through the buffers or the parity check circuitry. To assure VALID information at the $\overline{\text{ERROR}}$ pin, time must be allowed for the signal to propagate through the drivers (B to A), through the parity check circuitry (same as A to Parity), and to the $\overline{\text{ERROR}}$ output after the $\overline{\text{ERROR}}$ pin has been enabled (Output Enable times). VALID data at the $\overline{\text{ERROR}}$ pin ≥ (B to A) + (A to Parity) + (Output enable time).

AC WAVEFORMS



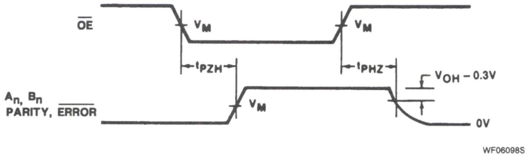
A_n, B_n, ODD/$\overline{\text{EVEN}}$ PARITY
V_M
V_M
t_{PHL}
t_{PLH}
PARITY, $\overline{\text{ERROR}}$
V_M
V_M
WF06011S

Waveform 1. Propagation Delay for Inverting Outputs



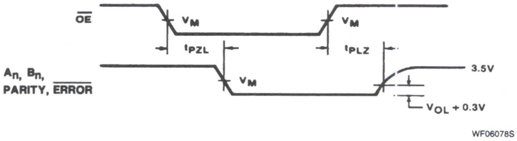
A_n, B_n, ODD/$\overline{\text{EVEN}}$ PARITY
V_M
V_M
t_{PLH}
t_{PHL}
A_n, B_n, PARITY, $\overline{\text{ERROR}}$
V_M
V_M
WF2122ES

Waveform 2. Propagation Delay for Non-Inverting Outputs



$\overline{\text{OE}}$
V_M
V_M
t_{PZH}
t_{PHZ}
$V_{OH} - 0.3V$
A_n, B_n PARITY, $\overline{\text{ERROR}}$
V_M
0V
WF06098S

Waveform 3. 3-State Enable Time to High Level and Disable Time From High Level

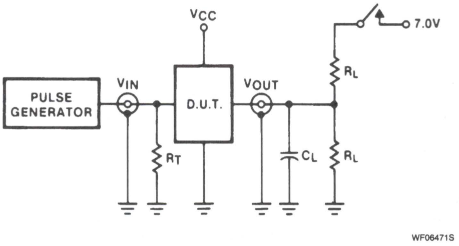


$\overline{\text{OE}}$
V_M
V_M
t_{PZL}
t_{PLZ}
3.5V
A_n, B_n, PARITY, $\overline{\text{ERROR}}$
V_M
$V_{OL} + 0.3V$
WF06078S

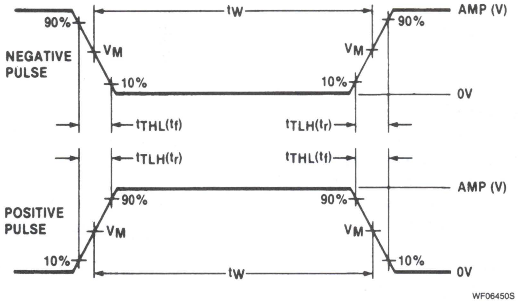
Waveform 4. 3-State Enable Time to Low Level and Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORMS


VCC
7.0V
RL
VIN
VOUT
PULSE GENERATOR
D.U.T.
RT
CL
RL
WF06471S

Test Circuit for 3-State Outputs


90%
tW
90%
AMP (V)
NEGATIVE PULSE
VM
VM
10%
10%
0V
tTHL(tf)
tTLH(tr)
tTLH(tr)
tTHL(tf)
AMP (V)
90%
90%
POSITIVE PULSE
VM
VM
10%
10%
0V
tW
WF06450S

$V_M = 1.5V$

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F670
4 × 4 Register File (3-State)

Preliminary Specification

FAST Products

FEATURES
- **Simultaneous and independent Read and Write operations**
- **Expandable to almost any word size and bit length**
- **3-State outputs**

DESCRIPTION
The 'F670 is a 16-bit 3-State Register File organized as 4 words of 4 bits each. Separate Read and Write Address and Enable inputs are available, permitting simultaneous writing into one word location and reading from another location. The 4-bit word to be stored is presented to four data inputs. The Write Address inputs (WA and WB) determine the location of the stored word. When the Write Enable ($\overline{WE}$) input is Low, the data is entered into the addressed location. The addressed location remains transparent to the data while the $\overline{WE}$ is Low. Data supplied at the inputs will be read out in true (non-inverting) form from the 3-State outputs. Data and Write Address inputs are inhibited when $\overline{WE}$ is High. Direct acquisition of data stored in any of the four registers is made possible by individual Read Address inputs (RA and RB). The addressed word appears at the four outputs when the Read Enable ($\overline{RE}$) is Low. Data outputs are in the High-impedance "OFF" state when the Read Enable input is High. This permits outputs to be tied together to increase the word capacity to very large numbers.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F670	10ns	45mA

ORDERING INFORMATION

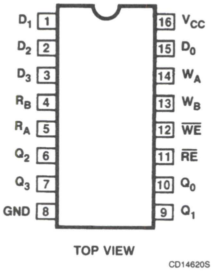
PACKAGE	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F670N
16-Pin Plastic SOL	N74F670D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$D_0 - D_3$	Data inputs	1.0/1.0	20μA/0.6mA
W_A, W_B	Write address inputs	1.0/1.0	20μA/0.6mA
R_A, R_B	Read address inputs	1.0/1.0	20μA/0.6mA
$\overline{WE}$	Write Enable input	1.0/1.0	20μA/0.6mA
$\overline{RE}$	Read Enable input	1.0/1.0	20μA/0.6mA
$Q_0 - Q_3$	Data outputs	150/40	3.0mA/24mA

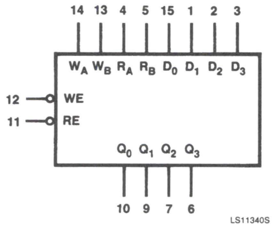
NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



D1 1
D2 2
D3 3
RB 4
RA 5
Q2 6
Q3 7
GND 8
16 VCC
15 D0
14 WA
13 WB
12 WE
11 RE
10 Q0
9 Q1
TOP VIEW
CD14620S

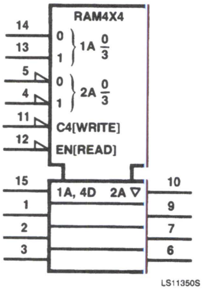
LOGIC SYMBOL



14 13 4 5 15 1 2 3
WA WB RA RB D0 D1 D2 D3
12 WE
11 RE
Q0 Q1 Q2 Q3
10 9 7 6
LS11340S

V_{CC} = Pin 16
GND = Pin 8

LOGIC SYMBOL (IEEE/IEC)



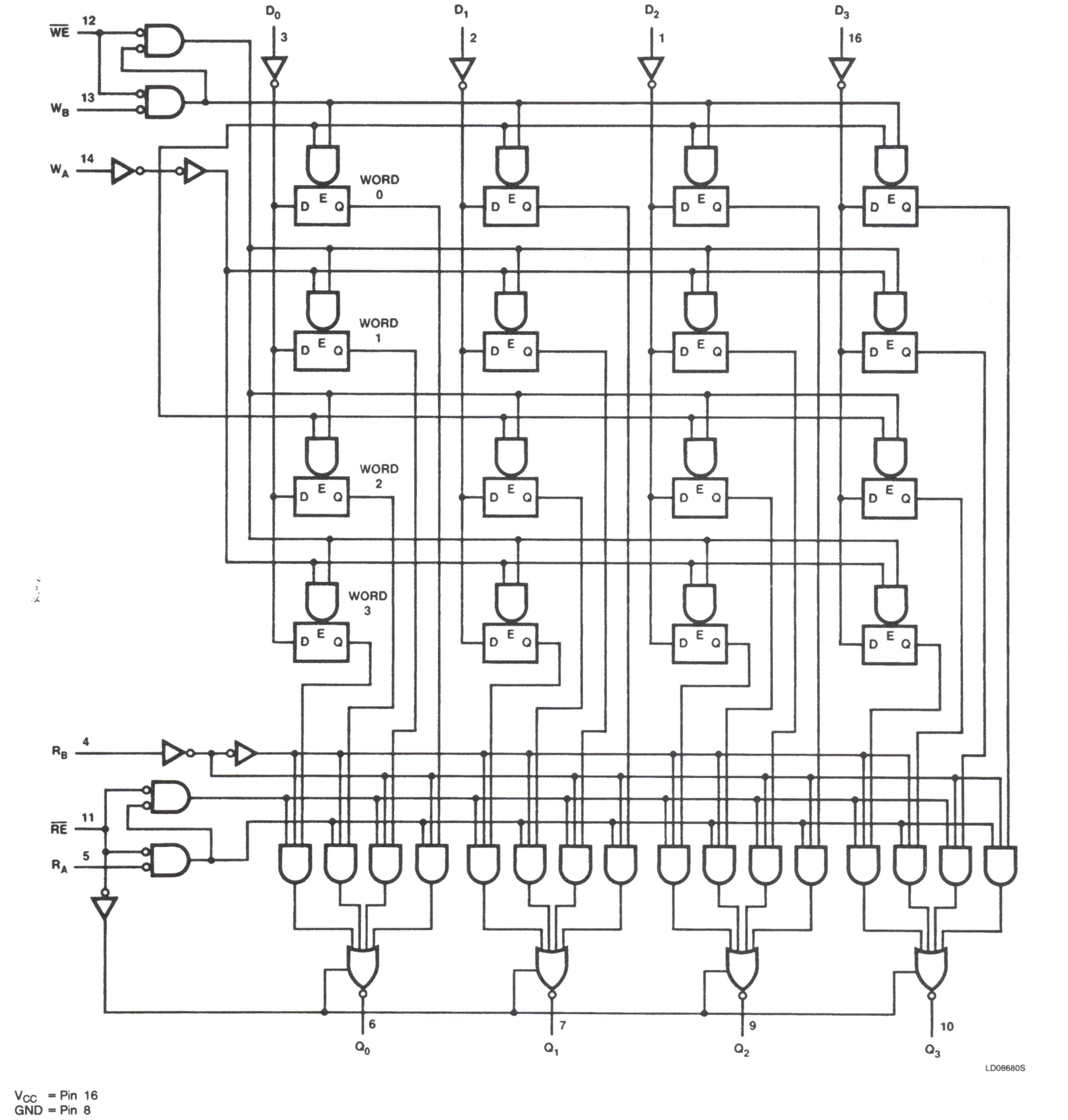
RAM4X4
14
13
0
1
1A 0/3
5
4
0
1
2A 0/3
11
12
C4[WRITE]
EN[READ]
15
1
2
3
1A, 4D
2A ▽
10
9
7
6
LS11350S

4 × 4 Register File (3-State)

FAST 74F670

Up to 128 devices can be stacked to increase the word size to 512 locations by tying the 3-State outputs together. Since the limiting factor for expansion is the output High current, further stacking is possible by tying pull-up resistors to the outputs to increase the I_{OH} current available. Design of the Read Enable signals for the stacked devices must ensure that there is no overlap in the Low levels which would cause more than one output to be active at the same time. Parallel expansion to generate n-bit words is accomplished by driving the Enable and Address inputs of each device in parallel.

LOGIC DIAGRAM



D0 3
D1 2
D2 1
D3 16
WE 12
WB 13
WA 14
WORD 0
WORD 1
WORD 2
WORD 3
D E Q
RB 4
RE 11
RA 5
6 Q0
7 Q1
9 Q2
10 Q3
LD08680S

VCC = Pin 16
GND = Pin 8
( ) = Pin Numbers

WRITE MODE FUNCTION TABLE

OPERATING MODE	INPUTS		INTERNAL LATCHES*
	$\overline{WE}$	D_n	
Write data	L	L	L
	L	H	H
Data latched	H	X	NC

NOTES:

H = High voltage level
L = Low voltage level
NC = No change
X = Don't care
* = The Write Address (W_A and W_B) to the "internal latches" must be stable while $\overline{WE}$ is Low for conventional operation.

READ MODE FUNCTION TABLE

OPERATING MODE	INPUT	INTERNAL LATCHES*	OUTPUT
	$\overline{RE}$		Q_n
Read	L	L	L
	L	H	H
Disabled	H	X	Z

NOTES:

H = High voltage level
L = Low voltage level
X = Don't care
Z = High-impedance (OFF) state
* = The selection of the "internal latches" by Read Address (R_A and R_B) are not constrained by $\overline{WE}$ or $\overline{RE}$ operation.

4 × 4 Register File (3-State) FAST 74F670

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−3	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]			LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = MIN V_{IL} = MAX V_{IH} = MIN	I_{OH} = MAX	±10% V_{CC}	2.4			V
				±5% V_{CC}	2.7	3.3		V
V_{OL}	Low-level output voltage	V_{CC} = MIN V_{IL} = MAX V_{IH} = MIN	I_{OL} = MAX	±10% V_{CC}		0.35	0.50	V
				±5% V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, $I_I = I_{IK}$				−0.73	−1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V					100	μA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V					−0.6	mA
I_{OZH}	OFF-state output current, High-level voltage applied	V_{CC} = MAX, V_O = 2.7V					50	μA
I_{OZL}	OFF-state output current, High-level voltage applied	V_{CC} = MAX, V_O = 0.5V					−50	μA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			−60		−150	mA
I_{CC}	Supply current (total)	V_{CC} = MAX				45	60	mA

NOTES:

1. For conditons shown as MIN or MAX, use the appropriate value under the recommended operating conditions for the applicable conditions.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			$T_A = +25°C$ $V_{CC} = 5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay R_A, R_B to Q_n	Waveform 2			10.0 10.0			ns
t_{PLH} t_{PHL}	Propagation delay $\overline{WE}$ to Q_n	Waveform 1			15.0 15.0			ns
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	Waveform 1			12.0 12.0			ns
t_{PZH} t_{PZL}	Output Enable time to High or Low Level	Waveform 3 Waveform 4			8.0 8.0			ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level	Waveform 3 Waveform 4			8.0 8.0			ns

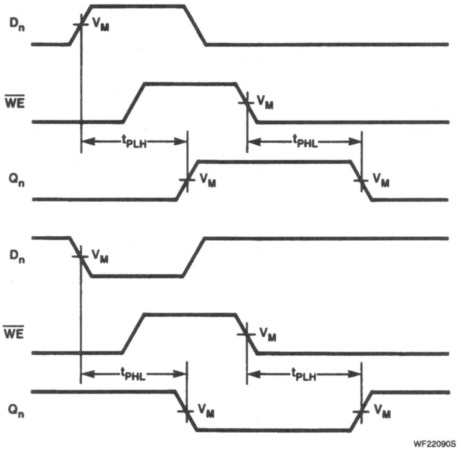
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			$T_A = +25°C$ $V_{CC} = 5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time D_n to positive going $\overline{WE}$	Waveform 2			3.0 3.0			ns
$t_h(H)$ $t_h(L)$	Hold time D_n to positive going $\overline{WE}$	Waveform 2			2.0 2.0			ns
$t_s(H)$ $t_s(L)$	Setup time W_A, W_B to negative going $\overline{WE}$[1]	Waveform 2			4.0 4.0			ns
$t_h(H)$ $t_h(L)$	Hold time W_A, W_B to positive going $\overline{WE}$[1]	Waveform 2			1.0 1.0			ns
$t_w(H)$ $t_w(L)$	$\overline{RE}$ Pulse width High or Low	Waveform 3			8.0 8.0			ns
$t_w(H)$ $t_w(L)$	$\overline{WE}$ Pulse width High or Low	Waveform 2 RE $\leqslant$ 0.8V			8.0 8.0			ns
t_{latch}	Latch time for new data[2]	Waveform 2			5.0			ns

NOTES:

1. Write Address setup time will protect the data written into the previous address. If protection of data in the previous address is not required, setup time for Write Address to $\overline{WE}$ can be ignored. Any address selection sustained for the final 30ns of the $\overline{WE}$ pulse and during hold time for Write Address to $\overline{WE}$ will result in data being written into that location.
2. Latch time is the time allowed for the internal output of the latch to assume the state of the new data. This is important only when attempting to read from location immediately after that location has received new data. This parameter is measured from the falling edge of WE to the rising or falling edge of R_A or R_B. $\overline{RE}$ must be Low.

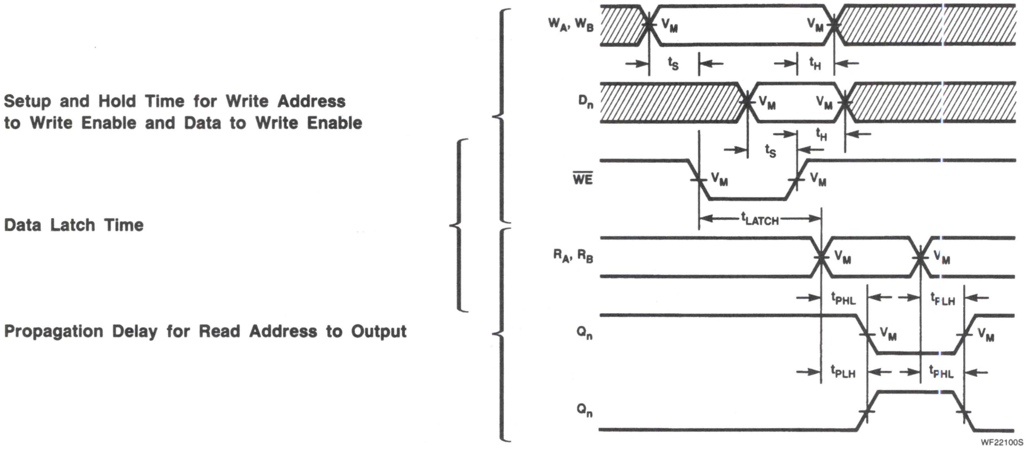
AC WAVEFORMS


D_n
V_M
$\overline{WE}$
V_M
t_{PLH}
t_{PHL}
Q_n
V_M
V_M
D_n
V_M
$\overline{WE}$
V_M
t_{PHL}
t_{PLH}
Q_n
V_M
V_M
WF22090S

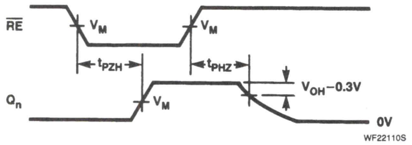
Waveform 1. Propagation Delay, Write Enable and Data to Outputs

NOTE: $V_M = 1.5V$.

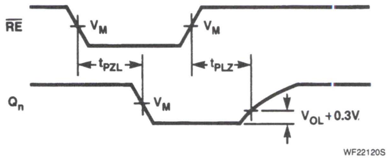
AC WAVEFORMS (Continued)


Setup and Hold Time for Write Address to Write Enable and Data to Write Enable
Data Latch Time
Propagation Delay for Read Address to Output
W_A, W_B
V_M
V_M
t_S
t_H
D_n
V_M
V_M
t_H
t_S
$\overline{WE}$
V_M
V_M
t_{LATCH}
R_A, R_B
V_M
V_M
t_{PHL}
t_{PLH}
Q_n
V_M
V_M
t_{PLH}
t_{PHL}
Q_n
WF22100S

Waveform 2. Data Setup and Hold Times, Write Address to Write Enable and Data to Write Enable, and Propagation Delay Read Address to Output


$\overline{RE}$
V_M
V_M
t_{PZH}
t_{PHZ}
$V_{OH}-0.3V$
Q_n
V_M
0V
WF22110S

Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time From High Level


$\overline{RE}$
V_M
V_M
t_{PZL}
t_{PLZ}
Q_n
V_M
$V_{OL}+0.3V$
WF22120S

Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time From Low Level

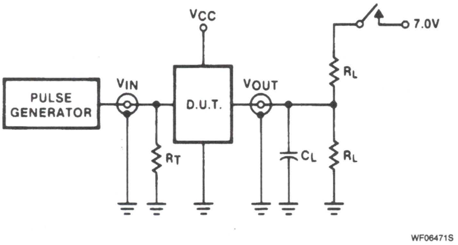
NOTE: $V_M = 1.5V$.

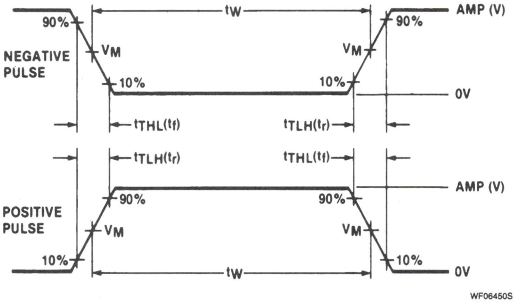
The shaded areas indicate when the input is permitted to change for predictable output performance.

4 × 4 Register File (3-State)

FAST 74F670

TEST CIRCUIT AND WAVEFORMS


VCC
7.0V
RL
VIN
VOUT
PULSE GENERATOR
D.U.T.
RT
CL
RL
WF06471S


tW
90%
AMP (V)
NEGATIVE PULSE
VM
VM
10%
10%
0V
tTHL(tf)
tTLH(tr)
tTLH(tr)
tTHL(tf)
AMP (V)
90%
90%
POSITIVE PULSE
VM
VM
10%
10%
0V
tW
WF06450S

Test Circuit for 3-State Outputs

$V_M = 1.5V$

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F673A

16-Bit Shift Register

16-Bit Shift Register (Serial-In/Serial-Parallel Out)
Preliminary Specification

FAST Products

FEATURES

- Serial-to-parallel converter
- 16-bit serial I/O shift register
- 16-bit parallel-out storage register
- Recirculating serial shifting
- Recirculating parallel transfer
- Common serial data I/O pin
- Available in 300mil-wide 24-Pin Slim DIP package

DESCRIPTION

The 'F673A contains a 16-bit serial-in/serial-out shift register and a 16-bit parallel-out storage register. A single pin serves either as an input for serial entry, or as a 3-State serial output. In the serial-out mode, the data recirculates in the shift register. By means of a separate clock, the contents of the shift register are transferred to the storage register for parallel outputting. The contents of the storage register can also be parallel loaded back into the shift register. A High-signal on the Chip Select input prevents both shifting and parallel transfer. The storage register may be cleared via STMR.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F673A	130MHz	106mA

ORDERING INFORMATION

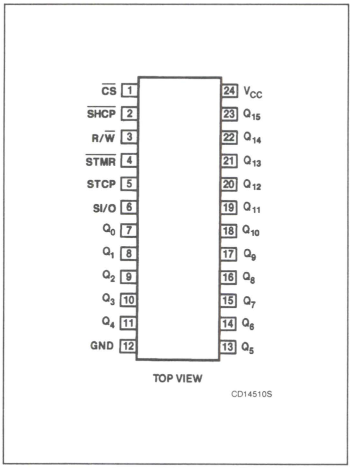
PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
24-Pin Plastic Slim DIP (300mil)	N74F673N
24-Pin Plastic SOL	N74F673D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$\overline{CS}$	Chip select input (active-Low)	1.0/1.0	20μA/0.6mA
$\overline{SHCP}$	Shift Clock Pulse input (active falling edge)	1.0/1.0	20μA/0.6mA
STMR	Store Master Reset input (active-Low)	1.0/1.0	20μA/0.6mA
STCP	Store clock pulse input	1.0/1.0	20μA/0.6mA
R/$\overline{W}$	Read/Write input	1.0/1.0	20μA/0.6mA
SI/O	Serial data input or	3.5/1.0	70μA/0.6mA
	3-State serial output	50/33	1.0mA/20mA
$Q_0 - Q_5$	Parallel data outputs	50/33	1.0mA/20mA

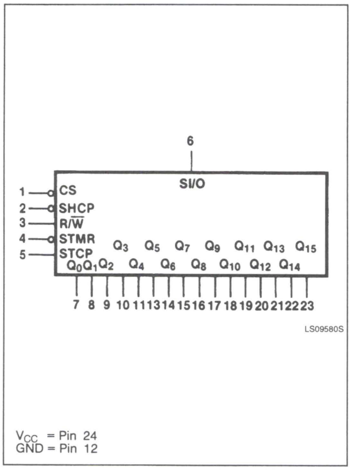
NOTE:
1. One (1.0) FAST unit load is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



$\overline{CS}$ 1
$\overline{SHCP}$ 2
R/$\overline{W}$ 3
$\overline{STMR}$ 4
STCP 5
SI/O 6
Q_0 7
Q_1 8
Q_2 9
Q_3 10
Q_4 11
GND 12
24 V_{CC}
23 Q_{15}
22 Q_{14}
21 Q_{13}
20 Q_{12}
19 Q_{11}
18 Q_{10}
17 Q_9
16 Q_8
15 Q_7
14 Q_6
13 Q_5
TOP VIEW
CD14510S

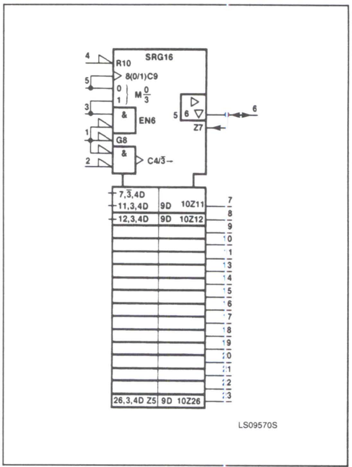
LOGIC SYMBOL



6
SI/O
1 CS
2 SHCP
3 R/$\overline{W}$
4 STMR
5 STCP
Q_0 Q_1 Q_2 Q_3 Q_4 Q_5 Q_6 Q_7 Q_8 Q_9 Q_{10} Q_{11} Q_{12} Q_{13} Q_{14} Q_{15}
7 8 9 10 11 13 14 15 16 17 18 19 20 21 22 23
LS09580S

V_{CC} = Pin 24
GND = Pin 12

LOGIC SYMBOL (IEEE/IEC)



SRG16
4
R10
8(0/1)C9
5
0
1
M $\frac{0}{3}$
3
&
EN6
1
G8
&
2
C4/$\overline{3}$→
5
6
6
Z7
7,$\overline{3}$,4D
11,3,4D
9D
10Z11
12,3,4D
9D
10Z12
26,3,4D Z5
9D
10Z26
7
8
9
10
11
13
14
15
16
17
18
19
20
21
22
23
LS09570S

16-Bit Shift Register

FAST 74F673A

FUNCTIONAL DESCRIPTION

The 16-bit shift register operates in one of four modes, as indicated in the Shift Register Operations Table. A High signal on the Chip Select ($\overline{CS}$) input prevents clocking and forces the Serial Input/Output (SI/O) 3-State buffer into the High-impedance state. During serial shift-out operations, the SI/O buffer is active (i.e., enabled) and the output data is also recirculated back into the shift register. When parallel loading the shift register from the storage register, serial shifting is inhibited.

The storage register has an asynchronous Master Reset ($\overline{STMR}$) input that overrides all other inputs and forces the $Q_0 - Q_{15}$ outputs Low. The storage register is in the Hold mode whether $\overline{CS}$ or the Read/Write ($R/\overline{W}$) input is High. With $\overline{CS}$ and $R/\overline{W}$ both Low, the storage register is parallel loaded from the shift register.

To prevent false clocking of the shift register, $\overline{SHCP}$ should be in the Low state during a Low-to-High transition of $\overline{CS}$. To prevent false clocking of the storage register, STCP should be Low during a High-to-Low transition of $\overline{CS}$ if $R/\overline{W}$ is Low, and should also be Low during a High-to-Low transition of $R/\overline{W}$ if $\overline{CS}$ is Low.

STORAGE REGISTER OPERATIONS TABLE

CONTROL INPUTS				OPERATING MODE
$\overline{STMR}$	$\overline{CS}$	$R/\overline{W}$	$\overline{STCP}$	
L	X	X	X	Reset; Outputs Low
H	H	X	X	Hold
H	X	H	X	Hold
H	L	L	↑	Parallel Load

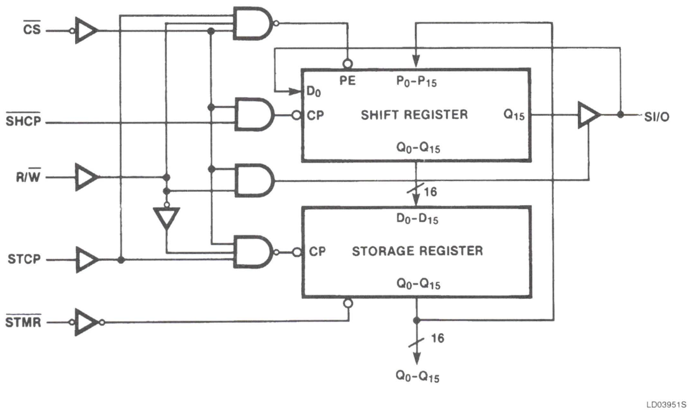
↑ = Low-to-High clock transition

SHIFT REGISTER OPERATIONS TABLE

CONTROL INPUTS				SI/O STATUS	OPERATING MODE
$\overline{CS}$	$R/\overline{W}$	$\overline{SHCP}$	STCP		
H	X	X	X	Hi-Z	Hold
L	L	↓	X	Data in	Serial load
L	H	↓	L	Data out	Serial output with recirculation
L	H	↓	H	Active	Parallel load; no shifting

H = High voltage level
L = Low voltage level
X = Don't care
↓ = High-to-Low clock transition

FUNCTIONAL BLOCK DIAGRAM



NOTE:
This diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		−0.5 to +7.0	V
V_{IN}	Input voltage		−0.5 to +7.0	V
I_{IN}	Input current		−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		−0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	SI/O	48	mA
		Q_0–Q_{15}	40	mA
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature range		−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	High-level output current	SI/O			−3.0	mA
		Q_0–Q_{15}			−1.0	mA
I_{OL}	Low-level input current	SI/O			24	mA
		Q_0–Q_{15}			20	mA
T_A	Operating free-air temperature		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage	$Q_0 - Q_{15}$	V_{CC} = MIN V_{IL} = MAX V_{IH} = MIN	$I_{OH} = -1mA$	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7	3.4		V
		SI/O		$I_{OH} = -3mA$	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.3		V
V_{OL}	High-level output voltage	$Q_0 - Q_{15}$	V_{CC} = MIN V_{IL} = MAX V_{IH} = MIN	$I_{OL} = 20mA$	±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
		SI/O		$I_{OL} = 24mA$	±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$				−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, $V_I = 7.0V$					100	μA
I_{IH}	High-level input current		V_{CC} = MAX, $V_I = 2.7V$					20	μA
I_{IL}	Low-level input current		V_{CC} = MAX, $V_I = 0.5V$					−20	μA
I_{OZH}	High-level input current	SI/O only	V_{CC} = MAX, $V_O = 2.7V$					50	μA
I_{OZL}	Low-level input current		V_{CC} = MAX, $V_O = 0.5V$					−50	μA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX			−60		−150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX						mA
		I_{CCL}						160	mA
		I_{CCZ}							mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at $V_{CC} = 5V$, $T_A = 25°C$.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of High-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequences of parameter tests, I_{OS} tests should be performed last.

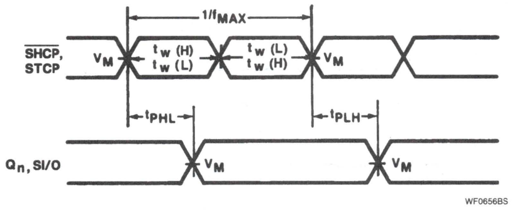
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	100	130				MHz
t_{PLH} t_{PHL}	Propagation delay STCP to Q_n	Waveform 1	7.5 9.5	13 16	18 22			ns
t_{PHL}	Propagation delay $\overline{STMR}$ to Q_n	Waveform 2	6.0	10	14			ns
t_{PLH} t_{PHL}	Propagation delay $\overline{SHCP}$ to SI/O	Waveform 1	4.5 5.0	8.0 9.0	11 12.5			ns
t_{PZH} t_{PZL}	Output enable time $\overline{CS}$ or R/$\overline{W}$ to SI/O	Waveform 5 Waveform 6	3.0 3.0	5.0 5.0	7.0 7.0			ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{CS}$ or R/$\overline{W}$ to SI/O	Waveform 5 Waveform 6	3.0 3.0	5.0 5.0	7.0 7.0			ns

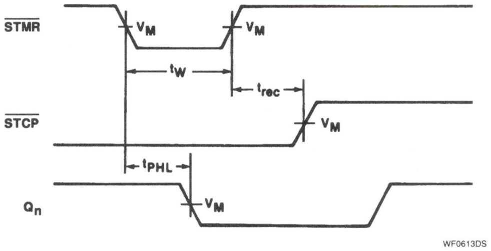
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{CS}$ or R/$\overline{W}$ to STCP	Waveform 3	7.0 7.0					ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{CS}$ or R/$\overline{W}$ to STCP		0 0					ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low SI/O to $\overline{SHCP}$	Waveform 3	3.0 3.0					ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low SI/O to $\overline{SHCP}$		0 0					ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{CS}$ or R/$\overline{W}$ to $\overline{SHCP}$	Waveform 3	5.0 5.0					ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{CS}$ or R/$\overline{W}$ to $\overline{SHCP}$		0 0					ns
$t_w(H)$ $t_w(L)$	$\overline{SHCP}$ pulse width, High or Low	Waveform 1	4.0 5.0					ns
$t_w(H)$ $t_w(L)$	STCP pulse width, High or Low	Waveform 1	5.0 10					ns
$t_w(L)$	$\overline{STMR}$ pulse width Low	Waveform 2	7.0					ns
t_{rec}	Recovery time $\overline{STMR}$ to STCP	Waveform 2	10					ns

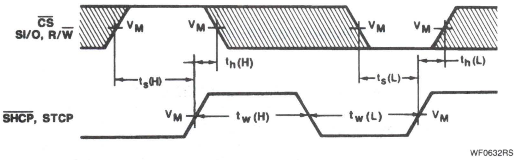
AC WAVEFORMS


1/fMAX
SHCP, STCP
VM
tw (H)
tw (L)
tw (L)
tw (H)
VM
tPHL
tPLH
Qn, SI/O
VM
VM
WF0656BS

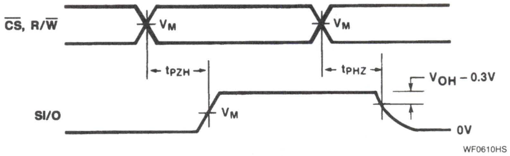
Waveform 1. Propagation Delay, Clock Input to Output, Clock Widths and Maximum Clock Frequency


STMR
VM
VM
tW
trec
STCP
VM
tPHL
Qn
VM
WF0613DS

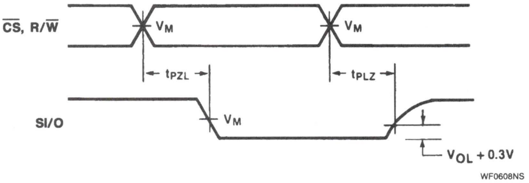
Waveform 2. Store Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time


CS
SI/O, R/W
VM
VM
VM
VM
th(H)
ts(H)
ts(L)
th(L)
SHCP, STCP
VM
tw(H)
tw(L)
VM
WF0632RS

Waveform 3. Data and Select Setup and Hold Times


CS, R/W
VM
VM
tPZH
tPHZ
VOH – 0.3V
SI/O
VM
0V
WF0610HS

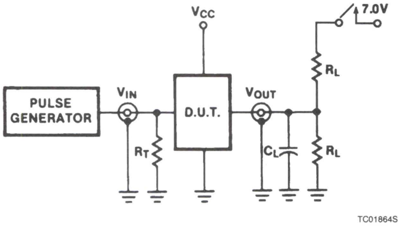
Waveform 4. 3-State Output Enable Time to High level and Output Disable Time From High Level


CS, R/W
VM
VM
tPZL
tPLZ
SI/O
VM
VOL + 0.3V
WF0608NS

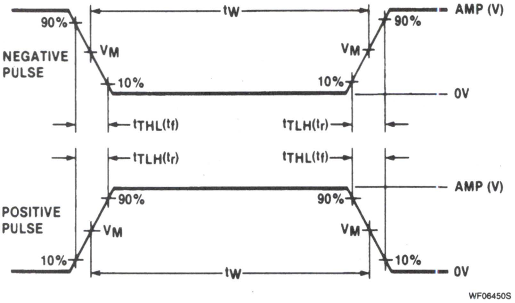
Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time From Low Level

NOTE: $V_M = 1.5V$.
The shaded area indicates when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS


VCC
7.0V
RL
PULSE GENERATOR
VIN
D.U.T.
VOUT
RT
CL
RL
TC01864S

Test Circuit for 3-State and Totem-Pole Outputs


90%
tW
90%
AMP (V)
NEGATIVE PULSE
VM
VM
10%
10%
0V
tTHL(tf)
tTLH(tr)
tTLH(tr)
tTHL(tf)
AMP (V)
90%
90%
POSITIVE PULSE
VM
VM
10%
10%
0V
tW
WF06450S

$V_M = 1.5V$

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS:

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F674

16-Bit Shift Register

16-Bit Shift Register, Serial-Parallel-In/Serial-Out (3-State)
Preliminary Specification

FAST Products

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F674	140MHz	53mA

FEATURES

- **16-bit serial I/O shift register**
- **16-bit parallel-in/serial-out converter**
- **Recirculating serial shifting**
- **Common serial data I/O pin**
- **Available in 300mil-wide 24-pin Slim DIP package**

DESCRIPTION

The 'F674 is a 16-bit shift register with serial and parallel load capability and serial output. A single pin serves alternately as an input for serial entry or as a 3-State serial output. In the Serial-out mode the data recirculates in the register. Chip Select, Read/Write and Mode inputs provide control flexibility.

FUNCTIONAL DESCRIPTION

The 16-bit shift register operates in one of four modes, as indicated in the Shift Register Operations Table.

Hold — a High signal on the Chip Select ($\overline{CS}$) input prevents clocking and forces the Serial Input/Output (SI/O) 3-State buffer into the high-impedance state.

ORDERING INFORMATION

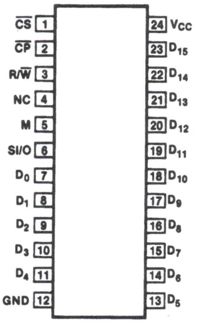
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C
24-Pin Plastic Slim DIP (300mil)	N74F674N
24-Pin Plastic SOL	N74F674D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$D_0 - D_{15}$	Parallel data inputs	1.0/1.0	20μA/0.6mA
$\overline{CS}$	Chip Select input (active-Low)	1.0/1.0	20μA/0.6mA
$\overline{CP}$	Clock Pulse input (active-Low)	1.0/1.0	20μA/0.6mA
M	Mode select input	1.0/1.0	20μA/0.6mA
R/$\overline{W}$	Read/Write input	1.0/1.0	20μA/0.6mA
SI/O	3-State serial data input or	3.75/1.0	70μA/0.6mA
	3-State serial output	150/33	3.0mA/20mA

NOTE:
1. One (1.0) FAST unit load is defined as: 20μA in the High state and 0.6mA in the Low state.

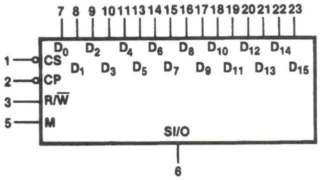
PIN CONFIGURATION



$\overline{CS}$ 1
$\overline{CP}$ 2
R/$\overline{W}$ 3
NC 4
M 5
SI/O 6
D_0 7
D_1 8
D_2 9
D_3 10
D_4 11
GND 12
13 D_5
14 D_6
15 D_7
16 D_8
17 D_9
18 D_{10}
19 D_{11}
20 D_{12}
21 D_{13}
22 D_{14}
23 D_{15}
24 V_{CC}

CD07891S

LOGIC SYMBOL

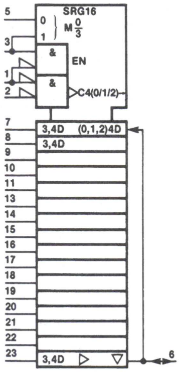


7 8 9 10 11 13 14 15 16 17 18 19 20 21 22 23
D_0 D_2 D_4 D_6 D_8 D_{10} D_{12} D_{14}
D_1 D_3 D_5 D_7 D_9 D_{11} D_{13} D_{15}
1 CS
2 CP
3 R/$\overline{W}$
5 M
SI/O
6

LS09601S

V_{CC} = Pin 24
GND = Pin 12

LOGIC SYMBOL (IEEE/IEC)



SRG16
0
1
M $\frac{0}{3}$
5
3
1
2
&
EN
&
C4(0/1/2)
7
8
9
10
11
13
14
15
16
17
18
19
20
21
22
23
3,4D
(0,1,2)4D
3,4D
3,4D
6

LS09590S

Serial Load — data present on the SI/O pin shifts into the register on the falling edge of $\overline{CP}$. Data enters the Q_0 position and shifts toward Q_{15} on successive clocks.

Serial Output — the SI/O 3-State buffer is active and the register contents are shifted out from Q_{15} and simultaneously shifted back into Q_0.

Parallel Load — data present on $P_0 - P_{15}$ are entered into the register on the falling edge of CP. The SI/O 3-State buffer is active and represents the Q_{15} output.

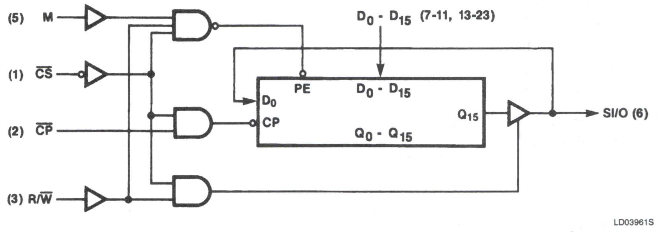
To prevent false clocking, CP must be Low during a Low-to-High transition of $\overline{CS}$.

STORAGE REGISTER OPERATIONS TABLE

CONTROL INPUTS				SI/O STATUS	OPERATING MODE
$\overline{CS}$	R/$\overline{W}$	M	$\overline{CP}$		
H L	X L	X X	X X	Hi-Z Data in	Hold Serial load
L	H	L	↓	Data out	Serial output with recirculation
L	H	H	↓	Active	Parallel load; no shifting

H = High voltage level
L = Low voltage level
X = Don't care
↓ = High-to-Low clock transition

LOGIC DIAGRAM



V_{CC} = Pin 24
GND = Pin 12
( ) = Pin numbers

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−3	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

16-Bit Shift Register

FAST 74F674

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]			LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = MAX	±10%V_{CC}	2.4			V
				±5%V_{CC}	2.7	3.3		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = MAX	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, $I_I = I_{IK}$				−0.73	−1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V					100	μA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V					−0.6	mA
I_{OZH}	OFF-state output current, High-level voltage applied	V_{CC} = MAX, V_O = 2.7V					70	μA
I_{OZL}	OFF-state output current Low-level voltage applied	V_{CC} = MAX, V_O = 0.5V					−600	μA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			−60		−150	mA
I_{CC}	Supply current (total)	V_{CC} = MAX				53	84	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

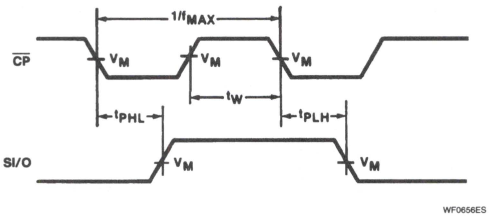
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C V_{CC} = +5.0V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = +5.0V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum input frequency	Waveform 1	100	140				MHz
t_{PLH}	Propagation delay	Waveform 1	4.5	8.0	11			ns
t_{PHL}	$\overline{CP}$ to SI/O		5.0	9.0	12.5			
t_{PZH}	Output enable time	Waveform 3	3.0	5.0	7.0			ns
t_{PZL}	$\overline{CS}$ or R/$\overline{W}$ to SI/O	Waveform 4	3.0	5.0	7.0			
t_{PHZ}	Output disable time	Waveform 3	3.0	5.0	7.0			ns
t_{PLZ}	$\overline{CS}$ or R/$\overline{W}$ to SI/O	Waveform 4	3.0	5.0	7.0			

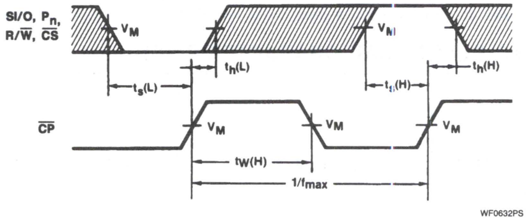
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low SIO to $\overline{CP}$	Waveform 2	7.0 7.0					ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low SI/O to $\overline{CP}$	Waveform 2	0 0					ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low P_n to $\overline{CP}$	Waveform 2	3.0 3.0					ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low P_n to $\overline{CP}$	Waveform 2	0 0					ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $R/\overline{W}$ or $\overline{CS}$ to $\overline{CP}$	Waveform 3	5.0 5.0					ns
$t_h(H)$	Hold time, High or Low $R/\overline{W}$ or $\overline{CS}$ to $\overline{CP}$	Waveform 3	0 0					ns
$t_w(H)$ $t_w(L)$	$\overline{CP}$ pulse width High or Low	Waveform 1	4.0 5.0					ns

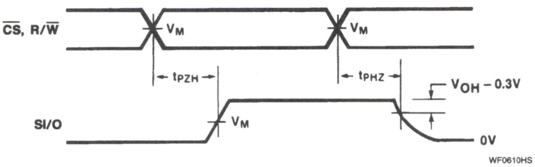
AC WAVEFORMS


$\overline{CP}$
1/f_MAX
V_M
V_M
V_M
t_W
t_PHL
t_PLH
SI/O
V_M
V_M
WF0656ES

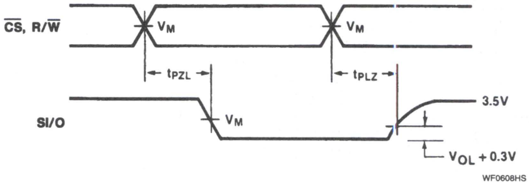
Waveform 1. Clock to Output Delays and Clock Pulse Width


SI/O, P_n, R/W̄, C̄S̄
V_M
V_M
t_h(L)
t_h(H)
t_s(L)
t_s(H)
$\overline{CP}$
V_M
V_M
V_M
tw(H)
1/f_max
WF0632PS

Waveform 2. Data Setup and Hold Times


C̄S̄, R/W̄
V_M
V_M
t_PZH
t_PHZ
V_OH − 0.3V
SI/O
V_M
0V
WF0610HS

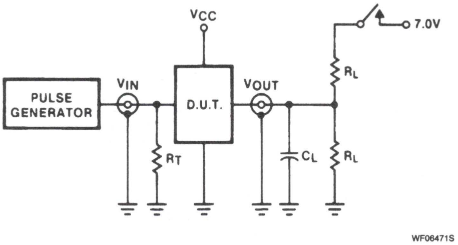
Waveform 3. 3-State Output Enable Time to Low Level and Output Disable Time From Low Level


C̄S̄, R/W̄
V_M
V_M
t_PZL
t_PLZ
3.5V
SI/O
V_M
V_OL + 0.3V
WF0608HS

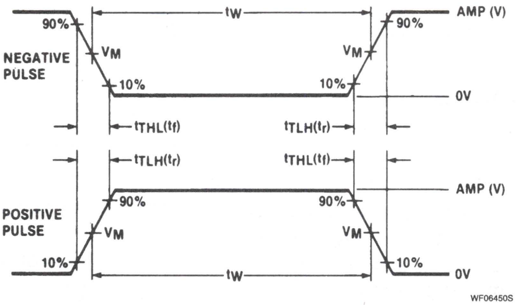
Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time From High Level

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS


VCC
7.0V
RL
PULSE GENERATOR
VIN
D.U.T.
VOUT
RT
CL
RL
WF06471S

Test Circuit for 3-State Outputs


tW
AMP (V)
90%
90%
NEGATIVE PULSE
VM
VM
10%
10%
0V
tTHL(tf)
tTLH(tr)
tTLH(tr)
tTHL(tf)
AMP (V)
90%
90%
POSITIVE PULSE
VM
VM
10%
10%
tW
0V
WF06450S

$V_M = 1.5V$
Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS
R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Signetics

FAST 74F675

16-Bit Shift Register

16-Bit Shift Registers (Serial-In/Serial-Parallel Out)
Preliminary Specification

FAST Products

FEATURES

- Serial-to-parallel converter
- 16-bit serial I/O shift register
- 16-bit parallel-out storage register
- Recirculating parallel transfer
- Expandable for longer words
- Available in 300mil-wide 24-pin Slim DIP package

DESCRIPTION

The 'F675 contains a 16-bit serial-in/serial-out shift register and a 16-bit parallel-out storage register. Separate serial input and output pins are provided for expansion to longer words. By means of a separate clock, the contents of the shift register are transferred to the storage register. The contents of the storage register can also be loaded back into the shift register. A High signal on the Chip Select input prevents both shifting and parallel loading.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F675	130MHz	106mA

ORDERING INFORMATION

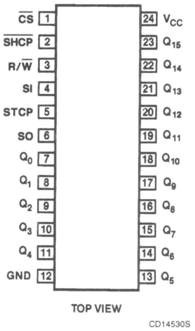
PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
24-Pin Plastic Slim DIP (300mil)	N74F675N
24-Pin Plastic SOL	N74F675D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
SI	Serial data input	1.0/1.0	20µA/0.6mA
$\overline{CS}$	Chip Select input (active-Low)	1.0/1.0	20µA/0.6mA
$\overline{SHCP}$	Shift clock pulse input (active falling edge)	1.0/1.0	20µA/0.6mA
STCP	Store clock pulse input (active rising edge)	1.0/1.0	20µA/0.6mA
R/$\overline{W}$	Read/Write input	1.0/1.0	20µA/0.6mA
SO	Serial data output	50/33	1.0mA/20mA
Q_0-Q_{15}	Parallel data outputs	50/33	1.0mA/20mA

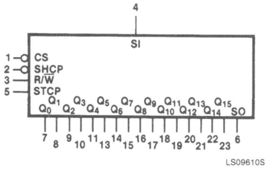
NOTE:
1. One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



$\overline{CS}$ 1
$\overline{SHCP}$ 2
R/$\overline{W}$ 3
SI 4
STCP 5
SO 6
Q_0 7
Q_1 8
Q_2 9
Q_3 10
Q_4 11
GND 12
24 V_{CC}
23 Q_{15}
22 Q_{14}
21 Q_{13}
20 Q_{12}
19 Q_{11}
18 Q_{10}
17 Q_9
16 Q_8
15 Q_7
14 Q_6
13 Q_5
TOP VIEW
CD14530S

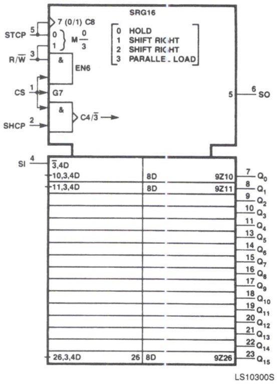
LOGIC SYMBOL



4
SI
1 CS
2 SHCP
3 R/W
5 STCP
Q_0 Q_1 Q_2 Q_3 Q_4 Q_5 Q_6 Q_7 Q_8 Q_9 Q_{10} Q_{11} Q_{12} Q_{13} Q_{14} Q_{15} SO
7 8 9 10 11 13 14 15 16 17 18 19 20 21 22 23 6
LS09610S

V_{CC} = Pin 24
GND = Pin 12

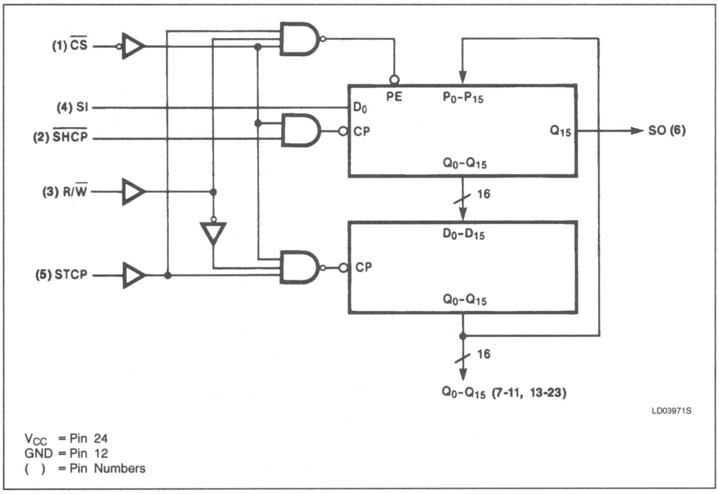
LOGIC SYMBOL (IEEE/IEC)



SRG16
STCP 5
R/$\overline{W}$ 3
CS 1
SHCP 2
7 (0/1) C8
0
1
M $\frac{0}{3}$
0 HOLD
1 SHIFT RIGHT
2 SHIFT RIGHT
3 PARALLEL LOAD
&
EN6
G7
&
C4/$\overline{3}$
5
6 SO
SI 4
$\overline{3}$,4D
10,3,4D
11,3,4D
26,3,4D
26
8D
8D
8D
9Z10
9Z11
9Z26
7 Q_0
8 Q_1
9 Q_2
10 Q_3
11 Q_4
13 Q_5
14 Q_6
15 Q_7
16 Q_8
17 Q_9
18 Q_{10}
19 Q_{11}
20 Q_{12}
21 Q_{13}
22 Q_{14}
23 Q_{15}
LS10300S

16-Bit Shift Register FAST 74F675

FUNCTIONAL BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The 16-bit shift register operates in one of four modes, as determined by the signals applied to the Chip Select ($\overline{CS}$), Read/Write (R/$\overline{W}$) and Store Clock Pulse (STCP) inputs. State changes are indicated by the falling edge of the Shift Clock Pulse ($\overline{SHCP}$). In the Shift-right mode, data enters D_0 from the Serial Input (SI) pin and exits from Q_{15} via the Serial Data Output (SO) pin. In the Parallel Load mode, data from the storage register outputs enter the shift register and serial shifting is inhibited.

The storage register is in the Hold mode when either $\overline{CS}$ or R/$\overline{W}$ is High. With $\overline{CS}$ and R/$\overline{W}$ both Low, the storage register is parallel loaded from the shift register on the rising edge of STCP.

To prevent false clocking of the shift register, $\overline{SHCP}$ should be in the Low state during a Low-to-High transition of $\overline{CS}$. To prevent false clocking of the storage register, STCP should be Low during a High-to-Low transition of $\overline{CS}$ if R/$\overline{W}$ is Low, and should also be Low during a High-to-Low transition of R/$\overline{W}$ if $\overline{CS}$ is Low.

REGISTER OPERATIONS TABLE

CONTROL INPUTS				OPERATING MODE
$\overline{CS}$	R/$\overline{W}$	$\overline{SHCP}$	$\overline{STCP}$	
H	X	X	X	Hold
L	L	↓	X	Shift right
L	H	↓	L	Shift right
L	H	↓	H	Parallel load; No shifting

STORAGE REGISTER OPERATIONS TABLE

INPUTS			OPERATING MODE
$\overline{CS}$	R/$\overline{W}$	$\overline{STCP}$	
H	X	X	Hold
L	H	X	Hold
L	L	↑	Parallel load

H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-to-High clock transition
↓ = High-to-Low clock transition

16-Bit Shift Register FAST 74F675

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature range	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = 1mA	±10%V_{CC}	2.5			V
			±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = 20mA	±10%V_{CC}		0.35	0.50	V
			±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V				−0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current (total)	V_{CC} = MAX			106	160	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of High-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

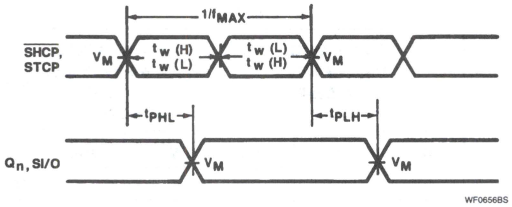
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	100	130				MHz
t_{PLH} t_{PHL}	Propagation delay STCP to Q_n	Waveform 1	7.5 9.5	13 16	18 22			ns
t_{PLH} t_{PHL}	Propagation delay SHCP to SO	Waveform 1	4.5 5.0	8.0 9.0	11 12.5			ns

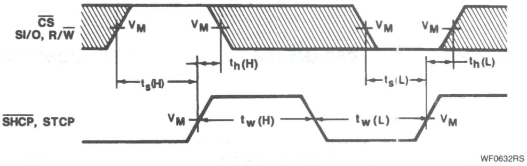
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{CS}$ or R/$\overline{W}$ to STCP	Waveform 2	7.0 7.0					ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{CS}$ or R/$\overline{W}$ to STCP	Waveform 2	0 0					ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low SI to $\overline{SHCP}$	Waveform 2	3.0 3.0					ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low SI to $\overline{SHCP}$	Waveform 2	0 0					ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low R/$\overline{W}$ or $\overline{CS}$ to $\overline{SHCP}$	Waveform 2	5.0 5.0					ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low R/$\overline{W}$ or $\overline{CS}$ to $\overline{SHCP}$	Waveform 2	0 0					ns
$t_w(H)$ $t_w(L)$	$\overline{SHCP}$ pulse width, High or Low	Waveform 1	4.0 5.0					ns
$t_w(H)$ $t_w(L)$	STCP pulse width, High or Low	Waveform 1	5.0 10					ns

AC WAVEFORMS


1/fMAX
SHCP, STCP
VM
tw (H)
tw (L)
tw (L)
tw (H)
VM
tPHL
tPLH
Qn, SI/O
VM
VM
WF06565BS

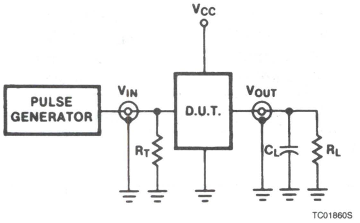
Waveform 1. Propagation Delay, Clock Input to Output, Clock Widths and Maximum Clock Frequency


CS
SI/O, R/W
VM
VM
VM
VM
th(H)
th(L)
ts(H)
ts(L)
SHCP, STCP
VM
tw (H)
tw (L)
VM
WF0632RS

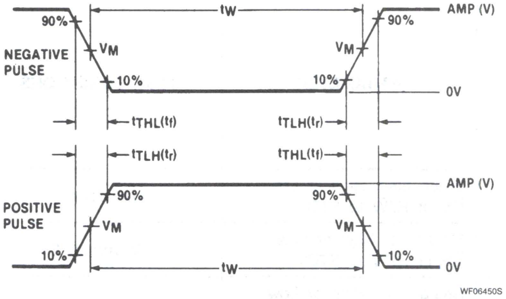
Waveform 2. Data and Select Setup and Hold Times

NOTE: $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS


VCC
PULSE GENERATOR
VIN
D.U.T.
VOUT
RT
CL
RL
TC01860S

Test Circuit for Totem-Pole Outputs


tw
90%
AMP (V)
NEGATIVE PULSE
VM
VM
10%
10%
90%
0V
tTHL(tf)
tTLH(tr)
tTLH(tr)
tTHL(tf)
AMP (V)
90%
90%
POSITIVE PULSE
VM
VM
10%
10%
tw
0V
WF06450S

$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F676
Shift Register

'F676 16-Bit Shift Register
Product Specification

FAST Products

FEATURES

- **16-bit parallel-to-serial conversion**
- **16-bit serial-in, serial-out**
- **Chip Select control**
- **Power supply current 48mA typical**
- **Shift frequency 110MHz typical**
- **Available in 300mil-wide 24-pin Slim DIP package**

DESCRIPTION

The 'F676 contains 16 flip-flops with provision for synchronous parallel or serial entry and serial output. When the Mode (M) input is High, information present on the parallel data ($D_0 - D_{15}$) inputs is entered on the falling edge of the Clock Pulse ($\overline{CP}$) input signal. When M is Low, data is shifted out of the most significant bit position while information present on the Serial (SI) input shifts into the least significant bit position. A High signal on the Chip Select ($\overline{CS}$) input prevents both parallel and serial operations.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F676	110MHz	48mA

ORDERING INFORMATION

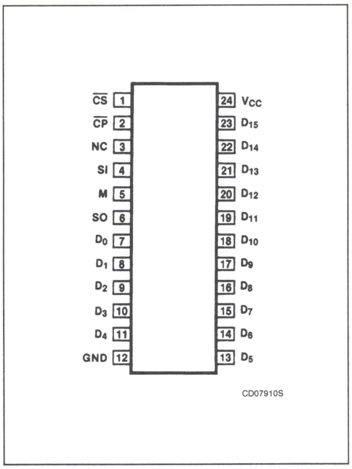
PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
24-Pin Plastic Slim DIP (300mil)	N74F676N
24-Pin Plastic SOL	N74F676D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

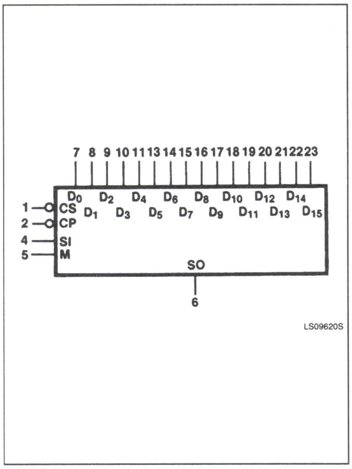
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$\overline{CS}$	Chip Select input (active-Low)	1.0/1.0	20μA/0.6mA
SI	Serial data input	1.0/1.0	20μA/0.6mA
M	Mode select input	1.0/1.0	20μA/0.6mA
$D_0 - D_{15}$	Parallel data inputs	1.0/1.0	20μA/0.6mA
$\overline{CP}$	Clock Pulse input (active falling edge)	1.0/1.0	20μA/0.6mA
SO	Serial data output	50/33	1mA/20mA

NOTE:
1. One (1.0) FAST unit load is defined as: 20μA in the High state and 0.6mA in the Low state.

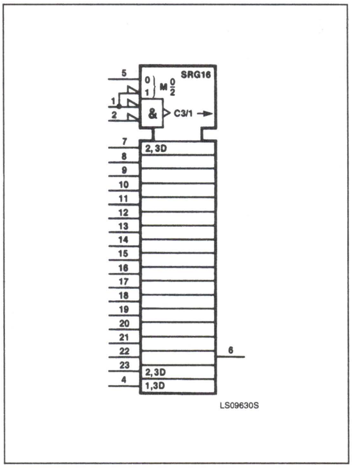
PIN CONFIGURATION


CS 1
CP 2
NC 3
SI 4
M 5
SO 6
D0 7
D1 8
D2 9
D3 10
D4 11
GND 12
24 VCC
23 D15
22 D14
21 D13
20 D12
19 D11
18 D10
17 D9
16 D8
15 D7
14 D6
13 D5
CD07910S

LOGIC SYMBOL


7 8 9 10 11 13 14 15 16 17 18 19 20 21 22 23
D0 D2 D4 D6 D8 D10 D12 D14
D1 D3 D5 D7 D9 D11 D13 D15
1 CS
2 CP
4 SI
5 M
SO
6
LS09620S

LOGIC SYMBOL (IEEE/IEC)


SRG16
5
0
1
M 0/2
1
2
&
C3/1
7
2,3D
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
2,3D
4
1,3D
6
LS09630S

Shift Register FAST 74F676

The 16-bit shift register operates in one of three modes, as indicated in the Shift Register Operations Table.

HOLD — a High signal on the Chip Select ($\overline{CS}$) input prevents clocking, and data is stored in the 16 registers.

Shift/Serial Load — data present on the SI pin shifts into the register on the falling edge of $\overline{CP}$. Data enters the Q_0 position and shifts toward Q_{15} on successive clocks, finally appearing on the SO pin.

Parallel Load — data present on $P_0 - P_{15}$ are entered into the register on the falling edge of $\overline{CP}$. The SO output represents the Q_{15} register output.

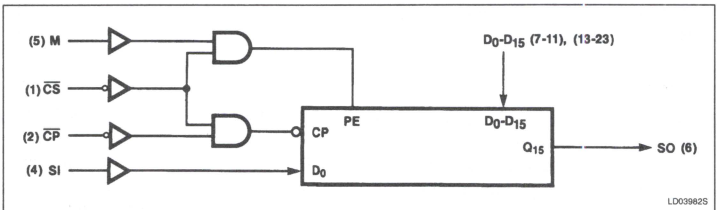
To prevent false clocking, $\overline{CP}$ must be Low during a Low-to-High transition of $\overline{CS}$.

FUNCTION TABLE

CONTROL INPUT			OPERATING MODE
$\overline{CS}$	M	$\overline{CP}$	
H	X	X	Hold
L	L	↓	Shift/serial load
L	H	↓	Parallel load

H = High voltage level
L = Low voltage level
X = Don't care
↓ = High-to-Low clock transition

LOGIC DIAGRAM



V_{CC} = Pin 24
GND = Pin 12
( ) = Pin numbers

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

Shift Register FAST 74F676

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.5			V
			±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.35	0.50	V
			±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, $I_I = I_{IK}$			−0.73	−1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V				−0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current (total)	V_{CC} = MAX			48	72	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

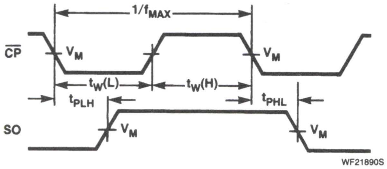
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C V_{CC} = +5.0V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = +5.0V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	100	110		90		MHz
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}$ to SO	Waveform 1	4.5 5.0	8.0 7.0	11 12.5	4.5 5.0	12 13.5	ns

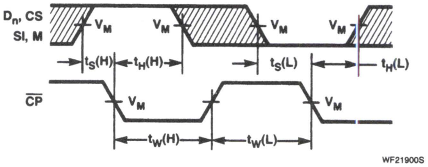
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low SI to $\overline{CP}$	Waveform 2	4.0 4.0			4.0 4.0		
$t_h(H)$ $t_h(L)$	Hold time, High or Low SI to $\overline{CP}$	Waveform 2	4.0 4.0			4.0 4.0		
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n $\overline{CP}$	Waveform 2	3.0 3.0			3.0 3.0		
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to $\overline{CP}$	Waveform 2	4.0 4.0			4.0 4.0		
$t_s(H)$ $t_s(L)$	Setup time, High or Low M to $\overline{CP}$	Waveform 2	8.0 8.0			8.0 8.0		
$t_h(H)$ $t_h(L)$	Hold time, High or Low M to $\overline{CP}$	Waveform 2	2.0 2.0			2.0 2.0		
$t_s(L)$	Setup time, Low $\overline{CS}$ to $\overline{CP}$	Waveform 2	10.0			10.0		
$t_h(H)$	Hold time, High $\overline{CS}$ to $\overline{CP}$	Waveform 2	10.0			10.0		
$t_w(H)$ $t_w(L)$	$\overline{CP}$ pulse width High or Low	Waveform 1	4.0 6.0			4.0 6.0		

AC WAVEFORMS



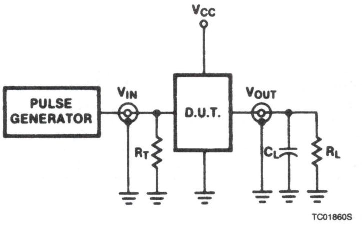
Waveform 1. Propagation Delay, Clock Input to Output, Clock Widths and Maximum Clock Frequency



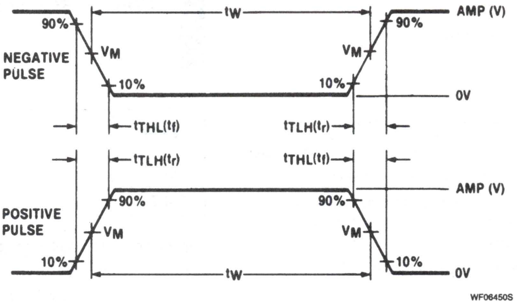
Waveform 2. Propagation Delay for Data to Output, Data and Select Setup, and Hold Times

NOTE: $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS


V_{CC}
PULSE GENERATOR
V_{IN}
D.U.T.
V_{OUT}
R_T
C_L
R_L
TC01860S

Test Circuit for Totem-Pole Outputs


t_W
90%
AMP (V)
NEGATIVE PULSE
V_M
10%
0V
$t_{THL}(t_f)$
$t_{TLH}(t_r)$
$t_{TLH}(t_r)$
$t_{THL}(t_f)$
POSITIVE PULSE
V_M
90%
10%
AMP (V)
0V
t_W
WF06450S

$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS
R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST Products

FAST 74F711, 74F712

74F711 Quint 2-to-1 Data Selector Multiplexer (3-State)
74F712 Quint 3-to-1 Data Selector Multiplexer
Preliminary Specification

FEATURES for 74F711

- **Consists of five 2-to-1 multiplexers**
- **Equivalent to two 'F257s**
- **Designed for address multiplexing of dynamic RAM and other applications**
- **3-State outputs sink 64mA**

FEATURES for 74F712

- **Consists of five 3-to-1 multiplexers**
- **Equivalent to four 'F157s**
- **Designed for address multiplexing of dynamic RAM and other applications**
- **Outputs sink 64mA**

DESCRIPTION

The 'F711 consists of five 2-to-1 multiplexers designed for address multiplexing dynamic RAMs and other multiplexing applications. The 'F711 has a common select(S) input and an Output Enable ($\overline{OE}$) to control the 3-State outputs. The 3-State outputs source 15mA and sink 64mA.

The 'F112 consists of five 3-to-1 multiplexers designed for address multiplexing dynamic RAMs and other multiplexing applications. The 'F712 has two select (S0, S1) inputs to determine which set of five inputs will be propagated to the five outputs.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F711	5.5ns	12mA
74F712	6.0ns	24mA

ORDERING INFORMATION

PACKAGES		COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
Plastic	DIP	N74F711N
	Slim DIP	N74F712N
Plastic	20-Pin SOL	N74F711D
	24-Pin SOL	N74F712D

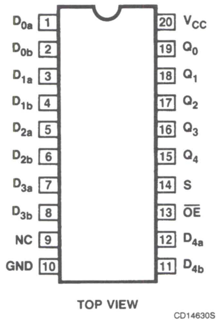
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

TYPE	PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
'F711	D_{na}, D_{nb}	Data inputs	1.0/2.0	20µA/1.2mA
	S	Select input	1.0/1.0	20µA/0.6mA
	$\overline{OE}$	Output Enable input	1.0/1.0	20µA/0.6mA
	$Q_0 - Q_4$	Data outputs	750/106.7	15mA/64mA
'F712	D_{na}, D_{nb}, D_{nc}	Data inputs	1.0/1.0	20µA/0.6mA
	S_0, S_1	Select inputs	1.0/1.0	20µA/0.6mA
	$Q_0 - Q_4$	Data outputs	750/106.7	15mA/64mA

NOTE:
1. One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION

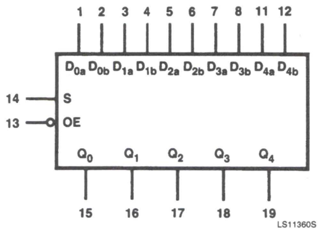
'F711



D_{0a} 1
D_{0b} 2
D_{1a} 3
D_{1b} 4
D_{2a} 5
D_{2b} 6
D_{3a} 7
D_{3b} 8
NC 9
GND 10
20 V_{CC}
19 Q_0
18 Q_1
17 Q_2
16 Q_3
15 Q_4
14 S
13 $\overline{OE}$
12 D_{4a}
11 D_{4b}
TOP VIEW
CD14630S

LOGIC SYMBOL

'F711

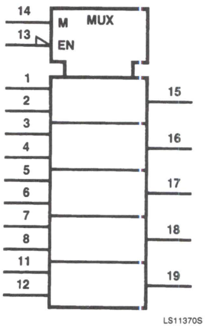


1 2 3 4 5 6 7 8 11 12
D_{0a} D_{0b} D_{1a} D_{1b} D_{2a} D_{2b} D_{3a} D_{3b} D_{4a} D_{4b}
14 S
13 OE
Q_0 Q_1 Q_2 Q_3 Q_4
15 16 17 18 19
LS11360S

V_{CC} = Pin 20
GND = Pin 10

LOGIC SYMBOL (IEEE/IEC)

'F711

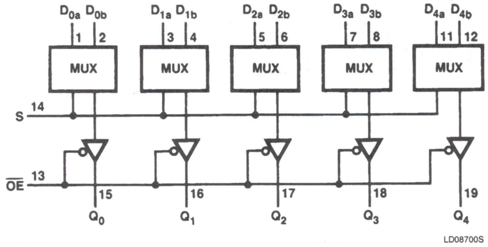


14
13
M
MUX
EN
1
2
3
4
5
6
7
8
11
12
15
16
17
18
19
LS11370S

June 1987

FAST 74F711, 74F712

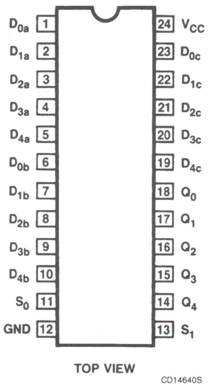
LOGIC DIAGRAM for 'F711


D_{0a} D_{0b}
1 2
D_{1a} D_{1b}
3 4
D_{2a} D_{2b}
5 6
D_{3a} D_{3b}
7 8
D_{4a} D_{4b}
11 12
MUX
MUX
MUX
MUX
MUX
S 14
$\overline{OE}$ 13
15 Q_0
16 Q_1
17 Q_2
18 Q_3
19 Q_4
LD08700S

V_{CC} = Pin 20
GND = Pin 10
NC = Pin 9

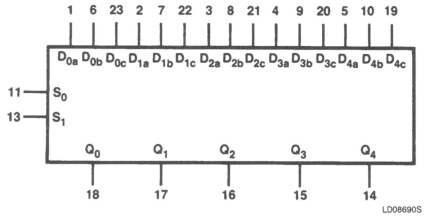
PIN CONFIGURATION

'F712


D_{0a} 1
D_{1a} 2
D_{2a} 3
D_{3a} 4
D_{4a} 5
D_{0b} 6
D_{1b} 7
D_{2b} 8
D_{3b} 9
D_{4b} 10
S_0 11
GND 12
24 V_{CC}
23 D_{0c}
22 D_{1c}
21 D_{2c}
20 D_{3c}
19 D_{4c}
18 Q_0
17 Q_1
16 Q_2
15 Q_3
14 Q_4
13 S_1
TOP VIEW
CD14640S

LOGIC SYMBOL

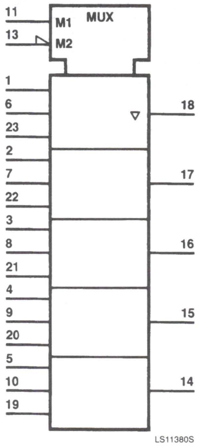
'F712


1 6 23 2 7 22 3 8 21 4 9 20 5 10 19
D_{0a} D_{0b} D_{0c} D_{1a} D_{1b} D_{1c} D_{2a} D_{2b} D_{2c} D_{3a} D_{3b} D_{3c} D_{4a} D_{4b} D_{4c}
11 S_0
13 S_1
Q_0 Q_1 Q_2 Q_3 Q_4
18 17 16 15 14
LD08690S

V_{CC} = Pin 24
GND = Pin 12

LOGIC SYMBOL (IEEE/IEC)

'F712

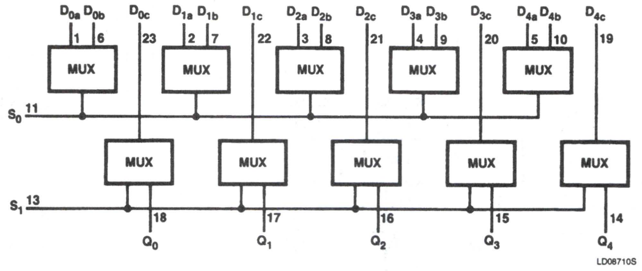

11
13
M1
M2
MUX
1
6
23
2
7
22
3
8
21
4
9
20
5
10
19
18
17
16
15
14
LS11380S

FUNCTION TABLE for 'F711

INPUTS				OUTPUT
S	$\overline{OE}$	D_{na}	D_{nb}	Q_n
L	L	data a	data b	data a
H	L	data a	data b	data b
X	H	X	X	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High-impedance

LOGIC DIAGRAM for 'F712


D0a D0b
D0c
D1a D1b
D1c
D2a D2b
D2c
D3a D3b
D3c
D4a D4b
D4c
1 6 23 2 7 22 3 8 21 4 9 20 5 10 19
MUX
S0 11
S1 13
18 17 16 15 14
Q0 Q1 Q2 Q3 Q4
LD08710S

VCC = Pin 24
GND = Pin 12

FUNCTION TABLE for 'F712

INPUTS					OUTPUT
S_0	S_1	D_{na}	D_{nb}	D_{nc}	Q_n
L	L	data a	data b	data c	data a
X	H	data a	data b	data c	data c
H	L	data a	data b	data c	data b

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	128	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−15	mA
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]			LIMITS			UNIT
							Min	Typ[2]	Max	
V_{OH}	High-level output voltage			V_{CC} = MIN V_{IL} = MAX V_{IH} = MIN	I_{OH} = −3mA	±10% V_{CC}	2.4			V
						±5% V_{CC}	2.7	3.4		V
					I_{OH} = −15mA	±10% V_{CC}	2.0			V
						±5% V_{CC}	2.0	3.3		V
V_{OL}	Low-level output voltage			V_{CC} = MIN V_{IL} = MAX V_{IH} = MIN	I_{OL} = 48mA	±10% V_{CC}		0.40	0.55	V
					I_{OL} = 64mA	5% V_{CC}		0.40	0.55	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, $I_I = I_{IK}$				−0.73	−1.2	V
I_I	Input current at maximum input voltage			V_{CC} = MAX, V_I = 7.0V					100	μA
I_{IH}	High-level input current			V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	Low-level input current	'F711	D_{na}, D_{nb}	V_{CC} = MAX, V_I = 0.5V					−1.2	mA
		others							−0.6	mA
I_{OZH}	OFF-state output current, High-level voltage applied	'F711 only		V_{CC} = MAX, V_O = 2.7V					70	μA
I_{OZL}	OFF-state output current, Low-level voltage applied	'F711 only		V_{CC} = MAX, V_O = 0.5V					−70	μA
I_{OS}	Short-circuit output current[3]			V_{CC} = MAX			−100		−225	mA
I_{CC}	Supply current (total)	'F711	I_{CCH}	V_{CC} = MAX				12		mA
			I_{CCL}					12		mA
			I_{CCZ}					12		mA
		'F712	I_{CCH}					18		mA
			I_{CCL}					24		mA
			I_{CCZ}					30		mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value under the recommended operating conditions for the applicable conditions.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} should be performed last.

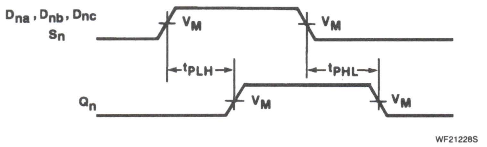
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			$T_A = +25°C$ $V_{CC} = 5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH}	Propagation delay D_{na}, D_{nb} to Q_n	Waveform 1, 2			6.0		7.0	ns
t_{PHL}					6.0		7.0	
t_{PLH}	Propagation delay S to Q_n	Waveform 1			9.5		10.0	ns
t_{PHL}					9.5		10.0	
t_{PZH}	Output Enable time $\overline{OE}$ to Q_n	Waveform 3			7.0		8.0	ns
t_{PZL}		Waveform 4			7.0		8.0	
t_{PHZ}	Output Disable time $\overline{OE}$ to Q_n	Waveform 3			6.0		6.5	ns
t_{PLZ}		Waveform 4			6.0		6.5	

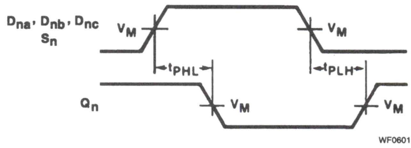
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			$T_A = +25°C$ $V_{CC} = 5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH}	Propagation delay D_{na}, D_{nb}, D_{nc} to Q_n	Waveform 1, 2			6.0		7.0	ns
t_{PHL}					6.0		7.0	
t_{PLH}	Propagation delay S_0, S_1 to Q_n	Waveform 1			11.0		10.0	ns
t_{PHL}					11.0		10.0	

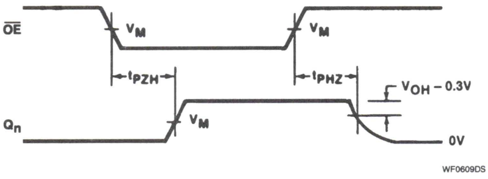
AC WAVEFORMS


Dna, Dnb, Dnc
Sn
VM
VM
tPLH
tPHL
Qn
VM
VM
WF21228S

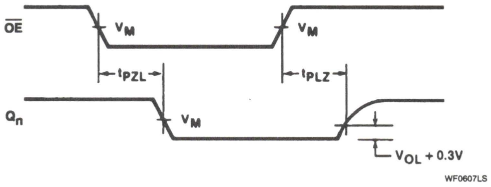
Waveform 1. Propagation Delay, Select and Busses


Dna, Dnb, Dnc
Sn
VM
VM
tPHL
tPLH
Qn
VM
VM
WF0601ES

Waveform 2. Propagation Delay, Select and Busses


OE
VM
VM
tPZH
tPHZ
VOH – 0.3V
Qn
VM
0V
WF0609DS

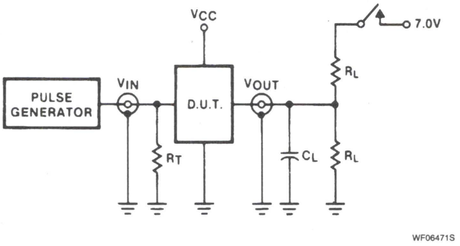
Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time From High Level


OE
VM
VM
tPZL
tPLZ
Qn
VM
VOL + 0.3V
WF0607LS

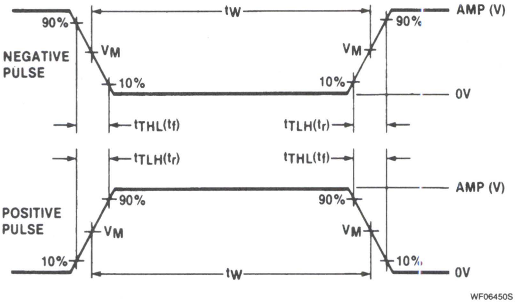
Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time From Low Level

NOTE: $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORMS


VCC
7.0V
RL
PULSE GENERATOR
VIN
D.U.T.
VOUT
RT
CL
RL
WF06471S

Test Circuit for 3-State Outputs


tW
90%
AMP (V)
NEGATIVE PULSE
VM
VM
10%
10%
0V
tTHL(tf)
tTLH(tr)
tTLH(tr)
tTHL(tf)
AMP (V)
90%
90%
POSITIVE PULSE
VM
VM
10%
10%
tW
0V
WF06450S

$V_M = 1.5V$

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F723, 74F725

74F723 Quad 3-to-1 Data Selector Multiplexer (3-State)
74F725 Quad 4-to-1 Data Selector Multiplexer
Preliminary Specification

FAST Products

FEATURES for 74F723

- Consists of four 3-to-1 multiplexers
- Equivalent to three 'F157s or 'F158s
- Inverting or non-inverting data path capability by an Enable input
- Designed for address multiplexing of dynamic RAM and other applications
- Multiple side pins for V_{CC} and GND to reduce lead inductance (improves speed and noise immunity)
- 3-State outputs sink 64mA

FEATURES for 74F725

- Consists of four 4-to-1 multiplexers
- Equivalent to two 'F253s without 3-State
- Outputs sink 64MA

DESCRIPTION

The 'F723 consists of four 3-to-1 line multiplexers designed for address multiplexing of dynamic RAMs and other applications. It can take place of either four 'F157s or 'F158s.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F723	5.5ns	28mA
74F725	6.0ns	29mA

ORDERING INFORMATION

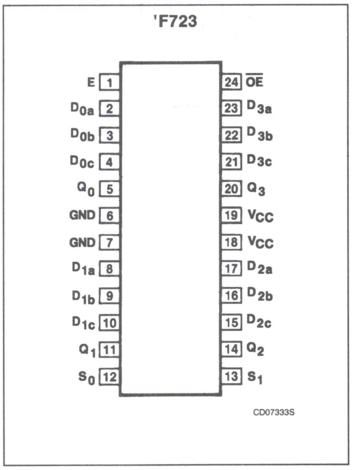
PACKAGE	COMMERCIAL RANGE V_{CC} = 5V± 10%, T_A = 0°C to +70°C
24-Pin Plastic Slim DIP (300mil)	N74F723N, N74F725N
24-Pin Plastic SOL	N74F723D, N74F725D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

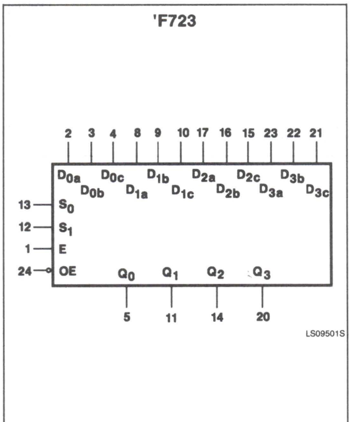
TYPE	PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
'F723	D_{na}, D_{nb} D_{nc}	Data inputs	1.0/2.0	20μA/1.2mA
	S_0, S_1	Select inputs	1.0/1.0	20μA/0.6mA
	E	Enable input	1.0/1.0	20μA/0.6mA
	$\overline{OE}$	Output Enable input	1.0/1.0	20μA/0.6mA
	$Q_0 - Q_3$	Data outputs	750/106.7	15mA/64mA
'F725	D_{na}, D_{nb} D_{nc}, D_{nd}	Data inputs	1.0/1.0	20μA/0.6mA
	S_0, S_1	Select inputs	1.0/1.0	20μA/0.6mA
	$Q_0 - Q_3$	Data outputs	750/106.7	15mA/64mA

NOTE:
1. One (1.0) FAST Unit Load is defind as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION

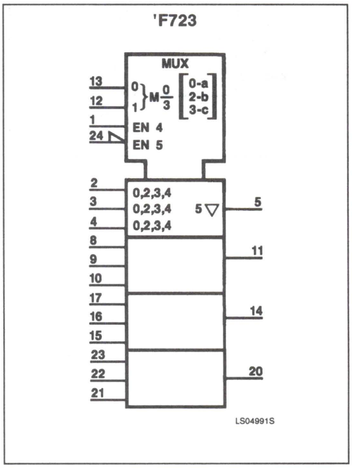

'F723
E 1
D0a 2
D0b 3
D0c 4
Q0 5
GND 6
GND 7
D1a 8
D1b 9
D1c 10
Q1 11
S0 12
24 OE
23 D3a
22 D3b
21 D3c
20 Q3
19 VCC
18 VCC
17 D2a
16 D2b
15 D2c
14 Q2
13 S1
CD07333S

LOGIC SYMBOL


'F723
2 3 4 8 9 10 17 16 15 23 22 21
D0a D0b D0c D1a D1b D1c D2a D2b D2c D3a D3b D3c
13 S0
12 S1
1 E
24 OE
Q0 Q1 Q2 Q3
5 11 14 20
LS09501S

V_{CC} = Pin 16, 19
GND = Pin 6, 7

LOGIC SYMBOL (IEEE/IEC)


'F723
MUX
13
12
1
24
0
1
M 0/3
0-a
2-b
3-c
EN 4
EN 5
2
3
4
0,2,3,4
0,2,3,4
0,2,3,4
5
8
9
10
11
17
16
15
14
23
22
21
20
LS04991S

FAST 74F723, 74F725

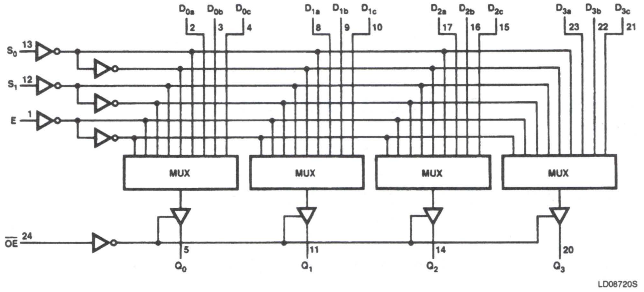
DESCRIPTION (Continued)

Select (S0 and S1) inputs control which line is to be selected, as defined in the Function Table for 'F723. The Enable(E) input, when Low, changes data path to inverting, and when High, changes the data path to non-inverting.

To improve speed and noise immunity, multiple side pins are used for V_{CC} and GND pins. The 3-State outputs sink 64MA.

The 'F725 consists of four 4-to-1 line multiplexers designed for general multiplexing purpose. The select (S0 and S1) inputs control line is to be selected, as defined in the Function Table for 'F725. It can take place of two 'F253s without 3-State function.

LOGIC DIAGRAM for 'F723

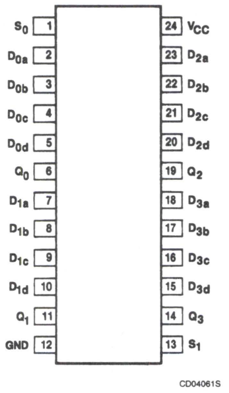


D0a D0b D0c 2 3 4
D1a D1b D1c 8 9 10
D2a D2b D2c 17 16 15
D3a D3b D3c 23 22 21
S0 13
S1 12
E 1
MUX
MUX
MUX
MUX
OE 24
5 Q0
11 Q1
14 Q2
20 Q3
LD08720S

V_{CC} = Pin 18, 19
GND = Pin 6, 7

PIN CONFIGURATION

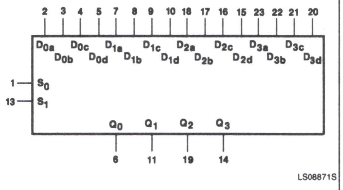
'F725



S0 1
D0a 2
D0b 3
D0c 4
D0d 5
Q0 6
D1a 7
D1b 8
D1c 9
D1d 10
Q1 11
GND 12
24 VCC
23 D2a
22 D2b
21 D2c
20 D2d
19 Q2
18 D3a
17 D3b
16 D3c
15 D3d
14 Q3
13 S1
CD04061S

LOGIC SYMBOL

'F725

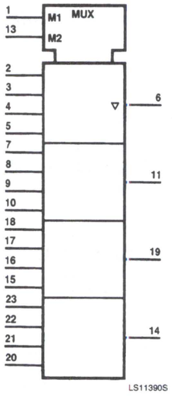


2 3 4 5 7 8 9 10 18 17 16 15 23 22 21 20
D0a D0b D0c D0d D1a D1b D1c D1d D2a D2b D2c D2d D3a D3b D3c D3d
1 S0
13 S1
Q0 Q1 Q2 Q3
6 11 19 14
LS08871S

V_{CC} = Pin 24
GND = Pin 12

LOGIC SYMBOL (IEEE/IEC)

'F725



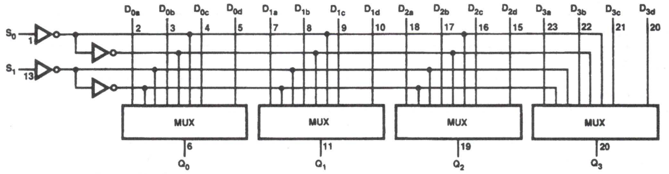
1 M1
13 M2
MUX
2 3 4 5
6
7 8 9 10
11
18 17 16 15
19
23 22 21 20
14
LS11390S

FUNCTION TABLE for 'F723

INPUTS							OUTPUT
S_0	S_1	E	$\overline{OE}$	D_{na}	D_{nb}	D_{nc}	Q_n
L	L	L	H	data a	data b	data c	$\overline{\text{data a}}$
L	L	H	H	data a	data b	data c	data a
H	L	L	H	data a	data b	data c	$\overline{\text{data b}}$
H	L	H	H	data a	data b	data c	data b
X	H	L	H	data a	data b	data c	$\overline{\text{data c}}$
X	H	H	H	data a	data b	data c	data c
X	X	X	L	X	X	X	Z

H = High Voltage level
L = Low voltage level
X = Don't care
Z = High-impedance "OFF" state

LOGIC DIAGRAM for 'F725


D_{0a}
D_{0b}
D_{0c}
D_{0d}
D_{1a}
D_{1b}
D_{1c}
D_{1d}
D_{2a}
D_{2b}
D_{2c}
D_{2d}
D_{3a}
D_{3b}
D_{3c}
D_{3d}
2
3
4
5
7
8
9
10
18
17
16
15
23
22
21
20
S_0
1
S_1
13
MUX
MUX
MUX
MUX
6
Q_0
11
Q_1
19
Q_2
20
Q_3
LD08730S

V_{CC} = Pin 24
GND = Pin 12

FUNCTION TABLE for 'F725

INPUTS						OUTPUT
S_0	S_1	D_{na}	D_{nb}	D_{nc}	D_{nd}	Q_n
L	L	data a	data b	data c	data d	data a
H	L	data a	data b	data c	data d	data b
L	H	data a	data b	data c	data d	data c
H	H	data a	data b	data c	data d	data d

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	128	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−15	mA
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]			74F723, 74F725			UNIT
							Min	Typ[2]	Max	
V_{OH}	High-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = −3mA	±10% V_{CC}	2.4			V
						±5% V_{CC}	2.7	3.4		V
					I_{OH} = −15mA	±10% V_{CC}	2.0			V
						±5% V_{CC}	2.0	3.3		V
V_{OL}	Low-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 48mA	±10% V_{CC}		0.40	0.55	V
					I_{OL} = 64mA	5% V_{CC}		0.40	0.55	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, $I_I = I_{IK}$				−0.73	−1.2	V
I_I	Input current at maximum input voltage			V_{CC} = MAX, V_I = 7.0V					100	μA
I_{IH}	High-level input current			V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	Low-level input current	'F723	D_{na}, D_{nb}	V_{CC} = MAX, V_I = 0.5V					−1.2	mA
		others							−0.6	mA
I_{OZH}	OFF-state output current, High-level voltage applied		'F723 only	V_{CC} = MAX, V_O = 2.7V					70	μA
I_{OZL}	OFF-state output current, Low-level voltage applied		'F723 only	V_{CC} = MAX, V_O = 0.5V					−70	μA
I_{OS}	Short-circuit output current[3]			V_{CC} = MAX			−100		−225	mA
I_{CC}	Supply current (total)	'F723	I_{CCH}	V_{CC} = MAX				28		mA
			I_{CCL}					26		mA
			I_{CCZ}					30		mA
		'F725	I_{CCH}					29		mA
			I_{CCL}					28		mA
			I_{CCZ}					30		mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value under the recommended operating conditions for the applicable conditions.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} should be performed last.

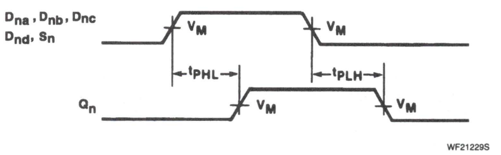
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			$T_A = +25°C$ $V_{CC} = 5.0V$ $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$, $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_{na}, D_{nb}, D_{nc} to Q_n	Waveform 1, 2			6.0 6.0		7.0 7.0	ns
t_{PLH} t_{PHL}	Propagation delay S_0, S_1 to Q_n	Waveform 1			9.5 9.5		10.0 10.0	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}$ to Q_n	Waveform 3 Waveform 4			7.0 7.0		8.0 8.0	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}$ to Q_n	Waveform 3 Waveform 4			6.0 6.0		6.5 6.5	ns

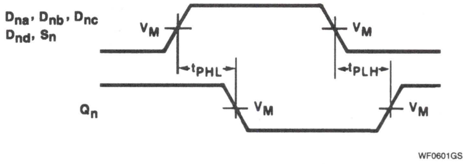
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			$T_A = +25°C$ $V_{CC} = 5.0V$ $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$, $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_{na}, D_{nb}, D_{nc}, D_{nd} to Q_n	Waveform 1, 2			6.0 6.0		7.0 7.0	ns
t_{PLH} t_{PHL}	Propagation delay S_0, S_1 to Q_n	Waveform 1			9.5 9.5		10.0 10.0	ns

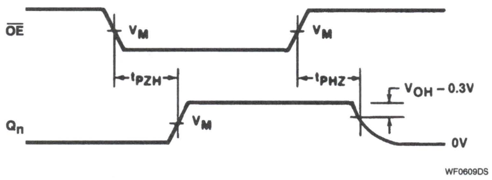
AC WAVEFORMS


Dna, Dnb, Dnc
Dnd, Sn
VM
VM
tPHL
tPLH
Qn
VM
VM
WF21229S

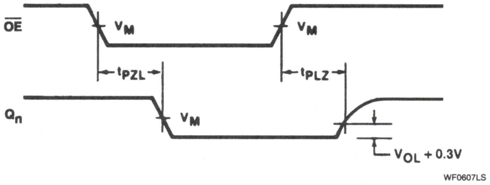
Waveform 1. Propagation Delay, Select and Busses


Dna, Dnb, Dnc
Dnd, Sn
VM
VM
tPHL
tPLH
Qn
VM
VM
WF0601GS

Waveform 2. Propagation Delay, Select and Busses


OE
VM
VM
tPZH
tPHZ
VOH – 0.3V
Qn
VM
0V
WF0609DS

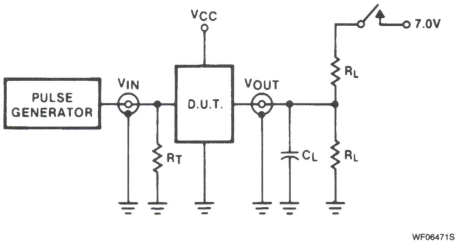
Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time From High Level


OE
VM
VM
tPZL
tPLZ
Qn
VM
VOL + 0.3V
WF0607LS

Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time From Low Level

NOTE: $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORMS


VCC
7.0V
RL
PULSE GENERATOR
VIN
D.U.T.
VOUT
RT
CL
RL
WF06471S

Test Circuit for 3-State Outputs

SWITCH POSITION

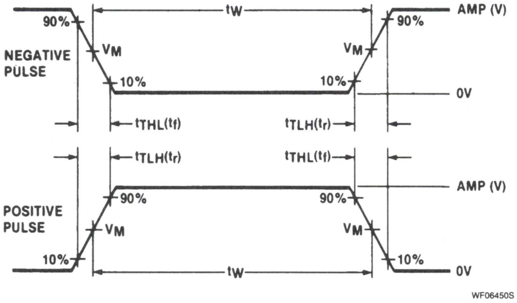
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.


90%
tW
90%
AMP (V)
NEGATIVE PULSE
VM
VM
10%
10%
0V
tTHL(tf)
tTLH(tr)
tTLH(tr)
tTHL(tf)
AMP (V)
90%
90%
POSITIVE PULSE
VM
VM
10%
tW
10%
0V
WF06450S

$V_M = 1.5V$

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST Products

FAST 74F732, 74F733

Multiplexers

'F732 Quad Data Multiplexer, Inverting (3-State)
'F733 Quad Data Multiplexer, Non-Inverting (3-State)
Preliminary Specification

FEATURES

- Quad 2-to-1 (two busses to one bus) Multiplexer
- Data can flow in either direction between busses resulting in six-way data paths (A → B, A → C, B → A, B → C, C → A, C → B)
- A built-in "break-before-make" feature eliminates current glitches and simplifies PC board design
- Output Enable for each bus to allow flexible contention control
- 3-State outputs sink 64mA

DESCRIPTION

'F732/'F733 are Quad Data Multiplexers designed to provide a simple means to control the flow of bidirectional data between three data busses.

The 'F732/'F733 consist of four multiplexers. Each multiplexer has three I/O (A_n,B_n,C_n) pins and one Output Enable ($\overline{OEA}$, $\overline{OEB}$, $\overline{OEC}$) pin. There are 3 Select (S_0,S_1,S_3) pins to control data flow paths for all four multiplexers.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F732	8.0ns	80mA
74F733	7.5ns	85mA

ORDERING INFORMATION

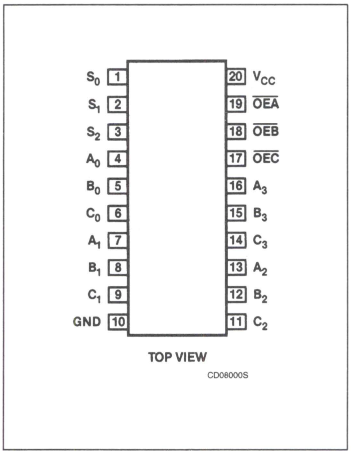
PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
20-Pin Plastic DIP	N74F732N, N74F733N
20-Pin Plastic SOL	N74F732D, N74F733D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

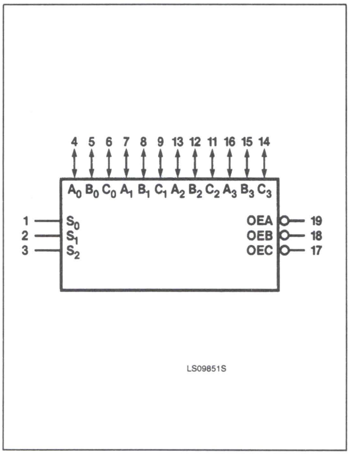
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$A_0 - A_3$	Data inputs for Bus A	3.5/1.0	70μA/0.6mA
$B_0 - B_3$	Data inputs for Bus B	3.5/1.0	70μA/0.6mA
$C_0 - C_3$	Data inputs for Bus C	3.5/1.0	70μA/0.6mA
$S_0 - S_2$	Select inputs	1.0/1.0	20μA/0.6mA
$\overline{OEA}$, $\overline{OEB}$, $\overline{OEC}$	Output enable inputs (active-Low)	1.0/1.0	20μA/0.6mA
$A_0 - A_3$	Data outputs for Bus A	750/106.7	15mA/64mA
$B_0 - B_3$	Data outputs for Bus B	750/106.7	15mA/64mA
$C_0 - C_3$	Data outputs for Bus C	750/106.7	15mA/64mA

NOTE:
1. One (1.0) FAST Unit Load is defined as: 20,μA in the High state and 0.6mA in the Low state.

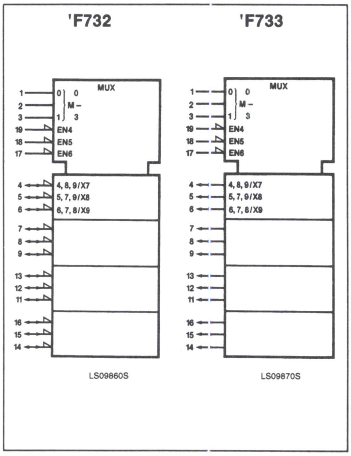
PIN CONFIGURATION


S0 1
S1 2
S2 3
A0 4
B0 5
C0 6
A1 7
B1 8
C1 9
GND 10
20 VCC
19 OEA
18 OEB
17 OEC
16 A3
15 B3
14 C3
13 A2
12 B2
11 C2
TOP VIEW
CD08000S

LOGIC SYMBOL


4 5 6 7 8 9 13 12 11 16 15 14
A0 B0 C0 A1 B1 C1 A2 B2 C2 A3 B3 C3
1 S0
2 S1
3 S2
OEA 19
OEB 18
OEC 17
LS09851S

LOGIC SYMBOL(IEEE/IEC)


'F732

'F733

MUX
0 0 M− 1 3
EN4
EN5
EN6
4, 8, 9/X7
5, 7, 9/X8
6, 7, 8/X9
1
2
3
19
18
17
4
5
6
7
8
9
13
12
11
16
15
14
LS09860S
LS09870S

With the Select control, data can flow in the following directions between busses: A to B, A to C, B to A, B to C, C to A, C to B, A to B and C.

A built-in "break-before-make" feature eliminates current glitches common to systems using 3-State transceivers to accomplish the same function.

FUNCTION TABLE

INPUTS						OPERATING MODE
S_0	S_1	S_2	$\overline{OEA}$	$\overline{OEB}$	$\overline{OEC}$	
X	X	X	H	X	X	Bus A disabled except for input
X	X	X	X	H	X	Bus B disabled except for input
X	X	X	X	X	H	Bus C disabled except for input
L	L	L	X	X	L	Data flow from Bus A to Bus C
H	L	L	L	X	X	Data flow from Bus C to Bus A
L	L	H	X	X	L	Data flow from Bus B to Bus C
H	L	H	X	L	X	Data flow from Bus C to Bus B
L	H	L	X	L	X	Data flow from Bus A to Bus B
H	H	L	L	X	X	Data flow from Bus B to Bus A
X	H	H	X	L	L	Data flow from Bus A to Bus B and Bus C

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	–0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			–18	mA
I_{OH}	High-level output current			–3	mA
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]			74F32, 74F33			UNIT
							Min	Typ[2]	Max	
V_{OH}	High-level output voltage			V_{CC} = MIN, V_{IL} = MAX, I_{IH} = MIN	I_{OH} = −3mA	±10%V_{CC}	2.4			V
						±5%V_{CC}	2.7	3.4		V
				V_{CC} = MIN, V_{IL} = MAX, I_{IH} = MIN	I_{OH} = −15mA	±10%V_{CC}	2.0			V
						±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage			V_{CC} = MIN, V_{IL} = MAX, I_{IH} = MIN	I_{OL} = 48mA	±10%V_{CC}		0.4	0.55	V
					I_{OL} = 64mA	±5%V_{CC}		0.4	0.55	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, $I_I = I_{IK}$				−0.73	−1.2	V
I_I	Input clamp current at maximum input voltage			V_{CC} = MAX, V_I = 7.0V					100	μA
I_{IH}	High-level input current	$\overline{OEA}$, $\overline{OEB}$, $\overline{OEC}$, $S_0 - S_3$		V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	Low-level input current	$\overline{OEA}$, $\overline{OEB}$, $\overline{OEC}$, $S_0 - S_2$		V_{CC} = MAX, V_I = 0.5V					−0.6	mA
I_{OZH} + I_{IH}	OFF-state output current, High-level voltage applied	$A_0 - A_3$, $B_0 - B_3$, $C_0 - C_3$		V_{CC} = MAX, V_O = 2.7V					70	μA
I_{OZL} + I_{IL}	OFF-state output Low-level current, voltage applied	$A_0 - A_3$, $B_0 - B_3$, $C_0 - C_3$		V_{CC} = MAX, V_O = 0.5V					−0.6	mA
I_{OS}	Short-circuit output current[3]			V_{CC} = MAX			−100		−225	mA
I_{CC}	Supply current (total)	'F732	I_{CCH}	V_{CC} = MAX					80	mA
			I_{CCL}						110	mA
			I_{CCZ}						100	mA
		'F733	I_{CCH}						70	mA
			I_{CCL}						100	mA
			I_{CCZ}						90	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of High-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

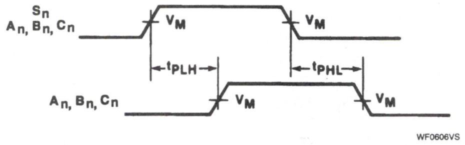
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F732					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$, $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n, B_n, C_n to B_n, C_n, A_n	Waveform 1, 2	3.0 3.0	8.5 8.5	12.5 12.5	2.0 2.0	14.0 14.0	ns
t_{PLH} t_{PHL}	Propagation delay $S_1 - A_n$, $S_2 - C_n$	Waveform 1	3.0 3.0	9.0 9.0	13.0 13.0	2.0 2.0	15.0 15.0	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OEA}$, $\overline{OEB}$, $\overline{OEC}$ to A_n, B_n, C_n	Waveform 3 Waveform 4	3.0 3.0	9.0 9.0	13.0 13.0	2.0 2.0	15.0 15.0	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OEA}$, $\overline{OEB}$, $\overline{OEC}$ to A_n, B_n, C_n	Waveform 3 Waveform 4	2.0 2.0	6.0 6.0	10.0 10.0	2.0 2.0	12.0 12.0	ns

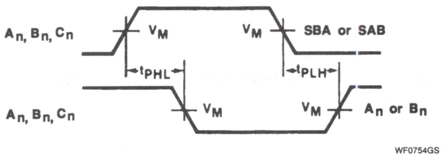
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F733					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n, B_n, C_n to B_n, C_n, A_n	Waveform 1, 2	2.0 2.0	7.5 7.5	12.5 12.5	2.0 2.0	14.0 14.0	ns
t_{PLH} t_{PHL}	Propagation delay $S_1 - A_n$, $S_2 - C_n$	Waveform 1	3.0 3.0	8.0 8.0	13.0 13.0	2.0 2.0	15.0 15.0	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OEA}$, $\overline{OEB}$, $\overline{OEC}$ to A_n, B_n, C_n	Waveform 3 Waveform 4	3.0 3.0	9.0 9.0	13.0 13.0	2.0 2.0	15.0 15.0	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OEA}$, $\overline{OEB}$, $\overline{OEC}$ to A_n, B_n, C_n	Waveform 3 Waveform 4	2.0 2.0	6.0 6.0	10.0 10.0	2.0 2.0		ns

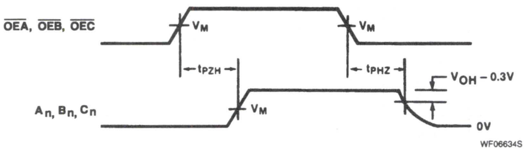
AC WAVEFORMS


Sn
An, Bn, Cn
VM
VM
tPLH
tPHL
An, Bn, Cn
VM
VM
WF0606VS

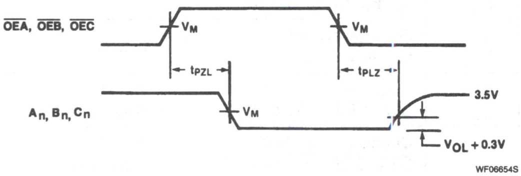
Waveform 1. Propagation Delay Select, Busses to Busses


An, Bn, Cn
VM
VM
SBA or SAB
tPHL
tPLH
An, Bn, Cn
VM
VM
An or Bn
WF0754GS

Waveform 2. Propagation Delay Busses to Busses


OEA, OEB, OEC
VM
VM
tPZH
tPHZ
VOH − 0.3V
An, Bn, Cn
VM
0V
WF06634S

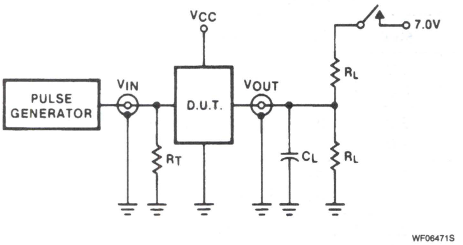
Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time From High Level


OEA, OEB, OEC
VM
VM
tPZL
tPLZ
3.5V
An, Bn, Cn
VM
VOL + 0.3V
WF06654S

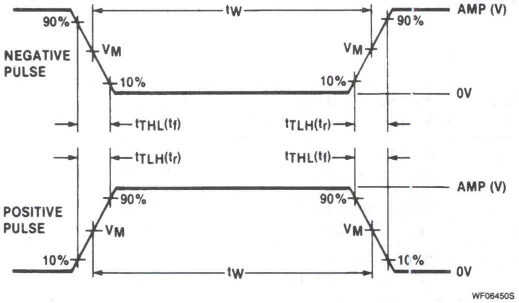
Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORMS


VCC
7.0V
RL
PULSE GENERATOR
VIN
D.U.T.
VOUT
RT
CL
RL
WF06471S

Test Circuit for 3-State Outputs


tW
AMP (V)
90%
90%
NEGATIVE PULSE
VM
VM
10%
10%
0V
tTHL(tf)
tTLH(tr)
tTLH(tr)
tTHL(tf)
AMP (V)
90%
90%
POSITIVE PULSE
VM
VM
10%
10%
0V
tW
WF06450S

$V_M = 1.5V$

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST Products

FAST 74F764/765, 74F764A/765A, 74F764-1/765-1
DRAM Dual-Ported Controllers

This document contains Product specifications for the 74F764/765 and 74F764-1/765-1, and Preliminary specification for the 74F764A/765A

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F764/765	150MHz	150mA
74F764A/765A	175MHz	150mA
74F764-1/765-1	150MHz	125mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$, $T_A = 0°C$ to $+70°C$
Plastic DIP	74F764N, 74F765N, 74F764AN, 74F765AN, 74F764-1N, 74F765-1N
PLCC-44	74F764A, 74F765A, 74F764AA, 74F765AA, 74F764-1A, 74F765-1A

FEATURES

- **Allows two microprocessors to access the same bank of dynamic RAM**
- **Performs arbitration, signal timing, address multiplexing, and refresh**
- **9 address output pins allow direct control of up to 256K dynamic RAMS**
- **External address multiplexing enables control of 1Mbit (or greater) dynamic RAMs**
- **Separate refresh clock allows adjustable refresh timing**
- **F764/F764A/F764-1 have on-chip 18-bit address input latch**
- **F764/765, F764-1/765-1 allow control of dynamic RAMs with row access times down to 40ns**
- **F764A/765A allow control of dynamic RAMs with row access times down to 30ns**
- **F764/765, F764A/765A output drivers designed for incident wave switching**
- **F764-1/765-1 output drivers designed for first reflected wave switching**

DESCRIPTION

The 74F764/765 DRAM Dual-ported Controller is a High-speed synchronous dual-port arbiter and timing generator that allows two microprocessors, microcontrollers, or any other memory accessing device to share the same block of DRAM. The device performs arbitration, signal timing, address multiplexing, and refresh address generation, replacing up to 25 discrete devices.

74F764 vs 74F765

The F764, though functionally and pin-to-pin compatible with the F765, differs from the later in that it has an on-chip address input latch. This is useful in systems that have unlatched or multiplexed address and data bus.

74F764/765 vs 74F764A/765A

The 74F764A/765A is a faster version of the F764/765. The F764/765, rated at a maximum clock frequency of 100MHz, can control dynamic RAMs with row access times down to 40ns. The F764A/765A devices on the other hand are rated at 150MHz which translates to control of 30ns dynamic RAMs.

74F764/765, 74F764A/765A vs 74F764-1/765-1

The 74F764-1/765-1, though as fast as the 74F764/765, differs from the 74F764/765 and 74F764A/765A in the following respects:

a) they reduce the row address hold time by half-a-clock cycle, and

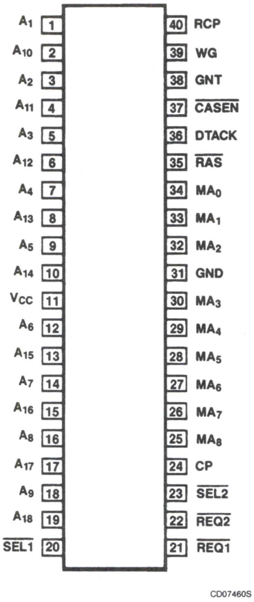
b) their outputs are optimized for first reflected wave switching as opposed to incident wave switching.

The specialized outputs eliminate the need for signal terminations inessentially all applications.

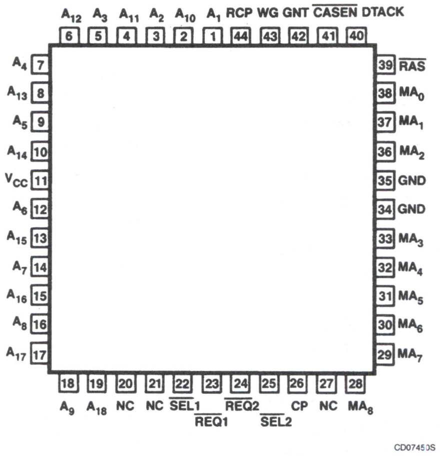
All devices are available in 40-pin plastic DIP or 44-pin PLCC with pinouts designed to allow convenient placement of microprocessors, DRAMs, and other support chips.

PIN CONFIGURATION

N Package

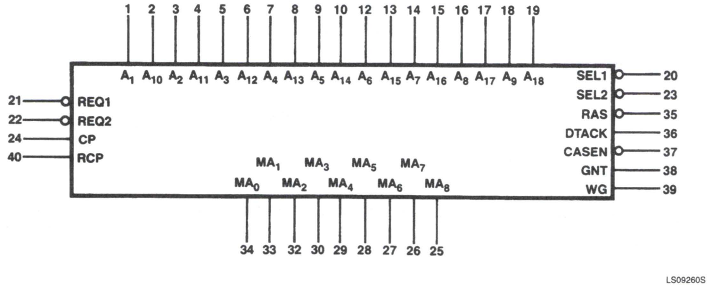

A1 1
A10 2
A2 3
A11 4
A3 5
A12 6
A4 7
A13 8
A5 9
A14 10
VCC 11
A6 12
A15 13
A7 14
A16 15
A8 16
A17 17
A9 18
A18 19
SEL1 20
40 RCP
39 WG
38 GNT
37 CASEN
36 DTACK
35 RAS
34 MA0
33 MA1
32 MA2
31 GND
30 MA3
29 MA4
28 MA5
27 MA6
26 MA7
25 MA8
24 CP
23 SEL2
22 REQ2
21 REQ1
CD07460S

A Package


A12 6
A3 5
A11 4
A2 3
A10 2
A1 1
RCP 44
WG 43
GNT 42
CASEN 41
DTACK 40
A4 7
A13 8
A5 9
A14 10
VCC 11
A6 12
A15 13
A7 14
A16 15
A8 16
A17 17
39 RAS
38 MA0
37 MA1
36 MA2
35 GND
34 GND
33 MA3
32 MA4
31 MA5
30 MA6
29 MA7
18 A9
19 A18
20 NC
21 NC
22 SEL1
23 REQ1
24 REQ2
25 SEL2
26 CP
27 NC
28 MA8
CD07450S

LOGIC SYMBOL

N Package


1 2 3 4 5 6 7 8 9 10 12 13 14 15 16 17 18 19
A1 A10 A2 A11 A3 A12 A4 A13 A5 A14 A6 A15 A7 A16 A8 A17 A9 A18
21 REQ1
22 REQ2
24 CP
40 RCP
SEL1 20
SEL2 23
RAS 35
DTACK 36
CASEN 37
GNT 38
WG 39
MA1 MA3 MA5 MA7
MA0 MA2 MA4 MA6 MA8
34 33 32 30 29 28 27 26 25
LS09260S

V_{CC} = Pin 11
GND = Pin 31

PIN DESCRIPTION

SYMBOL	PINS		TYPE	NAME AND FUNCTION
	DIP	PLCC		
A_1 A_2 A_3 A_4 A_5 A_6 A_7 A_8 A_9	1 3 5 7 9 12 14 16 18	1 3 5 7 9 12 14 16 18	I I I I I I I I I	Address inputs used to generate memory row address
A_{10} A_{11} A_{12} A_{13} A_{14} A_{15} A_{16} A_{17} A_{18}	2 4 6 8 10 13 15 17 19	2 4 6 8 10 13 15 17 19	I I I I I I I I I	Address inputs used to generate memory column address
$\overline{REQ}_1$	21	23	I	Memory access request from Microprocessor 1
$\overline{REQ}_2$	22	24	I	Memory access request from Microprocessor 2
CP	24	26	I	Clock input which determines the master timing
RCP	40	44	I	Refresh clock determines the period of refresh for each row after it is internally divided by 64
$\overline{SEL}_1$	20	22	O	Select signal is activated in response to active $\overline{REQ}_1$ input, indicating selection of Microprocessor 1
V_{CC}	11	11		Power supply +5V ±10%
GND	31	34 35		Ground
$\overline{SEL}_2$	23	25	O	Select signal is activated in response to active $\overline{REQ}_2$ input, indicating selection of Microprocessor 2
MA_0 MA_1 MA_2 MA_3 MA_4 MA_5 MA_6 MA_7 MA_8	34 33 32 30 29 28 27 26 25	38 37 36 33 32 31 30 29 28	O O O O O O O O O	Memory address output pins, designed to drive address lines of the DRAM
GNT	38	42	O	Grant output, activated upon start of a memory access cycle
$\overline{RAS}$	35	39	O	Row address strobe, used to latch the row address into the bank of DRAM (to be connected directly to the $\overline{RAS}$ inputs of the DRAMs)
WG	39	43	O	Write Gate may be gated with the microprocessor's write strobe to perform an early write cycle
$\overline{CASEN}$	37	41	O	Column Address Strobe Enable is used to latch the column address into the bank of DRAMs
DTACK	36	40	O	Data Transfer Acknowledge indicates that data on the DRAM output lines is valid or the proper access time has been met

ARCHITECTURE

The 74F764/765 DRAM dual-ported controller is a synchronous device, with all signal generation being a function of the input clock (CP).

The 'F764/765 arbitration logic is divided into two stages. The first stage controls which one of the two $\overline{\text{REQ}}$ inputs will be serviced by activating the corresponding $\overline{\text{SEL}}$ output. This arbitration takes place irrespective of whether or not a refresh cycle is in progress. The arbitration is accomplished by sampling the $\overline{\text{REQ}}_1$ and $\overline{\text{REQ}}_2$ inputs on different edges of the CP clock. $\overline{\text{REQ}}_1$ is sampled on the rising edge and $\overline{\text{REQ}}_2$ on the falling edge (refer to Figures 1 – 4).

Therefore, if access to the DRAM is requested by both processors at the same time, the contention is automatically resolved. The internal flip-flops of the device used in the arbitration process have been chosen for their immunity to metastable conditions.

The second stage of arbitration selects between the selected processor and any internal refresh request. Refresh always has priority and is serviced immediately after the current cycle is completed (if needed). This arbitration stage also indicates the start of an access cycle by asserting the GNT output.

The Refresh Clock (RCP) input determines the period for each row. This clock may be held in the High state for external or no refresh applications. When used, a refresh request is internally generated every 64 RCP cycles. The refresh counter is incremented at the end of every refresh cycle, and provides the refresh address.

Since $\overline{\text{SEL}}$ outputs indicate which one of the two memory accessing devices has been selected to be serviced, these provide an indication of which processor's address bus should be asserted at the controller address inputs. A Data Transfer Acknowledge (DTACK) signal is generated by the timing logic and either this signal or GNT may be used with the $\overline{\text{SEL}}$ outputs to indicate the end or beginning of an access cycle for each processor.

FUNCTIONAL DESCRIPTION

As described earlier, the timing, arbitration, refresh and multiplexing functions provided by the controller are all derived from the CP input. The period of this clock for the F764/765 and F764A/765A should be set equal to: (Tras(of the DRAM) + 16 – 5)/4ns plus any system guard-band required.

For the F764-1/765-1 the CP clock input period should be equal to:
(Tras(of the DRAM) + 22 – 10)/4ns plus any system guard-band required.

A microprocessor requests access to the DRAM by activating the appropriate $\overline{\text{REQ}}$ input. If a refresh cycle is not in process and the other request input is not active, the $\overline{\text{SEL}}$ output corresponding to the active $\overline{\text{REQ}}$ input will be asserted to indicate the selected processor. The GNT output then goes High to indicate the start of a memory access cycle. If however, a refresh cycle is in process, and there is only one active $\overline{\text{REQ}}$ input, the $\overline{\text{SEL}}$ output corresponding to the active input $\overline{\text{REQ}}$ will be asserted but the GNT output will not go High until after the completion of the refresh cycle (see Figures 10, 11, 14 and 15).

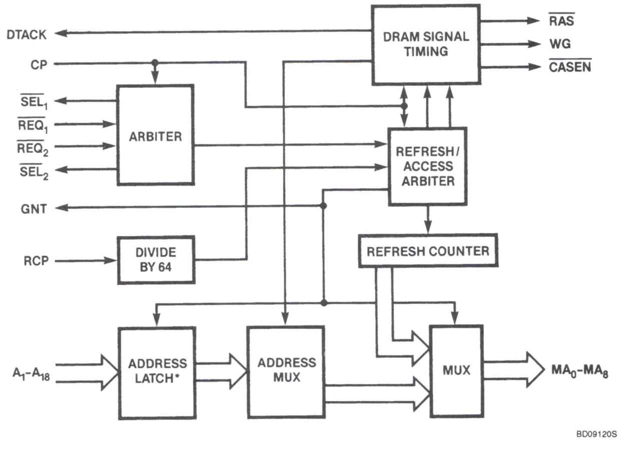
When the device is servicing a memory access cycle and a memory access is also requested by the other processor before the current cycle is completed, the $\overline{\text{SEL}}$ output for the other processor will not be issued, though GNT is asserted at that time, because the other processor is performing an access cycle. This will ensure that there is no contention on the address bus, i.e., the address bus is not driven by both processors at the same time.

Following the completion of the current memory access cycle, the $\overline{\text{SEL}}$ output corresponding to the awaiting $\overline{\text{REQ}}$ input will be asserted, followed by the GNT output. If however, there were any pending refresh requests, assertion of the GNT output will be held OFF until the refresh request has been serviced.

When GNT goes High, the $A_1 - A_{18}$ address inputs to the 'F764/F764A/F764-1 are latched internally and the $A_1 - A_9$ signals are propagated to the $MA_0 - MA_8$ outputs. The address inputs are not latched by the 'F765/F765A/F765-1 and therefore, $A_1 - A_9$ inputs propagate directly to the $MA_0 - MA_8$ outputs.

A half-clock cycle is allowed for the address signals to propagate through to the outputs, after which the $\overline{\text{RAS}}$ output is asserted.

BLOCK DIAGRAM



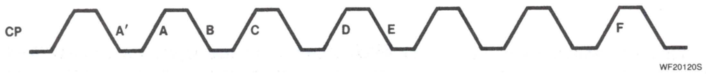
NOTE:
* The address input latch is available only on the 74F764, 74F764A, and 74F764-1.

One clock cycle later, the $A_{10}-A_{18}$ latch outputs on the 'F764/F764A or $A_{10}-A_{18}$ inputs to the 'F765/F765A are selected and propagated to the MA_0-MA_8 outputs. This occurs half a clock cycle earlier on the F764-1/765-1 (refer to Figures 3 and 4). The Write Gate (WG) output becomes valid at this time to indicate the proper time to gate the Write signal from the selected processor to the DRAM to perform an Early Write cycle.

A half-clock cycle is again allowed for the $A_{10}-A_{18}$ signals to propagate and stabilize. $\overline{\text{CASEN}}$ then becomes valid. $\overline{\text{CASEN}}$ can be used as $\overline{\text{CAS}}$ output or decoded with Higher-order address signals to produce multiple $\overline{\text{CAS}}$ signals. After $\overline{\text{CASEN}}$ is valid, the controller will wait for 2½ clock cycles before negating $\overline{\text{RAS}}$, making a total $\overline{\text{RAS}}$ pulse width of approximately 4 clock cycles. Since this width matches the standard DRAM access time, the controller next asserts DTACK output, indicating that valid data is on the DRAM data lines or that a memory access cycle is complete. DTACK may be used to assert valid data transfer acknowledge for processors requiring this signal (i.e., the 68000 family of processors).

All controller output signals are held in this final state until the selected processor withdraws its request by driving its $\overline{\text{REQ}}$ input High. When the request is withdrawn, internal synchronization takes place, the controller output signals become inactive, and any pending memory access or refresh cycles are serviced.

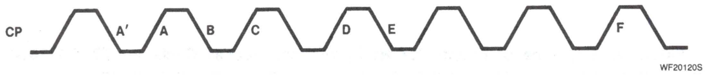
A refresh cycle is serviced by propagating the 9 refresh counter address signals to the MA_0-MA_8 outputs. After a half-clock cycle the $\overline{\text{RAS}}$ output is asserted for four cycles and then negated for three clock cycles to meet the $\overline{\text{RAS}}$ precharge requirements of the DRAMs (see Figures 5 and 6).



A' $\overline{\text{REQ}}_2$ sampled
A $\overline{\text{REQ}}_1$ sampled
  $\overline{\text{SEL}}_1$ triggered ($\overline{\text{SEL}}_1$ triggered by $\overline{\text{REQ}}_1$ sample circuitry) ($\overline{\text{REQ}}_2$ disabled by $\overline{\text{SEL}}_1$ circuitry)
B GNT triggered
  A_1-A_{18} latched (Input address latch triggered by GNT circuitry)*
  A_1-A_9 propagate to MA_0-MA_8 outputs
C $\overline{\text{RAS}}$ triggered
D WG triggered
  $A_{10}-A_{18}$ selected and propagated to MA_0-MA_8 outputs
E $\overline{\text{CASEN}}$ triggered
F $\overline{\text{RAS}}$ negated
  DTACK triggered

* Only on the 'F764/F764A.

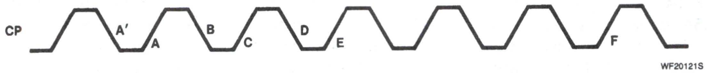
Figure 1. Sequence of Events for $\overline{\text{REQ}}_1$ Memory Access Cycle for F764/765 and F764A/765A



A' $\overline{\text{REQ}}_2$ sampled
  $\overline{\text{SEL}}_2$ triggered ($\overline{\text{SEL}}_2$ triggered by $\overline{\text{REQ}}_2$ sampling circuitry)
A $\overline{\text{REQ}}_1$ is not sampled (disabled by $\overline{\text{SEL}}_2$ circuitry)
B GNT triggered
  A_1-A_{18} latched (Input address latch triggered by GNT circuitry)*
  A_1-A_9 propagate to MA_0-MA_8 outputs
C $\overline{\text{RAS}}$ triggered
D WG triggered
  $A_{10}-A_{18}$ selected and propagated to MA_0-MA_8 outputs
E $\overline{\text{CASEN}}$ triggered
F $\overline{\text{RAS}}$ negated
  DTACK triggered

* Only on the 'F764/F764A.

Figure 2. Sequence of Events for $\overline{\text{REQ}}_2$ Memory Access Cycle for F764/765 and F764A/765A



A' $\overline{REQ}_2$ sampled

A $\overline{REQ}_1$ sampled ($\overline{REQ}_2$ disabled by $\overline{SEL}_1$ circuitry)
$\overline{SEL}_1$ triggered ($\overline{SEL}_1$ triggered by $\overline{REQ}_1$ sample circuitry)

B GNT triggered
$A_1 - A_{18}$ latched (Input address latch triggered by GNT circuitry)*
$A_1 - A_9$ propagate to $MA_0 - MA_8$ outputs

C $\overline{RAS}$ triggered

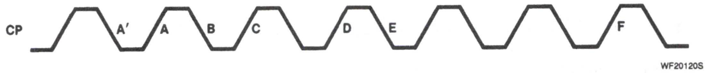
D WG triggered
$A_{10} - A_{18}$ selected and propagated to $MA_0 - MA_8$ outputs

E $\overline{CASEN}$ triggered

F $\overline{RAS}$ negated
DTACK triggered

* Only on the F764-1.

Figure 3. Sequence of Events for $\overline{REQ}_1$ Memory Access Cycle for F764-1/765-1



A' $\overline{REQ}_2$ sampled
$\overline{SEL}_2$ triggered ($\overline{SEL}_2$ triggered by $\overline{REQ}_2$ sampling circuitry)

A $\overline{REQ}_1$ is not sampled (disabled by $\overline{SEL}_2$ circuitry)

B GNT triggered
$A_1 - A_{18}$ latched (Input address latch triggered by GNT circuitry)*
$A_1 - A_9$ propagate to $MA_0 - MA_8$ outputs

C $\overline{RAS}$ triggered

D WG triggered
$A_{10} - A_{18}$ selected and propagated to $MA_0 - MA_8$ outputs

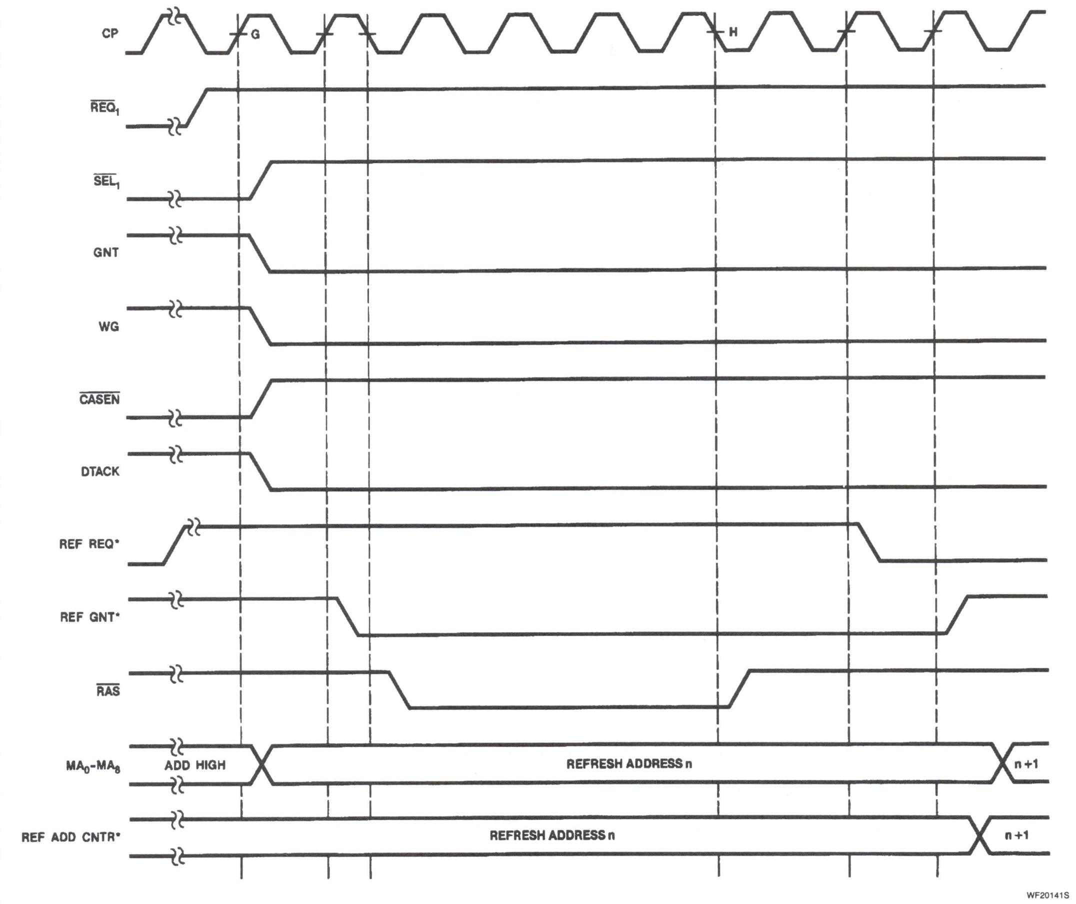
E $\overline{CASEN}$ triggered

F $\overline{RAS}$ negated
DTACK triggered

* Only on the 'F764-1.

Figure 4. Sequence of Events for $\overline{REQ}_2$ Memory Access Cycle for F764-1/765-1

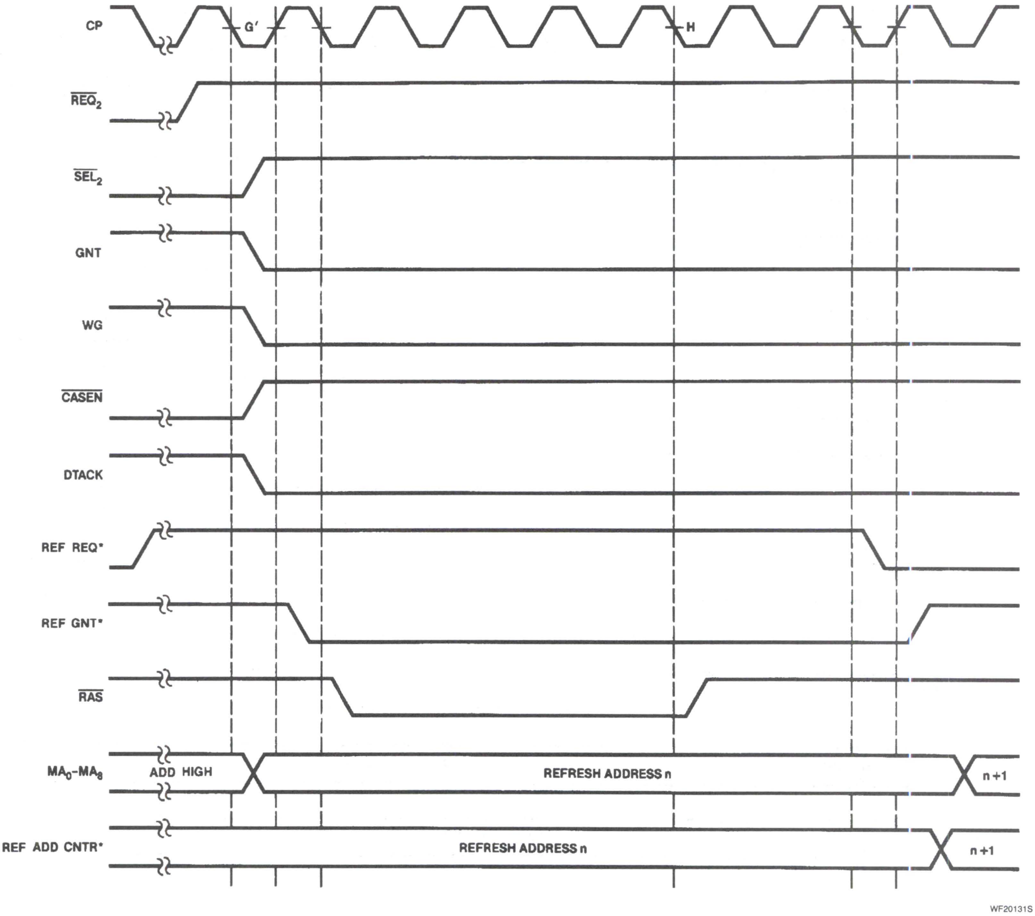
AC WAVEFORMS


CP
G
H
REQ1
SEL1
GNT
WG
CASEN
DTACK
REF REQ*
REF GNT*
RAS
MA0-MA8
ADD HIGH
REFRESH ADDRESS n
n+1
REF ADD CNTR*
REFRESH ADDRESS n
n+1
WF20141S

NOTE:
* These are internal signals only.

Figure 5. Refresh Cycle Timing Following a $\overline{\text{REQ}}_1$ Memory Access Cycle for All Devices

AC WAVEFORMS


CP
G'
H
$\overline{REQ_2}$
$\overline{SEL_2}$
GNT
WG
$\overline{CASEN}$
DTACK
REF REQ*
REF GNT*
$\overline{RAS}$
MA_0-MA_8
ADD HIGH
REFRESH ADDRESS n
n+1
REF ADD CNTR*
REFRESH ADDRESS n
n+1
WF20131S

NOTE:
* These are internal signals only.

Figure 6. Refresh Cycle Timing Following a $\overline{REQ_2}$ Memory Access Cycle for All Devices

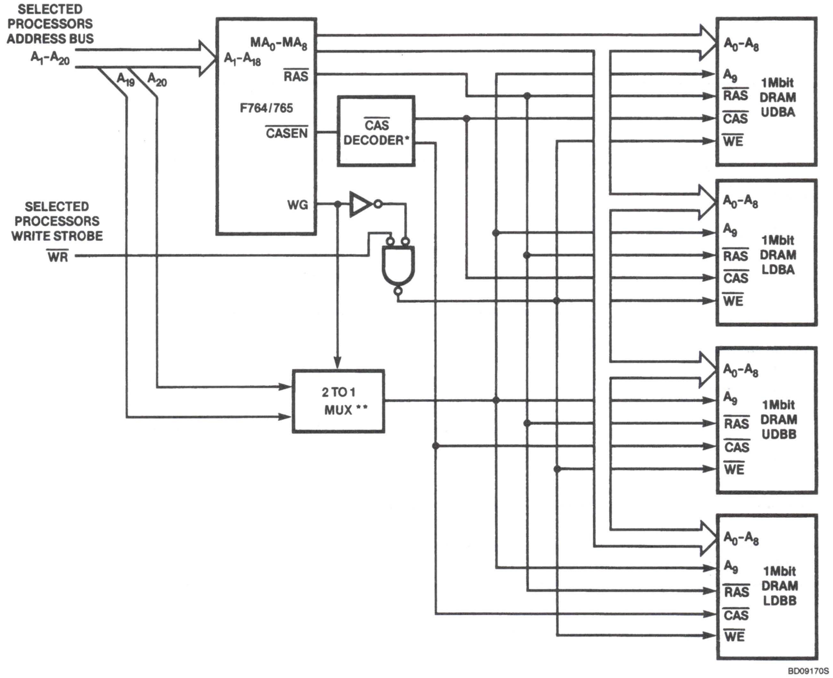
USING 74F764/765, 74F764A/765A, AND 74F764-1/765-1 TO ADDRESS 1MBIT DRAMS

The addressing capabilities of the DRAM dual-ported controllers can be extended to address 1Mbit (or greater) DRAMs by using an external multiplexer to multiplex additional address bits.

Figure 7 shows an application, using an external 2-to-1 multiplexer to address 1Mbit dynamic RAMs. The 9-bit internal refresh counter of the controller provides 512 row addresses which more than meet the refreshing needs for most industry standard 1Mbit DRAMs. Therefore, it is unnecessary to provide for any additional refresh address bits for DRAMs with up to 512 rows.

Additional address bits (for larger DRAMs) may also be multiplexed externally as long as the DRAM refreshing requirements do not exceed 512 row addresses.

The WG output of the controller should be used to multiplex between the external row and column address bits. However it is important that the propagation delay through the external multiplexer does not cause column address setup violations on the dynamic RAM.


SELECTED PROCESSORS ADDRESS BUS
A_1-A_{20}
A_{19}
A_{20}
MA_0-MA_8
A_1-A_{18}
$\overline{RAS}$
F764/765
$\overline{CASEN}$
$\overline{CAS}$ DECODER*
WG
SELECTED PROCESSORS WRITE STROBE
$\overline{WR}$
2 TO 1 MUX **
A_0-A_8
A_9
$\overline{RAS}$
$\overline{CAS}$
$\overline{WE}$
1Mbit DRAM UDBA
1Mbit DRAM LDBA
1Mbit DRAM UDBB
1Mbit DRAM LDBB
BD09170S

* The $\overline{CAS}$ decode logic is not necessary if multiple $\overline{CAS}$ signals are not required. The application also does not show further decoding of multiple $\overline{CAS}$ signals to distinguish between Upper and Lower data bytes. If required, multiple $\overline{CAS}$ signal generation and Upper and Lower byte decoding can be accomplished as shown in Figures 16 – 18.

** Propagation delay through the multiplexer should be considered when using the controller for 1Mbit addressing.

Figure 7. Using the Controller to Address 1Mbit DRAMs

AC WAVEFORMS

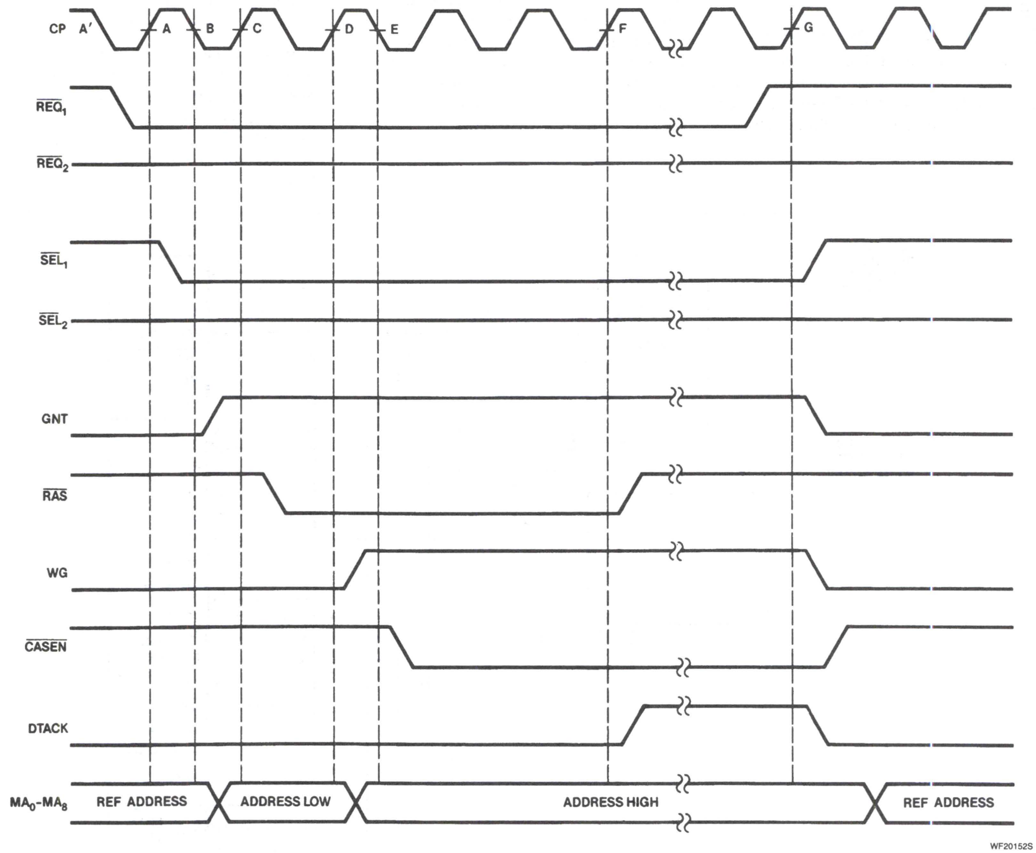

CP
A′
A
B
C
D
E
F
G
$\overline{REQ}_1$
$\overline{REQ}_2$
$\overline{SEL}_1$
$\overline{SEL}_2$
GNT
$\overline{RAS}$
WG
$\overline{CASEN}$
DTACK
MA_0-MA_8
REF ADDRESS
ADDRESS LOW
ADDRESS HIGH
REF ADDRESS
WF20152S

Figure 8. Request 1 ($\overline{REQ}_1$) Memory Access Cycle Timing for F764/765 and F764A/765A

AC WAVEFORMS

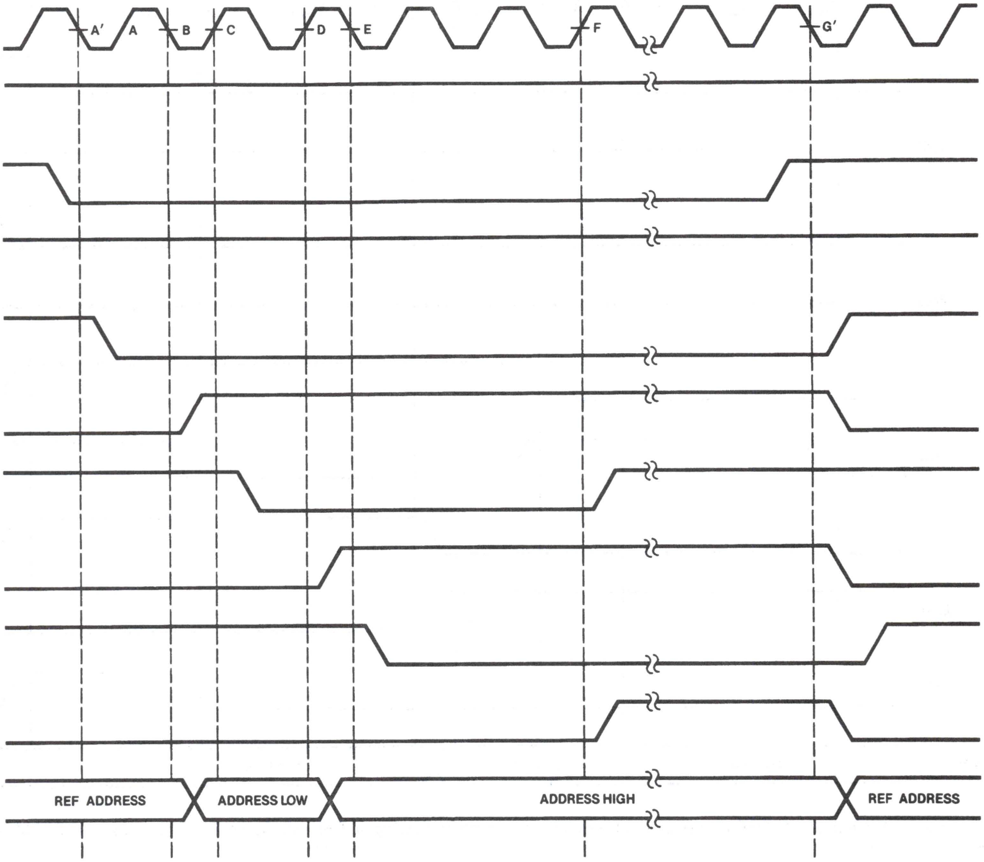

CP
A'
A
B
C
D
E
F
G'
$\overline{REQ_1}$
$\overline{REQ_2}$
$\overline{SEL_1}$
$\overline{SEL_2}$
GNT
$\overline{RAS}$
WG
$\overline{CASEN}$
DTACK
MA_0-MA_8
REF ADDRESS
ADDRESS LOW
ADDRESS HIGH
REF ADDRESS
WF20162S

Figure 9. Request 2 ($\overline{REQ_2}$) Memory Access Cycle Timing for F764/765 and F764A/765A

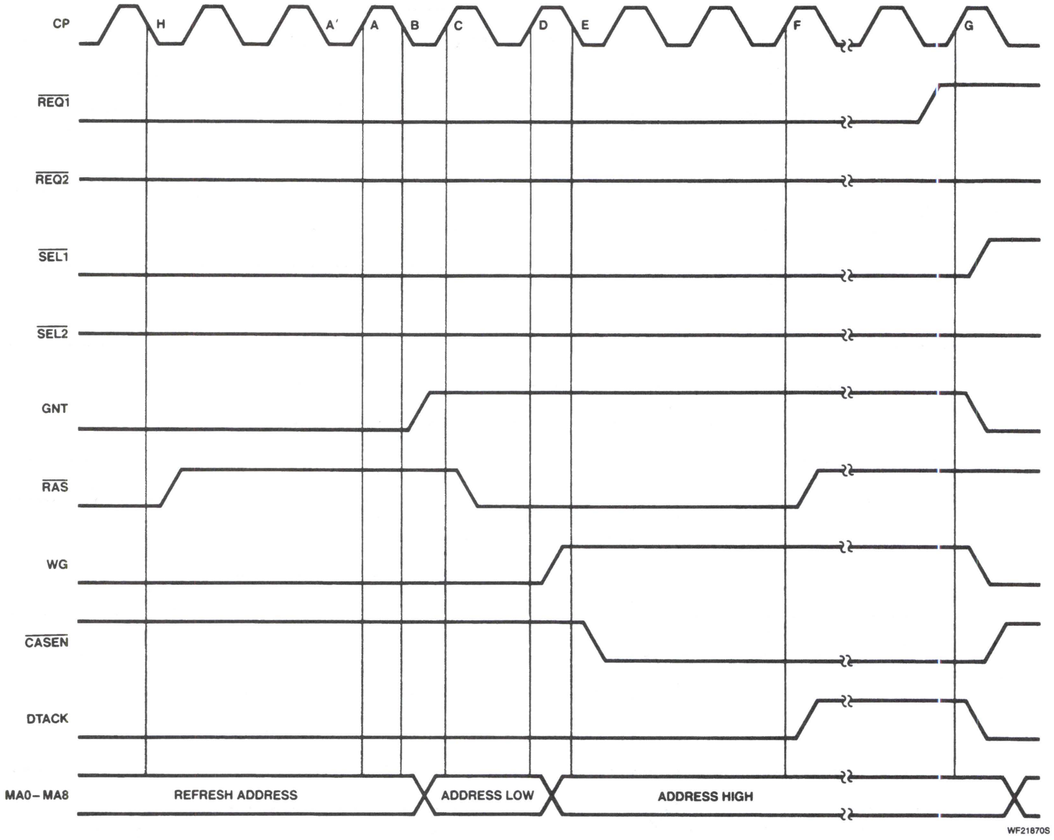

CP
H
A'
A
B
C
D
E
F
G
REQ1
REQ2
SEL1
SEL2
GNT
RAS
WG
CASEN
DTACK
MA0 – MA8
REFRESH ADDRESS
ADDRESS LOW
ADDRESS HIGH
WF21870S

Figure 10. Request 1 ($\overline{REQ_1}$) Memory Access Cycle Timing Following a Refresh Cycle for F764/765 and F764A/765A

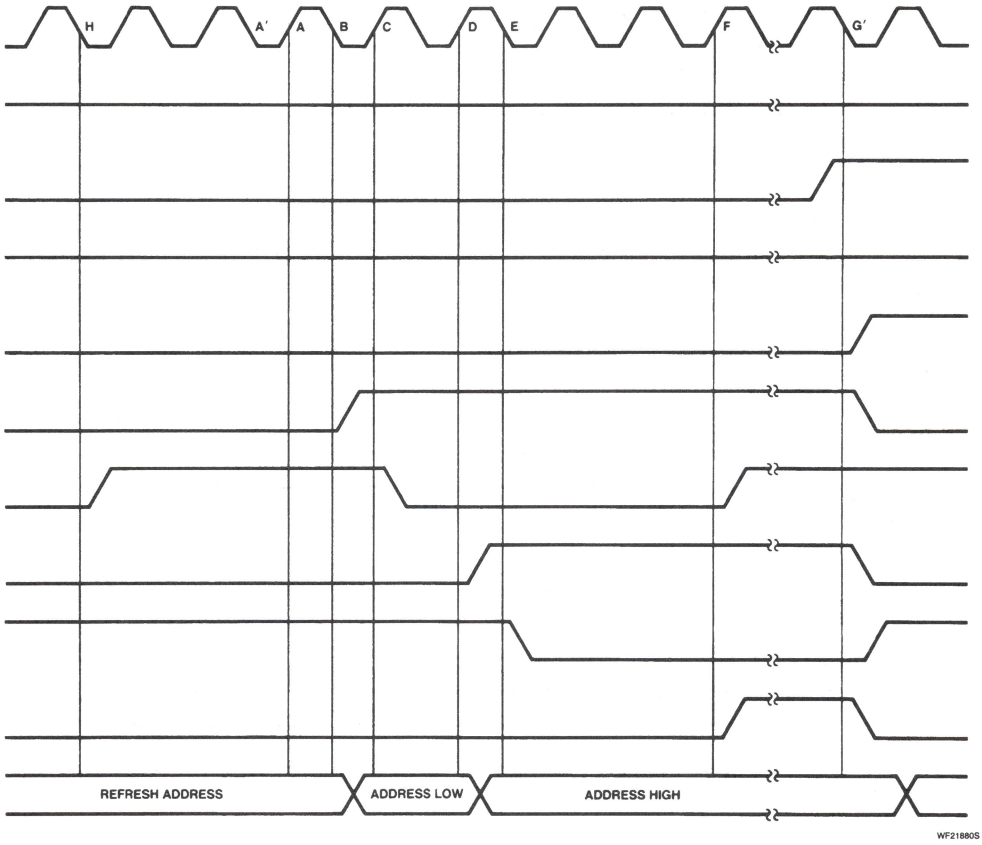

CP
H
A′
A
B
C
D
E
F
G′
REQ1
REQ2
SEL1
SEL2
GNT
RAS
WG
CASEN
DTACK
MA0 – MA8
REFRESH ADDRESS
ADDRESS LOW
ADDRESS HIGH
WF21880S

Figure 11. Request 2 ($\overline{REQ_2}$) Memory Access Cycle Timing Following a Refresh Cycle for F764/765 and F764A/765A

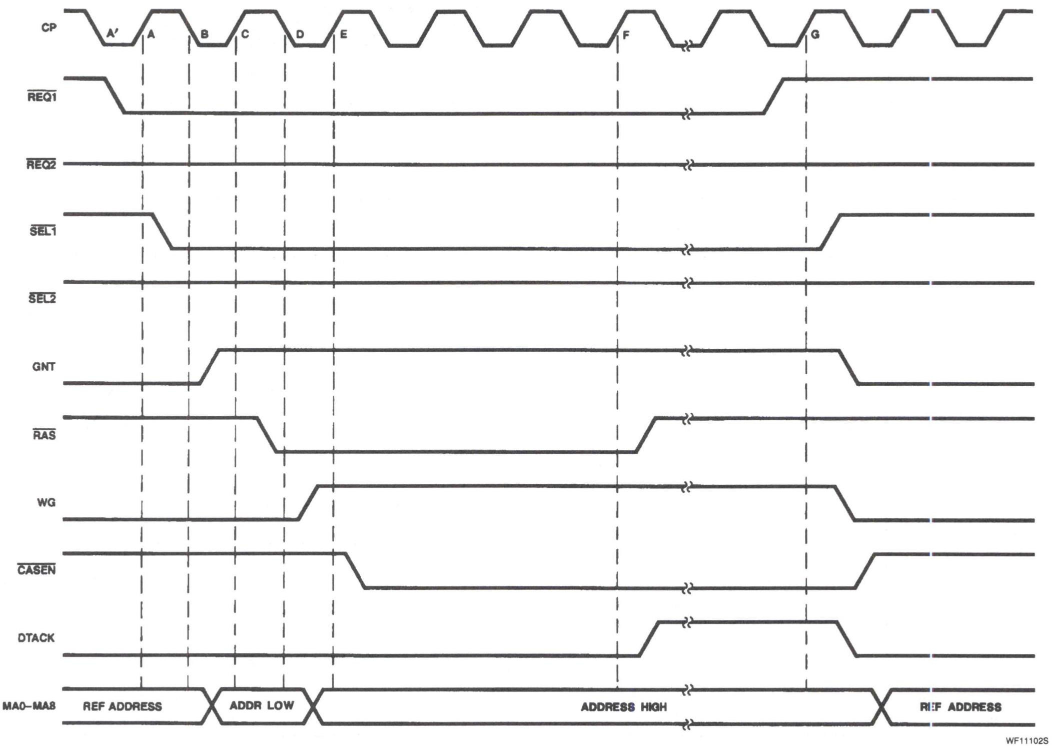

CP
A'
A
B
C
D
E
F
G
$\overline{REQ1}$
$\overline{REQ2}$
$\overline{SEL1}$
$\overline{SEL2}$
GNT
$\overline{RAS}$
WG
$\overline{CASEN}$
DTACK
MA0–MA8
REF ADDRESS
ADDR LOW
ADDRESS HIGH
REF ADDRESS
WF11102S

Figure 12. Request 1 ($\overline{REQ_1}$) Memory Access Cycle Timing for F764-1/765-1

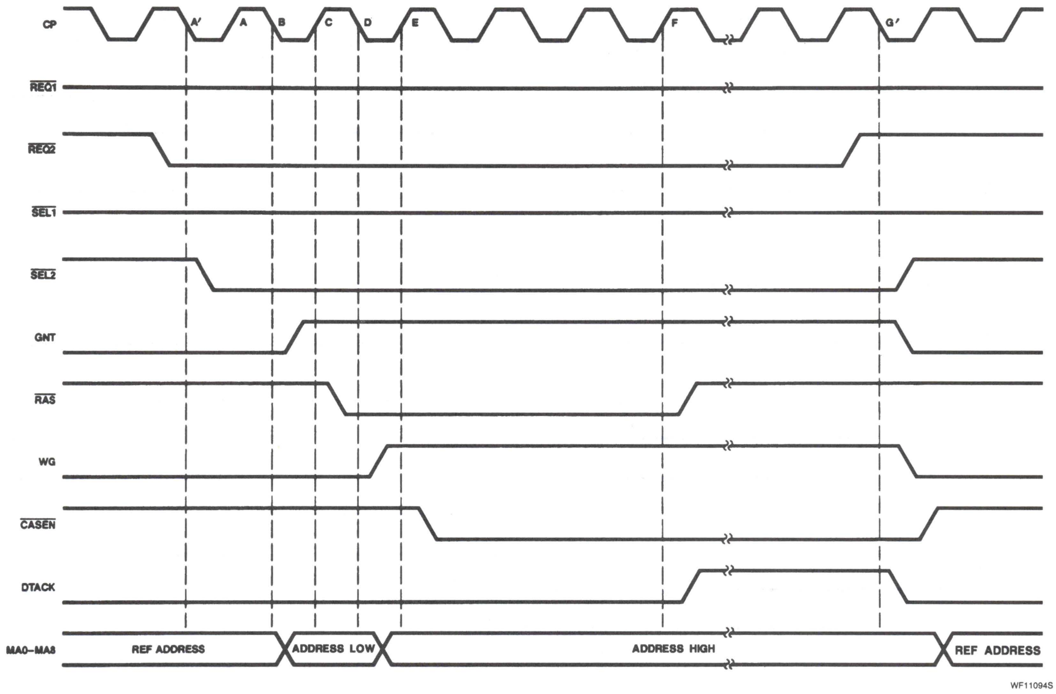

CP
A'
A
B
C
D
E
F
G'
$\overline{REQ1}$
$\overline{REQ2}$
$\overline{SEL1}$
$\overline{SEL2}$
GNT
$\overline{RAS}$
WG
$\overline{CASEN}$
DTACK
MA0–MA8
REF ADDRESS
ADDRESS LOW
ADDRESS HIGH
REF ADDRESS
WF11094S

Figure 13. Request 2 ($\overline{REQ_2}$) Memory Access Cycle Timing for F764-1/765-1

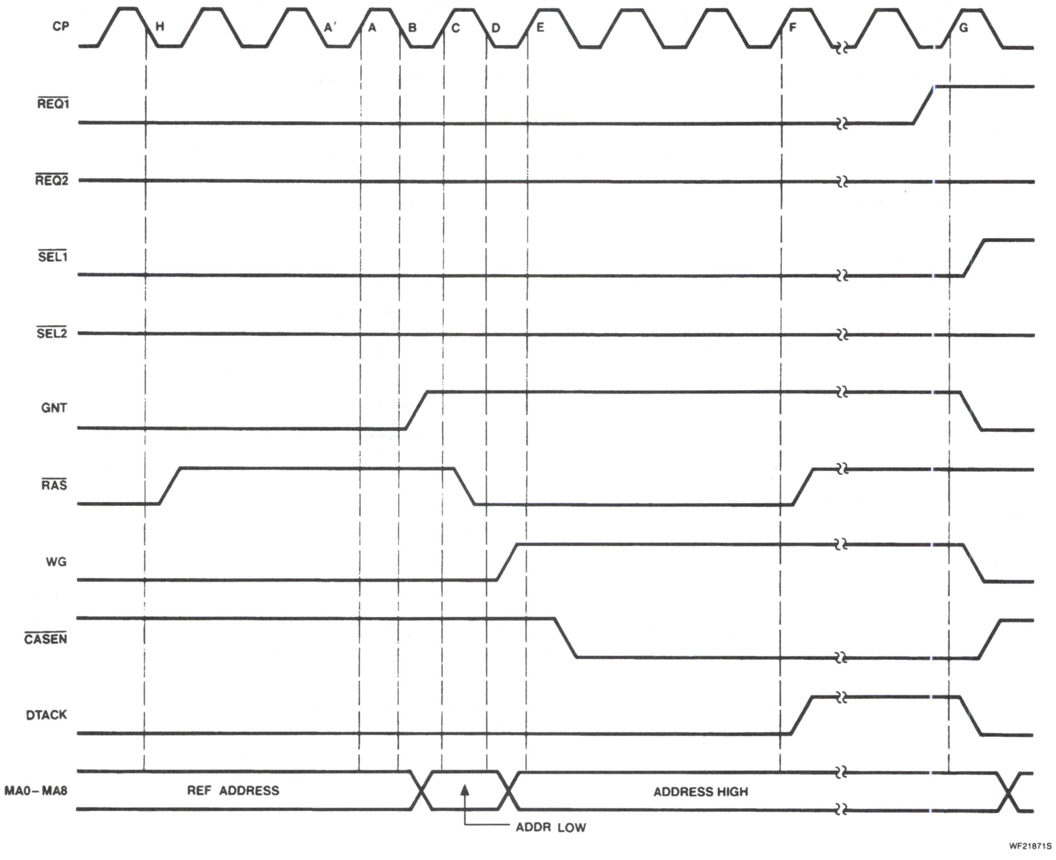

CP
H
A′
A
B
C
D
E
F
G
REQ1
REQ2
SEL1
SEL2
GNT
RAS
WG
CASEN
DTACK
MA0 – MA8
REF ADDRESS
ADDRESS HIGH
ADDR LOW
WF21871S

Figure 14. Request 1 ($\overline{REQ_1}$) Memory Access Cycle Timing Following a Refresh Cycle for F764-1/765-1

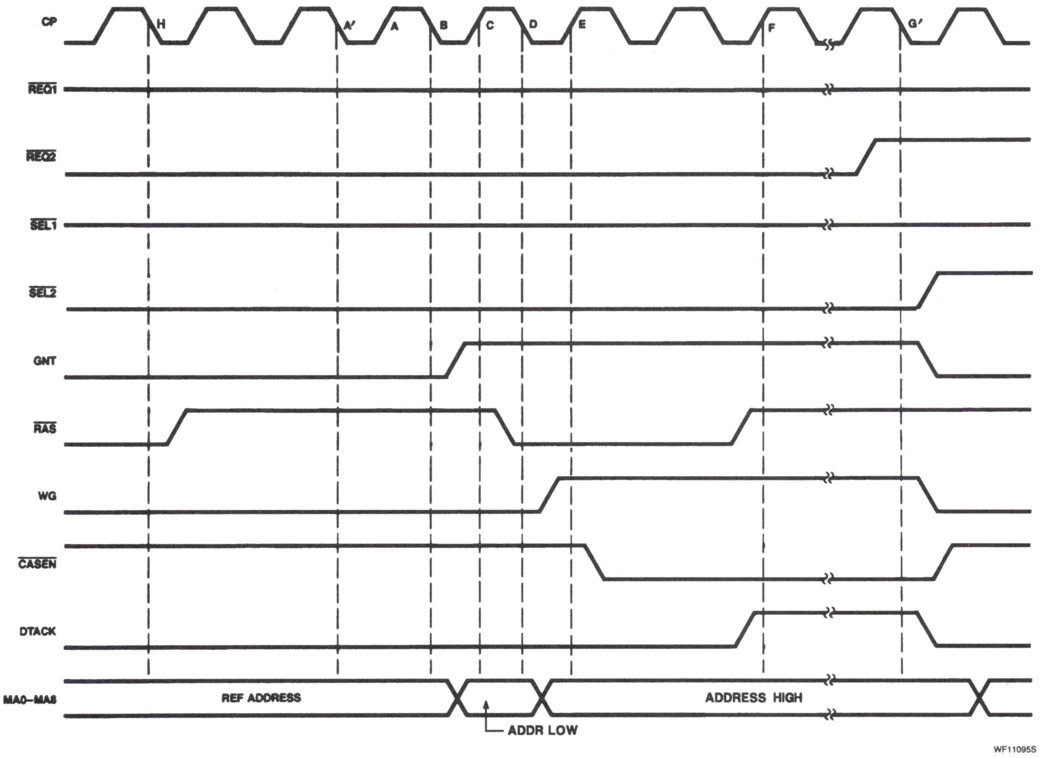

CP
H
A'
A
B
C
D
E
F
G'
$\overline{REQ1}$
$\overline{REQ2}$
$\overline{SEL1}$
$\overline{SEL2}$
GNT
$\overline{RAS}$
WG
$\overline{CASEN}$
DTACK
MA0–MA8
REF ADDRESS
ADDRESS HIGH
ADDR LOW
WF11095S

Figure 15. Request 2 ($\overline{REQ_2}$) Memory Access Cycle Timing Following a Refresh Cycle for F764-1/765-1

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range).

SYMBOL	PARAMETER	74F764/765, 74F764A/765A	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	500	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature range	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74F764/765, 74F764A/765A			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−15	mA
I_{OL}	Low-level output current[1]			24	mA
T_A	Operating free-air temperature[1]	0		70	°C

NOTE:

1. Transient currents will exceed these values in actual operation. Please refer to Appendix A for detailed discussion.

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			74F764/765, 74F764A/765A			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = −15mA	±10%V_{CC}	2.5	3.2		V
					±5%V_{CC}	2.7	3.4		V
V_{OH2}[3]	High-level output voltage			I_{OH2}[3] = −35mA	±5%V_{CC}	2.4			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 24mA	±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
V_{OL2}[4]	Low-level output voltage			I_{OL2}[4] = 60mA	±5%V_{CC}		0.45	0.80	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$				−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = 0.0V, V_I = 7.0V					100	μA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					−0.6	mA
I_{OS}	Short-circuit output current[5]		V_{CC} = MAX			−100		−225	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				150	200	mA
		I_{CCL}					165	210	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value under the recommended operating conditions for the applicable conditions.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Refer to Appendix A.
4. Refer to Appendix A.
5. Not more than one output should be shorted at a time. For testing I_{OS}, the use of High-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well over the normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER[1]	74F764/765, 74F764A/765A					UNIT
		$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 300pF$ $R_L = 70\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 300pF$ $R_L = 70\Omega$		
		Min	Typ	Max	Min	Max	
t_{PLH}	Propagation delay CP(G) to $\overline{SEL}_1$	5	10	14	5	16	ns
t_{PHL}	Propagation delay CP(A) to $\overline{SEL}_1$	5	10	14	5	16	ns
t_{PLH}	Propagation delay CP(G′) to $\overline{SEL}_2$	5	10	14	5	16	ns
t_{PHL}	Propagation delay CP(A′) to $\overline{SEL}_2$	5	10	14	5	16	ns
t_{PLH}	Propagation delay CP(B) to GNT	5	10	14	5	16	ns
t_{PHL}	Propagation delay CP(G or G′) to GNT	5	10	15	5	16	ns
t_{PLH} t_{PHL}	Propagation delay CP(B) to MA(row address)	5 5	12 11	17 15	5 5	18 16	ns
t_{PLH}	Propagation delay CP(F or H) to $\overline{RAS}$	5	10	14	5	16	ns
t_{PHL}	Propagation delay CP(C) to $\overline{RAS}$	5	10	14	5	16	ns
t_{PLH}	Propagation delay CP(D) to WG	5	10	14	5	16	ns
t_{PHL}	Propagation delay CP(G or G′) to WG	8	13	17	8	18	ns
t_{PLH} t_{PHL}	Propagation delay CP(D) to MA(column address)	5 5	12 10	17 15	5 5	18 16	ns
t_{PLH}	Propagation delay CP(G or G′) to $\overline{CASEN}$	7	17	23	7	25	ns
t_{PHL}	Propagation delay CP(E) to $\overline{CASEN}$	5	10	14	5	16	ns
t_{PLH}	Propagation delay CP(F) to DTACK	5	10	14	5	16	ns
t_{PHL}	Propagation delay CP(G or G′) to DTACK	6	13	17	5	18	ns
74F765, 74F765A Only							
t_{PLH} t_{PHL}	Propagation delay $A_1 - A_{18}$ to $MA_0 - MA_8$	4 2	7 5	12 8	4 4	13 19	ns

NOTE:

[1] For test conditions, see the AC waveforms.

AC SETUP AND HOLD REQUIREMENTS

SYMBOL	PARAMETER[2]	74F764/765, 74F764A/765A					UNIT
		$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 300pF$ $R_L = 70\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 300pF$ $R_L = 70\Omega$		
		Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{REQ}_1$, $\overline{REQ}_2$ to CP	2 2			2 2		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low CP to $\overline{REQ}_1$, $\overline{REQ}_2$	2 2			3 3		ns
$t_w(H)$ $t_w(L)$	CP pulse width High or Low	5 5			5 5		ns
$t_w(H)$ $t_w(L)$	RCP pulse width High or Low	10 10			10 10		ns
74F764, 74F764A Only							
$t_s(H)$ $t_s(L)$	Setup time, High or Low $A_1 - A_{18}$ to CP(↓)	−4[1] −4			−5 −5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low CP(↓) to $A_1 - A_{18}$	5 5			5 5		ns
74F764/765 Only							
f_{MAX}	Input clock frequency	100	150		100		MHz
74F764A/765A Only							
f_{MAX}	Input clock frequency	150	175		150		MHz

NOTES:

1. These numbers indicate that the address inputs have a negative setup time and could be valid 4ns after the falling edge of the CP clock. It is suggested that $\overline{SEL}_2$ be used to enable Address Bus 2 and the opposite polarity of the same be used, instead of $\overline{SEL}_1$ to enable Address Bus 1. This will insure that setup time for Address Bus 1 is not violated.
2. For the Test Conditions, see the AC Waveforms.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range).

SYMBOL	PARAMETER	74F764-1/765-1	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	500	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature range	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74F764-1/765-1			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current[1]			−20	mA
I_{OL}	Low-level output current[1]			8	mA
T_A	Operating free-air temperature	0		70	°C

NOTE:

1. Transient currents will exceed these values in actual operation. Please refer to Appendix A for detailed discussion.

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]			74F764-1, 74F765-1			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	$I_{OH} = -20mA$	±10%V_{CC}	2.4	2.70		V
				±5%V_{CC}	2.6	3.0		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	$I_{OL} = 8mA$	±10%V_{CC}		0.30	0.50	V
				±5%V_{CC}		0.30	0.50	V
V_{OL2}[3]	Low-level output voltage		I_{OL2}[3] = 75mA	±5%V_{CC}		2.1	2.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, $I_I = I_{IK}$				−0.7	−1.2	V
I_I	Input current at maximum input voltage	V_{CC} = 0.0V, V_I = 7.0V					100	μA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V				−0.2	−0.6	mA
I_{OS}	Short-circuit output current[4]	V_{CC} = MAX			−80	−150	−225	mA
I_{CC}	Supply current (total) I_{CCH}	V_{CC} = MAX				120	165	mA
	I_{CCL}					125	170	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value under the recommended operating conditions for the applicable conditions.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Refer to Appendix A.
4. Not more than one output should be shorted at a time. For testing I_{OS}, the use of High-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well over the normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	74F764-1/765-1					UNIT
		$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 300pF$ $R_L = 70\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 300pF$ $R_L = 70\Omega$		
		Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	100	150		100		MHz
t_{PLH}	Propagation delay CP(G) to $\overline{SEL}_1$	9	12	15	8	17	ns
t_{PHL}	Propagation delay CP(A) to $\overline{SEL}_1$	13	16	20	12	22	ns
t_{PLH}	Propagation delay CP(G′) to $\overline{SEL}_2$	9	12	15	8	17	ns
t_{PHL}	Propagation delay CP(A′) to $\overline{SEL}_2$	13	16	20	12	22	ns
t_{PLH}	Propagation delay CP(B) to GNT	9	12	14	8	16	ns
t_{PHL}	Propagation delay CP(G or G′) to GNT	20	23	26	17	28	ns
t_{PLH} t_{PHL}	Propagation delay CP(B) to MA(row address)	11 14	14 18	17 22	10 13	19 24	ns
t_{PLH}	Propagation delay CP(F or H) to $\overline{RAS}$	11	14	16	10	18	ns
t_{PHL}	Propagation delay CP(C) to $\overline{RAS}$	13	17	20	12	22	ns
t_{PLH}	Propagation delay CP(D) to WG	9	11	14	8	16	ns
t_{PHL}	Propagation delay CP(G or G′) to WG	20	23	26	19	26	ns
t_{PLH} t_{PHL}	Propagation delay CP(D) to MA(column address)	12 14	14 18	17 21	11 13	19 23	ns
t_{PLH}	Propagation delay CP(G or G′) to $\overline{CASEN}$	14	17	20	12	22	ns
t_{PHL}	Propagation delay CP(E) to $\overline{CASEN}$	14	16	19	13	21	ns
t_{PLH}	Propagation delay CP(F) to DTACK	10	12	15	9	17	ns
t_{PHL}	Propagation delay CP(G or G′) to DTACK	20	23	26	19	28	ns
74F765-1 Only							
t_{PLH} t_{PHL}	Propagation delay $A_1 - A_{18}$ to $MA_0 - MA_8$	9 9	11 12	14 15	8 8	16 17	ns

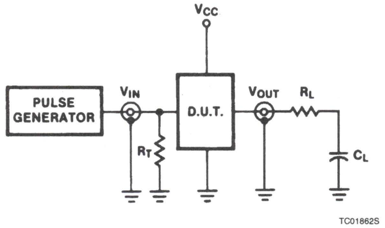
AC SETUP AND HOLD REQUIREMENTS

SYMBOL	PARAMETER	74F764-1/765-1					UNIT
		$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 300pF$ $R_L = 70\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 300pF$ $R_L = 70\Omega$		
		Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{REQ}_1$, $\overline{REQ}_2$ to CP	3	1		4		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low CP to $\overline{REQ}_1$, $\overline{REQ}_2$	2	0		3		ns
$t_w(H)$ $t_w(L)$	CP pulse width High or Low	5	3		5		ns
$t_w(H)$ $t_w(L)$	RCP pulse width High or Low	5			5		ns
74F764-1 Only							
$t_s(H)$ $t_s(L)$	Setup time, High or Low $A_1 - A_{18}$ to CP(↓)	0	−1[1]		1		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low CP(↓) to $A_1 - A_{18}$	5	3		6		ns

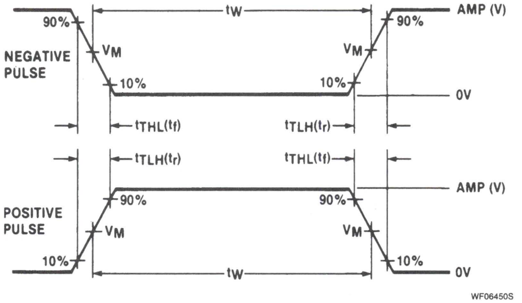
NOTE:

1. These numbers indicate that the address inputs have a negative setup time and could be valid 1ns after the falling edge of the CP clock. It is suggested that $\overline{SEL}_2$ be used to enable Address Bus 2 and the opposite polarity of the same be used, instead of $\overline{SEL}_1$ to enable Address Bus 1. This will insure that setup time for Address Bus 1 is not violated.

TEST CIRCUIT AND WAVEFORMS FOR ALL DEVICES



Test Circuit Simulating RAM Boards



$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS

R_L = Load resistor to GND; see AC Characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

APPLICATIONS

The DRAM dual-ported controller can be designed into a wide range of single and dual-port interface configurations. The processors could be general or special-purpose (microcontrollers) and the data bus may differ in size.

Figure 16 shows a 68000 processor sharing a 64K × 8 (two banks each consisting of sixteen 16K × 1 devices) memory with a Z-80 processor. Since neither Z-80 nor 68000 have multiplexed address and data bus, the 'F765/F765A/F765-1 is appropriate.

Since the Z-80 has an 8-bit wide data bus, data buffers are used to convert the 16-bit memory data bus to an 8-bit wide processor bus. Address bit (A_0) from the Z-80 serves as an enable to one of the two data buffers at a given time. Address bit (A_{15}) from either the Z-80 or the 68000 distinguishes between Memory Banks A and B. Where Bank A consists of Upper Data Byte A (UDBA) and Lower Data Byte A (LDBA) and Bank B consists of Upper Data Byte B (UDBB) and Lower Data Byte B (LDBB).

When the Z-80 is selected and A_{15} is a zero, all even bytes will be accessed from UDBA and all odd bytes from LDBA. Similarly, when A_{15} is a one, UDBB will contain all even bytes and LDBB all odd bytes.

For 68000, Upper and Lower Data Strobes ($\overline{UDS}$ and $\overline{LDS}$) determine whether a byte or word transfer will take place. The $\overline{WAIT}$ input on the Z-80 is asserted when $\overline{REQ_1}$ is generated, and is negated when the GNT output is asserted by the controller. The additional gating circuitry is to ensure that $\overline{DTACK}$ to the 68000 is asserted only when it is selected.

Figure 17 shows two 8086 processors sharing 1MByte (two banks each consisting of sixteen 256K × 1 devices) of dynamic RAM. Using 74F764 in this application may eliminate the need for an external address latch.

Similarly, Figure 18 shows two 68020 processors sharing the same amount of memory.

APPLICATIONS

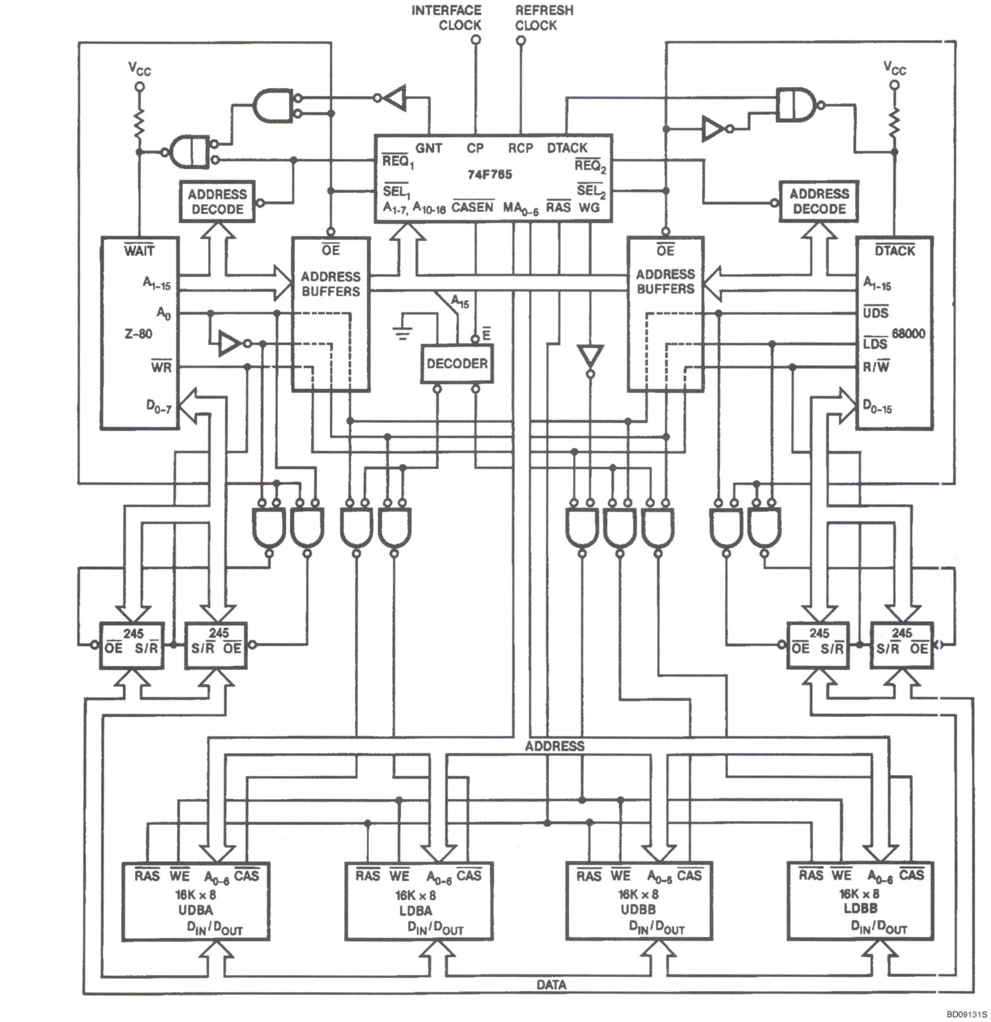
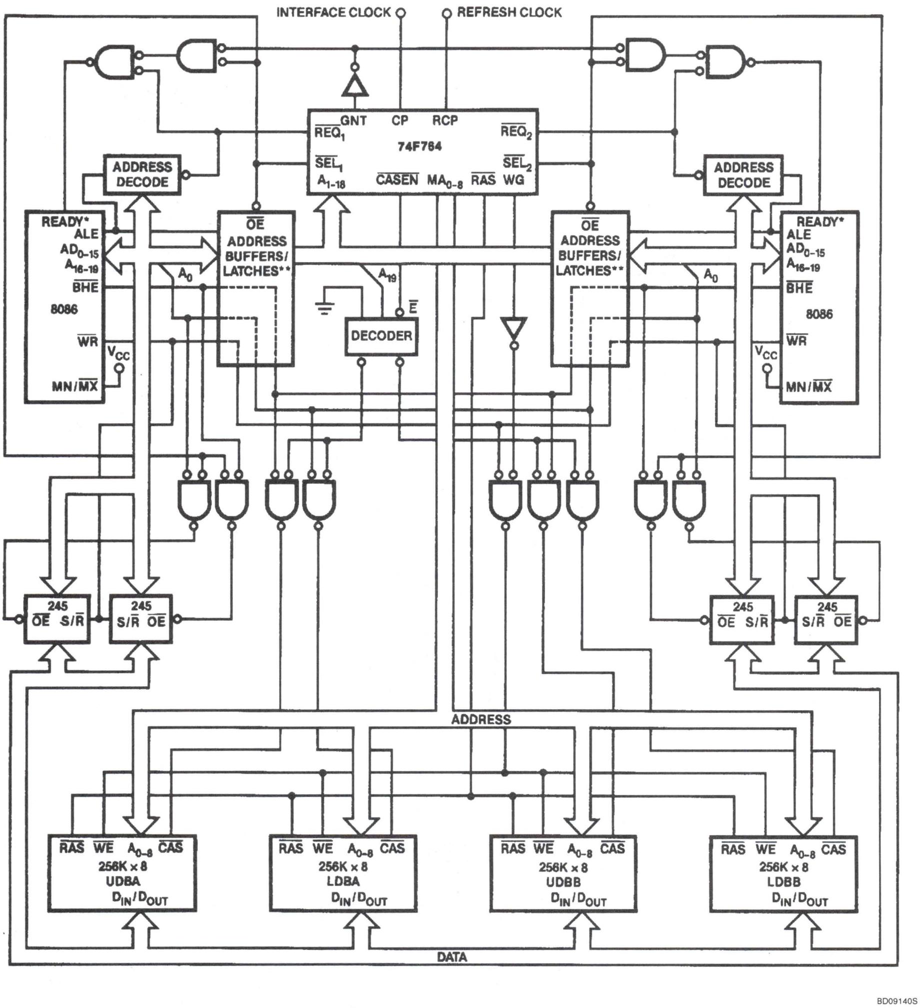

INTERFACE CLOCK
REFRESH CLOCK
V_{CC}
V_{CC}
GNT
CP
RCP
DTACK
$\overline{REQ_1}$
74F765
$\overline{REQ_2}$
$\overline{SEL_1}$
$\overline{SEL_2}$
A_{1-7}, A_{10-16}
$\overline{CASEN}$
MA_{0-6}
$\overline{RAS}$
WG
ADDRESS DECODE
ADDRESS DECODE
$\overline{WAIT}$
A_{1-15}
A_0
Z-80
$\overline{WR}$
D_{0-7}
$\overline{OE}$
ADDRESS BUFFERS
A_{15}
$\overline{E}$
DECODER
$\overline{OE}$
ADDRESS BUFFERS
$\overline{DTACK}$
A_{1-15}
$\overline{UDS}$
$\overline{LDS}$
68000
$R/\overline{W}$
D_{0-15}
245
$\overline{OE}$ $S/\overline{R}$
245
$S/\overline{R}$ $\overline{OE}$
245
$\overline{OE}$ $S/\overline{R}$
245
$S/\overline{R}$ $\overline{OE}$
ADDRESS
$\overline{RAS}$ $\overline{WE}$ A_{0-6} $\overline{CAS}$
16K x 8
UDBA
D_{IN}/D_{OUT}
$\overline{RAS}$ $\overline{WE}$ A_{0-6} $\overline{CAS}$
16K x 8
LDBA
D_{IN}/D_{OUT}
$\overline{RAS}$ $\overline{WE}$ A_{0-6} $\overline{CAS}$
16K x 8
UDBB
D_{IN}/D_{OUT}
$\overline{RAS}$ $\overline{WE}$ A_{0-6} $\overline{CAS}$
16K x 8
LDBB
D_{IN}/D_{OUT}
DATA
BD09131S

Figure 16. A 68000 Processor Sharing 64K × 8 DRAM With a Z-80

APPLICATIONS


INTERFACE CLOCK
REFRESH CLOCK
GNT
CP
RCP
REQ1
74F764
REQ2
SEL1
SEL2
A1-18
CASEN
MA0-8
RAS
WG
ADDRESS DECODE
ADDRESS DECODE
READY*
ALE
AD0-15
A16-19
BHE
8086
WR
VCC
MN/MX
OE
ADDRESS BUFFERS/ LATCHES**
A0
A19
E
DECODER
245
OE
S/R
ADDRESS
RAS
WE
A0-8
CAS
256K × 8
UDBA
LDBA
UDBB
LDBB
DIN/DOUT
DATA
BD09140S

* It might be necessary to synchronize READY by the 8284A. Please refer to the 8086 data sheet.
** Whether or not the 8086 address bus needs to be latched externally, should be determined by the relative speeds of the 8086 and the controller.

Figure 17. Two 8086 Processors Sharing 1MBYTE of DRAM

APPLICATIONS

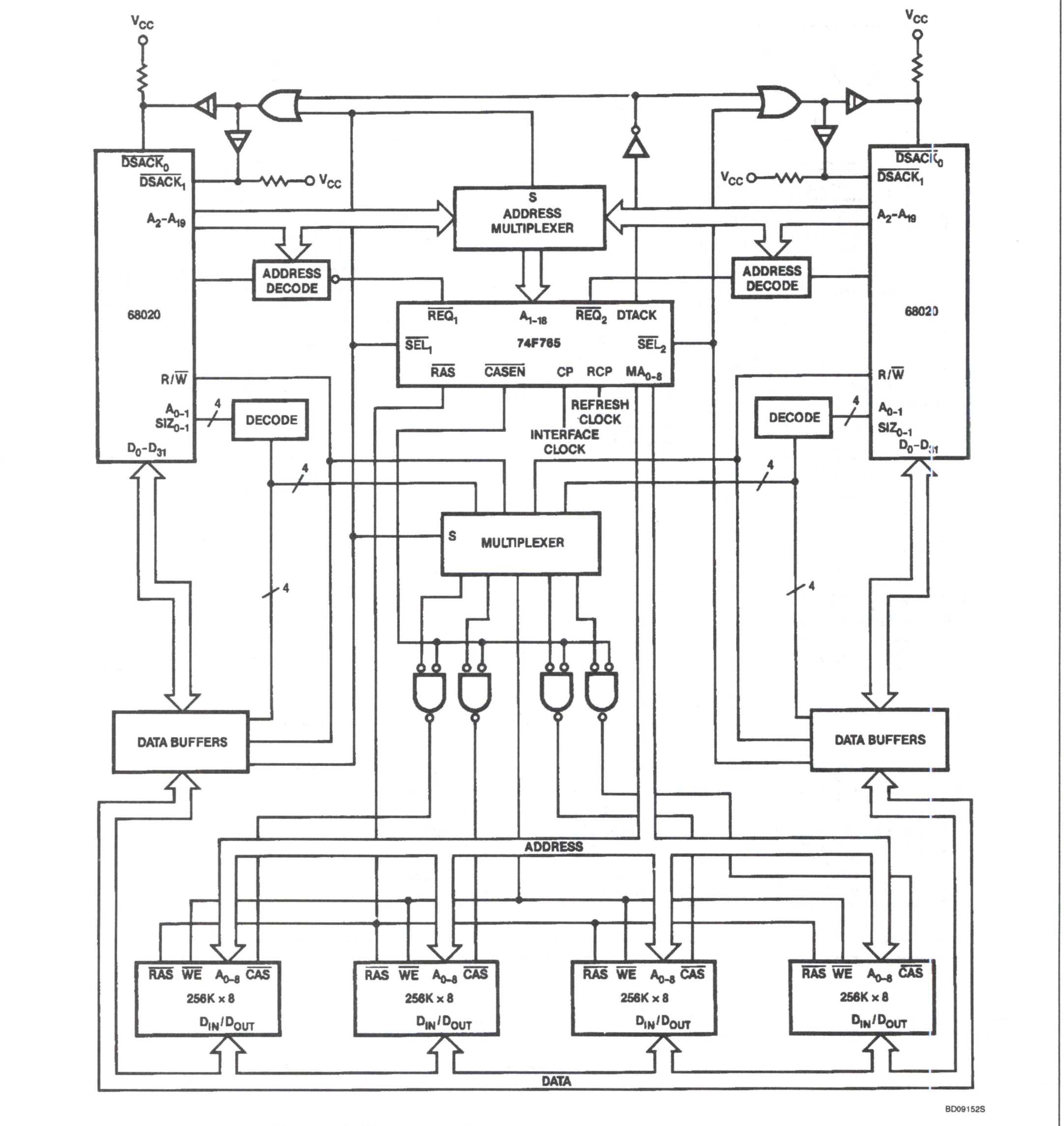

VCC
VCC
DSACK0
DSACK1
A2-A19
68020
R/W
A0-1
SIZ0-1
D0-D31
4
DECODE
ADDRESS DECODE
S
ADDRESS MULTIPLEXER
REQ1
A1-18
REQ2
DTACK
SEL1
74F765
SEL2
RAS
CASEN
CP
RCP
MA0-8
REFRESH CLOCK
INTERFACE CLOCK
S
MULTIPLEXER
DATA BUFFERS
ADDRESS
RAS WE A0-8 CAS
256K x 8
DIN/DOUT
DATA
BD09152S

Figure 18. Two 68020 Processors Sharing 1MBYTE of DRAM

74F764 FAMILY LINE DRIVING CHARACTERISTICS

The 74F764/765 and 74F764A/765A are designed to provide incident wave switching in Dual-Inline-Package (DIP) or Zig-zag-Inline-Package (ZIP) housed memory arrays and first reflected wave switching in Single-Inline-Package (SIP) or Single-Inline-Module (SIM) housed arrays. The 74F764-1/765-1, on the other hand, are designed to provide first reflected wave switching with as wide a range of characteristic impedances as possible.

The I_{OL2}/V_{OL2} and I_{OH2}/V_{OH2} parameters are included in the product specifications to assist engineers in designing systems which will switch memory array signal lines in the above mentioned manner. For example, the characteristic impedance of signal lines in DIP housed memory arrays is usually around 70Ω. If a signal line has settled out in a High state at 4 volts and must be pulled down to 0.8 volts or less on the incident wave, the DRAM Controller output must sink (4-0.8)/70A or 46mA at 0.8 volts. The I_{OL2}/V_{OL2} parameter indicates that the signal line in question will always be switched on the incident wave over the full commercial operating range.

It should be noted here that I_{OL2}/V_{OL2} and I_{OH2}/V_{OH2} are intended for transient use only and that steady state operation at I_{OH2} or I_{OL2} is not recommended (long term, steady state operation at these currents may result in electromigration).

Figures 1 – 4 show the output I/V characteristics of the DRAM Controller family of devices. These figures also demonstrate a graphical method for determining the incident wave (and first reflected wave) characteristics of the devices.

The suggested line termination for the 74F764/765 or 74F764A/765A driving dual-inline packaged or zig-zag packaged DRAMs is shown in Figure 8a. When driving single-inline modules using the 74F764/765 or 74F764A/765A, or when driving any type of memory arrays with the 74F764-1/765-1, the schottky diode termination shown in Figure 8b can be used (most of these will need no termination at all).

Figures 5 – 7 are double exposures showing the High to Low and Low to High transitions while driving four banks of eight Dual-Inline-Packaged DRAMs. The signal line is unterminated in Figures 5 and 6, allowing the 74F764/765/764A/765A to ring two volts below ground while the 74F764-1/765-1 make nice clean transitions. In Figure 7 the 74F764/765/764A/765A is driving the same signal line but with one of its four branches terminated with its characteristic impedance in series with 300pF to ground (the worst of the four branches is shown).

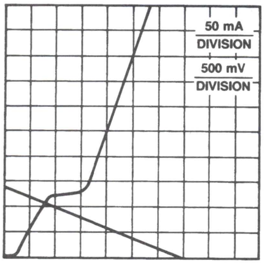


Figure 1. I-V Output Characteristics of the 74F764 and 765 in the Low State. Light Line is the I-V Curve of a 25Ω Transmission Line Settled to 3.5V (Typical for Recommended Termination). The High to Low Incident Wave on This Line Would Typically be to .8V

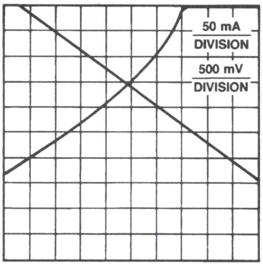


Figure 2. I-V Output Characteristics of the 74F764 and 765 in the High State. Light Line is the I-V Curve of a 35Ω Transmission Line Settled to .25V. The Incident Wave on the Low to High Transition Will Typically be to 2.4V on This Line. Any Line Over 35Ω Will Typically be Switched on the Incident Wave

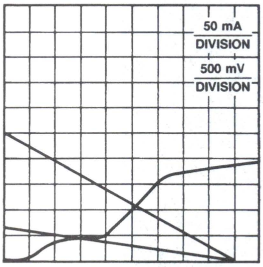


Figure 3. I-V Output Characteristics of the 74F764-1 and 765-1 in the Low State. Any Unterminated Line Impedance Between 18Ω and 70Ω (Both Shown) Will Typically Switch on the First Reflected Wave Without Violating the-1V Minimum Input Voltage Specification Typical of DRAMs

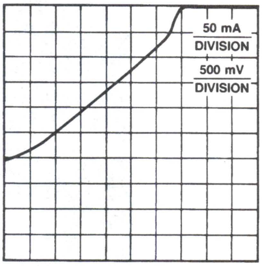


Figure 4. I-V Output Characteristics of the 74F764-1 and 765-1 While in the High State

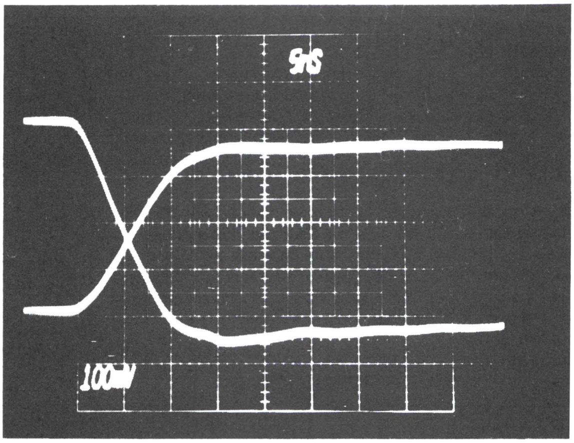


Figure 5. 74F764-1/765-1 Driving 32 DRAMs (Unterminated)

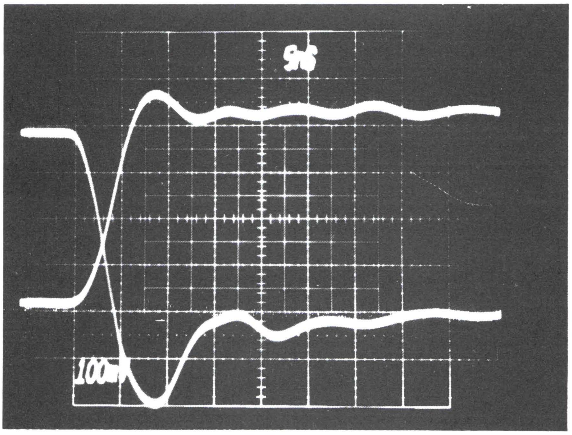


Figure 6. 74F764/765/764A/765A Driving 32 DRAMs (Unterminated)

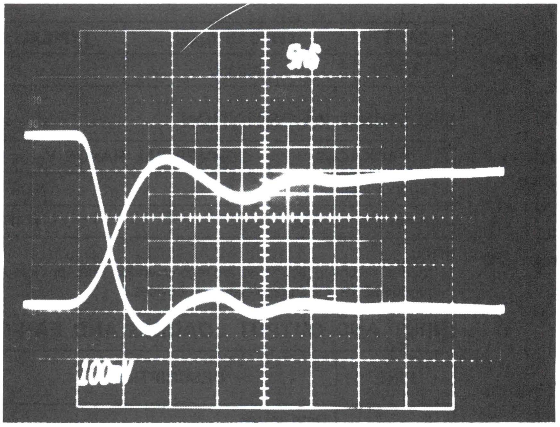


Figure 7. 74F764/765/764A/765A Driving 32 DRAMs (Terminated as in Figure 8a)

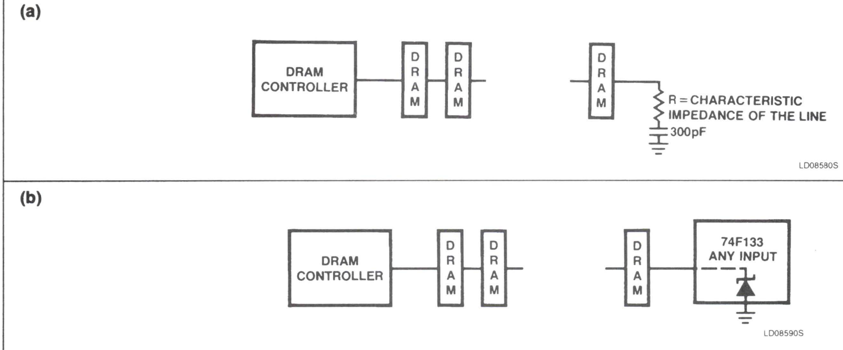

(a)
DRAM CONTROLLER
DRAM
DRAM
DRAM
R = CHARACTERISTIC IMPEDANCE OF THE LINE
300pF
LD08580S
(b)
DRAM CONTROLLER
DRAM
DRAM
DRAM
74F133 ANY INPUT
LD08590S

Figure 8

Signetics

FAST 74F779
8-Bit Counter

8-Bit Bidirectional Binary Counter (3-State)
Product Specification

FAST Products

FEATURES

- **Multiplexed 3-State I/O ports for bus oriented applications**
- **Built-in look-ahead carry capability**
- **Center power pins to reduce effects of package inductance**
- **Count frequency 145MHz typical**
- **Supply current 90mA typical**
- **See 'F269 for 24-pin separate I/O port version**
- **See 'F579 for 20-pin version**

DESCRIPTION

The 'F779 is a fully synchronous 8-stage up/down counter with multiplexed 3-State I/O ports for bus-oriented applications. All control functions (hold, count up, count down, synchronous load) are controlled by two mode pins (S_0, S_1). The device also features carry look-ahead for easy cascading. All state changes are initiated by the rising edge of the clock.

When $\overline{CET}$ is High the data outputs are held in their current state and $\overline{TC}$ is held High. The $\overline{TC}$ output is not recommended for use as a clock or asynchronous reset due to the possibility of decoding spikes.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F779	145MHz	90mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
16-Pin Plastic DIP	N74F779N
16-Pin Plastic SOL[1]	N74F779D

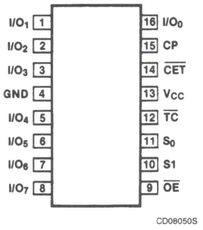
NOTE:
1. Thermal mounting techniques are recommended. See App Note AN SMD-100 for a discussion of thermal considerations for surface mounted devices.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

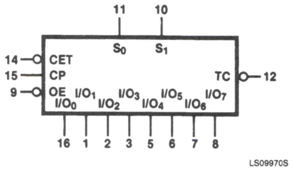
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$I/O_0 - I/O_7$	Data inputs	3.5/1.0	70μA/0.6mA
	Data outputs	150/40	3mA/24mA
S_0, S_1	Select inputs	1.0/1.0	20μA/0.6mA
$\overline{OE}$	Output enable input (active-Low)	1.0/1.0	20μA/0.6mA
$\overline{CET}$	Count enable trickle input (active-Low)	1.0/1.0	20μA/0.6mA
CP	Clock input pulse (active rising edge)	1.0/1.0	20μA/0.6mA
$\overline{TC}$	Terminal count output (active-Low)	50/33	1mA/20mA

NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION

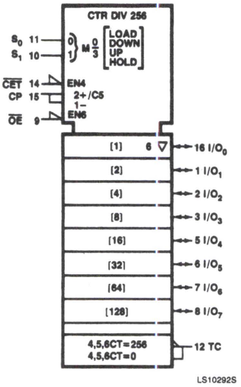

I/O1 1
I/O2 2
I/O3 3
GND 4
I/O4 5
I/O5 6
I/O6 7
I/O7 8
16 I/O0
15 CP
14 CET
13 Vcc
12 TC
11 S0
10 S1
9 OE
CD08050S

LOGIC SYMBOL


11
10
S0
S1
14
15
9
CET
CP
OE
TC
12
I/O0
I/O1
I/O2
I/O3
I/O4
I/O5
I/O6
I/O7
16 1 2 3 5 6 7 8
LS09970S

V_{CC} = Pin 13
GND = Pin 4

LOGIC SYMBOL (IEEE/IEC)

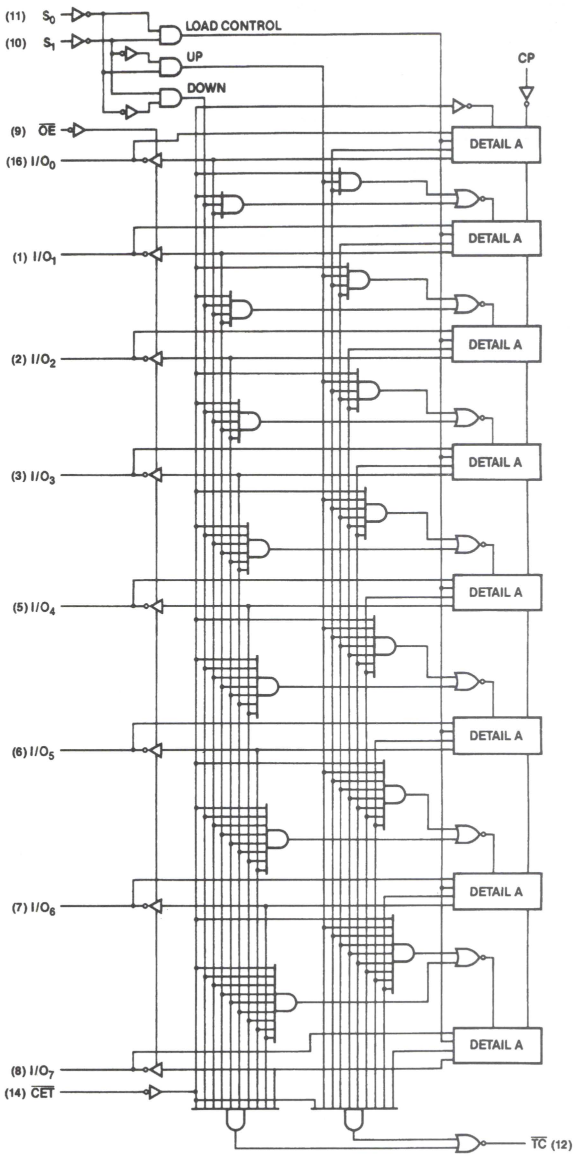

CTR DIV 256
S0 11
S1 10
0
1
M 0/3
LOAD
DOWN
UP
HOLD
CET 14
CP 15
OE 9
EN4
2+/C5
1−
EN6
[1]
6
16 I/O0
[2]
1 I/O1
[4]
2 I/O2
[8]
3 I/O3
[16]
5 I/O4
[32]
6 I/O5
[64]
7 I/O6
[128]
8 I/O7
4,5,6CT=256
4,5,6CT=0
12 TC
LS10292S

FUNCTION TABLE

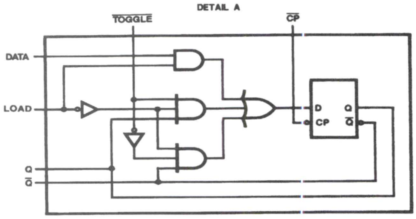
INPUTS					OPERATING MODE
S1	S0	$\overline{CET}$	$\overline{OE}$	CP	
X	X	X	H	X	I/Oa to I/Oh in Hi-Z
X	X	X	L	X	Flip-flop outputs appear on I/O lines
L	L	X	X	↑	Parallel load all flip-flops
(not LL)		H	X	↑	Hold ($\overline{TC}$ held High)
H	L	L	X	↑	Count up
L	H	L	X	↑	Count down

H = High voltage level
L = Low voltage level
X = don't care
↑ = Low-to-High clock transition
(not LL) = $\overline{CS}$ and $\overline{PE}$ should never be Low voltage level at the same time in the hold mode only.

LOGIC DIAGRAM


(11) S0
(10) S1
LOAD CONTROL
UP
DOWN
CP
(9) OE
(16) I/O0
(1) I/O1
(2) I/O2
(3) I/O3
(5) I/O4
(6) I/O5
(7) I/O6
(8) I/O7
(14) CET
DETAIL A
TC (12)

LD04181S


DETAIL A
TOGGLE
CP
DATA
LOAD
Q
Q̄
D
Q
CP
Q̄

LD03904S

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		−0.5 to +7.0	V
V_{IN}	Input voltage		−0.5 to +7.0	V
I_{IN}	Input current		−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		−0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	$\overline{TC}$	40	mA
		I/O_n	48	mA
T_A	Operating free-air temperature range		0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.50	5.0	5.50	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	High-level output current	$I/O_0 - I/O_7$			−3	mA
		$\overline{TC}$			−1	mA
I_{OL}	Low-level output current	$I/O_0 - I/O_7$			24	mA
		$\overline{TC}$			20	mA
T_A	Operating free-air temperature		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage	$\overline{TC}$	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = −1mA	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7	3.4		V
		I/O$_n$		I_{OH} = −3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX		±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$				−0.73	−1.2	V
I_I	Input current at maximum input voltage	I/O$_n$	V_{CC} = MAX, V_I = 7.0V					1.0	μA
		others	V_{CC} = 5.5V, V_I = 5.5V					100	mA
I_{IH}	High-level input current	except I/O$_n$	V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					−0.6	mA
$I_{OZH} + I_{IH}$	OFF-state current High-level voltage applied	I/O$_n$	V_{CC} = MAX, V_O = 2.7V					70	μA
$I_{OZL} + I_{IL}$	OFF-state current Low-level voltage applied		V_{CC} = MAX, V_O = 0.5V					−600	μA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX			−60		−150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				82	116	mA
		I_{CCL}					91	128	mA
		I_{CCZ}					97	136	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

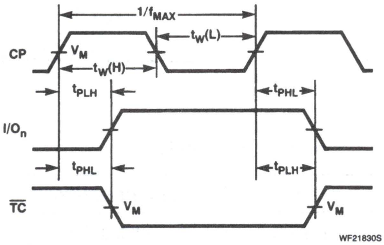
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C V_{CC} = +5.0V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	125	145		115		MHz
t_{PLH} t_{PHL}	Propagation delay CP to I/O$_n$	Waveform 1	4.5 5.5	7.0 8.0	10.5 10.5	4.5 5.5	11.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{TC}$	Waveform 1	4.5 4.5	7.0 7.0	9.0 9.0	4.5 4.5	10.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CET}$ to $\overline{TC}$	Waveform 2	3.0 3.0	4.5 5.5	6.5 7.5	2.5 2.5	7.5 8.0	ns
t_{PZH} t_{PZL}	Disable time from High or Low level	Waveform 4 Waveform 5	2.5 4.5	4.5 6.5	7.0 9.0	2.5 4.5	8.0 9.5	ns
t_{PHZ} t_{PLZ}	Enable time from High or Low level	Waveform 4 Waveform 5	1.0 1.0	3.0 4.0	6.5 7.0	1.0 1.0	8.0 8.0	ns

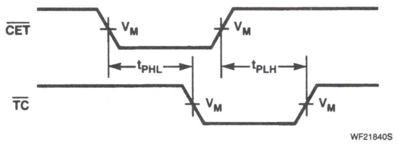
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			LIMITS $T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		UNIT
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low I/O_n to CP	Waveform 3	5.0 5.0			5.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low I/O_n to CP	Waveform 3	1.0 1.0			1.0 1.0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{CET}$ to CP	Waveform 3	5.0 5.5			5.0 6.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{CET}$ to CP	Waveform 3	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low S_n to CP	Waveform 3	8.0 8.0			8.5 8.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low S_n to CP	Waveform 3	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	Clock pulse width High or Low	Waveform 1	4.0 4.0			4.0 4.0		ns

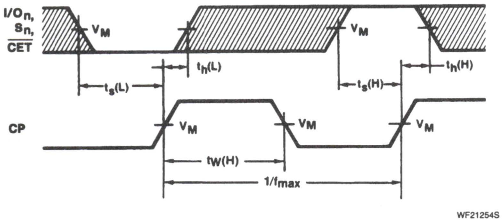
AC WAVEFORMS


1/f_MAX
t_w(L)
CP
V_M
t_w(H)
t_PLH
t_PHL
I/O_n
t_PHL
t_PLH
TC
V_M
V_M
WF21830S

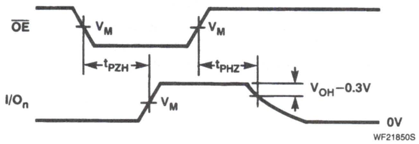
Waveform 1. Propagation Delay, Clock input to Output, Clock Widths and Maximum Clock Frequency


CET
V_M
V_M
t_PHL
t_PLH
TC
V_M
V_M
WF21840S

Waveform 2. Propagation Delay, $\overline{CET}$ input to Terminal Count Output

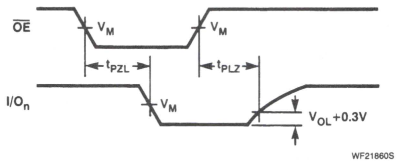

I/O_n, S_n, CET
V_M
V_M
t_h(L)
t_h(H)
t_s(L)
t_s(H)
CP
V_M
V_M
V_M
tw(H)
1/f_max
WF21254S

Waveform 3. Setup and Hold Times


OE
V_M
V_M
t_PZH
t_PHZ
V_OH−0.3V
I/O_n
V_M
0V
WF21850S

Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time From High Level

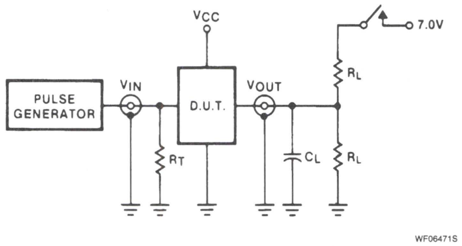
AC WAVEFORMS (Continued)


$\overline{OE}$
V_M
V_M
t_{PZL}
t_{PLZ}
I/O_n
V_M
$V_{OL}+0.3V$
WF21860S

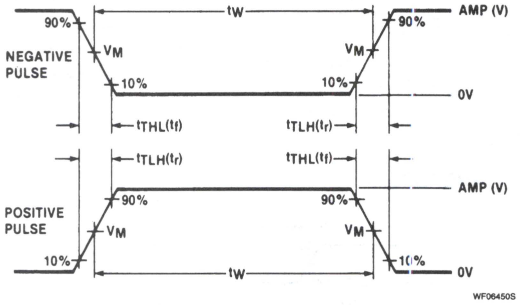
Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS


VCC
7.0V
R_L
PULSE GENERATOR
VIN
D.U.T.
VOUT
R_T
C_L
R_L
WF06471S

Test Circuit for 3-State Outputs


90%
tW
90%
AMP (V)
NEGATIVE PULSE
VM
VM
10%
10%
0V
tTHL(tf)
tTLH(tr)
tTLH(tr)
tTHL(tf)
AMP (V)
POSITIVE PULSE
90%
90%
VM
VM
10%
10%
tW
0V
WF06450S

$V_M = 1.5V$
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS
R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F784
Multiplier

8-Bit Serial/Parallel Multiplier (With Adder/Subtracter)
Preliminary Specification

FAST Products

FEATURES

- Serial (n × 8)-bit multiplication
- Final stage adder/subtracter for optional use in adding a B bit to obtain S± B.
- Two's Complement multiplication
- Cascadable for any number of bits
- Full Adder and B – 1 input included for maximum flexibility
- Maximum clock frequency 50MHz guaranteed
- Supply current 100mA max

DESCRIPTION

The 'F784 is a serial (n × 8)-bit multiplier with a final stage adder/subtracter for optional use in adding a B bit to obtain S± B. A 'B – 1' bit can also be added via an internal flip-flop to achieve a 1-bit delay. The X word is parallel loaded (8 bits wide) into latches and the Y word is clocked in serially from a shift register. The 'F784 is particularly useful for high-speed digital filtering or butterfly networks in fast Fourier transforms.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F784	65MHz	67mA

ORDERING INFORMATION

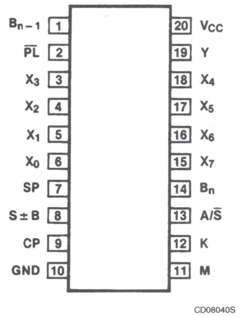
PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
20-Pin Plastic DIP	N74F784N
20-Pin Plastic SOL	N74F784D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$X_0 - X_7$	Multiplicand data inputs	1.0/1.0	20μA/0.6mA
Y	Serial multiplier input	1.0/1.0	20μA/0.6mA
CP	Clock Pulse input	1.0/1.0	20μA/0.6mA
K	Serial expansion input	1.0/1.0	20μA/0.6mA
M	Mode control input	1.0/1.0	20μA/0.6mA
$\overline{PL}$	Parallel Load input	1.0/2.0	20μA/1.2mA
$A/\overline{S}$	Add/subtract input	1.0/1.0	20μA/0.6mA
B_n	Serial B input	1.0/1.0	20μA/0.6mA
B_{n-1}	Delayed serial B input	1.0/1.0	20μA/0.6mA
SP	Serial X·Y product output	50/33.3	1mA/20mA
S± B	Serial Y·Y± B output	50/33.3	1mA/20mA

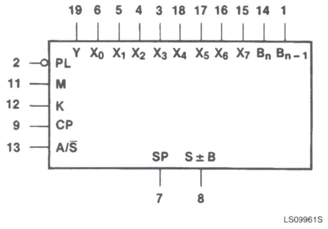
NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



B n-1 1
PL 2
X3 3
X2 4
X1 5
X0 6
SP 7
S±B 8
CP 9
GND 10
20 VCC
19 Y
18 X4
17 X5
16 X6
15 X7
14 Bn
13 A/S
12 K
11 M
CD08040S

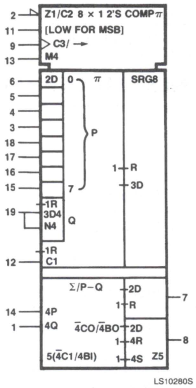
LOGIC SYMBOL



19 6 5 4 3 18 17 16 15 14 1
Y X0 X1 X2 X3 X4 X5 X6 X7 Bn Bn-1
2 PL
11 M
12 K
9 CP
13 A/S
SP S±B
7 8
LS09961S

V_{CC} = Pin 20
GND = Pin 10

LOGIC SYMBOL (IEEE/IEC)



Z1/C2 8 × 1 2'S COMP π
[LOW FOR MSB]
C3/ →
M4
2D
0
π
SRG8
P
7
1R
3D4
N4
Q
1R
C1
1 R
3D
Σ/P–Q
2D
1 R
4P
4Q
4CO/4BO
2D
1 4R
5(4C1/4BI)
1 4S
Z5
2
11
9
13
6
5
4
3
18
17
16
15
19
12
14
1
7
8
LS10280S

June 1987

Multiplier

FAST 74F784

The 'F784 is a serial/parallel 8-bit multiplier. Also included is an adder/subtracter stage. The X word (multiplicand) is loaded into a register while simultaneously clearing the arithmetic cell flip-flops in preparation for a multiplication. The Y word (multiplier) is clocked in serially.

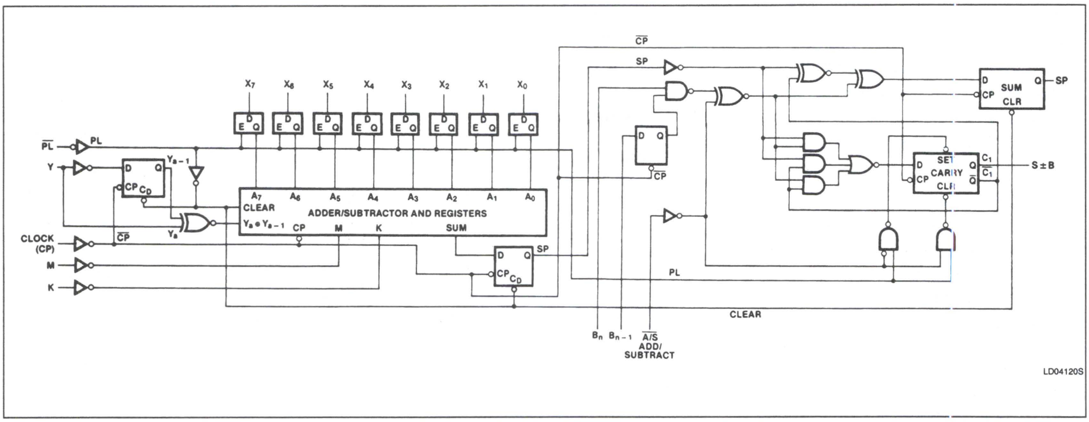
Expansion capability is provided via the M and K inputs. The K (cascade) input is connected to the SO output of the more significant chip. The M (mode) input is used to determine whether the multiplicand is to be treated as a Two's Complement or unsigned number.

The 'F784 has logic to enable complex arithmetic to be performed. A serial adder/subtracter enables constants to be added to the product. Typically, this feature would be used in FFT butterfly networks to reduce package count and power.

Two outputs are provided: the product X•Y and the product X•Y± B. Because of the internal adder/subtracter, a speed advantage is gained when using the 'F784 over using a separate adder and multiplier chip.

During a multiplication operation, the first clock cycle is used to load both the X word (multiplicand) and the first bit of the Y word (operand) into the input registers. At this time there is no valid data at the SP output, so that B bits added will not give the correct sum output. In order to load the first B bit on the same clock as X and Y, a B_{n-1} input is provided which delays the B data by one clock cycle. Thus, a valid output results.

LOGIC DIAGRAM



$\overline{CP}$
SP
X_7
X_6
X_5
X_4
X_3
X_2
X_1
X_0
D
E Q
$\overline{PL}$
PL
Y
D Q
CP C_D
Y_{s-1}
A_7
A_6
A_5
A_4
A_3
A_2
A_1
A_0
CLEAR
ADDER/SUBTRACTOR AND REGISTERS
$Y_s \oplus Y_{s-1}$
CP
M
K
SUM
CLOCK (CP)
$\overline{CP}$
Y_s
M
K
SP
D Q
CP
SUM
CLR
SP
SET
CARRY
CLR
C_1
$\overline{C_1}$
S±B
PL
CLEAR
B_n
B_{n-1}
$\overline{A}/S$
ADD/SUBTRACT
LD04120S

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		74F784			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OL} = MAX V_{IH} = MIN,	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current	$\overline{PL}$	V_{CC} = MAX, V_I = 0.5V				-1.2	mA
		Others				-0.4	-0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)		V_{CC} = MAX			67	100	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

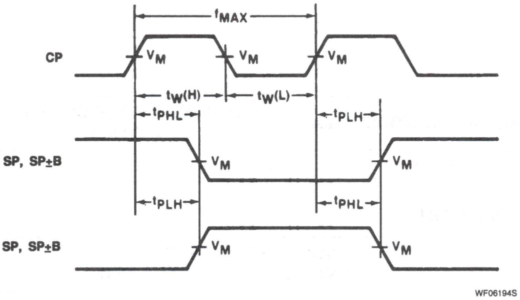
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F784					UNIT
			T_A = +25°C V_{CC} = +5.0V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = +5.0V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	50	65		50		MHz
t_{PHL}	Propagation delay $\overline{PL}$ to SP	Waveform 2	6.0		13.0	5.0	14.5	ns
t_{PHL}	Propagation delay $\overline{PL}$ to S ± B	Waveform 2	5.5		12.0	4.5	13.5	ns
t_{PLH} t_{PHL}	Propagation delay CP to SP	Waveform 1	4.0 4.5		9 10.5	3.5 4.0	10.0 12.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to S ± B	Waveform 1	4.0 4.0		9.0 9.0	3.5 3.5	10.0 10.0	ns

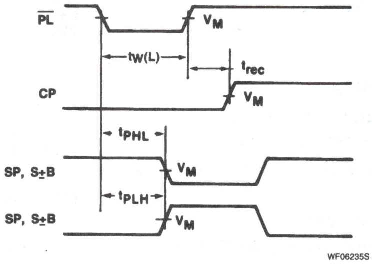
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	74F784					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_s(H) t_s(L)	Setup time K to CP	Waveform 3	13.0 9.0			14.0 10.0		ns
t_h(H) t_h(L)	Hold time K to CP	Waveform 3	0 1.0			0 1.0		ns
t_s(H) t_s(L)	Setup time Y to CP	Waveform 3	15 15			16.0 16.0		ns
t_h(H) t_h(L)	Hold time Y to CP	Waveform 3	1.5 1.5			1.5 1.5		ns
t_s(H) t_s(L)	Setup time X_3 to $\overline{PL}$	Waveform 3	5.0 5.0			6.0 6.0		ns
t_h(H) t_h(L)	Hold time X_3 to $\overline{PL}$	Waveform 3	2.0 2.0			2.0 2.0		ns
t_s(H) t_s(L)	Setup time B_n to CP	Waveform 3	7.0 7.0			8.0 8.0		ns
t_h(H) t_h(L)	Hold time B_n to CP	Waveform 3	0 0			0 0		ns
t_s(H) t_s(L)	Setup time A/$\overline{S}$ to CP	Waveform 3	12.0 12.0			13.0 13.0		ns
t_h(H) t_h(L)	Hold time A/$\overline{S}$ to CP	Waveform 3	1.5 1.5			1.5 1.5		ns
t_s(H) t_s(L)	Setup time B_n to CP	Waveform 3	4.0 4.0			5.0 5.0		ns
t_h(H) t_h(L)	Hold time B_n to CP	Waveform 3	0 0			1.0 1.0		ns
t_{rec}	Recovery time $\overline{PL}$ to CP	Waveform 2	6.5			7.5		ns
t_w(L)	Pulse width		5.0			6.0		ns
t_w(H) t_w(L)	CP pulse width	Waveform 1	5.0 5.0			6.0 6.0		ns

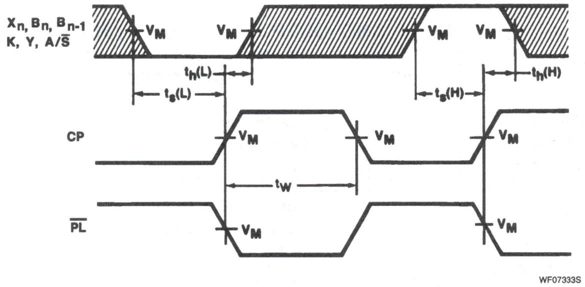
AC WAVEFORMS


fMAX
CP
VM
VM
VM
tW(H)
tW(L)
tPHL
tPLH
SP, SP±B
VM
VM
tPLH
tPHL
SP, SP±B
VM
VM
WF06194S

Waveform 1. Clock to Output Delays, Clock Pulse Width, and Maximum Clock Frequency


PL
VM
tW(L)
trec
CP
VM
tPHL
SP, S±B
VM
tPLH
SP, S±B
VM
WF06235S

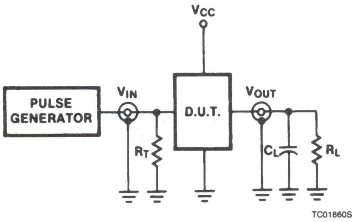
Waveform 2. Parallel Load Pulse Width, Parallel Load to Output Delay and Parallel Load to Clock Recovery Time


Xn, Bn, Bn-1
K, Y, A/S
VM
VM
VM
VM
th(L)
ts(L)
ts(H)
th(H)
CP
VM
VM
VM
tW
PL
VM
VM
WF07333S

Waveform 3. Data Setup and Hold Times

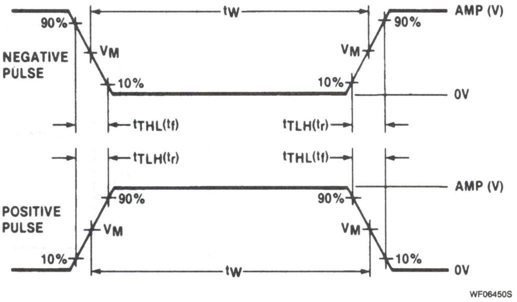
NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS


VCC
PULSE GENERATOR
VIN
D.U.T.
VOUT
RT
CL
RL
TC01860S

Test Circuit for Totem-Pole Outputs

DEFINITIONS
R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.


tW
AMP (V)
90%
90%
NEGATIVE PULSE
VM
VM
10%
10%
0V
tTHL(tf)
tTLH(tr)
tTLH(tr)
tTHL(tf)
AMP (V)
90%
90%
POSITIVE PULSE
VM
VM
10%
10%
0V
tW
WF06450S

$V_M = 1.5V$

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST Products

FAST 74F786
4-Input Asynchronous Bus Arbiter

Preliminary Specification

FEATURES

- **Arbitrates between 4 asynchronous inputs**
- **Separate grant output for each input**
- **Common output enable**
- **On-board 4-input AND gate**

DESCRIPTION

The 74F786 is an asynchronous 4-input arbiter designed for high-speed real-time applications. The priority of arbitration is determined on first-come first-served basis.

Separate Bus Grant ($\overline{BG}_n$) outputs are available to indicate which one of the request inputs is served by the arbitration logic. All $\overline{BG}$ outputs are enabled by a common enable ($\overline{EN}$) input.

The 74F786 is available in a 16-pin plastic DIP and SO packages. In order to generate a bus request signal, a separate 4-input AND gate is provided. This may also be used as an independent AND gate.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F786	5.5ns	55mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V± 10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F786N
16-Pin Plastic SO	N74F786D

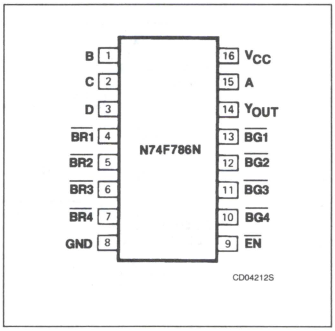
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$\overline{BR1}$ – $\overline{BR4}$	Bus Request inputs (active-Low)	3.0/3.0	20μA/1.8mA
A, B, C, D	AND gate inputs	1.0/1.0	20μA/0.6mA
$\overline{EN}$	Common Bus Grant output enable input (active-Low)	1.0/1.0	20μA/0.6mA
Yout	AND gate output	150/40	3.0mA/24mA
$\overline{BG1}$ – $\overline{BG4}$	Bus Grant outputs (active-Low)	150/40	3.0mA/24mA

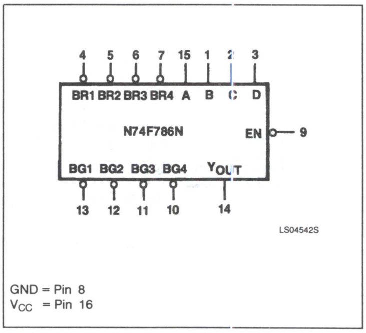
NOTE:

1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION


B 1
C 2
D 3
BR1 4
BR2 5
BR3 6
BR4 7
GND 8
N74F786N
16 VCC
15 A
14 YOUT
13 BG1
12 BG2
11 BG3
10 BG4
9 EN
CD04212S

LOGIC SYMBOL


4 5 6 7 15 1 2 3
BR1 BR2 BR3 BR4 A B C D
N74F786N
EN 9
BG1 BG2 BG3 BG4 YOUT
13 12 11 10 14
LS04542S

GND = Pin 8
V_{CC} = Pin 16

Signetics

FAST Products

FAST 74F821/822/823/824/825/826

Bus Interface Registers

Preliminary Specification

'F821 10-Bit Bus Interface Register, Non-Inverting (3-State)
'F822 10-Bit Bus Interface Register, Inverting (3-State)
'F823 9-Bit Bus Interface Register, Non-Inverting (3-State)
'F824 9-Bit Bus Interface Register, Inverting (3-State)
'F825 8-Bit Bus Interface Register, Non-Inverting (3-State)
'F826 8-Bit Bus Interface Register, Inverting (3-State)

FEATURES

- High-speed parallel registers with positive edge-triggered D-type flip-flops
- Extra data width for wide address/data paths or buses with parity
- High-impedance NPN base input structure minimizes bus loading
- I_{IL} is 20μA vs 1000μA for AM29821 series
- Buffered control inputs reduce AC effects
- Ideal where high-speed, light-loading, or increased fan-in are required as with MOS microprocessors
- Positive and negative overshoots are clamped to ground
- 3-State outputs glitch free during power-up and down
- 48mA Sink current
- Slim DIP 300mil package
- Broadside pinout
- Pin-for-pin and function compatible with AMD AM29821–29826 series

DESCRIPTION

The 74F821 Series Bus Interface Registers are designed to eliminate the extra packages required to buffer existing registers and provide extra data width for wider address/data paths or buses carrying parity.

The 'F821 and 'F822 are buffered 10-bit wide versions of the popular 'F374/'F534 functions.

The 'F823 and 'F824 are 9-bit wide buffered registers with Clock Enable and Master Reset which are ideal for parity bus interfacing in high-performance microprogrammed systems.

The 'F825 and 'F826 are 8-bit buffered registers with all the 'F823/'F824 controls plus multiple Enables ($\overline{OE}_0$, $\overline{OE}_1$, $\overline{OE}_2$) to allow multiuser control of the interface, e.g., CS, DMA, and RD/$\overline{WR}$. They are ideal for use as an output port requiring high $\overline{I_{OL}}/\overline{I_{OH}}$.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
'F821/ 'F822/ 'F823 'F824/ 'F825/ 'F826	115MHz	75mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ± 10%; T_A = 0°C to +70°C
24-Pin Plastic Slim DIP (300mil)	N74F821N, N74F823N, N74F825N N74F822N, N74F824N, N74F826N
24-Pin Plastic SOL	N74F821D, N74F823D, N74F825D N74F822D, N74F824D, N74F826D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

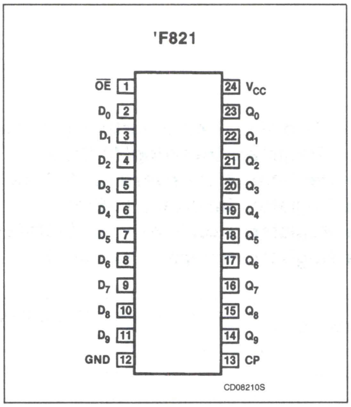
TYPE	PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
'F821 'F822	D_n	Data input	1.0/0.033	20μA/20μA
	CP	Clock input	1.0/0.033	20μA/20μA
	$\overline{OE}$	Output Enable input (active-Low)	1.0/0.033	20μA/20μA
	Q_n, $\overline{Q}_n$	Data Outputs	750/106.7	15μA/64μA
'F823 'F824	D_n	Data input	1.0/0.033	20μA/20μA
	CP	Clock input	1.0/0.033	20μA/20μA
	$\overline{EN}$	Clock Enable input (active-Low)	1.0/0.033	20μA/20μA
	$\overline{MR}$	Master Reset input (active-Low)	1.0/0.033	20μA/20μA
	$\overline{OE}$	Output Enable input	1.0/0.033	20μA/20μA
	Q_n, $\overline{Q}_n$	Data outputs	750/106.7	15mA/64mA
'F825 'F826	D_n	Data input	1.0/0.033	20μA/20μA
	CP	Clock input	1.0/0.033	20μA/20μA
	$\overline{EN}$	Clock Enable input (active-Low)	1.0/0.033	20μA/20μA
	$\overline{MR}$	Master Reset input (active-Low)	1.0/0.033	20μA/20μA
	$\overline{OE}$, $\overline{OE}_n$	Output Enable inputs	1.0/0.033	20μA/20μA
	Q_n, $\overline{Q}_n$	Data outputs	750/106.7	15mA/64mA

NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

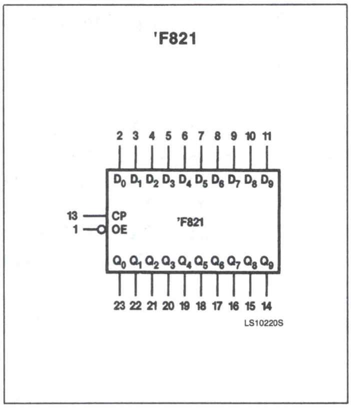
Bus Interface Registers

FAST 74F821/822/823/824/825/826

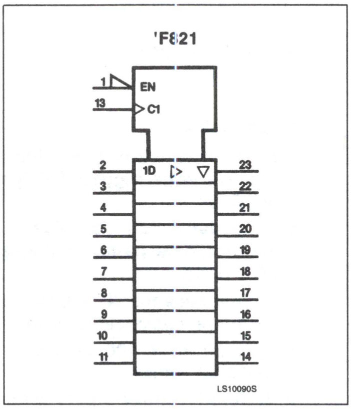
PIN CONFIGURATION


'F821
$\overline{OE}$ 1
D_0 2
D_1 3
D_2 4
D_3 5
D_4 6
D_5 7
D_6 8
D_7 9
D_8 10
D_9 11
GND 12
24 V_{CC}
23 Q_0
22 Q_1
21 Q_2
20 Q_3
19 Q_4
18 Q_5
17 Q_6
16 Q_7
15 Q_8
14 Q_9
13 CP
CD08210S

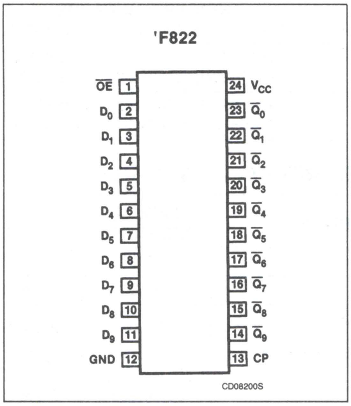
LOGIC SYMBOL


'F821
2 3 4 5 6 7 8 9 10 11
D_0 D_1 D_2 D_3 D_4 D_5 D_6 D_7 D_8 D_9
13 CP
1 OE
'F821
Q_0 Q_1 Q_2 Q_3 Q_4 Q_5 Q_6 Q_7 Q_8 Q_9
23 22 21 20 19 18 17 16 15 14
LS10220S

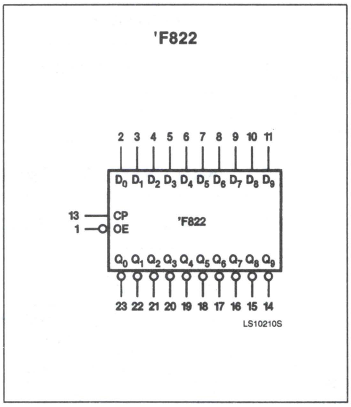
LOGIC SYMBOL (IEEE/IEC)


'F821
1 EN
13 C1
2 1D 23
3 22
4 21
5 20
6 19
7 18
8 17
9 16
10 15
11 14
LS10090S

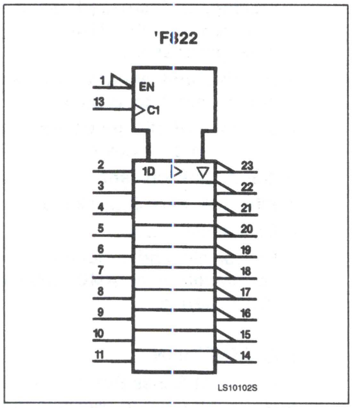
PIN CONFIGURATION


'F822
$\overline{OE}$ 1
D_0 2
D_1 3
D_2 4
D_3 5
D_4 6
D_5 7
D_6 8
D_7 9
D_8 10
D_9 11
GND 12
24 V_{CC}
23 $\overline{Q}_0$
22 $\overline{Q}_1$
21 $\overline{Q}_2$
20 $\overline{Q}_3$
19 $\overline{Q}_4$
18 $\overline{Q}_5$
17 $\overline{Q}_6$
16 $\overline{Q}_7$
15 $\overline{Q}_8$
14 $\overline{Q}_9$
13 CP
CD08200S

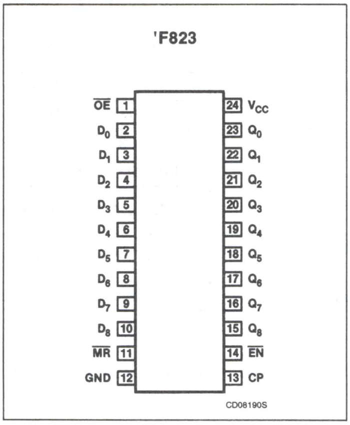
LOGIC SYMBOL


'F822
2 3 4 5 6 7 8 9 10 11
D_0 D_1 D_2 D_3 D_4 D_5 D_6 D_7 D_8 D_9
13 CP
1 OE
'F822
Q_0 Q_1 Q_2 Q_3 Q_4 Q_5 Q_6 Q_7 Q_8 Q_9
23 22 21 20 19 18 17 16 15 14
LS10210S

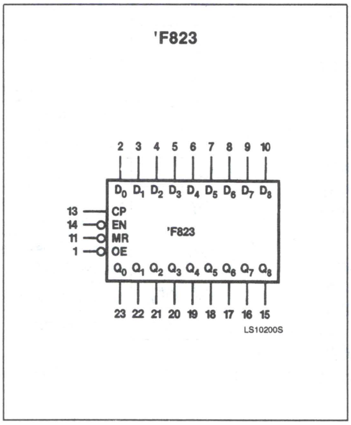
LOGIC SYMBOL (IEEE/IEC)


'F822
1 EN
13 C1
2 1D 23
3 22
4 21
5 20
6 19
7 18
8 17
9 16
10 15
11 14
LS10102S

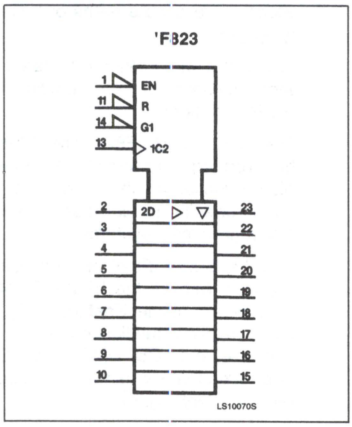
PIN CONFIGURATION


'F823
$\overline{OE}$ 1
D_0 2
D_1 3
D_2 4
D_3 5
D_4 6
D_5 7
D_6 8
D_7 9
D_8 10
$\overline{MR}$ 11
GND 12
24 V_{CC}
23 Q_0
22 Q_1
21 Q_2
20 Q_3
19 Q_4
18 Q_5
17 Q_6
16 Q_7
15 Q_8
14 $\overline{EN}$
13 CP
CD08190S

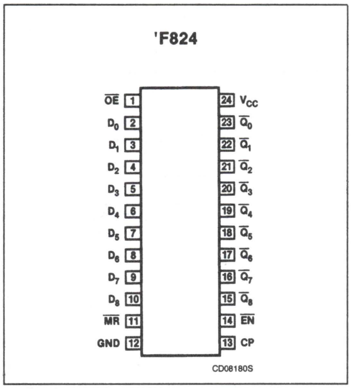
LOGIC SYMBOL


'F823
2 3 4 5 6 7 8 9 10
D_0 D_1 D_2 D_3 D_4 D_5 D_6 D_7 D_8
13 CP
14 EN
11 MR
1 OE
'F823
Q_0 Q_1 Q_2 Q_3 Q_4 Q_5 Q_6 Q_7 Q_8
23 22 21 20 19 18 17 16 15
LS10200S

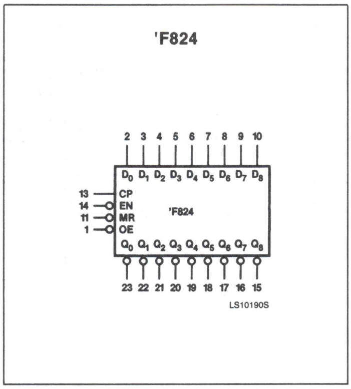
LOGIC SYMBOL (IEEE/IEC)


'F823
1 EN
11 R
14 G1
13 1C2
2 2D 23
3 22
4 21
5 20
6 19
7 18
8 17
9 16
10 15
LS10070S

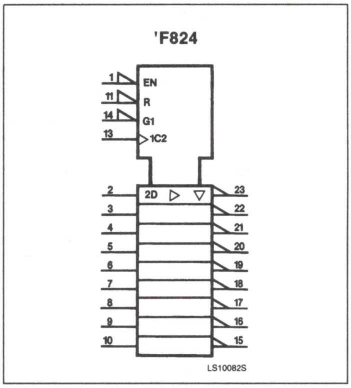
PIN CONFIGURATION


'F824
$\overline{OE}$ 1
D_0 2
D_1 3
D_2 4
D_3 5
D_4 6
D_5 7
D_6 8
D_7 9
D_8 10
$\overline{MR}$ 11
GND 12
24 V_{CC}
23 $\overline{Q}_0$
22 $\overline{Q}_1$
21 $\overline{Q}_2$
20 $\overline{Q}_3$
19 $\overline{Q}_4$
18 $\overline{Q}_5$
17 $\overline{Q}_6$
16 $\overline{Q}_7$
15 $\overline{Q}_8$
14 $\overline{EN}$
13 CP
CD08180S

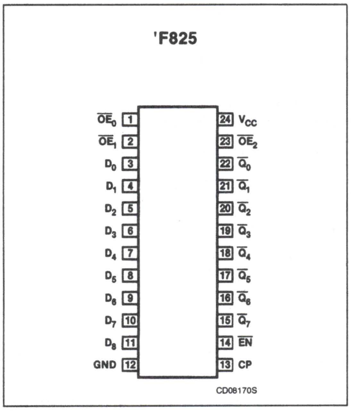
LOGIC SYMBOL


'F824
2 3 4 5 6 7 8 9 10
D_0 D_1 D_2 D_3 D_4 D_5 D_6 D_7 D_8
13 CP
14 EN
11 MR
1 OE
'F824
Q_0 Q_1 Q_2 Q_3 Q_4 Q_5 Q_6 Q_7 Q_8
23 22 21 20 19 18 17 16 15
LS10190S

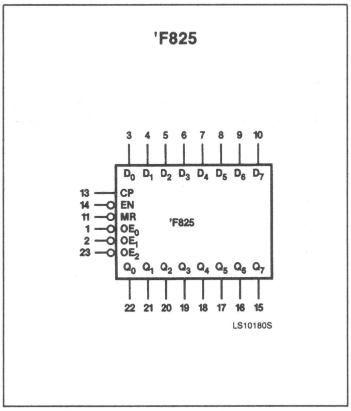
LOGIC SYMBOL (IEEE/IEC)


'F824
1 EN
11 R
14 G1
13 1C2
2 2D
3 4 5 6 7 8 9 10
23 22 21 20 19 18 17 16 15
LS10082S

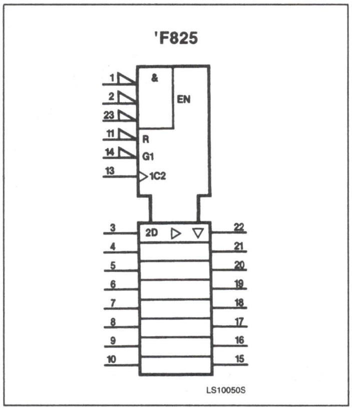
PIN CONFIGURATION


'F825
$\overline{OE}_0$ 1
$\overline{OE}_1$ 2
D_0 3
D_1 4
D_2 5
D_3 6
D_4 7
D_5 8
D_6 9
D_7 10
D_8 11
GND 12
24 V_{CC}
23 $\overline{OE}_2$
22 $\overline{Q}_0$
21 $\overline{Q}_1$
20 $\overline{Q}_2$
19 $\overline{Q}_3$
18 $\overline{Q}_4$
17 $\overline{Q}_5$
16 $\overline{Q}_6$
15 $\overline{Q}_7$
14 $\overline{EN}$
13 CP
CD08170S

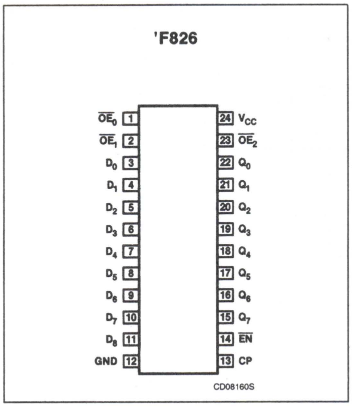
LOGIC SYMBOL


'F825
3 4 5 6 7 8 9 10
D_0 D_1 D_2 D_3 D_4 D_5 D_6 D_7
13 CP
14 EN
11 MR
1 OE_0
2 OE_1
23 OE_2
'F825
Q_0 Q_1 Q_2 Q_3 Q_4 Q_5 Q_6 Q_7
22 21 20 19 18 17 16 15
LS10180S

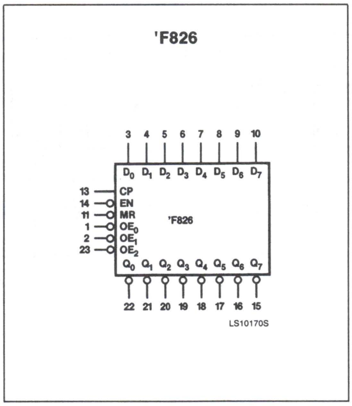
LOGIC SYMBOL (IEEE/IEC)


'F825
1 2 23 &
EN
11 R
14 G1
13 1C2
3 2D
4 5 6 7 8 9 10
22 21 20 19 18 17 16 15
LS10050S

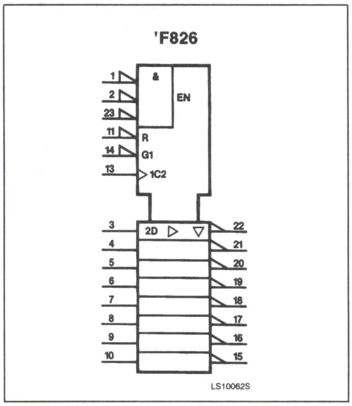
PIN CONFIGURATION


'F826
$\overline{OE}_0$ 1
$\overline{OE}_1$ 2
D_0 3
D_1 4
D_2 5
D_3 6
D_4 7
D_5 8
D_6 9
D_7 10
D_8 11
GND 12
24 V_{CC}
23 $\overline{OE}_2$
22 Q_0
21 Q_1
20 Q_2
19 Q_3
18 Q_4
17 Q_5
16 Q_6
15 Q_7
14 $\overline{EN}$
13 CP
CD08160S

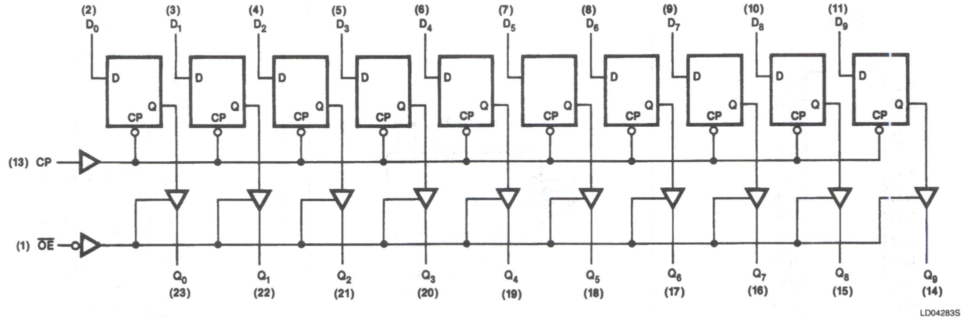
LOGIC SYMBOL


'F826
3 4 5 6 7 8 9 10
D_0 D_1 D_2 D_3 D_4 D_5 D_6 D_7
13 CP
14 EN
11 MR
1 OE_0
2 OE_1
23 OE_2
'F826
Q_0 Q_1 Q_2 Q_3 Q_4 Q_5 Q_6 Q_7
22 21 20 19 18 17 16 15
LS10170S

LOGIC SYMBOL (IEEE/IEC)

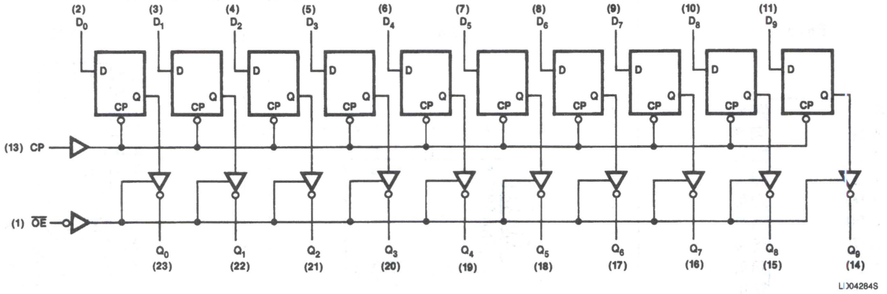

'F826
1 2 23 &
EN
11 R
14 G1
13 1C2
3 2D
4 5 6 7 8 9 10
22 21 20 19 18 17 16 15
LS10062S

LOGIC DIAGRAM for 'F821


(2) D_0
(3) D_1
(4) D_2
(5) D_3
(6) D_4
(7) D_5
(8) D_6
(9) D_7
(10) D_8
(11) D_9
D
CP
Q
(13) CP
(1) $\overline{OE}$
Q_0 (23)
Q_1 (22)
Q_2 (21)
Q_3 (20)
Q_4 (19)
Q_5 (18)
Q_6 (17)
Q_7 (16)
Q_8 (15)
Q_9 (14)
LD04283S

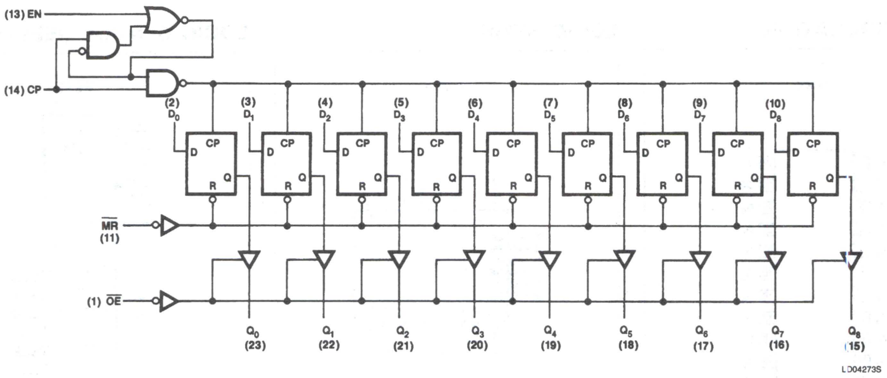
V_{CC} = Pin 24
GND = Pin 12

LOGIC DIAGRAM for 'F822


(2) D_0
(3) D_1
(4) D_2
(5) D_3
(6) D_4
(7) D_5
(8) D_6
(9) D_7
(10) D_8
(11) D_9
D
CP
Q
(13) CP
(1) $\overline{OE}$
Q_0 (23)
Q_1 (22)
Q_2 (21)
Q_3 (20)
Q_4 (19)
Q_5 (18)
Q_6 (17)
Q_7 (16)
Q_8 (15)
Q_9 (14)
LD04284S

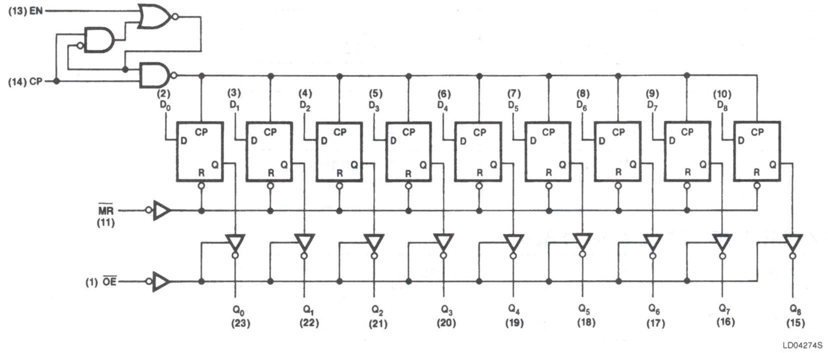
V_{CC} = Pin 24
GND = Pin 12

LOGIC DIAGRAM for 'F823


(13) EN
(14) CP
(2) D_0
(3) D_1
(4) D_2
(5) D_3
(6) D_4
(7) D_5
(8) D_6
(9) D_7
(10) D_8
D
CP
R
Q
$\overline{MR}$ (11)
(1) $\overline{OE}$
Q_0 (23)
Q_1 (22)
Q_2 (21)
Q_3 (20)
Q_4 (19)
Q_5 (18)
Q_6 (17)
Q_7 (16)
Q_8 (15)
LD04273S

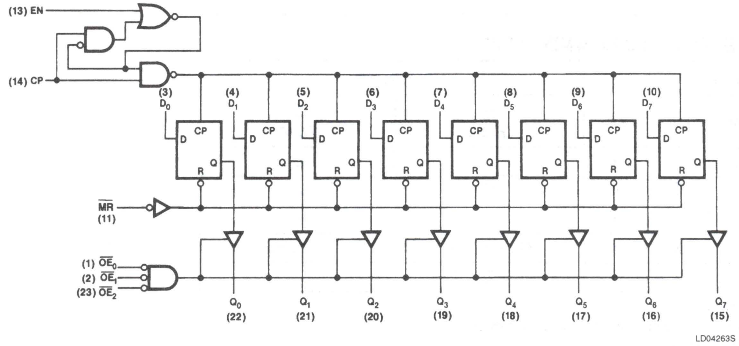
V_{CC} = Pin 24
GND = Pin 12

LOGIC DIAGRAM for 'F824


(13) EN
(14) CP
(2) D0
(3) D1
(4) D2
(5) D3
(6) D4
(7) D5
(8) D6
(9) D7
(10) D8
CP
D
Q
R
MR
(11)
(1) OE
Q0 (23)
Q1 (22)
Q2 (21)
Q3 (20)
Q4 (19)
Q5 (18)
Q6 (17)
Q7 (16)
Q8 (15)
LD04274S

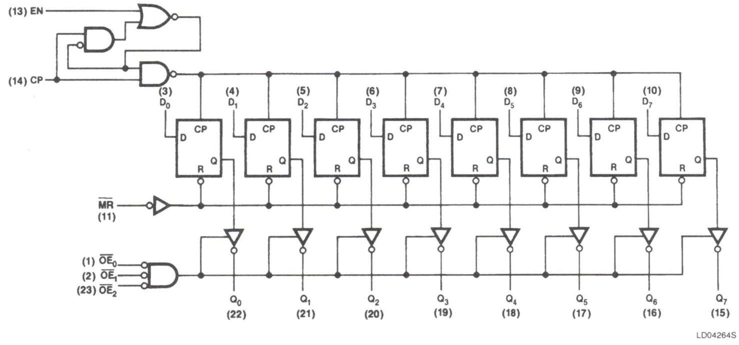
V_{CC} = Pin 24
GND = Pin 12

LOGIC DIAGRAM for 'F825


(13) EN
(14) CP
(3) D0
(4) D1
(5) D2
(6) D3
(7) D4
(8) D5
(9) D6
(10) D7
CP
D
Q
R
MR
(11)
(1) OE0
(2) OE1
(23) OE2
Q0 (22)
Q1 (21)
Q2 (20)
Q3 (19)
Q4 (18)
Q5 (17)
Q6 (16)
Q7 (15)
LD04263S

V_{CC} = Pin 24
GND = Pin 12

LOGIC DIAGRAM for 'F826


(13) EN
(14) CP
(3) D0
(4) D1
(5) D2
(6) D3
(7) D4
(8) D5
(9) D6
(10) D7
CP
D
Q
R
MR
(11)
(1) OE0
(2) OE1
(23) OE2
Q0 (22)
Q1 (21)
Q2 (20)
Q3 (19)
Q4 (18)
Q5 (17)
Q6 (16)
Q7 (15)
LD04264S

V_{CC} = Pin 24
GND = Pin 12

FUNCTION TABLE FOR 'F821 AND 'F822

INPUTS			OUTPUTS	
$\overline{OE}$	CP	D_n	Q 'F821	$\overline{Q}$ 'F822
L	↑	l	L	H
L	↑	h	H	L
L	L	X	No change	No change
L	H	X	No change	No change
H	X	X	Z	Z

FUNCTION TABLE FOR 'F823 AND 'F824

INPUTS					OUTPUTS	
$\overline{OE}$	$\overline{MR}$	$\overline{EN}$	CP	D_n	Q 'F823	$\overline{Q}$ 'F824
L	L	X	X	X	L	L
L	H	L	↑	h	H	L
L	H	L	↑	l	L	H
L	H	H	X	X	No change	No change
H	X	X	X	X	Z	Z

FUNCTION TABLE FOR 'F825 AND 'F826

INPUTS					OUTPUTS	
$\overline{OE}_n$	$\overline{MR}$	$\overline{EN}$	CP	D_n	Q 'F825	$\overline{Q}$ 'F826
L	L	X	X	X	L	L
L	H	L	↑	h	H	L
L	H	L	↑	l	L	H
L	H	H	X	X	No change	No change
H	X	X	X	X	Z	Z

H = High voltage level steady state
h = High voltage level one setup time prior to the Low-to-High clock transition
L = Low voltage level steady state
l = Low voltage level one setup time prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition
Z = High-Impedance

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	128	mA
T_A	Operating free-air temperature range	0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−15	mA
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			74F821, 822, 823 74F824, 825, 826			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = −3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.3		V
				I_{OH} = −15mA	±10%V_{CC}	2.0			V
					±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 48mA	±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
				I_{OL} = 64mA	±5%V_{CC}		0.40	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$				-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = 0.0V, V_I = 7.0V					100	μA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					-20	μA
I_{OZH}	OFF-state output current, High-level voltage applied		V_{CC} = MAX, V_O = 2.7V					50	μA
I_{OZL}	OFF-state output current, Low-level voltage applied		V_{CC} = MAX, V_O = 0.5V					-50	μA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX			−100		-225	mA
I_{CC}	Supply current (total)	'F821, 'F822	V_{CC} = MAX				75	110	mA
		'F823, 'F824						110	mA
		'F825, 'F826						86	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

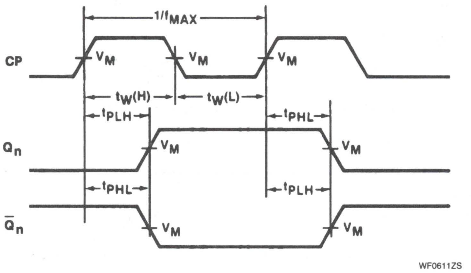
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	74F821, 74F822, 74F823, 74F824, 74F825, 74F826					UNIT
				$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
				Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency		Waveform 1	100					MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n or $\overline{Q}_n$		Waveform 1			7.0 9.5			ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n or $\overline{Q}_n$	'F823, 'F824 'F825, 'F826	Waveform 2			15.0			ns
t_{PZH} t_{PZL}	Output enable time to High or Low level		Waveform 4 Waveform 5			10.5 9.5			ns
t_{PHZ} t_{PLZ}	Output disable time from High or Low level		Waveform 5 Waveform 5			7.0 7.0			ns

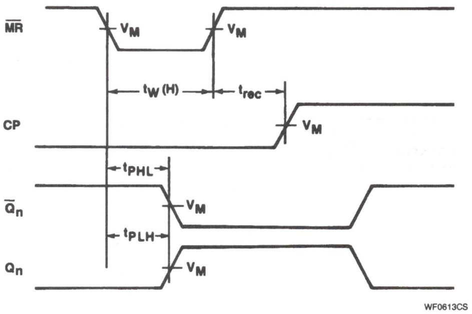
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER		TEST CONDITIONS	74F821, 74F822, 74F823, 74F824, 74F825, 74F826					UNIT
				$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
				Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to CP		Waveform 3	2.0 2.0					ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to CP		Waveform 3	2.0 2.0					ns
$t_w(H)$ $t_w(L)$	Clock pulse width High or Low		Waveform 3	2.0 2.0					ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low, $\overline{E}_n$ to CP	'F823, 'F824, 'F825, 'F826	Waveform 3	3.0 3.0					ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low, $\overline{E}_n$ to CP		Waveform 3	0 0					ns
$t_w(L)$	$\overline{MR}$ Pulse width, Low		Waveform 2	5.0					ns
t_{rec}	$\overline{MR}$ Recovery time		Waveform 2	5.0					ns

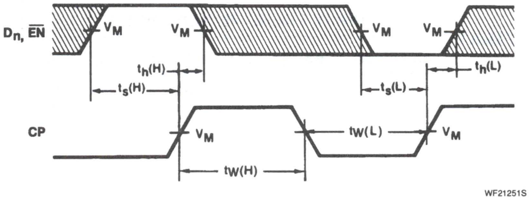
AC WAVEFORMS


1/fMAX
CP
VM
VM
VM
tW(H)
tW(L)
tPLH
tPHL
Qn
VM
VM
tPHL
tPLH
Q̄n
VM
VM
WF0611ZS

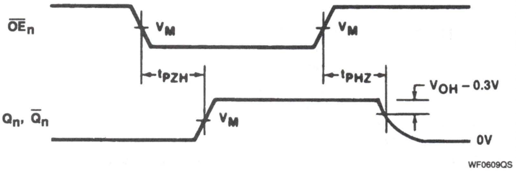
Waveform 1. Propagation Delay for Clock to Outputs


M̄R̄
VM
VM
tW (H)
trec
CP
VM
tPHL
Q̄n
VM
tPLH
Qn
VM
WF0613CS

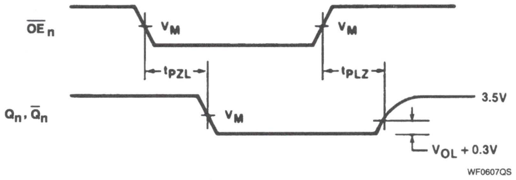
Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time


Dn, ĒN̄
VM
VM
VM
VM
th(H)
ts(H)
ts(L)
th(L)
CP
VM
tW(L)
VM
tW(H)
WF21251S

Waveform 3. Data and Enable Setup and Hold Times


ŌĒn
VM
VM
tPZH
tPHZ
VOH − 0.3V
Qn, Q̄n
VM
0V
WF0609QS

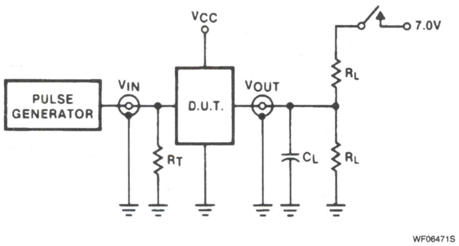
Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time From High Level


ŌĒn
VM
VM
tPZL
tPLZ
3.5V
Qn, Q̄n
VM
VOL + 0.3V
WF0607QS

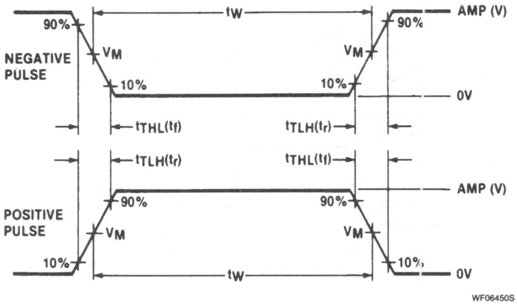
Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS


VCC
7.0V
RL
PULSE GENERATOR
VIN
D.U.T.
VOUT
RT
CL
RL
WF06471S

Test Circuit for 3-State Outputs


90%
tW
90%
AMP (V)
NEGATIVE PULSE
VM
VM
10%
10%
0V
tTHL(tf)
tTLH(tr)
tTLH(tr)
tTHL(tf)
AMP (V)
90%
90%
POSITIVE PULSE
VM
VM
10%
tW
10%
0V
WF06450S

$V_M = 1.5V$

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F827, 74F828
Buffers

'F827 10-Bit Buffer/Line Driver, Non-Inverting (3-State)
'F828 10-Bit Buffer/Line Driver, Inverting (3-State)
Product Specification

FAST Products

FEATURES

- Outputs sink 64mA
- High-impedance NPN base inputs for reduced loading (20μA in High and Low states)
- I_{IL} is 20μA vs FAST family spec of 600μA and 1000μA for AMD 29827/828 series
- Ideal where high speed, light bus loading, and increased fan-in are required
- Controlled rise and fall times to minimize ground bounce
- Glitch free power up in 3-State
- Flow through pinout architecture for microprocessor oriented applications
- Slim 300mil-wide plastic 24-pin package
- Pinout and function compatible with AMD 29827/828 series

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F827 74F828	6.0ns 6.0ns	60mA 55mA

ORDERING INFORMATION

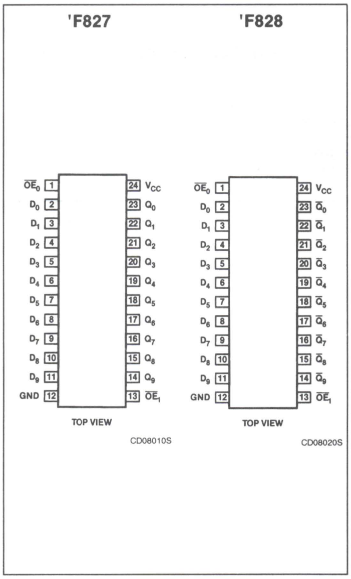
PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
24-Pin Plastic Slim DIP (300mil)	N74F827N, N74F828N
24-Pin Plastic SOL	N74F827D, N74F828D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

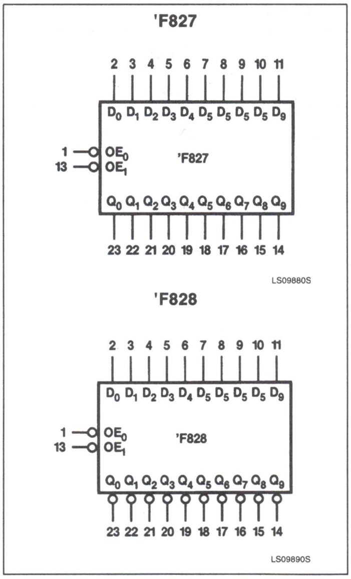
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$D_0 - D_9$	Data inputs	1.0/0.033	20μA/20mA
$\overline{OE}_0$, $\overline{OE}_1$	Output enable inputs (active-Low)	1.0/0.033	20μA/20mA
$Q_0 - Q_9$	Data outputs for 'F827	750/106.7	15mA/64mA
$\overline{Q}_0 - \overline{Q}_9$	Data outputs for 'F828	750/106.7	15mA/64mA

NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

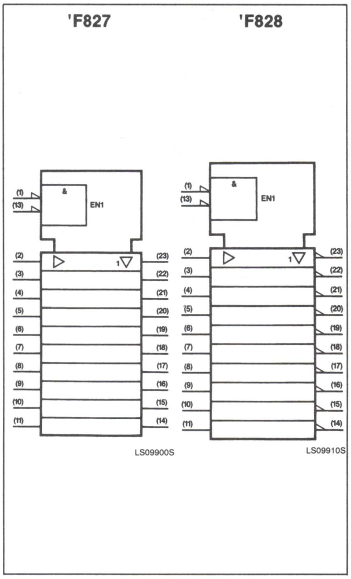
PIN CONFIGURATION


'F827
'F828
OE0 1
D0 2
D1 3
D2 4
D3 5
D4 6
D5 7
D6 8
D7 9
D8 10
D9 11
GND 12
24 VCC
23 Q0
22 Q1
21 Q2
20 Q3
19 Q4
18 Q5
17 Q6
16 Q7
15 Q8
14 Q9
13 OE1
TOP VIEW
CD08010S
CD08020S

LOGIC SYMBOL


'F827
2 3 4 5 6 7 8 9 10 11
D0 D1 D2 D3 D4 D5 D5 D5 D5 D9
1 OE0
13 OE1
'F827
Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7 Q8 Q9
23 22 21 20 19 18 17 16 15 14
LS09880S
'F828
2 3 4 5 6 7 8 9 10 11
D0 D1 D2 D3 D4 D5 D5 D5 D5 D9
1 OE0
13 OE1
'F828
Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7 Q8 Q9
23 22 21 20 19 18 17 16 15 14
LS09890S

LOGIC SYMBOL (IEEE/IEC)


'F827
'F828
(1)
(13)
&
EN1
1
(2)
(3)
(4)
(5)
(6)
(7)
(8)
(9)
(10)
(11)
(23)
(22)
(21)
(20)
(19)
(18)
(17)
(16)
(15)
(14)
LS09900S
LS09910S

Buffers

FAST 74F827, 74F828

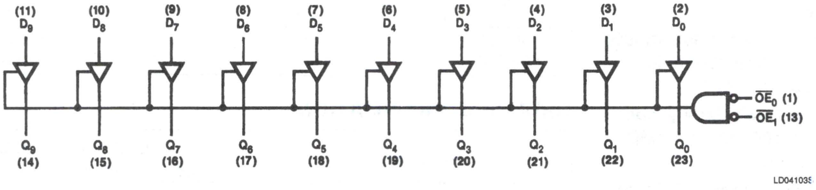
DESCRIPTION

The 'F827 and 'F828 10-Bit bus buffers provide High performance bus interface buffering for wide data/address paths or busses carrying parity. They have NOR Output Enables ($\overline{OE}_0$, $\overline{OE}_1$) for maximum control flexibility.

The 'F827 and 'F828 are functionally and pin compatible to AMD AM29827 and AM29828.

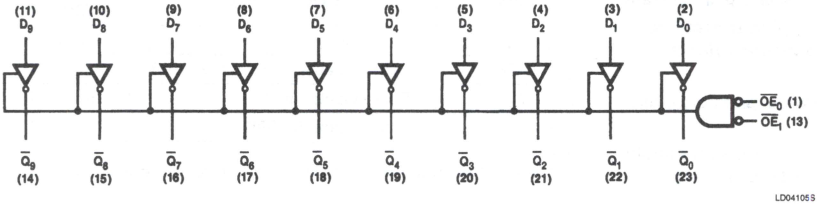
The 'F828 is an inverting version of 'F827.

LOGIC DIAGRAM FOR 'F827


(11) D_9
(10) D_8
(9) D_7
(8) D_6
(7) D_5
(6) D_4
(5) D_3
(4) D_2
(3) D_1
(2) D_0
$\overline{OE}_0$ (1)
$\overline{OE}_1$ (13)
Q_9 (14)
Q_8 (15)
Q_7 (16)
Q_6 (17)
Q_5 (18)
Q_4 (19)
Q_3 (20)
Q_2 (21)
Q_1 (22)
Q_0 (23)
LD04103S

V_{CC} = Pin 24
GND = Pin 12
( ) = Pin numbers

LOGIC DIAGRAM FOR 'F828


(11) D_9
(10) D_8
(9) D_7
(8) D_6
(7) D_5
(6) D_4
(5) D_3
(4) D_2
(3) D_1
(2) D_0
$\overline{OE}_0$ (1)
$\overline{OE}_1$ (13)
$\overline{Q}_9$ (14)
$\overline{Q}_8$ (15)
$\overline{Q}_7$ (16)
$\overline{Q}_6$ (17)
$\overline{Q}_5$ (18)
$\overline{Q}_4$ (19)
$\overline{Q}_3$ (20)
$\overline{Q}_2$ (21)
$\overline{Q}_1$ (22)
$\overline{Q}_0$ (23)
LD04105S

V_{CC} = Pin 24
GND = Pin 12
( ) = Pin numbers

FUNCTION TABLE

INPUTS		OUTPUTS		OPERATING MODE
$\overline{OE}_n$	D_n	'F827	'F828	
		Q_n	Q_n	
L	L	L	H	Transparent
L	H	H	L	Transparent
H	X	Z	Z	Hi-Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High-impedance

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to +5.0	V
I_{OUT}	Current applied to output in Low output state	128	mA
T_A	Operating free-air temperature range	0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−15	mA
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]			74F827, 74F828			UNIT
							Min	Typ[2]	Max	
V_{OH}	High-level output voltage			V_{CC} = MIN V_{IL} = MAX V_{IH} = MIN	I_{OH} = −3mA	±10%V_{CC}	2.4			V
						±5%V_{CC}	2.7	3.3		V
					I_{OH} = −15mA	±10%V_{CC}	2.0			V
						±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage			V_{CC} = MIN V_{IL} = MAX V_{IH} = MIN	I_{OL} = 48mA	±10%V_{CC}		0.35	0.50	V
					I_{OL} = 64mA	±5%V_{CC}		0.40	0.55	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, $I_I = I_{IK}$				−0.73	−1.2	V
I_I	Input current at maximum input voltage			V_{CC} = 0.0V = 7.0V					100	μA
I_{IH}	High-level input current			V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	Low-level input current			V_{CC} = MAX, V_I = 0.5V				−0.4	−20	mA
I_{OZH}	OFF-state output current, High-level voltage applied			V_{CC} = MAX, V_O = 2.7V					50	μA
I_{OZL}	OFF-state output current, Low-level voltage applied			V_{CC} = MAX, V_O = 0.5V					−50	μA
I_{OS}	Short-circuit output current[3]			V_{CC} = MAX			−100		−225	mA
I_{CC}	Supply current (total)	'F827	I_{CCH}	V_{CC} = MAX				50	70	mA
			I_{CCL}					70	100	mA
			I_{CCZ}					60	90	mA
		'F828	I_{CCH}	V_{CC} = MAX				30	45	mA
			I_{CCL}					65	85	mA
			I_{CCZ}					55	70	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of High-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

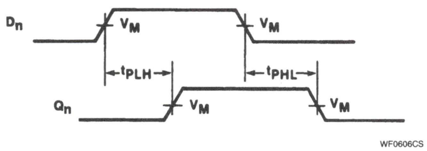
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F827					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	Waveform 1	2.0 2.0	5.5 4.5	8.5 8.5	2.0 2.0	9.0 9.0	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}$ to Q_n	Waveform 3 Waveform 4	5.0 4.0	10.0 7.0	13.5 12.0	4.5 4.0	15.5 13.0	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}$ to Q_n	Waveform 3 Waveform 4	2.5 2.5	5.0 5.0	8.0 8.0	2.0 2.0	8.5 8.5	ns

AC ELECTRICAL CHARACTERISTICS

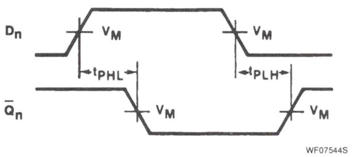
SYMBOL	PARAMETER	TEST CONDITIONS	74F828					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_n to $\overline{Q}_n$	Waveform 2	2.0 1.0	6.0 3.0	8.5 7.0	2.0 1.0	9.5 8.0	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}$ to $\overline{Q}_n$	Waveform 3 Waveform 4	7.5 6.5	10.0 8.5	13.0 12.0	7.0 6.0	15.0 13.0	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}$ to $\overline{Q}_n$	Waveform 3 Waveform 4	2.5 1.5	5.0 4.0	8.5 7.0	2.0 1.5	9.0 8.0	ns

AC WAVEFORMS



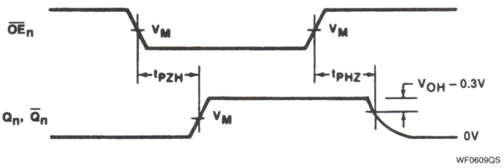
Dn
VM
VM
tPLH
tPHL
Qn
VM
VM
WF0606CS

Waveform 1. Propagation Delay for Non-Inverting Outputs



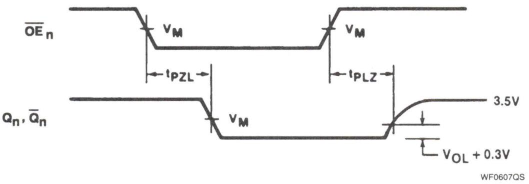
Dn
VM
VM
tPHL
tPLH
Q̄n
VM
VM
WF07544S

Waveform 2. Propagation Delay for Inverting Outputs



OEn
VM
VM
tPZH
tPHZ
VOH − 0.3V
Qn, Q̄n
VM
0V
WF0609QS

Waveform 3. 3-State Enable Time to High Level and Disable Time From High Level

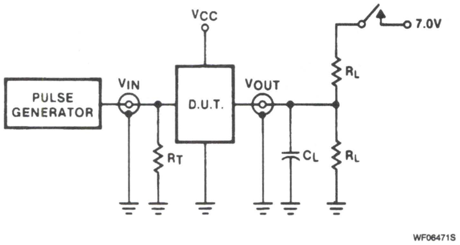


OEn
VM
VM
tPZL
tPLZ
3.5V
Qn, Q̄n
VM
VOL + 0.3V
WF0607QS

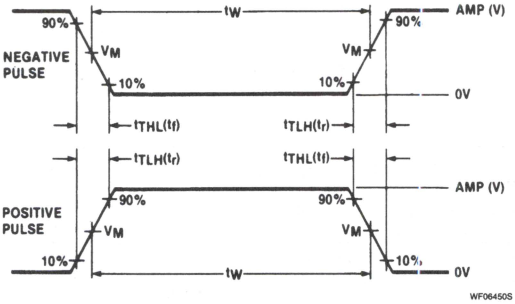
Waveform 4. 3-State Enable Time to Low Level and Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORMS


VCC
7.0V
RL
PULSE GENERATOR
VIN
D.U.T.
VOUT
RT
CL
RL
WF06471S

Test Circuit for 3-State Outputs


tW
AMP (V)
90%
90%
NEGATIVE PULSE
VM
VM
10%
10%
0V
tTHL(tf)
tTLH(tr)
tTLH(tr)
tTHL(tf)
AMP (V)
90%
90%
POSITIVE PULSE
VM
VM
10%
10%
0V
tW
WF06450S

$V_M = 1.5V$

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F838

Microprogram Sequence Controller

Preliminary Specification

FAST Products

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
N74F838	90MHz	65mA

FEATURES

- 5-bit address generator (32 Micro-instruction addressability)
- Two subroutine branching capability
- Interrupt branching
- Cascadable for increased addressing
- Direct branching over full address range

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V± 10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F838
20-Pin Plastic SOL	N74F838D

DESCRIPTION

The Signetics 74F838 Microprogram Sequence Controller generates addresses to access instructions from a microprogram memory.

This high-speed device provides an efficient means of controlling the flow through a microprogram by providing a powerful set of sequencing functions.

In addition to providing branching facility over the entire address range, the device also supports two subroutines and an interrupt level.

The 74F838 can directly address up to 32 micro-instructions; however, two or more of these devices may be cascaded for increased addressing. For example: two devices can address 1K and three devices can address up to 32K of program storage.

Combined with memory, the 74F838 forms a powerful control section for CPUs and I/O controllers.

The device is available in a 20-pin Dual-In-Line (DIP) and SOL Packages.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
JS0 – JS4	Jump State inputs	1.0/1.0	20μA/0.6mA
JMP	Jump input	1.0/2.0	20μA/0.6mA
SUB1,SUB2	Subroutine inputs	1.0/1.0	20μA/0.6mA
$\overline{\text{INT}}$	Interrupt input (active-Low)	1.0/1.0	20μA/0.6mA
CLK	Clock input	1.0/1.0	20μA/0.6mA
CI	Cascade-In/input	1.0/1.0	20μA/0.6mA
$\overline{\text{RESET}}$	Reset input (active-Low)	1.0/1.0	20μA/0.6mA
PS0 – PS4	Present state outputs	150/40	3mA/24mA
CO	Cascade-Out/output	150/40	3mA/24mA

NOTE:

1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6 mA in the Low state.

FAST 74F841/842/843/844/845/846

Bus Interface Latches

Preliminary Specification for 74F843 and 74F845
Product Specification for 74F841, 74F842, 74F844, and 74F846

'F841/'F842 10-Bit Bus Interface Latches, NINV/INV (3-State)
'F843/'F844 9-Bit Bus Interface Latches, NINV/INV (3-State)
'F845/'F846 8-Bit Bus Interface Latches, NINV/INV (3-State)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F841, 74F842	5.5ns	60mA
74F843, 74F844	6.2ns	65mA
74F845, 74F846	6.2ns	60mA

FEATURES

- High-speed parallel latches
- Extra data width for wide address/data paths or buses carrying parity
- High-impedance NPN base input structure minimizes bus loading
- I_{IL} is 20μA vs 1000μA for AM29841 series
- Buffered control inputs to reduce AC effects
- Ideal where high-speed, light loading, or increased fan-in are required as with MOS microprocessors
- Positive and negative over-shoots are clamped to ground
- 3-State outputs glitch free during power-up and power-down
- 48mA sink current
- Slim DIP 300mil package
- Broadside pinout
- Pin-for-pin and function compatible with AMD AM29841 – 29846 series

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
24-Pin Plastic Slim DIP (300mil)	N74F841N, N74F842N, N74F843N N74F844N, N74F845N, N74F846N
24-Pin Plastic SOL	N74F841D, N74F842D, N74F843D N74F844N, N74F845N, N74F846N

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_n	Data input	1.0/0.033	20μA/20μA
LE	Latch Enable input	1.0/0.033	20μA/20μA
$\overline{OE}$, $\overline{OE}_n$	Output Enable input (active-Low)	1.0/0.033	20μA/20μA
$\overline{MR}$	Master Reset input (active-Low)	1.0/0.033	20μA/20μA
$\overline{PRE}$	Preset input (active-Low)	1.0/0.033	20μA/20μA
Q_n	Data output	750/80	15mA/48mA
$\overline{Q}_n$	Data output	750/80	15mA/48mA

NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

DESCRIPTION

The 'F841 – 'F846 bus interface latch series are designed to provide extra data width for wider address/data paths or busses carrying parity. The 'F841 – 'F846 series are functionally and pin compatible to AMD AM29841 – AM29846 series.

The 'F841 consists of ten D-type latches with 3-State outputs. The flip-flops appear transparent to the data when Latch Enable (LE) is High. This allows asynchronous operation, as the output transition follows the data in transition. On the LE High-to-Low transition, the data that meets the setup and hold time is latched.

Data appears on the bus when the Output Enable ($\overline{OE}$) is Low. When OE is High the output is in the High-impedance state. The 'F842 is the inverted output version of 'F841.

The 'F843 consists of nine D-type latches with 3-State outputs.

In addition to the LE and $\overline{OE}$ pins, the 'F843 has a Master Reset ($\overline{MR}$) pin and a Preset ($\overline{PRE}$) pin. These pins are ideal for parity bus interfacing in high performance systems. When $\overline{MR}$ is Low, the outputs are Low if $\overline{OE}$ is Low. When $\overline{MR}$ is High, data can be entered into the latch. When $\overline{PRE}$ is Low, the outputs are High, if $\overline{OE}$ is Low. $\overline{PRE}$ overrides $\overline{MR}$. The 'F844 is the inverted output version of 'F843. The 'F845 consists of eight D-type latches with 3-State outputs.

In addition to the LE, $\overline{OE}$, $\overline{MR}$ and $\overline{PRE}$ pins, the 'F845 has two additional $\overline{OE}$ pins making a total of three Output Enable ($\overline{OE}_0$, $\overline{OE}_1$, $\overline{OE}_2$) pins.

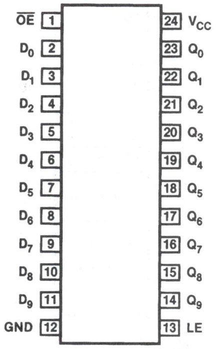
The multiple Output Enables ($\overline{OE}_0$, $\overline{OE}_1$, $\overline{OE}_2$) allow multiuser control of the interface, e.g., $\overline{CS}$, DMA, and RD/$\overline{WR}$. The 'F846 is the inverted output version of 'F845.

Bus Interface Latches

FAST 74F841/842/843/844/845/846

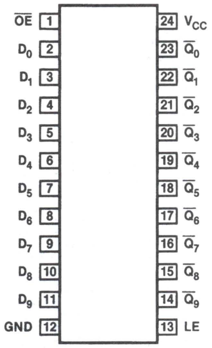
PIN CONFIGURATION

'F841


$\overline{OE}$ 1
D_0 2
D_1 3
D_2 4
D_3 5
D_4 6
D_5 7
D_6 8
D_7 9
D_8 10
D_9 11
GND 12
24 V_{CC}
23 Q_0
22 Q_1
21 Q_2
20 Q_3
19 Q_4
18 Q_5
17 Q_6
16 Q_7
15 Q_8
14 Q_9
13 LE

CD08150S

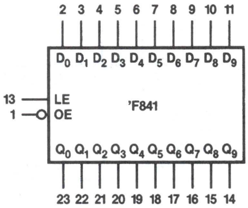
'F842


$\overline{OE}$ 1
D_0 2
D_1 3
D_2 4
D_3 5
D_4 6
D_5 7
D_6 8
D_7 9
D_8 10
D_9 11
GND 12
24 V_{CC}
23 $\overline{Q}_0$
22 $\overline{Q}_1$
21 $\overline{Q}_2$
20 $\overline{Q}_3$
19 $\overline{Q}_4$
18 $\overline{Q}_5$
17 $\overline{Q}_6$
16 $\overline{Q}_7$
15 $\overline{Q}_8$
14 $\overline{Q}_9$
13 LE

CD08140S

LOGIC SYMBOL

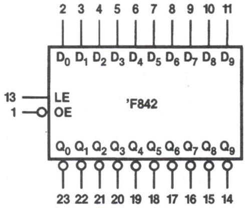
'F841


2 3 4 5 6 7 8 9 10 11
D_0 D_1 D_2 D_3 D_4 D_5 D_6 D_7 D_8 D_9
13 LE
1 OE
'F841
Q_0 Q_1 Q_2 Q_3 Q_4 Q_5 Q_6 Q_7 Q_8 Q_9
23 22 21 20 19 18 17 16 15 14

LS10160S

V_{CC} = Pin 24
GND = Pin 12

'F842

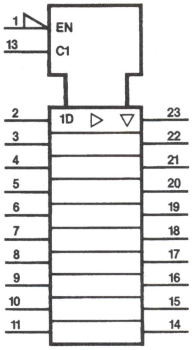

2 3 4 5 6 7 8 9 10 11
D_0 D_1 D_2 D_3 D_4 D_5 D_6 D_7 D_8 D_9
13 LE
1 OE
'F842
Q_0 Q_1 Q_2 Q_3 Q_4 Q_5 Q_6 Q_7 Q_8 Q_9
23 22 21 20 19 18 17 16 15 14

LS10150S

V_{CC} = Pin 24
GND = Pin 12

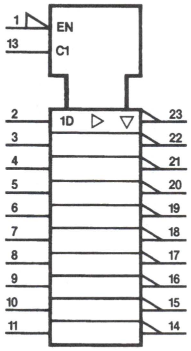
LOGIC SYMBOL (IEEE/IEC)

'F841


1
13
EN
C1
1D
2 3 4 5 6 7 8 9 10 11
23 22 21 20 19 18 17 16 15 14

LS10030S

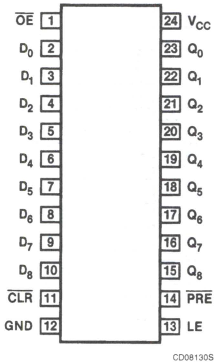
'F842


1
13
EN
C1
1D
2 3 4 5 6 7 8 9 10 11
23 22 21 20 19 18 17 16 15 14

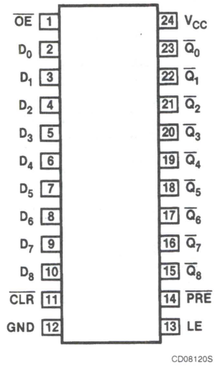
LS10040S

PIN CONFIGURATION

'F843

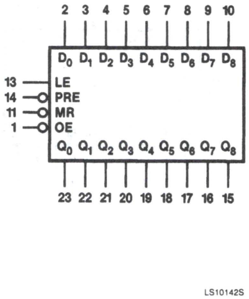

$\overline{OE}$ 1
D_0 2
D_1 3
D_2 4
D_3 5
D_4 6
D_5 7
D_6 8
D_7 9
D_8 10
$\overline{CLR}$ 11
GND 12
24 V_{CC}
23 Q_0
22 Q_1
21 Q_2
20 Q_3
19 Q_4
18 Q_5
17 Q_6
16 Q_7
15 Q_8
14 $\overline{PRE}$
13 LE
CD08130S

'F844


$\overline{OE}$ 1
D_0 2
D_1 3
D_2 4
D_3 5
D_4 6
D_5 7
D_6 8
D_7 9
D_8 10
$\overline{CLR}$ 11
GND 12
24 V_{CC}
23 $\overline{Q}_0$
22 $\overline{Q}_1$
21 $\overline{Q}_2$
20 $\overline{Q}_3$
19 $\overline{Q}_4$
18 $\overline{Q}_5$
17 $\overline{Q}_6$
16 $\overline{Q}_7$
15 $\overline{Q}_8$
14 $\overline{PRE}$
13 LE
CD08120S

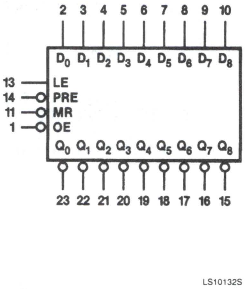
LOGIC SYMBOL

'F843


2 3 4 5 6 7 8 9 10
D_0 D_1 D_2 D_3 D_4 D_5 D_6 D_7 D_8
13 LE
14 PRE
11 MR
1 OE
Q_0 Q_1 Q_2 Q_3 Q_4 Q_5 Q_6 Q_7 Q_8
23 22 21 20 19 18 17 16 15
LS10142S

V_{CC} = Pin 24
GND = Pin 12

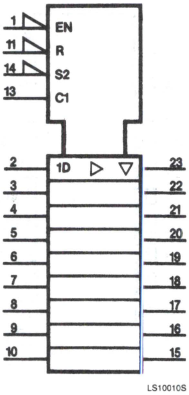
'F844


2 3 4 5 6 7 8 9 10
D_0 D_1 D_2 D_3 D_4 D_5 D_6 D_7 D_8
13 LE
14 PRE
11 MR
1 OE
Q_0 Q_1 Q_2 Q_3 Q_4 Q_5 Q_6 Q_7 Q_8
23 22 21 20 19 18 17 16 15
LS10132S

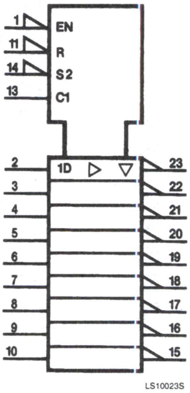
V_{CC} = Pin 24
GND = Pin 12

LOGIC SYMBOL (IEEE/IEC)

'F843

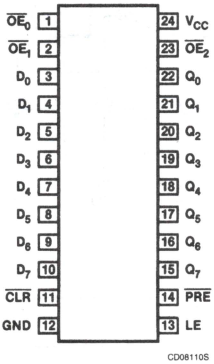

1 EN
11 R
14 S2
13 C1
1D
2 3 4 5 6 7 8 9 10
23 22 21 20 19 18 17 16 15
LS10010S

'F844

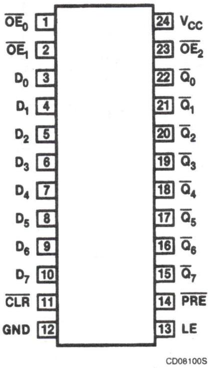

1 EN
11 R
14 S2
13 C1
1D
2 3 4 5 6 7 8 9 10
23 22 21 20 19 18 17 16 15
LS10023S

PIN CONFIGURATION

'F845

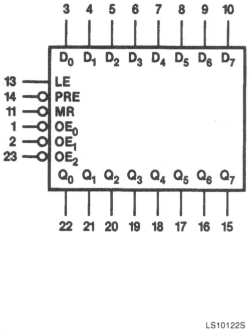

$\overline{OE}_0$ 1
$\overline{OE}_1$ 2
D_0 3
D_1 4
D_2 5
D_3 6
D_4 7
D_5 8
D_6 9
D_7 10
$\overline{CLR}$ 11
GND 12
24 V_{CC}
23 $\overline{OE}_2$
22 Q_0
21 Q_1
20 Q_2
19 Q_3
18 Q_4
17 Q_5
16 Q_6
15 Q_7
14 $\overline{PRE}$
13 LE
CD08110S

'F846


$\overline{OE}_0$ 1
$\overline{OE}_1$ 2
D_0 3
D_1 4
D_2 5
D_3 6
D_4 7
D_5 8
D_6 9
D_7 10
$\overline{CLR}$ 11
GND 12
24 V_{CC}
23 $\overline{OE}_2$
22 $\overline{Q}_0$
21 $\overline{Q}_1$
20 $\overline{Q}_2$
19 $\overline{Q}_3$
18 $\overline{Q}_4$
17 $\overline{Q}_5$
16 $\overline{Q}_6$
15 $\overline{Q}_7$
14 $\overline{PRE}$
13 LE
CD08100S

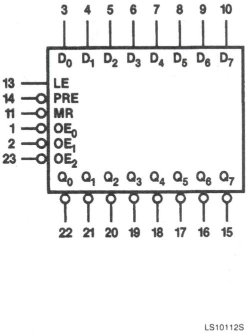
LOGIC SYMBOL

'F845


3 4 5 6 7 8 9 10
D_0 D_1 D_2 D_3 D_4 D_5 D_6 D_7
13 LE
14 PRE
11 MR
1 OE_0
2 OE_1
23 OE_2
Q_0 Q_1 Q_2 Q_3 Q_4 Q_5 Q_6 Q_7
22 21 20 19 18 17 16 15
LS10122S

V_{CC} = Pin 24
GND = Pin 12

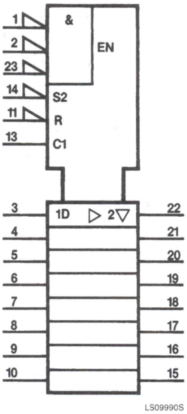
'F846


3 4 5 6 7 8 9 10
D_0 D_1 D_2 D_3 D_4 D_5 D_6 D_7
13 LE
14 PRE
11 MR
1 OE_0
2 OE_1
23 OE_2
Q_0 Q_1 Q_2 Q_3 Q_4 Q_5 Q_6 Q_7
22 21 20 19 18 17 16 15
LS10112S

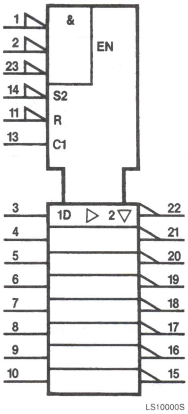
V_{CC} = Pin 24
GND = Pin 12

LOGIC SYMBOL (IEEE/IEC)

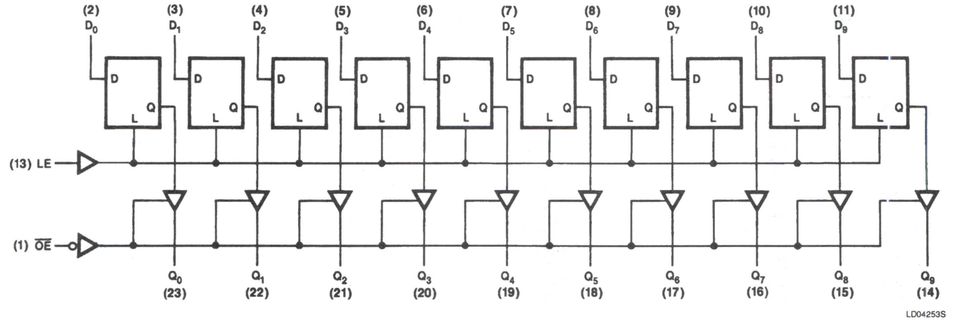
'F845


1
2
23
&
EN
14 S2
11 R
13 C1
3 1D ▷ 2▽ 22
4 21
5 20
6 19
7 18
8 17
9 16
10 15
LS09990S

'F846

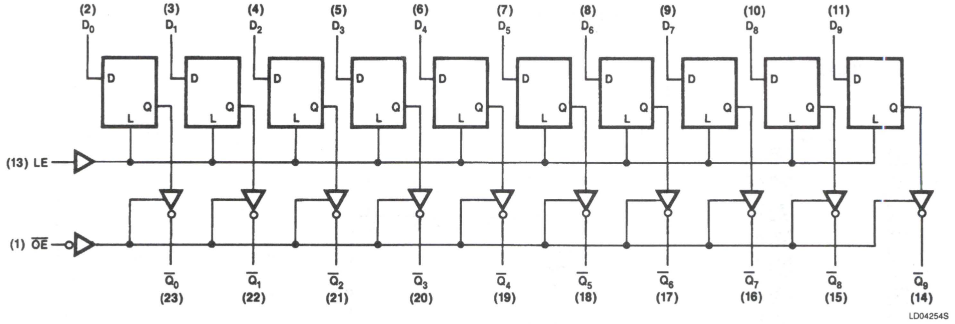

1
2
23
&
EN
14 S2
11 R
13 C1
3 1D ▷ 2▽ 22
4 21
5 20
6 19
7 18
8 17
9 16
10 15
LS10000S

LOGIC DIAGRAM FOR 'F841


(2) D_0
(3) D_1
(4) D_2
(5) D_3
(6) D_4
(7) D_5
(8) D_6
(9) D_7
(10) D_8
(11) D_9
D
Q
L
(13) LE
(1) $\overline{OE}$
Q_0 (23)
Q_1 (22)
Q_2 (21)
Q_3 (20)
Q_4 (19)
Q_5 (18)
Q_6 (17)
Q_7 (16)
Q_8 (15)
Q_9 (14)
LD04253S

V_{CC} = Pin 24
GND = Pin 12

LOGIC DIAGRAM FOR 'F842


(2) D_0
(3) D_1
(4) D_2
(5) D_3
(6) D_4
(7) D_5
(8) D_6
(9) D_7
(10) D_8
(11) D_9
D
Q
L
(13) LE
(1) $\overline{OE}$
$\overline{Q}_0$ (23)
$\overline{Q}_1$ (22)
$\overline{Q}_2$ (21)
$\overline{Q}_3$ (20)
$\overline{Q}_4$ (19)
$\overline{Q}_5$ (18)
$\overline{Q}_6$ (17)
$\overline{Q}_7$ (16)
$\overline{Q}_8$ (15)
$\overline{Q}_9$ (14)
LD04254S

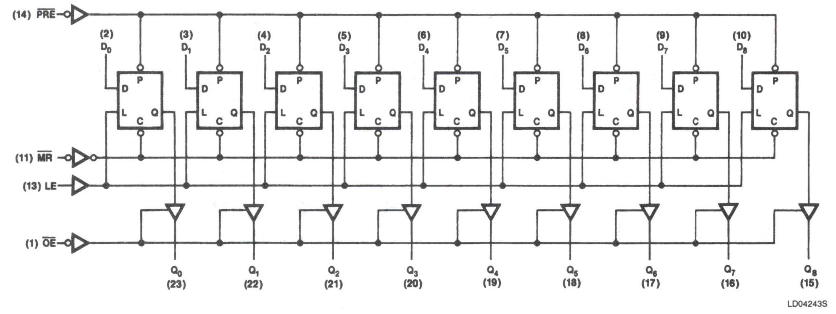
V_{CC} = Pin 24
GND = Pin 12

FUNCTION TABLE FOR 'F841 AND 'F842

INPUTS			OUTPUTS		OPERATING MODE
			'F841	'F842	
$\overline{OE}$	LE	D_n	Q	$\overline{Q}$	
L L	H H	L H	L H	H L	Transparent
L L	↓ ↓	l h	L H	H L	Latched
H	X	X	Z	Z	Hi-Z
L	L	X	NC	NC	Hold

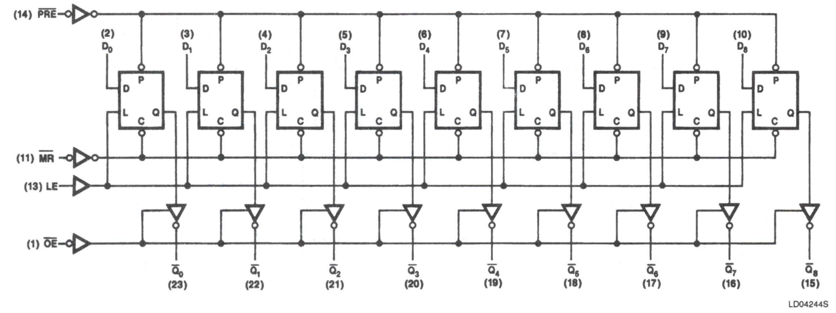
H = High voltage level steady state
h = High voltage level one setup time prior to the High-to-Low transition of LE
L = Low voltage level steady state
l = Low voltage level one setup time prior to the High-to-Low transition of LE
X = Don't care
Z = High-impedance
NC = No change
↓ = High-to-Low transition

LOGIC DIAGRAM FOR 'F843


(14) $\overline{PRE}$
(2) D_0
(3) D_1
(4) D_2
(5) D_3
(6) D_4
(7) D_5
(8) D_6
(9) D_7
(10) D_8
D
P
L
C
Q
(11) $\overline{MR}$
(13) LE
(1) $\overline{OE}$
Q_0 (23)
Q_1 (22)
Q_2 (21)
Q_3 (20)
Q_4 (19)
Q_5 (18)
Q_6 (17)
Q_7 (16)
Q_8 (15)
LD04243S

V_{CC} = Pin 24
GND = Pin 12

LOGIC DIAGRAM FOR 'F844


(14) $\overline{PRE}$
(2) D_0
(3) D_1
(4) D_2
(5) D_3
(6) D_4
(7) D_5
(8) D_6
(9) D_7
(10) D_8
D
P
L
C
Q
(11) $\overline{MR}$
(13) LE
(1) $\overline{OE}$
$\overline{Q}_0$ (23)
$\overline{Q}_1$ (22)
$\overline{Q}_2$ (21)
$\overline{Q}_3$ (20)
$\overline{Q}_4$ (19)
$\overline{Q}_5$ (18)
$\overline{Q}_6$ (17)
$\overline{Q}_7$ (16)
$\overline{Q}_8$ (15)
LD04244S

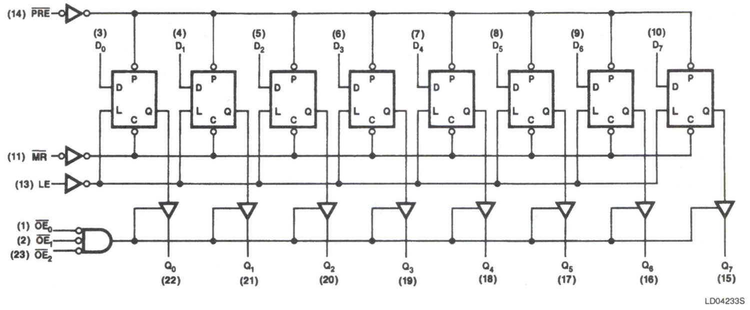
V_{CC} = Pin 24
GND = Pin 12

FUNCTION TABLE FOR 'F843 AND 'F844

INPUTS					OUTPUTS		OPERATING MODE
					'F843	'F844	
$\overline{OE}$	$\overline{PRE}$	$\overline{MR}$	LE	D_n	Q	$\overline{Q}$	
H	X	X	X	X	Z	Z	Hi-Z
L	L	X	X	X	H	H	Preset
L	H	L	X	X	L	L	Clear
L	H	H	H	L	L	H	Transparent
L	H	H	H	H	H	L	
L	H	H	↓	l	L	H	Latched
L	H	H	↓	h	H	L	
L	H	H	L	X	NC	NC	Hold

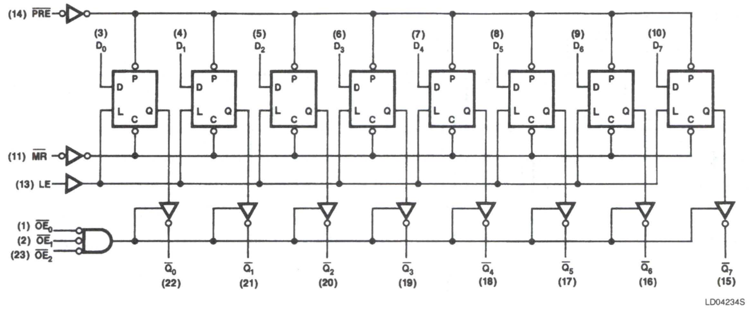
H = High voltage level steady state
h = High voltage level one setup time prior to the High-to-Low transition of LE
L = Low voltage level steady state
l = Low voltage level one setup time prior to the High-to-Low transition of LE
X = Don't care
Z = High-impedance
NC = No change
↓ = High-to-Low transition

LOGIC DIAGRAM FOR 'F845


(14) $\overline{PRE}$
(3) D_0
(4) D_1
(5) D_2
(6) D_3
(7) D_4
(8) D_5
(9) D_6
(10) D_7
D
P
L
C
Q
(11) $\overline{MR}$
(13) LE
(1) $\overline{OE}_0$
(2) $\overline{OE}_1$
(23) $\overline{OE}_2$
Q_0 (22)
Q_1 (21)
Q_2 (20)
Q_3 (19)
Q_4 (18)
Q_5 (17)
Q_6 (16)
Q_7 (15)
LD04233S

V_{CC} = Pin 24
GND = Pin 12

LOGIC DIAGRAM FOR 'F846


(14) $\overline{PRE}$
(3) D_0
(4) D_1
(5) D_2
(6) D_3
(7) D_4
(8) D_5
(9) D_6
(10) D_7
D
P
L
C
Q
(11) $\overline{MR}$
(13) LE
(1) $\overline{OE}_0$
(2) $\overline{OE}_1$
(23) $\overline{OE}_2$
$\overline{Q}_0$ (22)
$\overline{Q}_1$ (21)
$\overline{Q}_2$ (20)
$\overline{Q}_3$ (19)
$\overline{Q}_4$ (18)
$\overline{Q}_5$ (17)
$\overline{Q}_6$ (16)
$\overline{Q}_7$ (15)
LD04234S

V_{CC} = Pin 24
GND = Pin 12

FUNCTION TABLE FOR 'F845 AND 'F846

INPUTS					OUTPUTS		OPERATING MODE
					'F845	'F846	
$\overline{OE}_n$	$\overline{PRE}$	$\overline{MR}$	LE	D_n	Q	$\overline{Q}$	
H	X	X	X	X	Z	Z	Hi-Z
L	L	X	X	X	H	H	Preset
L	H	L	X	X	L	L	Clear
L L	H H	H H	H H	L H	L H	H L	Transparent
L L	H H	H H	↓ ↓	l h	L H	H L	Latched
L	H	H	L	X	NC	NC	Hold

H = High voltage level steady state
h = High voltage level one setup time prior to the High-to-Low transition of LE
L = Low voltage level steady state
l = Low voltage level one setup time prior to the High-to-Low transition of LE
X = Don't care
Z = High-impedance
NC = No change
↓ = High-to-Low transition

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	84	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−15	mA
I_{OL}	Low-level output current			48	mA
T_A	Operating free-air temperature	0		70	°C

Bus Interface Latches

FAST 74F841/842/843/844/845/846

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]			74F843, 74F845, 74F841, 74F842, 74F844, 74F846			UNIT
							Min	Typ[2]	Max	
V_{OH}	High-level output voltage			V_{CC} = MIN V_{IL} = MAX V_{IH} = MIN	I_{OH} = −15mA	±10%V_{CC}	2.0			V
						±5%V_{CC}	2.0			V
					I_{OH} = −3mA	±10%V_{CC}	2.4			V
						±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage			V_{CC} = MIN V_{IL} = MAX V_{IH} = MIN	I_{OL} = MAX	±10%V_{CC}		0.35	0.55	V
						±5%V_{CC}		0.35	0.55	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, $I_I = I_{IK}$				−0.73	−1.2	V
I_I	Input current at maximum input voltage			V_{CC} = 0.0V, V_I = 7.0V					100	μA
I_{IH}	High-level input current			V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	Low-level input current			V_{CC} = MAX, V_I = 0.5V					−20	mA
I_{OZH}	OFF-state output current, High-level voltage applied			V_{CC} = MAX, V_O = 2.7V					50	μA
I_{OZL}	OFF-state output current, Low-level voltage applied			V_{CC} = MAX, V_O = 0.5V					−50	μA
I_{OS}	Short-circuit output current[3]			V_{CC} = MAX			−100		−225	mA
I_{CC}	Supply current (total)	'F841	I_{CCH}	V_{CC} = MAX				50	70	mA
			I_{CCL}					60	80	mA
			I_{CCZ}					70	95	mA
I_{CC}	Supply current (total)	'F842	I_{CCH}	V_{CC} = MAX				40	60	mA
			I_{CCL}					65	90	mA
			I_{CCZ}					60	90	mA
I_{CC}	Supply current (total)	'F844 'F846	I_{CCH}	V_{CC} = MAX				50	70	mA
			I_{CCL}					70	100	mA
			I_{CCZ}					70	100	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	74F841, 74F842					UNIT
				$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$, $R_L = 500\Omega$		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n or $\overline{Q}_n$	'F841	Waveform 1, 2	2.0 2.5	4.0 4.5	7.5 7.5	2.0 2.5	8.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay LE to Q_n or $\overline{Q}_n$		Waveform 1, 2	4.5 4.0	6.5 6.0	9.5 9.0	4.0 3.5	10.5 9.5	ns
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n or $\overline{Q}_n$	'F842	Waveform 1, 2	3.5 3.0	5.5 5.0	8.5 8.0	4.5 4.0	9.0 8.5	ns
t_{PLH} t_{PHL}	Propagation delay LE to Q_n or $\overline{Q}_n$		Waveform 1, 2	5.0 4.5	7.0 6.5	10.0 9.0	3.0 3.0	10.5 9.5	ns
t_{PZH} t_{PZL}	Output enable time to High or Low level, $\overline{OE}_n$ to Q_n or $\overline{Q}_n$		Waveform 5 Waveform 6	2.5 6.5	4.5 8.5	8.0 12.0	2.0 5.5	8.5 13.0	ns
t_{PHZ} t_{PLZ}	Output enable time to High or Low level, $\overline{OE}_n$ to Q_n or $\overline{Q}_n$		Waveform 5 Waveform 6	1.0 1.0	4.5 5.0	8.0 8.0	1.0 1.0	8.5 8.5	ns

AC SETUP REQUIREMENTS

SYMBOL	PARAMETER		TEST CONDITIONS	74F841, 74F842				UNIT
				$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$, $R_L = 500\Omega$		$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$, $R_L = 500\Omega$		
				Min	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to LE		Waveform 2	0.0 0.0		1.0 1.0		ns
$t_h(H)$ $t_s(L)$	Hold time, High or Low D_n to LE	'F841	Waveform 2	2.5 3.0		3.0 4.0		ns
$t_w(H)$	LE pulse width, High		Waveform 2	3.5		4.0		ns
$t_h(H)$ $t_s(L)$	Hold time, High or Low D_n to LE	'F842	Waveform 2	3.0 3.5		3.5 4.5		ns
$t_w(H)$	LE pulse width, High		Waveform 2	3.0		3.0		ns

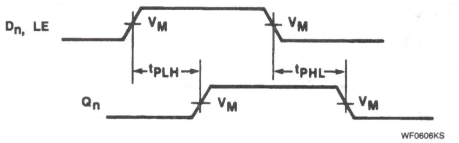
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F844, 74F846					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$, $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n or $\overline{Q}_n$	Waveform 1, 2	3.5 3.0	5.5 5.0	8.5 8.0	3.0 3.0	9.5 8.5	ns
t_{PLH} t_{PHL}	Propagation delay LE to Q_n or $\overline{Q}_n$	Waveform 1, 2	5.0 4.5	7.0 6.5	10.0 9.0	5.0 4.5	10.5 9.5	ns
t_{PLH}	Propagation delay $\overline{PRE}$ to Q_n or $\overline{Q}_n$	Waveform 3	3.5	5.5	8.5	3.0	9.5	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n or $\overline{Q}_n$	Waveform 3	5.0	7.0	10.0	4.5	10.5	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level, $\overline{OE}_n$ to Q_n or $\overline{Q}_n$	Waveform 5 Waveform 6	2.5 6.5	5.0 8.5	7.5 11.5	2.0 5.5	8.0 12.5	ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level, $\overline{OE}_n$ to Q_n or $\overline{Q}_n$	Waveform 5 Waveform 6	1.0 1.0	4.5 5.0	8.0 8.0	1.0 1.0	8.5 8.5	ns

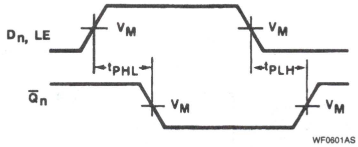
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	74F844, 74F846				UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$, $R_L = 500\Omega$		$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$, $R_L = 500\Omega$		
			Min	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to LE	Waveform 2	0.0 0.0		0.0 0.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to LE	Waveform 2	3.0 4.0		3.0 4.0		ns
$t_w(H)$	LE Pulse width, High	Waveform 2	3.0		3.0		ns
$t_w(L)$	$\overline{PRE}$ Pulse width, Low	Waveform 2	4.0		5.0		ns
$t_w(L)$	$\overline{MR}$ Pulse width, Low	Waveform 2	4.0		5.0		ns
t_{rec}	$\overline{PRE}$ Recovery time	Waveform 2	0.0		0.0		ns
t_{rec}	$\overline{MR}$ Recovery time	Waveform 2	3.5		4.5		ns

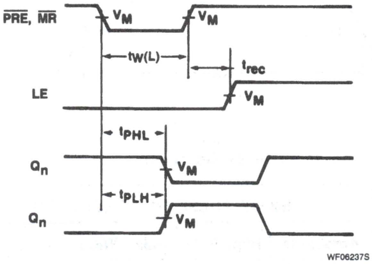
AC WAVEFORMS


Dn, LE
VM
VM
tPLH
tPHL
Qn
VM
VM
WF0606KS

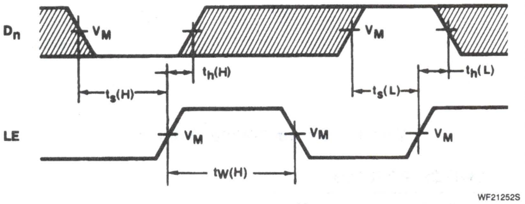
Waveform 1. Propagation Delay for Non-Inverting Outputs


Dn, LE
VM
VM
tPHL
tPLH
Q̄n
VM
VM
WF0601AS

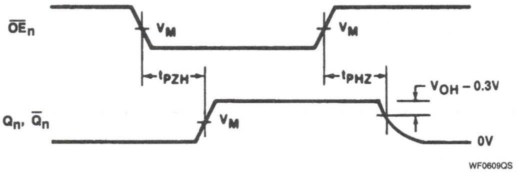
Waveform 2. Propagation Delay for Inverting Outputs


PRE, MR
VM
VM
tW(L)
trec
LE
VM
tPHL
Qn
VM
tPLH
Qn
VM
WF06237S

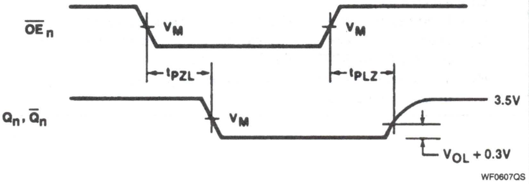
Waveform 3. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time


Dn
VM
th(H)
ts(H)
VM
th(L)
ts(L)
LE
VM
tW(H)
VM
VM
WF21252S

Waveform 4. Data and Select Setup and Hold Times


OEn
VM
VM
tPZH
tPHZ
VOH – 0.3V
Qn, Q̄n
VM
0V
WF0609QS

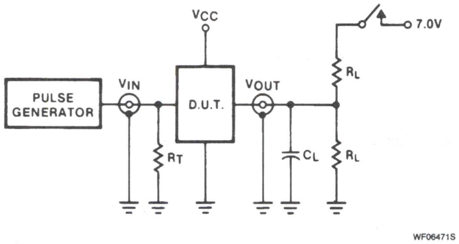
Waveform 5. 3-State Output Enable Time to High Level and Output Disable Time From High Level


OEn
VM
VM
tPZL
tPLZ
3.5V
Qn, Q̄n
VM
VOL + 0.3V
WF0607QS

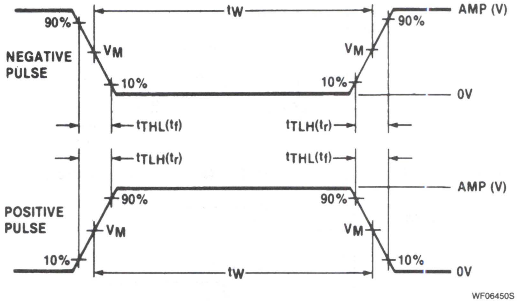
Waveform 6. 3-State Output Enable Time to Low Level and Output Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS


VCC
7.0V
RL
PULSE GENERATOR
VIN
D.U.T.
VOUT
RT
CL
RL
WF06471S

Test Circuit for 3-State Outputs


NEGATIVE PULSE
90%
VM
10%
tW
AMP (V)
0V
tTHL(tf)
tTLH(tr)
POSITIVE PULSE
90%
VM
10%
tTLH(tr)
tTHL(tf)
AMP (V)
0V
tW
WF06450S

$V_M = 1.5V$

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F861, 74F862, 74F863, 74F864

Bus Transceivers

'F861/'F862 10-Bit Bus Transceivers, NINV/INV (3-State)
'F863/'F864 9-Bit Bus Transceivers, NINV/INV (3-State)
Product Specification

FAST Products

FEATURES

- **Provide high-performance bus interface buffering for wide data/address paths or buses carrying parity**
- **High-impedance NPN base inputs for reduced loading (70μA in High and Low states)**
- **I_{IL} is 20μA vs 1000μA for AM29861 series**
- **Buffered control inputs to light loading, or increased fan-in are required as with MOS microprocessors**
- **Positive and negative over-shoots are clamped to ground**
- **3-State outputs glitch free during power-up and power-down**
- **Slim DIP 300mil package**
- **Broadside pinout compatible with AMD AM29861 – 29864 series**
- **Outputs sink 64mA**

DESCRIPTION

The 'F861 series Bus Transceivers provide High–performance bus interface buffering for wide data/address paths or buses carrying parity.

The 'F863/'F864 9-Bit Bus Transceivers have NORed Transmit and Receive Output Enables for maximum control flexibility.

All Data Transmit and Receive inputs have 200mV minimum input hysteresis to provide improved noise rejection.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F861, 74F863	6.0ns	140mA
74F862, 74F864	6.0ns	105mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$, $T_A = 0°C$ to $+70°C$
24-Pin Plastic Slim DIP (300mil)	N74F861N, N74F862N, N74F863N, N74F864N
24-Pin Plastic SOL[1]	N74F861D, N74F862D, N74F863D, N74F864D

NOTES:
1. Thermal mounting techniques are recommended. See App Note AN SMD-100 for a discussion of thermal considerations for surface mounted devices.

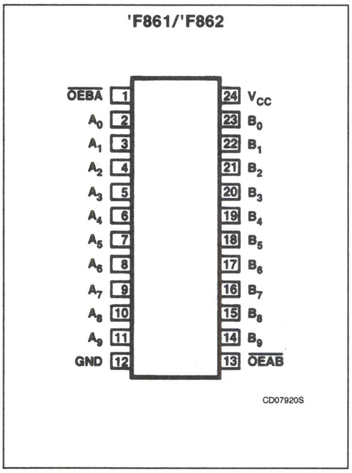
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

TYPE	PINS	DESCRIPTION	74F(U.L) HIGH/LOW	LOAD VALUE HIGH/LOW
'F861 'F862	$A_0 - A_9$	Data transmit inputs	3.5/0.117	70μA/70μA
	$B_0 - B_9$	Data receive inputs	3.5/0.117	70μA/70μA
	$\overline{OEBA}$	Transmit output enable input	1.0/0.033	20μA/20μA
	$\overline{OEAB}$	Receive output enable input	1.0/0.033	20μA/20μA
	$\bar{A}_0 - \bar{A}_9$	Data transmit outputs	750/106.7	15mA/64mA
	$\bar{B}_0 - \bar{B}_9$	Data receive outputs	750/106.7	15mA/64mA
'F863 'F864	$A_0 - A_8$	Data transmit inputs	3.5/0.117	70μA/70μA
	$B_0 - B_8$	Data receive inputs	3.5/0.117	70μA/70μA
	$\overline{OEBA_0}$ $\overline{OEBA_1}$	Transmit output enable inputs	1.0/0.033	20μA/20μA
	$\overline{OEAB_0}$ $\overline{OEAB_1}$	Receive output enable inputs	1.0/0.033	20μA/20μA
	$A_0 - A_8$	Data transmit outputs	750/106.7	15mA/64mA
	$B_0 - B_8$	Data receive outputs	750/106.7	15mA/64mA

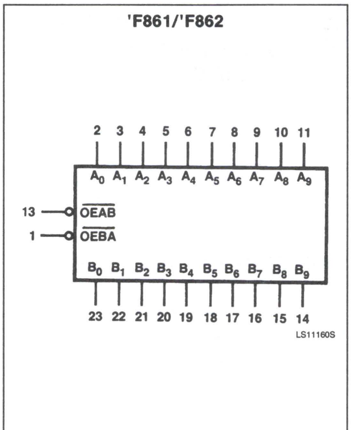
Bus Transceivers

FAST 74F861, 74F862, 74F863, 74F864

PIN CONFIGURATION

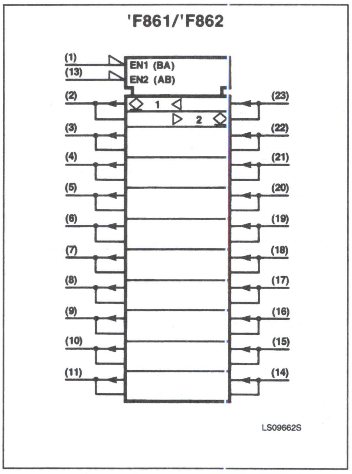

'F861/'F862
$\overline{OEBA}$ 1
A_0 2
A_1 3
A_2 4
A_3 5
A_4 6
A_5 7
A_6 8
A_7 9
A_8 10
A_9 11
GND 12
24 V_{CC}
23 B_0
22 B_1
21 B_2
20 B_3
19 B_4
18 B_5
17 B_6
16 B_7
15 B_8
14 B_9
13 $\overline{OEAB}$
CD07920S

LOGIC SYMBOL

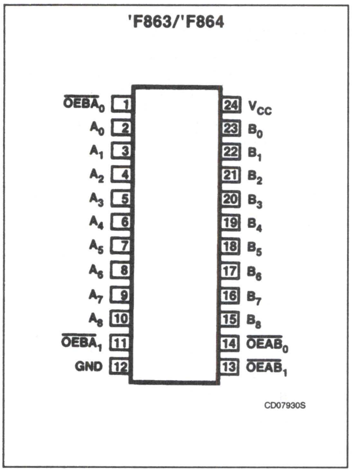

'F861/'F862
2 3 4 5 6 7 8 9 10 11
A_0 A_1 A_2 A_3 A_4 A_5 A_6 A_7 A_8 A_9
13 $\overline{OEAB}$
1 $\overline{OEBA}$
B_0 B_1 B_2 B_3 B_4 B_5 B_6 B_7 B_8 B_9
23 22 21 20 19 18 17 16 15 14
LS11160S

V_{CC} = Pin 24
GND = Pin 12

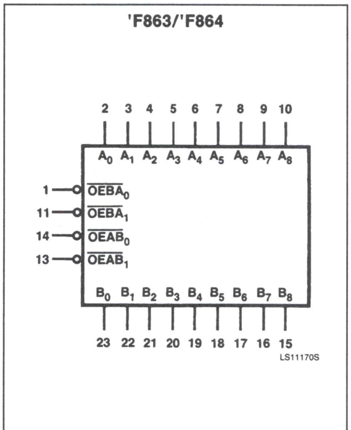
LOGIC SYMBOL (IEEE/IEC)


'F861/'F862
(1)
(13)
EN1 (BA)
EN2 (AB)
1
2
(2)
(3)
(4)
(5)
(6)
(7)
(8)
(9)
(10)
(11)
(23)
(22)
(21)
(20)
(19)
(18)
(17)
(16)
(15)
(14)
LS09662S

PIN CONFIGURATION

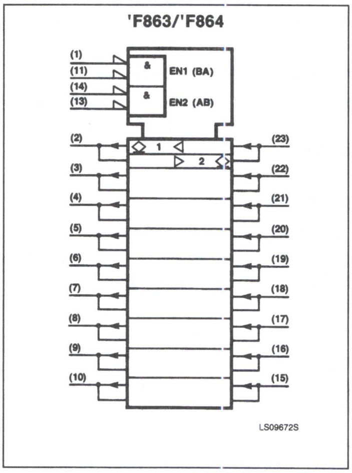

'F863/'F864
$\overline{OEBA}_0$ 1
A_0 2
A_1 3
A_2 4
A_3 5
A_4 6
A_5 7
A_6 8
A_7 9
A_8 10
$\overline{OEBA}_1$ 11
GND 12
24 V_{CC}
23 B_0
22 B_1
21 B_2
20 B_3
19 B_4
18 B_5
17 B_6
16 B_7
15 B_8
14 $\overline{OEAB}_0$
13 $\overline{OEAB}_1$
CD07930S

LOGIC SYMBOL


'F863/'F864
2 3 4 5 6 7 8 9 10
A_0 A_1 A_2 A_3 A_4 A_5 A_6 A_7 A_8
1 $\overline{OEBA}_0$
11 $\overline{OEBA}_1$
14 $\overline{OEAB}_0$
13 $\overline{OEAB}_1$
B_0 B_1 B_2 B_3 B_4 B_5 B_6 B_7 B_8
23 22 21 20 19 18 17 16 15
LS11170S

V_{CC} = Pin 24
GND = Pin 12

LOGIC SYMBOL (IEEE/IEC)

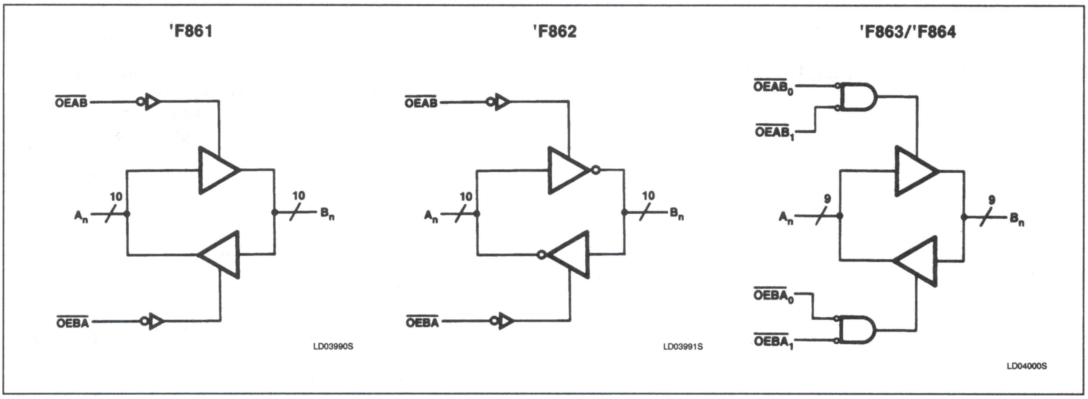

'F863/'F864
(1)
(11)
(14)
(13)
&
&
EN1 (BA)
EN2 (AB)
1
2
(2)
(3)
(4)
(5)
(6)
(7)
(8)
(9)
(10)
(23)
(22)
(21)
(20)
(19)
(18)
(17)
(16)
(15)
LS09672S

FUNCTION TABLE FOR 'F861 AND 'F862

INPUTS		MODE OF OPERATION	
$\overline{\text{OEAB}}$	$\overline{\text{OEBA}}$	'F861	'F862
L	H	A data to B bus	A data to B bus
H	L	B bus to A data	B bus to A data
H	H	Z	Z

H = High voltage level
L = Low voltage level
Z = High-impedance state

LOGIC DIAGRAM


'F861
'F862
'F863/'F864
$\overline{\text{OEAB}}$
$\overline{\text{OEBA}}$
A_n
B_n
10
10
LD03990S
$\overline{\text{OEAB}}$
$\overline{\text{OEBA}}$
A_n
B_n
10
10
LD03991S
$\overline{\text{OEAB}}_0$
$\overline{\text{OEAB}}_1$
$\overline{\text{OEBA}}_0$
$\overline{\text{OEBA}}_1$
A_n
B_n
9
9
LD04000S

FUNCTION TABLE FOR 'F863 AND 'F864

INPUTS				MODE OF OPERATION	
$OEAB_0$	$OEAB_1$	$OEBA_0$	$OEBA_1$	'F863	'F864
L	L	H	X	A data to B bus	A data to $\overline{B}$ bus
L	L	X	H		
H	X	L	L	B bus to A data	B bus to $\overline{A}$ data
X	H	L	L		
H	H	H	H	Z	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High-impedance state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +1	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	128	mA
T_A	Operating free-air temperature range	0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			–18	mA
I_{OH}	High-level output current			–15	mA
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]			74F861, 74F862 74F863, 74F864			UNIT
							Min	Typ[2]	Max	
V_{OH}	High-level output voltage			V_{CC} = MIN V_{IL} = MAX V_{IH} = MIN	I_{OH} = –15mA	±10%V_{CC}	2.0			V
						±5%V_{CC}	2.0			V
					I_{OH} = –3mA	±10%V_{CC}	2.4			V
						±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage			V_{CC} = MIN V_{IL} = MAX V_{IH} = MIN	I_{OL} = 48mA	±10%V_{CC}		0.35	0.50	V
					I_{OL} = 64mA	±5%V_{CC}		0.40	0.55	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, $I_I = I_{IK}$				–0.73	–1.2	V
I_I	Input current at maximum input voltage		CTRL	V_{CC} = 0.0V, V_I = 7.0V					100	μA
			A_n, B_n	V_{CC} = 5.5V, V_I = 5.5V					1	mA
I_{IH}	High-level input current			V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	Low-level input current			V_{CC} = MAX, V_I = 0.5V					–20	μA
I_{IH} + I_{OZH}	High-level input current		$A_0 - A_9$ $B_0 - B_9$	V_{CC} = MAX, V_O = 2.7V					70	μA
I_{IL} + I_{OZL}	Low-level input current			V_{CC} = MAX, V_O = 0.5V					–70	μA
I_{OS}	Short-circuit output current[3]			V_{CC} = MAX			–100		–225	mA
I_{CC}	Supply current (total)	861/863	I_{CCH}	V_{CC} = MAX				145	195	mA
			I_{CCL}					140	195	mA
			I_{CCZ}					130	190	mA
		862/864	I_{CCH}	V_{CC} = MAX				90	130	mA
			I_{CCL}					120	170	mA
			I_{CCZ}					100	145	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of High-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

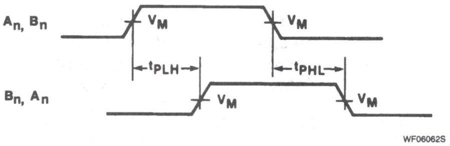
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F861, 74F863					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n	Waveform 1	4.0 3.0	6.0 5.0	9.0 8.0	3.5 2.5	10.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay B_n to A_n	Waveform 1	4.0 2.5	6.0 5.0	9.0 8.0	3.5 2.5	10.0 9.0	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level $\overline{OEBA}_n$ to A_n	Waveform 3 Waveform 4	6.0 4.5	8.0 7.0	11.5 10.5	5.0 4.5	13.0 12.0	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level $\overline{OEAB}_n$ to B_n	Waveform 3 Waveform 4	6.0 5.5	8.0 7.5	11.0 11.0	5.0 4.5	13.0 12.0	ns
t_{PHZ} t_{PLZ}	Output Enable time from High or Low level $\overline{OEBA}_n$ to A_n	Waveform 3 Waveform 4	3.5 2.5	5.5 5.0	9.0 8.5	3.0 2.0	9.5 9.5	ns
t_{PHZ} t_{PLZ}	Output Enable time from High or Low level $\overline{OEAB}_n$ to B_n	Waveform 3 Waveform 4	3.5 2.5	5.5 4.5	8.5 8.5	3.0 2.0	9.5 9.5	ns

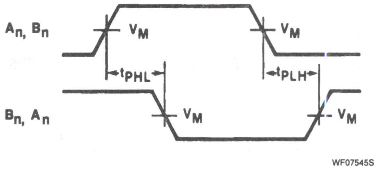
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F862, 74F864					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n	Waveform 2	4.0 1.5	6.0 3.5	9.0 6.5	3.0 1.5	10.5 7.0	ns
t_{PLH} t_{PHL}	Propagation delay B_n to A_n	Waveform 2	4.0 1.5	6.0 3.5	9.0 6.5	3.0 1.5	10.5 7.0	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level $\overline{OEBA}_n$ to A_n	Waveform 3 Waveform 4	6.5 7.0	8.5 9.5	12.0 13.5	5.5 6.0	13.5 15.5	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level $\overline{OEAB}_n$ to B_n	Waveform 3 Waveform 4	6.5 7.5	8.0 9.5	11.5 13.5	5.5 6.5	13.5 15.5	ns
t_{PHZ} t_{PLZ}	Output Enable time from High or Low level $\overline{OEBA}_n$ to A_n	Waveform 3 Waveform 4	3.0 2.5	5.0 4.0	8.5 8.5	2.5 2.0	9.5 9.0	ns
t_{PHZ} t_{PLZ}	Output Enable time from High or Low level $\overline{OEAB}_n$ to B_n	Waveform 3 Waveform 4	3.0 2.5	5.0 4.0	8.5 8.5	2.5 2.0	9.5 9.0	ns

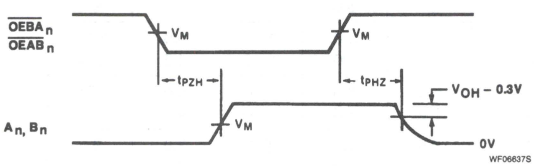
AC WAVEFORMS


An, Bn
VM
VM
tPLH
tPHL
Bn, An
VM
VM
WF06062S

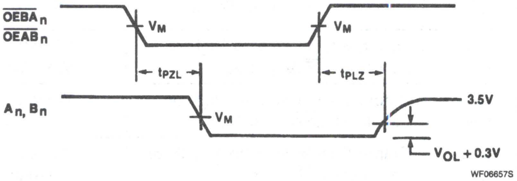
Waveform 1. Propagation Delay for Non-Inverting Outputs


An, Bn
VM
VM
tPHL
tPLH
Bn, An
VM
VM
WF07545S

Waveform 2. Propagation Delay for Inverting Outputs


OEBAn
OEABn
VM
VM
tPZH
tPHZ
VOH – 0.3V
An, Bn
VM
0V
WF06637S

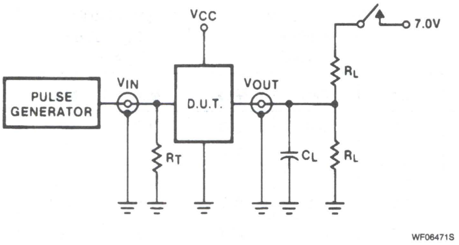
Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time From High Level


OEBAn
OEABn
VM
VM
tPZL
tPLZ
An, Bn
VM
3.5V
VOL + 0.3V
WF06657S

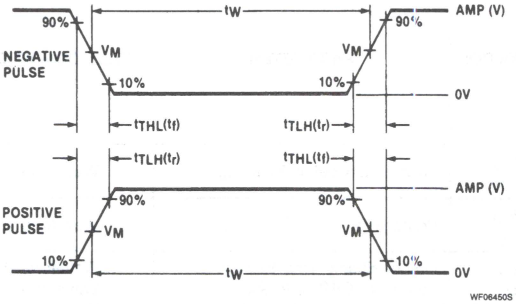
Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORMS


VCC
7.0V
RL
PULSE GENERATOR
VIN
D.U.T.
VOUT
RT
CL
RL
WF06471S

Test Circuit for 3-State Outputs


tW
AMP (V)
90%
90%
NEGATIVE PULSE
VM
VM
10%
10%
0V
tTHL(tf)
tTLH(tr)
tTLH(tr)
tTHL(tf)
AMP (V)
90%
90%
POSITIVE PULSE
VM
VM
10%
10%
0V
tW
WF06450S

$V_M = 1.5V$

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F881

Arithmetic Logic Unit/Function Generator

Product Specification

FAST Products

FEATURES

- Full look-ahead carry for High-speed arithmetic operation on long words
- Arithmetic Operating Modes:
  - addition
  - subtraction
  - shift operand A one position
  - magnitude comparison
  - plus twelve other arithmetic operations
- Logic Function Modes:
  - exclusive-OR
  - comparator
  - AND, NAND, OR, NOR
  - provides status register check
  - plus ten other logic operations
- Replaces 'AS 881
- Same pinout and function as 'F181 except for $\overline{P}$, $\overline{G}$, and C_{n+4} outputs when the device is in Logic Mode (M = H)
- Available in 300mil-wide 24-pin Slim DIP package

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F881	7.3ns	43mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C
24-Pin Plastic Slim DIP (300mil)	N74F881N
24-Pin Plastic SOL	N74F881D

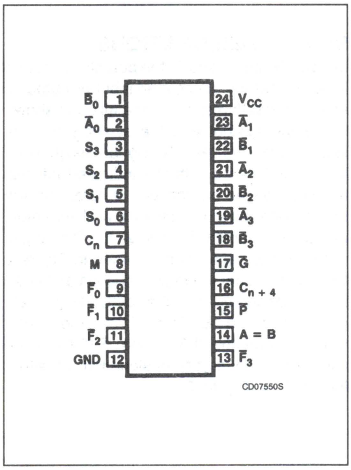
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
M	Mode control input	1.0/1.0	20μA/0.6mA
$\overline{A}_0 - \overline{A}_3$, $\overline{B}_0 - \overline{B}_3$	Operand inputs	3.0/3.0	60μA/1.8mA
$S_0 - S_3$	Function select inputs	4.0/4.0	80μA/2.4mA
C_n	Carry input	6.0/6.0	120μA/3.6mA
C_{n+4}	Carry output	50/33	1.0mA/20mA
A = B	Compare output	OC*/33	OC*/20mA
$\overline{F}_0 - \overline{F}_3$	Outputs	50/33	1.0mA/20mA
$\overline{G}$	Carry generate output	50/33	1.0mA/20mA
$\overline{P}$	Carry propagate output	50/33	1.0mA/20mA

NOTES:

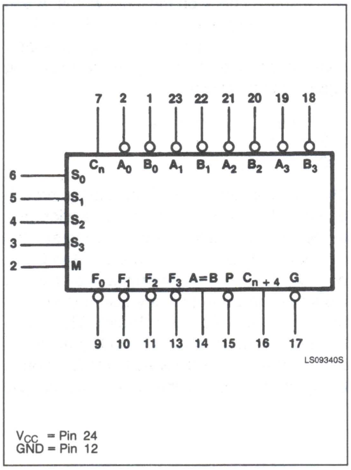
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.
2. OC* = Open-Collector

PIN CONFIGURATION



$\overline{B}_0$ 1
$\overline{A}_0$ 2
S_3 3
S_2 4
S_1 5
S_0 6
C_n 7
M 8
$\overline{F}_0$ 9
$\overline{F}_1$ 10
$\overline{F}_2$ 11
GND 12
24 V_{CC}
23 $\overline{A}_1$
22 $\overline{B}_1$
21 $\overline{A}_2$
20 $\overline{B}_2$
19 $\overline{A}_3$
18 $\overline{B}_3$
17 $\overline{G}$
16 C_{n+4}
15 $\overline{P}$
14 A = B
13 $\overline{F}_3$
CD07550S

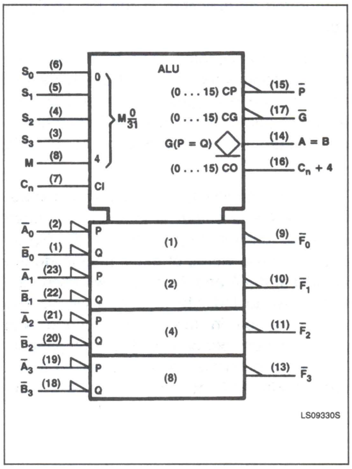
LOGIC SYMBOL



7 2 1 23 22 21 20 19 18
C_n A_0 B_0 A_1 B_1 A_2 B_2 A_3 B_3
6 S_0
5 S_1
4 S_2
3 S_3
2 M
F_0 F_1 F_2 F_3 A=B P C_{n+4} G
9 10 11 13 14 15 16 17
LS09340S

V_{CC} = Pin 24
GND = Pin 12

LOGIC SYMBOL (IEEE/IEC)



ALU
S_0 (6)
S_1 (5)
S_2 (4)
S_3 (3)
M (8)
C_n (7)
0
4
$M\frac{0}{31}$
CI
(0 . . . 15) CP
(0 . . . 15) CG
G(P = Q)
(0 . . . 15) CO
(15) $\overline{P}$
(17) $\overline{G}$
(14) A = B
(16) $C_n + 4$
$\overline{A}_0$ (2) P
$\overline{B}_0$ (1) Q
(1)
(9) $\overline{F}_0$
$\overline{A}_1$ (23) P
$\overline{B}_1$ (22) Q
(2)
(10) $\overline{F}_1$
$\overline{A}_2$ (21) P
$\overline{B}_2$ (20) Q
(4)
(11) $\overline{F}_2$
$\overline{A}_3$ (19) P
$\overline{B}_3$ (18) Q
(8)
(13) $\overline{F}_3$
LS09330S

Arithmetic Logic Unit/Function Generator

FAST 74F881

PIN DESIGNATION TABLE

PIN NUMBER	2	1	23	22	21	20	19	18	9	10	11	13	7	16	15	17
I (active-Low data)	$\overline{A}_0$	$\overline{B}_0$	$\overline{A}_1$	$\overline{B}_1$	$\overline{A}_2$	$\overline{B}_2$	$\overline{A}_3$	$\overline{B}_3$	$\overline{F}_0$	$\overline{F}_1$	$\overline{F}_2$	$\overline{F}_3$	C_n	C_{n+4}	$\overline{P}$	$\overline{G}$
II (active-High data)	A_0	B_0	A_1	B_1	A_2	B_2	A_3	B_3	F_0	F_1	F_2	F_3	$\overline{C}_n$	$\overline{C}_{n+4}$	X	Y

DESCRIPTION

The 'F881 is an arithmetic logic unit (ALU)/function generator that has a complexity of 77 equivalent gates on a monolithic chip. This circuit performs 16 binary arithmetic operations on two 4-bit words as shown in Tables 1 and 2. These operations are selected by the four function-select lines (S_0, S_1, S_2, S_3) and include addition, subtraction, decrement, and straight transfer. When performing arithmetic manipulations, the internal carries must be enabled by applying a Low-level voltage to the mode control input (M). A full carry look-ahead scheme is made available in these devices for fast, simultaneous carry generation by means oftwo cascade-ouputs (pins 15 and 17) for the four bits in the package. When used in conjunction with the 'F882 full carry look-ahead circuit, High-speed arithmetic operations can be performed.

The method of cascading 'F882 circuits with these ALUs to provide multi-level full carry look-ahead is illustrated under signal designations.

If High-speed is not of importance, a ripple-carry input (C_n) and a ripple-carry output (C_{n+4}) are available. However, the ripple-carry delay has also been minimized so that arithmetic manipulations for small word lengths can be performed without external circuitry.

The 'F881 will accommodate active-High or active-Low data if the pin designations are interpreted as indicated in the Pin Designation Table.

Subtraction is accomplished by 1's Complement addition where the 1's Complement of the subtrahend is generated internally. The resultant output is $A-B-1$, which requires an end-around or forced carry to provide $A-B$.

The 'F881 can also be utilized as a comparator. The A = B output is internally decoded from the function outputs (F_0, F_1, F_2, F_3) so that when two words of equal magnitude are applied at the A and B inputs, it will assume a High level to indicate equality (A = B). The ALU must be in the subtract mode with $C_n = H$ when performing this comparison. The A = B output is open-collector so that it can be wire-AND connected to give a comparison for more than four bits. The carry output (C_{n+4}) can also be used to supply relative magnitude information. Again, the ALU must be placed in the subtract mode by placing the function select inputs S_3, S_2, S_1, S_0 at L, H, H, L, respectively.

COMPARATOR TABLE

INPUT C_n	OUTPUT C_{n+4}	ACTIVE-LOW DATA	ACTIVE-HIGH DATA
H	H	$A \geqslant B$	$A \leqslant B$
H	L	$A < B$	$A > B$
L	H	$A > B$	$A < B$
L	L	$A \leqslant B$	$A \geqslant B$

This circuit has been designed to not only incorporate all of the designer's requirements for arithmetic operations, but also to provide 16 possible functions of two Boolean variables without the use of external circuitry. These logic functions are selected by use of the four function-select inputs (S_0, S_1, S_2, S_3) with the mode-control input (M) at a High level to disable the internal carry. The 16 logic functions are detailed in the Logic Function Table and include Exclusive-OR, NAND, AND, NOR, and OR functions.

The 'F881 has the same pinout and same functionality as the 'F181 except for the $\overline{P}$, $\overline{G}$, and C_{n+4} outputs when the device is in the logic mode (M = H).

In the logic mode the 'F881 provides the user with a status check on the input words, A and B, and the output word F. While in the logic mode the $\overline{P}$, $\overline{G}$ and C_{n+4} outputs supply status information based upon the folLowing logical combinations:

$$\overline{P} = F_0 + F_1 + F_2 + F_3$$
$$\overline{G} = H$$
$$C_{n+4} = PC_n$$

The combination of signals on the S_3 through S_0 control lines determine the operation performed on the data words to generate the output bits F_i. By monitoring the $\overline{P}$ and C_{n+4} outputs, the user can determine if all pairs of input bits are equal or if any pair of inputs are both High (see Function Table). The 'F881 has the unique feature of providing an A = B status while the exclusive-OR (⊕) function is being utilized. When the control inputs (S_3, S_2, S_1, S_0) equal H, L, L, H; a status check is generated to determine whether all pairs (A_i, B_i) are equal in the folLowing manner: $\overline{P} = (A_0 \oplus B_0) + (A_1 \oplus B_1) + (A_2 \oplus B_2) + (A_3 \oplus B_3)$. This unique bit-by-bit comparison of the data words which is available on the totem pole $\overline{P}$ output is particularly useful when cascading 'F881's. As the A = B condition is sensed in the first stage the signal is propagated through the same ports used for carry generation in the arithmetic mode ($\overline{P}$ and $\overline{G}$). Thus the A = B status is transmitted to the second stage more quickly without the need for external multiplexing logic. The A = B open-collector output alLows the user to check the validity of the bit-by-bit result by comparing the two signals for parity.

If the user wishes to check for any pair of data inputs ($\overline{A}_i$, $\overline{B}_i$) being High, it is necessary to set the control lines (S_3, S_2, S_1, S_0) to L, H, L, L. The data pairs will then be ANDed together and the results ORed in the folLowing manner: $\overline{P} = \overline{A}_0\overline{B}_0 + \overline{A}_1\overline{B}_1 + \overline{A}_2\overline{B}_2 + \overline{A}_3\overline{B}_3$.

SIGNAL DESIGNATIONS

In both Figures 1 and 2, the polarity indicators indicate that the associated input or output is active-Low with respect to the function shown inside the symbol and the symbols are the same in both figures. The signal designations in Figure 1 agree with the indicated internal functions based on active-Low data, and are for use with the logic functions and arithmetic operations shown in Table 1. The signal designations have been changed in Figure 2 to accommodate the logic functions and arithmetic operations for the active-High data given in Table 2. The 'F181 and 'F881 together with the 'F882 and 'F182 can be used with the signal designation of either Figure 1 or Figure 2.

FUNCTION TABLE FOR INPUT BITS EQUAL/NOT EQUAL

$S_0 = S_3 = H$, $S_1 = S_2 = L$, and $M = H$

C_n	DATA INPUTS				OUTPUTS		
					$\overline{G}$	$\overline{P}$	C_{n+4}
H	$A_0 = B_0$	$A_1 = B_1$	$A_2 = B_2$	$A_3 = B_3$	H	L	H
L	$A_0 = B_0$	$A_1 = B_1$	$A_2 = B_2$	$A_3 = B_3$	H	L	L
X	$A_0 \neq B_0$	X	X	X	H	H	L
X	X	$A_1 \neq B_1$	X	X	H	H	L
X	X	X	$A_2 \neq B_2$	X	H	H	L
X	X	X	X	$A_3 \neq B_3$	H	H	L

FUNCTION TABLE FOR INPUT PAIRS HIGH/NOT HIGH

$S_0 = S_1 = S_3 = L$, $S_2 = H$, and $M = H$

C_n	DATA INPUTS				OUTPUTS		
					$\overline{G}$	$\overline{P}$	C_{n+4}
H	$\overline{A}_0$ or $\overline{B}_0 = L$	$\overline{A}_1$ or $\overline{B}_1 = L$	$\overline{A}_2$ or $\overline{B}_2 = L$	$\overline{A}_3$ or $\overline{B}_3 = L$	H	L	
L	$\overline{A}_0$ or $\overline{B}_0 = L$	$\overline{A}_1$ or $\overline{B}_1 = L$	$\overline{A}_2$ or $\overline{B}_2 = L$	$\overline{A}_3$ or $\overline{B}_3 = L$	H	L	
X	$\overline{A}_0 = \overline{B}_0 = H$	X	X	X	H	H	L
X	X	$\overline{A}_1 = \overline{B}_1 = H$	X	X	H	H	L
X	X	X	$\overline{A}_2 = \overline{B}_2 = H$	X	H	H	L
X	X	X	X	$\overline{A}_3 = \overline{B}_3 = H$	H	H	L

SELECT TABLE FOR DATA INPUT PAIRS

S_3	S_2	S_1	S_0	M	$\overline{P} = F_0 + F_1 + F_2 + F_3$
L	H	L	L	H	$\overline{A}_0\overline{B}_0 + \overline{A}_1\overline{B}_1 + \overline{A}_2\overline{B}_2 + \overline{A}_3\overline{B}_3$
H	L	L	H	H	$(A_0 \oplus B_0) + (A_1 \oplus B_1) + (A_2 \oplus B_2) + (A_3 \oplus B_3)$

Arithmetic Logic Unit/Function Generator FAST 74F881

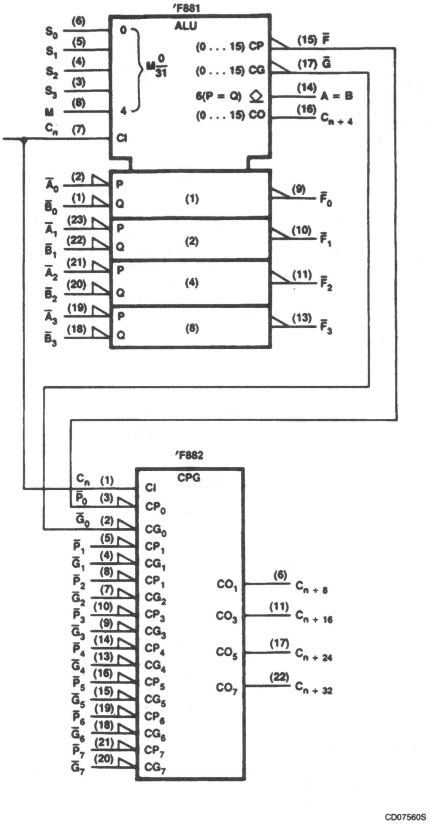

'F881
ALU
S0 (6)
S1 (5)
S2 (4)
S3 (3)
M (8)
Cn (7)
M 0/31
CI
(0 . . . 15) CP
(0 . . . 15) CG
&(P = Q)
(0 . . . 15) CO
(15) P̄
(17) Ḡ
(14) A = B
(16) Cn + 4
Ā0 (2)
B̄0 (1)
Ā1 (23)
B̄1 (22)
Ā2 (21)
B̄2 (20)
Ā3 (19)
B̄3 (18)
P
Q
(1)
(2)
(4)
(8)
(9) F̄0
(10) F̄1
(11) F̄2
(13) F̄3
'F882
CPG
Cn (1)
P̄0 (3)
Ḡ0 (2)
P̄1 (5)
Ḡ1 (4)
P̄2 (8)
Ḡ2 (7)
P̄3 (10)
Ḡ3 (9)
P̄4 (14)
Ḡ4 (13)
P̄5 (16)
Ḡ5 (15)
P̄6 (19)
Ḡ6 (18)
P̄7 (21)
Ḡ7 (20)
CI
CP0
CG0
CP1
CG1
CP1
CG2
CP3
CG3
CP4
CG4
CP5
CG5
CP6
CG6
CP7
CG7
CO1 (6) Cn + 8
CO3 (11) Cn + 16
CO5 (17) Cn + 24
CO7 (22) Cn + 32
CD07560S

Figure 1
(Use With Table 1)

Table 1

SELECTION				ACTIVE-LOW DATA		
					M = L; Arithmetic Operations	
S_3	S_2	S_1	S_0	M – H Logic Functions	C_n = L (no carry)	C_n = H (with carry)
L	L	L	L	F = $\overline{A}$	F = A MINUS 1	F = A
L	L	L	H	F = $\overline{AB}$	F = AB MINUS 1	F = AB
L	L	H	L	F = $\overline{A}$ + B	F = A$\overline{B}$ MINUS 1	F = A$\overline{B}$
L	L	H	H	F = 1	F = MINUS 1 (2's COMP)	F = ZERO
L	H	L	L	F = $\overline{A + B}$	F = A PLUS (A + $\overline{B}$)	F = A PLUS (A + $\overline{B}$) PLUS 1
L	H	L	H	F = $\overline{B}$	F = AB PLUS (A + $\overline{B}$)	F = AB PLUS (A + $\overline{B}$) PLUS 1
L	H	H	L	F = $\overline{A \oplus B}$	F = A MINUS B MINUS 1	F = A MINUS B
L	H	H	H	F = A + $\overline{B}$	F = A + $\overline{B}$	F = (A + $\overline{B}$) PLUS 1
H	L	L	L	F = $\overline{A}$B	F = A PLUS (A + B)	F = A PLUS (A + B) PLUS 1
H	L	L	H	F = A ⊕ B	F = A PLUS B	F = A PLUS B PLUS 1
H	L	H	L	F = B	F = A$\overline{B}$ PLUS (A + B)	F = A$\overline{B}$ PLUS (A + B) PLUS 1
H	L	H	H	F = A + B	F = (A + B)	F = (A + B) PLUS 1
H	H	L	L	F = 0	F = A PLUS A*	F = A PLUS A PLUS 1
H	H	L	H	F = A$\overline{B}$	F = AB PLUS A	F = AB PLUS A PLUS 1
H	H	H	L	F = AB	F = A$\overline{B}$ PLUS A	F = A$\overline{B}$ PLUS A PLUS 1
H	H	H	H	F = A	F = A	F = A PLUS 1

*Each bit is shifted to the next more significant position.

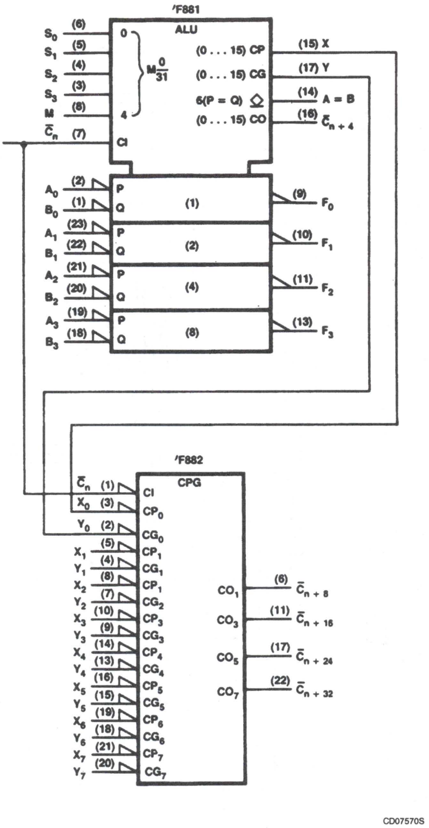

'F881
ALU
S_0 (6)
S_1 (5)
S_2 (4)
S_3 (3)
M (8)
$\overline{C}_n$ (7)
0
4
$M\frac{0}{31}$
CI
(0 . . . 15) CP
(0 . . . 15) CG
6(P = Q)
(0 . . . 15) CO
(15) X
(17) Y
(14) A = B
(16) $\overline{C}_{n+4}$
A_0 (2) P
B_0 (1) Q
(1)
A_1 (23) P
B_1 (22) Q
(2)
A_2 (21) P
B_2 (20) Q
(4)
A_3 (19) P
B_3 (18) Q
(8)
(9) F_0
(10) F_1
(11) F_2
(13) F_3
'F882
CPG
$\overline{C}_n$ (1) CI
X_0 (3) CP_0
Y_0 (2) CG_0
X_1 (5) CP_1
Y_1 (4) CG_1
X_2 (8) CP_1
Y_2 (7) CG_2
X_3 (10) CP_3
Y_3 (9) CG_3
X_4 (14) CP_4
Y_4 (13) CG_4
X_5 (16) CP_5
Y_5 (15) CG_5
X_6 (19) CP_6
Y_6 (18) CG_6
X_7 (21) CP_7
Y_7 (20) CG_7
CO_1 (6) $\overline{C}_{n+8}$
CO_3 (11) $\overline{C}_{n+16}$
CO_5 (17) $\overline{C}_{n+24}$
CO_7 (22) $\overline{C}_{n+32}$
CD07570S

Figure 2
(Use with Table 2)

Table 2

SELECTION				ACTIVE-LOW DATA		
				M – H Logic Functions	M = L; Arithmetic Operations	
S_3	S_2	S_1	S_0		$\overline{C}_n$ = H (no carry)	$\overline{C}_n$ = L (with carry)
L	L	L	L	$F = \overline{A}$	F = A	F = A PLUS 1
L	L	L	H	$F = \overline{A + B}$	F = A + B	F = (A + B) PLUS 1
L	L	H	L	$F = \overline{A}B$	$F = A + \overline{B}$	$F = (A + \overline{B})$ PLUS 1
L	L	H	H	F = 0	F = MINUS 1 (2's COMPL)	F = ZERO
L	H	L	L	$F = \overline{AB}$	F = A PLUS $A\overline{B}$	F = A PLUS $A\overline{B}$ PLUS 1
L	H	L	H	$F = \overline{B}$	F = (A + B) PLUS $A\overline{B}$	F = (A + B) PLUS $A\overline{B}$ PLUS 1
L	H	H	L	$F = A \oplus B$	F = A MINUS B MINUS 1	F = A MINUS B
L	H	H	H	$F = A\overline{B}$	$F = A\overline{B}$ MINUS 1	$F = A\overline{B}$
H	L	L	L	$F = \overline{A} + B$	F = A PLUS AB	F = A PLUS AB PLUS 1
H	L	L	H	$F = \overline{A \oplus B}$	F = A PLUS B	F = A PLUS B PLUS 1
H	L	H	L	F = B	$F = (A + \overline{B})$ PLUS AB	$F = (A + \overline{B})$ PLUS AB PLUS 1
H	L	H	H	F = AB	F = AB MINUS 1	F = AB
H	H	L	L	F = 1	F = A PLUS A*	F = A PLUS A PLUS 1
H	H	L	H	$F = A + \overline{B}$	F = (A + B) PLUS A	F = (A + B) PLUS A PLUS 1
H	H	H	L	F = A + B	$F = (A + \overline{B})$ PLUS A	$F = (A + \overline{B})$ PLUS A PLUS 1
H	H	H	H	F = A	F = A MINUS 1	F = A

*Each bit is shifted to the next more significant position.

LOGIC DIAGRAM (POSITIVE LOGIC)

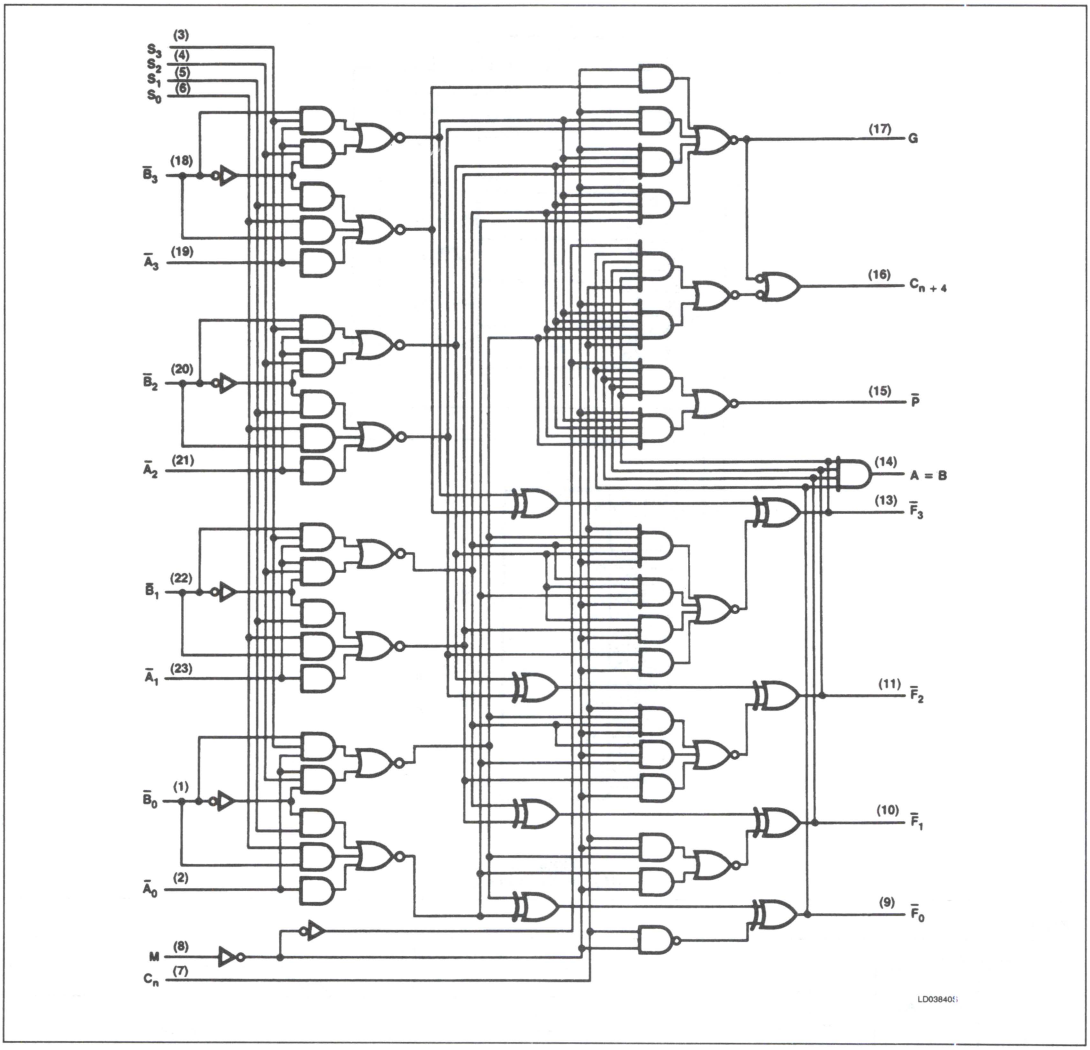

S_3 (3)
S_2 (4)
S_1 (5)
S_0 (6)
$\bar{B}_3$ (18)
$\bar{A}_3$ (19)
$\bar{B}_2$ (20)
$\bar{A}_2$ (21)
$\bar{B}_1$ (22)
$\bar{A}_1$ (23)
$\bar{B}_0$ (1)
$\bar{A}_0$ (2)
M (8)
C_n (7)
(17) G
(16) C_{n+4}
(15) $\bar{P}$
(14) A = B
(13) $\bar{F}_3$
(11) $\bar{F}_2$
(10) $\bar{F}_1$
(9) $\bar{F}_0$
LD03840

Table 3. SUM MODE TEST TABLE

Function Inputs: $S_0 = S_3 = 4.5V$, $S_1 = S_2 = M = 0V$

PARAMETER	INPUT UNDER TEST	OTHER INPUT, SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST
		Apply 4.5V	Apply GND	Apply 4.5V	Apply GND	
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{B}_i$	None	$\overline{A}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}
t_{PLH} t_{PHL}	$\overline{B}_i$	None	$\overline{A}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}
t_{PLH} t_{PHL}	C_n	None	None	All $\overline{A}$	All $\overline{B}$	Any $\overline{F}$ or C_{n+4}

Table 4. DIFF MODE TEST TABLE

Function Inputs: $S_1 = S_2 = 4.5V$, $S_0 = S_3 = M = 0V$

PARAMETER	INPUT UNDER TEST	OTHER INPUT, SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST
		Apply 4.5V	Apply GND	Apply 4.5V	Apply GND	
t_{PLH} t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{B}_i$	None	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	C_{n+4}
t_{PLH} t_{PHL}	$\overline{B}_i$	None	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	C_{n+4}
t_{PLH} t_{PHL}	C_n	None	None	All $\overline{A}$ and $\overline{B}$	None	Any $\overline{F}$ or C_{n+4}

Table 5. LOGIC MODE TEST TABLE

PARAMETER	INPUT UNDER TEST	OTHER INPUT, SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	FUNCTION INPUTS
		Apply 4.5V	Apply GND	Apply 4.5V	Apply GND		
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{F}_i$	$S_1 = S_2 = M = 4.5V$ $S_0 = S_3 = 0V$
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{F}_i$	$S_1 = S_2 = M = 4.5V$ $S_0 = S_3 = 0V$

Table 6. INPUT BITS EQUAL/NOT EQUAL TEST TABLE

Function Inputs: $S_0 = S_3 = M = 4.5V$, $S_1 = S_2 = 0V$

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST
		Apply 4.5V	Apply GND	Apply 4.5V	Apply GND	
t_{PLH}	$\overline{A}_i$	$\overline{B}_i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	None	$\overline{P}$
t_{PHL}						
t_{PLH}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	None	$\overline{P}$
t_{PHL}						
t_{PLH}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{A}$ and $\overline{B}$, C_n	None	$\overline{P}$
t_{PHL}						
t_{PLH}	$\overline{B}_i$	None	$\overline{A}_i$	Remaining $\overline{A}$ and $\overline{B}$, C_n	None	$\overline{P}$
t_{PHL}						
t_{PLH}	$\overline{A}_i$	$\overline{B}_i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	None	C_{n+4}
t_{PHL}						
t_{PLH}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	None	C_{n+4}
t_{PHL}						
t_{PLH}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{A}$ and $\overline{B}$, C_n	None	C_{n+4}
t_{PHL}						
t_{PLH}	$\overline{B}_i$	None	$\overline{A}_i$	Remaining $\overline{A}$ and $\overline{B}$, C_n	None	C_{n+4}
t_{PHL}						

Table 7. INPUT PAIRS HIGH/NOT HIGH TEST TABLE

Function Inputs: $S_2 = M = 4.5V$, $S_0 = S_1 = S_3 = 0V$

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST
		Apply 4.5V	Apply GND	Apply 4.5V	Apply GND	
t_{PLH}	$\overline{A}_i$	$\overline{B}_i$	None	Remaining $\overline{A}$, C_n	Remaining $\overline{B}$	$\overline{P}$
t_{PHL}						
t_{PLH}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{B}$, C_n	Remaining $\overline{A}$	$\overline{P}$
t_{PHL}						
t_{PLH}	$\overline{A}_i$	$\overline{B}_i$	None	Remaining $\overline{A}$, C_n	Remaing $\overline{B}$	C_{n+4}
t_{PHL}						
t_{PLH}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{B}$, C_n	Remaining $\overline{A}$	C_{n+4}
t_{PHL}						

Arithmetic Logic Unit/Function Generator FAST 74F881

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		−0.5 to +7.0	V
V_{IN}	Input voltage		−0.5 to +7.0	V
I_{IN}	Input current		−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		−0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	Any output except $\overline{G}$	40	mA
		$\overline{G}$	96	mA
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature range		−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Typ	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
V_{OH}	High-level output voltage	A = B only			4.5	V
I_{OH}	High-level output current	except A = B			−1	mA
I_{OL}	Low-level output current				20	mA
T_A	Operating free-air temperature		0		70	°C

Arithmetic Logic Unit/Function Generator

FAST 74F881

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
I_{OH}	High-level output current	A = B only	V_{CC} = MAX, V_{IH} = MIN, V_{IL} = MAX, V_{OH} = 4.5V				250	μA
V_{OH}	High-level output voltage	Any output except A = B	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	$\pm 10\%V_{CC}$	2.5			V
				$\pm 5\%V_{CC}$	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = 20mA	$\pm 10\%V_{CC}$		0.35	0.50	V
				$\pm 5\%V_{CC}$		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	High-level input current	M	V_{CC} = MAX, V_I = 2.7V				20	μA
		A_n, B_n					60	μA
		S_n					80	μA
		C_n					120	μA
I_{IL}	Low-level input current	M	V_{CC} = MAX, V_I = 0.5V				−0.6	mA
		A_n, B_n					−1.8	mA
		S_n					−2.4	mA
		C_n					−3.6	mA
I_{OH}	High-level output current	A = B only	V_{CC} = MAX, V_{IH} = MIN, V_{IL} = MAX, V_{OH} = 4.5V				250	μA
I_{OS}	Short-circuit output current[3]	Any output except A = B	V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	$S_0 - S_3 = M = \overline{A}_0 - \overline{A}_3 = 4.5V$ $\overline{B}_0 - \overline{B}_3 = C_n = GND$		48	65	mA
		I_{CCL}		$S_0 - S_3 = M = 4.5V$ $\overline{B}_0 - \overline{B}_3 = C_n = \overline{A}_0 - \overline{A}_3 = GND$		48	65	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of High-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Arithmetic Logic Unit/Function Generator FAST 74F881

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS				LIMITS					UNIT
						$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
		Mode	T^1	W^2	Conditions	Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay C_n to C_{n+4}					2.0 2.0	5.0 6.5	7.5 8.5	2.0 2.0	9.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ or $\overline{B}_n$ to C_{n+4}	Sum	III	1	$M = S_1 = S_2 = 0V$, $S_0 = S_3 = 4.5V$	5.5 5.5	10.0 8.5	13.0 13.0	5.0 5.0	14.0 14.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ or B_n to C_{n+4}	Diff	IV	4	$M = S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$	5.5 5.5	10.5 9.0	14.0 13.0	5.0 5.0	15.0 14.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ or $\overline{B}_n$ to C_{n+4} (status check)	Equality $\overline{A}_i = \overline{B}_i$ or $\overline{A}_i \neq \overline{B}_i$	VI	1	$M = C_n = 4.5V$, $S_0 = S_3 = 4.5V$ $S_1 = S_2 = 0V$	5.0 5.0	9.0 10.0	13.0 13.0	4.5 4.5	14.0 14.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ or $\overline{B}_n$ to C_{n+4} (status check)	$\overline{A}_i = \overline{B}_i = H$ or $\overline{A}_i = \overline{B}_i = L$		1	$M = C_n = 4.5V$ $S_2 = 4.5V$ $S_0 = S_1 = S_3 = 0V$	5.0 5.0	9.0 10.5	13.0 14.0	4.5 4.5	14.0 15.0	ns
t_{PLH} t_{PHL}	Propagation delay C_n to $\overline{F}_n$		IV	2		3.0 3.0	5.5 5.5	8.0 8.5	2.5 2.5	9.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ or $\overline{B}_n$ to $\overline{G}$	Sum	III	2	$M = S_1 = S_2 = 0V$, $S_0 = S_3 = 4.5V$	3.0 3.0	5.0 5.0	8.0 8.5	2.5 2.5	9.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ or $\overline{B}_n$ to $\overline{G}$	Diff	IV	3	$M = S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$	3.0 3.0	5.0 5.5	8.5 9.0	2.5 2.5	9.5 9.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ or $\overline{B}_n$ to $\overline{P}_n$	Sum	III	2	$M = S_1 = S_2 = 0V$, $S_0 = S_3 = 4.5V$	2.0 2.0	4.5 5.0	7.5 8.0	2.0 2.0	8.5 8.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ or $\overline{B}_n$ to $\overline{P}_n$	Diff	IV	3	$M = S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$	2.5 2.5	5.0 5.5	8.5 8.5	2.0 2.0	9.5 9.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ or $\overline{B}_n$ to P_n (status check)	Equality $\overline{A}_i = \overline{B}_i$ or $\overline{A}_i \neq \overline{B}_i$	VI	3	$M = C_n = 0V$, $S_2 = S_3 = 4.5V$	6.0 4.0	9.5 7.0	13.0 11.0	6.0 4.0	14.5 12.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ or $\overline{B}_n$ to $\overline{P}_n$ (status check)	$\overline{A}_i = \overline{B}_i = H$ or $\overline{A}_i = \overline{B}_i = L$	VII	3	$M = C_n = 4.5V$ $S_2 = 4.5V$ $S_0 = S_1 = S_3 = 0V$	6.0 4.0	10.0 7.5	13.0 11.0	6.0 4.0	14.5 12.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_i$ or $\overline{B}_i$ to $\overline{F}_i$	Sum	III	2	$M = S_1 = S_2 = 0V$, $S_0 = S_3 = 4.5V$	2.0 3.0	4.5 5.5	7.5 8.5	2.0 3.0	8.5 9.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_i$ or $\overline{B}_i$ to $\overline{F}_i$	Diff	IV	3	$M = S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$	2.5 3.5	5.0 6.0	8.0 9.0	2.0 3.0	8.5 9.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_i$ or $\overline{B}_i$ to $\overline{F}_i$	Logic	V	3	$M = 4.5V$	3.5 3.0	6.0 5.5	9.0 9.0	3.0 2.5	10.5 9.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ or $\overline{B}_n$ to $A = B$	Diff	IV	3	$M = S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$	8.0 6.0	14.5 9.0	20.0 12.5	8.0 6.0	22.0 14.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ or $\overline{B}_n$ to $\overline{F}_n$	Sum		1 + 2		3.5 3.5	6.5 7.0	10.0 10.5	3.0 3.5	11.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ or $\overline{B}_n$ to $\overline{F}_n$	Diff		1 + 2		3.5 3.5	7.0 7.5	10.5 11.0	3.0 3.5	11.5 11.5	ns

AC ELECTRICAL CHARACTERISTICS (Continued)

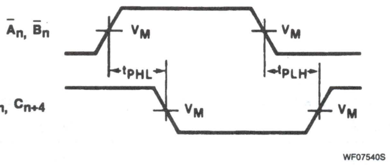
SYMBOL	PARAMETER	TEST CONDITIONS				LIMITS					UNIT
						$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
		Mode	T[1]	W[2]	Conditions	Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{F}_n$			1 + 2		2.5 3.0	6.0 6.5	10.0 10.5	2.0 3.0	11.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay S_n to A = B			1 + 2		12.0 5.5	16.5 9.0	22.0 13.0	11.0 5.0	24.0 14.0	ns
t_{PLH} t_{PHL}	Propagation delay S_n to C_{n+4}			1		4.0 4.0	10.0 7.5	12.5 10.0	4.0 4.0	14.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{G}$			2		3.0 3.0	5.0 5.0	8.0 8.0	2.5 2.5	9.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{P}$			2		2.5 3.5	7.5 7.0	13.0 11.0	2.0 3.5	14.0 12.0	ns
t_{PLH} t_{PHL}	Propagation delay M to $\overline{F}_n$	Sum		1 + 2		3.0 3.0	7.0 6.5	9.5 9.5	3.0 3.0	10.5 10.5	ns
t_{PLH} t_{PHL}	Propagation delay M to $\overline{F}_n$	Diff		1 + 2		3.0 3.0	6.5 6.0	9.5 9.5	3.0 3.0	10.5 10.5	ns
t_{PLH} t_{PHL}	Propagation delay M to A = B	Sum		1 + 2		13.0 5.5	16.5 9.5	22.0 12.0	12.0 5.0	24.0 13.5	ns
t_{PLH} t_{PHL}	Propagation delay M to A = B	Diff		1 + 2		13.5 5.5	16.5 9.5	22.0 12.0	12.0 5.0	24.0 13.5	ns

NOTES:

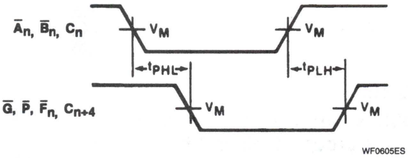
T = Table

W = Waveform

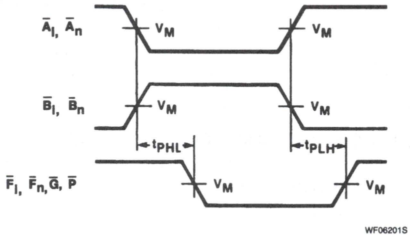
AC WAVEFORMS


$\overline{A}_n$, $\overline{B}_n$
V_M
V_M
t_{PHL}
t_{PLH}
$\overline{F}_n$, C_{n+4}
V_M
V_M
WF07540S

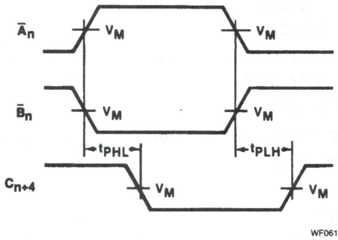
Waveform 1. Propagation Delay for Operands to Carry Output and Outputs


$\overline{A}_n$, $\overline{B}_n$, C_n
V_M
V_M
t_{PHL}
t_{PLH}
$\overline{G}$, $\overline{P}$, $\overline{F}_n$, C_{n+4}
V_M
V_M
WF0605ES

Waveform 2. Propagation Delays for Carry Input to Carry Output, Carry Input to Outputs, and Operands to Carry Generate and Carry Propagate Outputs


$\overline{A}_I$, $\overline{A}_n$
V_M
V_M
$\overline{B}_I$, $\overline{B}_n$
V_M
V_M
t_{PHL}
t_{PLH}
$\overline{F}_I$, $\overline{F}_n$, $\overline{G}$, $\overline{P}$
V_M
V_M
WF06201S

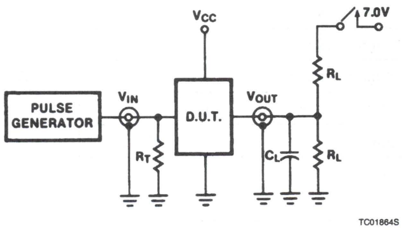
Waveform 3. Propagation Delay for Operands to Carry Generate and Propagate Outputs, Operands to A = B Output, and Outputs


$\overline{A}_n$
V_M
V_M
$\overline{B}_n$
V_M
V_M
t_{PHL}
t_{PLH}
C_{n+4}
V_M
V_M
WF06181S

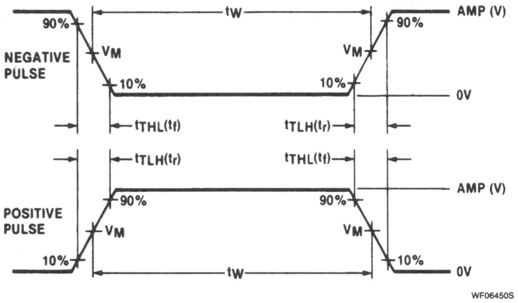
Waveform 4. Propagation Delays for Operands Carry Output

NOTE: For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORMS


V_{CC}
7.0V
PULSE GENERATOR
V_{IN}
D.U.T.
V_{OUT}
R_L
R_T
C_L
R_L
TC01864S

Test Circuit for Totem-Pole and Open-Collector Outputs


NEGATIVE PULSE
90%
V_M
10%
t_W
90%
V_M
10%
AMP (V)
0V
$t_{THL}(t_f)$
$t_{TLH}(t_r)$
$t_{TLH}(t_r)$
$t_{THL}(t_f)$
POSITIVE PULSE
90%
V_M
10%
90%
V_M
10%
AMP (V)
0V
t_W
WF06450S

$V_M = 1.5V$

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
Open-Collector	closed
Totem-Pole	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F882
Look-Ahead Carry Generator

32-bit Look-Ahead Carry Generator
Product Specification

FAST Products

FEATURES

- **Capable of anticipating the carry across a group of eight 4-bit binary adders**
- **Cascadable to perform look-ahead across n-bit adders**
- **Available in 300mil wide 24 pin Slim DIP package**
- **Typical Carry Time, C_n to any C_{n+1} is less than 6_{ns}**
- **Replaces AS 882**
- **Available in 300mil-wide 24-pin Slim DIP package**

DESCRIPTION

The 'F882 is a high-speed carry look-ahead generator capable of anticipating the carry across a group of eight 4-bit adders, thereby permitting the designer to implement look-ahead for a 32-bit ALU with a single package. In addition, full look-ahead is possible across n-bit adders cascading 'F882's.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F882	4.0ns	20mA

ORDERING INFORMATION

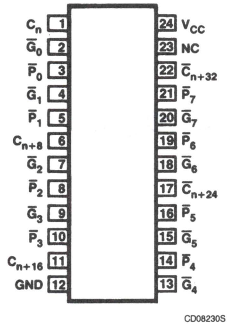
PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
24-Pin Plastic Slim DIP (300mil)	N74F882N
24-Pin Plastic SOL	N74F882D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

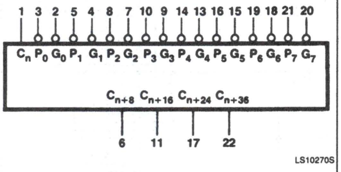
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
C_n	Carry input	5.0/1.0	100μA/0.6mA
$\overline{G}_0$, $\overline{G}_4$	Carry generate inputs	6.0/8.0	120μA/4.8mA
$\overline{G}_1$	Carry generate input	9.0/12.0	180μA/7.2mA
$\overline{G}_2$	Carry generate input	9.0/11.0	160μA/6.6mA
$\overline{G}_3$	Carry generate input	10.0/13.0	200μA/7.8mA
$\overline{G}_5$	Carry generate input	7.0/9.0	140μA/5.4mA
$\overline{G}_6$	Carry generate input	2.0/2.0	40μA/1.2mA
$\overline{G}_7$	Carry generate input	3.0/3.0	60μA/1.8mA
$\overline{P}_0$, $\overline{P}_1$	Carry propagate inputs	3.0/4.0	60μA/2.4mA
$\overline{P}_2$, $\overline{P}_3$	Carry propagate inputs	2.0/2.6	40μA/1.6mA
$\overline{P}_4$, $\overline{P}_5$, $\overline{P}_6$, $\overline{P}_7$	Carry propagate inputs	1.0/1.0	20μA/0.6mA
C_{n+8}	Carry output	50/33	1.0mA/20mA
C_{n+16}	Carry output	50/33	1.0mA/20mA
C_{n+24}	Carry output	50/33	1.0mA/20mA
C_{n+32}	Carry output	50/33	1.0mA/20mA

NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

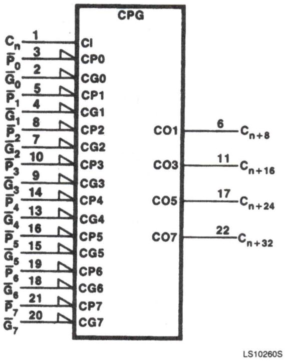
PIN CONFIGURATION


C_n 1
$\overline{G}_0$ 2
$\overline{P}_0$ 3
$\overline{G}_1$ 4
$\overline{P}_1$ 5
C_{n+8} 6
$\overline{G}_2$ 7
$\overline{P}_2$ 8
$\overline{G}_3$ 9
$\overline{P}_3$ 10
C_{n+16} 11
GND 12
24 V_{CC}
23 NC
22 $\overline{C}_{n+32}$
21 $\overline{P}_7$
20 $\overline{G}_7$
19 $\overline{P}_6$
18 $\overline{G}_6$
17 $\overline{C}_{n+24}$
16 $\overline{P}_5$
15 $\overline{G}_5$
14 $\overline{P}_4$
13 $\overline{G}_4$
CD08230S

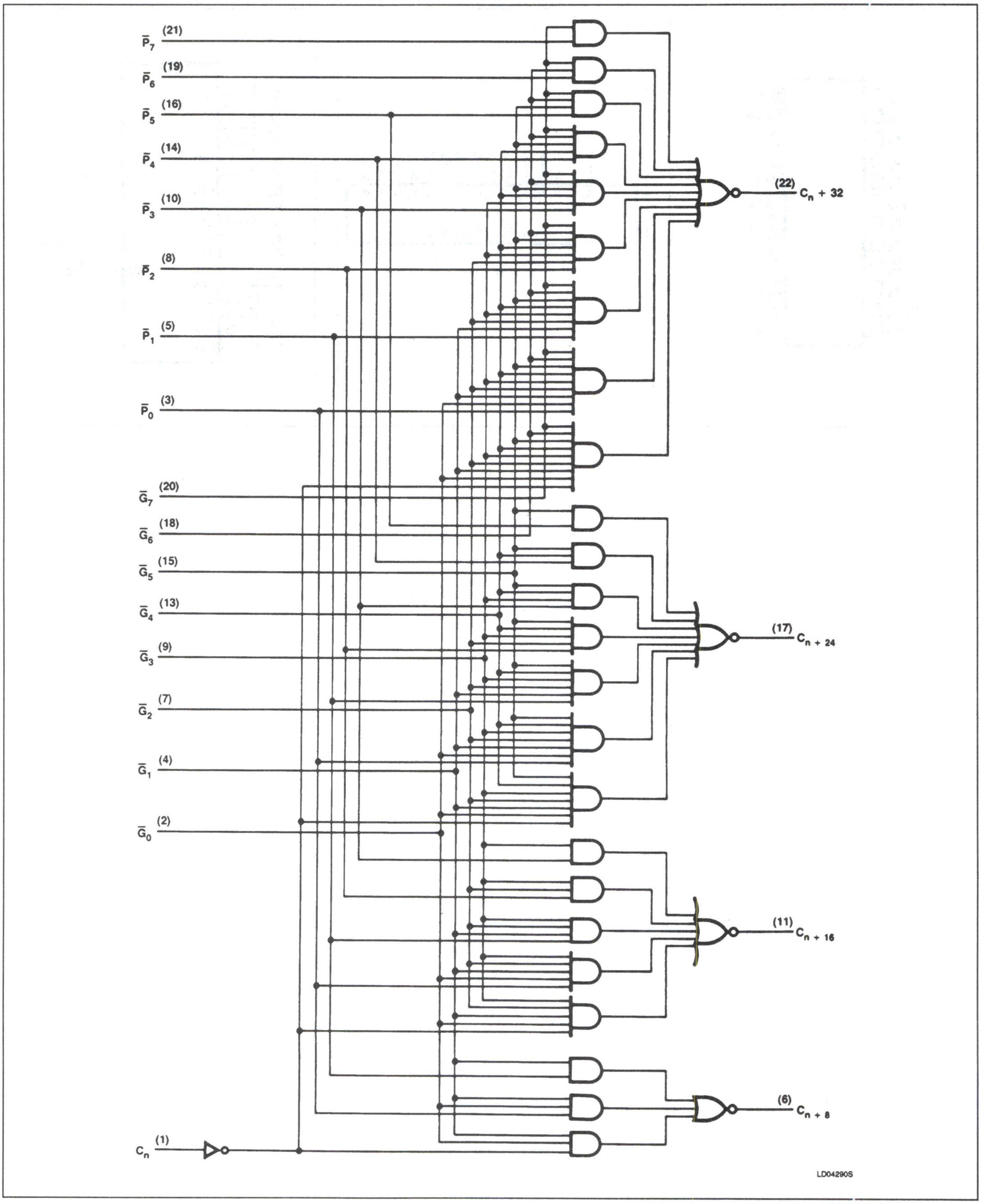
LOGIC SYMBOL


1 3 2 5 4 8 7 10 9 14 13 16 15 19 18 21 20
C_n P_0 G_0 P_1 G_1 P_2 G_2 P_3 G_3 P_4 G_4 P_5 G_5 P_6 G_6 P_7 G_7
C_{n+8} C_{n+16} C_{n+24} C_{n+36}
6 11 17 22
LS10270S

LOGIC SYMBOL (IEEE/IEC)


CPG
C_n 1 CI
$\overline{P}_0$ 3 CP0
$\overline{G}_0$ 2 CG0
$\overline{P}_1$ 5 CP1
$\overline{G}_1$ 4 CG1
$\overline{P}_2$ 8 CP2
$\overline{G}_2$ 7 CG2
$\overline{P}_3$ 10 CP3
$\overline{G}_3$ 9 CG3
$\overline{P}_4$ 14 CP4
$\overline{G}_4$ 13 CG4
$\overline{P}_5$ 16 CP5
$\overline{G}_5$ 15 CG5
$\overline{P}_6$ 19 CP6
$\overline{G}_6$ 18 CG6
$\overline{P}_7$ 21 CP7
$\overline{G}_7$ 20 CG7
CO1 6 C_{n+8}
CO3 11 C_{n+16}
CO5 17 C_{n+24}
CO7 22 C_{n+32}
LS10260S

LOGIC DIAGRAM


$\bar{P}_7$ (21)
$\bar{P}_6$ (19)
$\bar{P}_5$ (16)
$\bar{P}_4$ (14)
$\bar{P}_3$ (10)
$\bar{P}_2$ (8)
$\bar{P}_1$ (5)
$\bar{P}_0$ (3)
$\bar{G}_7$ (20)
$\bar{G}_6$ (18)
$\bar{G}_5$ (15)
$\bar{G}_4$ (13)
$\bar{G}_3$ (9)
$\bar{G}_2$ (7)
$\bar{G}_1$ (4)
$\bar{G}_0$ (2)
C_n (1)
(22) C_{n+32}
(17) C_{n+24}
(11) C_{n+16}
(6) C_{n+8}
LD04290S

FUNCTION TABLE FOR C_{n+32} OUTPUT

INPUTS																	OUTPUT
$\overline{G}_7$	$\overline{G}_6$	$\overline{G}_5$	$\overline{G}_4$	$\overline{G}_3$	$\overline{G}_2$	$\overline{G}_1$	$\overline{G}_0$	$\overline{P}_7$	$\overline{P}_6$	$\overline{P}_5$	$\overline{P}_4$	$\overline{P}_3$	$\overline{P}_2$	$\overline{P}_1$	$\overline{P}_0$	C_n	C_{n+32}
L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	H
X	L	X	X	X	X	X	X	L	X	X	X	X	X	X	X	X	H
X	X	L	X	X	X	X	X	L	L	X	X	X	X	X	X	X	H
X	X	X	L	X	X	X	X	L	L	L	X	X	X	X	X	X	H
X	X	X	X	L	X	X	X	L	L	L	L	X	X	X	X	X	H
X	X	X	X	X	L	X	X	L	L	L	L	L	X	X	X	X	H
X	X	X	X	X	X	L	X	L	L	L	L	L	L	X	X	X	H
X	X	X	X	X	X	X	L	L	L	L	L	L	L	L	X	X	H
X	X	X	X	X	X	X	X	L	L	L	L	L	L	L	L	H	H
All other combinations																	L

FUNCTION TABLE FOR C_{n+24} OUTPUT

INPUTS													OUTPUT
$\overline{G}_5$	$\overline{G}_4$	$\overline{G}_3$	$\overline{G}_2$	$\overline{G}_1$	$\overline{G}_0$	$\overline{P}_5$	$\overline{P}_4$	$\overline{P}_3$	$\overline{P}_2$	$\overline{P}_1$	$\overline{P}_0$	C_n	C_{n+24}
L	X	X	X	X	X	X	X	X	X	X	X	X	H
X	L	X	X	X	X	L	X	X	X	X	X	X	H
X	X	L	X	X	X	L	L	X	X	X	X	X	H
X	X	X	L	X	X	L	L	L	X	X	X	X	H
X	X	X	X	L	X	L	L	L	L	X	X	X	H
X	X	X	X	X	L	L	L	L	L	L	X	X	H
X	X	X	X	X	X	L	L	L	L	L	L	H	H
All other combinations													L

FUNCTION TABLE FOR C_{n+16} OUTPUT

INPUTS									OUTPUT
$\overline{G}_3$	$\overline{G}_2$	$\overline{G}_1$	$\overline{G}_0$	$\overline{P}_3$	$\overline{P}_2$	$\overline{P}_1$	$\overline{P}_0$	C_n	C_{n+16}
L	X	X	X	X	X	X	X	X	H
X	L	X	X	L	X	X	X	X	H
X	X	L	X	L	L	X	X	X	H
X	X	X	L	L	L	L	X	X	H
X	X	X	X	L	L	L	L	H	H
All other combinations									L

FUNCTION TABLE FOR C_{n+8} OUTPUT

INPUTS					OUTPUT
$\overline{G}_1$	$\overline{G}_0$	$\overline{P}_1$	$\overline{P}_0$	C_n	C_{n+8}
L	X	X	X	X	H
X	L	L	X	X	H
X	X	L	L	H	H
All other combinations					L

NOTE:
Any inputs not shown in a given table are irrelevant with respect to that output.

Look-Ahead Carry Generator FAST 74F882

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +1	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = MAX	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = MAX	±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$				-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V					100	μA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	Low-level input current	C_n, $\overline{P}_4$, $\overline{P}_5$, $\overline{P}_6$, $\overline{P}_7$	V_{CC} = MAX, V_I = 0.5V					-0.6	mA
		$\overline{G}_0$, $\overline{G}_4$						-4.2	mA
		$\overline{G}_1$, $\overline{G}_2$						-5.4	mA
		$\overline{G}_3$						-6.0	mA
		$\overline{G}_5$						-4.8	mA
		$\overline{G}_6$, $\overline{P}_2$, $\overline{P}_3$						-1.2	mA
		$\overline{G}_7$						-1.8	mA
		$\overline{P}_0$, $\overline{P}_1$						-2.4	mA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX			-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				35	50	mA
		I_{CCL}					45	65	mA

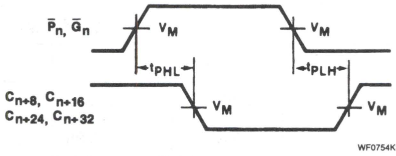
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value under the recommended operating conditions for the applicable conditions.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} should be performed last.

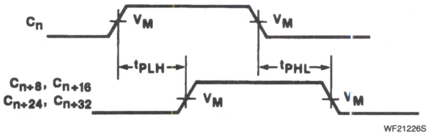
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F882					UNIT
			T_A = +25°C V_{CC} = +5.0V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = +5.0V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay C_n to Any output	Waveform 2	2.5 3.0	5.0 5.5	8.5 9.5	2.0 3.0	9.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{P}_n$ or $\overline{G}_n$ to C_{n+8}	Waveform 1	1.0 1.0	3.5 2.5	6.0 5.5	1.0 1.0	7.0 6.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{P}_n$ to $\overline{G}_n$ to C_{n+16}	Waveform 1	2.0 1.0	4.0 2.5	7.0 6.0	2.0 1.0	8.0 7.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{P}_n$ or $\overline{G}_n$ to C_{n+24}	Waveform 1	2.0 2.0	4.0 4.0	7.5 7.5	1.5 1.5	8.5 8.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{P}_n$ or $\overline{G}_n$ to C_{n+32}	Waveform 1	1.5 1.0	4.5 4.5	8.0 8.0	1.0 1.0	8.5 8.5	ns

AC WAVEFORMS


$\overline{P}_n$, $\overline{G}_n$
V_M
V_M
t_{PHL}
t_{PLH}
C_{n+8}, C_{n+16}
C_{n+24}, C_{n+32}
V_M
V_M
WF0754KS

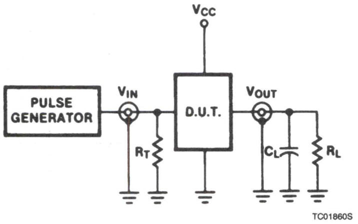
Waveform 1. Propagation Delay for Carry Propagate, Carry Generate Inputs to Carry Outputs


C_n
V_M
V_M
t_{PLH}
t_{PHL}
C_{n+8}, C_{n+16}
C_{n+24}, C_{n+32}
V_M
V_M
WF21226S

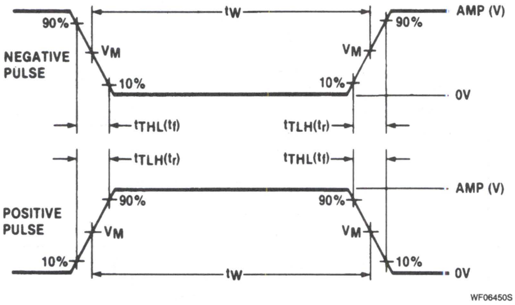
Waveform 2. Propagation Delay for Carry Input to Carry Outputs

NOTE: For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORMS


V_{CC}
PULSE GENERATOR
V_{IN}
D.U.T.
V_{OUT}
R_T
C_L
R_L
TC01860S

Test Circuit for Totem-Pole Outputs


NEGATIVE PULSE
90%
V_M
10%
t_W
90%
V_M
10%
AMP (V)
0V
$t_{THL}(t_f)$
$t_{TLH}(t_r)$
$t_{TLH}(t_r)$
$t_{THL}(t_f)$
POSITIVE PULSE
90%
V_M
10%
90%
V_M
10%
t_W
AMP (V)
0V
WF06450S

$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS

R_L = Load resistor to GND; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

FAST 74F1240, F1241
Buffers

'F1240 Octal Inverter Buffer (3-State)
'F1241 Octal Buffer (3-State)
Product Specification

FAST Products

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F1240	3.5ns	40mA
74F1241	4.5ns	46mA

FEATURES

- High-impedance NPN base inputs for reduced loading (20μA in High and Low states)
- Low-power, light-bus loading
- Functional pin for pin equivalent of 'F240 and 'F241
- 1/30th the bus loading of 'F240 or 'F241
- Provides ideal interface and increases fan-out of MOS Microprocessors
- Octal bus interface
- 3-State buffer outputs sink 64mA
- 15mA source current

DESCRIPTION

The 'F1240 and 'F1241 are octal buffers that are ideal for driving bus lines or buffer memory address registers. The outputs are capable of sinking 64mA and sourcing up to 15mA, producing very good capacitive drive characteristics. The device features two Output Enables, $\overline{OE}_n$, each controlling four of the 3-State outputs.

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
20-Pin Plastic DIP	N74F1240N, N74F1241N
20-Pin Plastic SOL	N74F1240D, N74F1241D

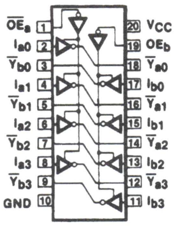
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$\overline{OE}_a$, $\overline{OE}_b$	3-State output enable input (active-Low)	1.0/0.033	20μA/20μA
OE_b	3-State output enable input (active-High)	1.0/0.033	20μA/20μA
$I_{a0} - I_{a3}$, $I_{b0} - I_{b3}$	Data inputs	1.0/0.033	20μA/20μA
$\overline{Y}_{a0} - \overline{Y}_{a3}$, $\overline{Y}_{b0} - \overline{Y}_{b3}$ 'F1240	Data outputs	750/106.7	15mA/64mA
$Y_{a0} - Y_{a3}$, $Y_{b0} - Y_{b3}$ 'F1241	Data outputs	750/106.7	15mA/64mA

NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION

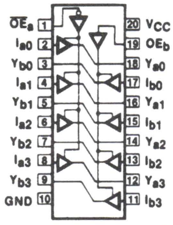
'F1240



$\overline{OE}_a$ 1
I_{a0} 2
$\overline{Y}_{b0}$ 3
I_{a1} 4
$\overline{Y}_{b1}$ 5
I_{a2} 6
$\overline{Y}_{b2}$ 7
I_{a3} 8
$\overline{Y}_{b3}$ 9
GND 10
20 V_{CC}
19 OE_b
18 $\overline{Y}_{a0}$
17 I_{b0}
16 $\overline{Y}_{a1}$
15 I_{b1}
14 $\overline{Y}_{a2}$
13 I_{b2}
12 $\overline{Y}_{a3}$
11 I_{b3}

CD04102S

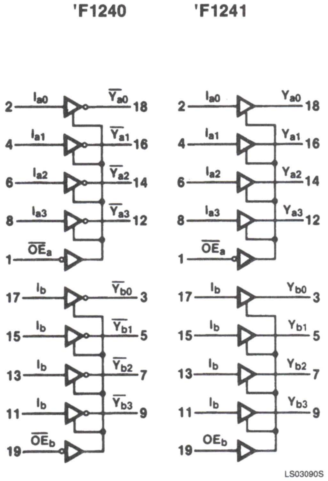
'F1241



$\overline{OE}_a$ 1
I_{a0} 2
Y_{b0} 3
I_{a1} 4
Y_{b1} 5
I_{a2} 6
Y_{b2} 7
I_{a3} 8
Y_{b3} 9
GND 10
20 V_{CC}
19 OE_b
18 Y_{a0}
17 I_{b0}
16 Y_{a1}
15 I_{b1}
14 Y_{a2}
13 I_{b2}
12 Y_{a3}
11 I_{b3}

CD04152S

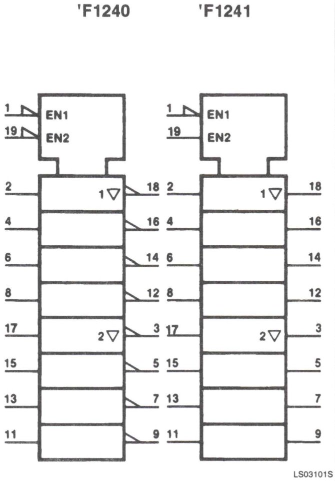
LOGIC SYMBOL



'F1240
'F1241
2 I_{a0} $\overline{Y}_{a0}$ 18
4 I_{a1} $\overline{Y}_{a1}$ 16
6 I_{a2} $\overline{Y}_{a2}$ 14
8 I_{a3} $\overline{Y}_{a3}$ 12
1 $\overline{OE}_a$
17 I_b $\overline{Y}_{b0}$ 3
15 I_b $\overline{Y}_{b1}$ 5
13 I_b $\overline{Y}_{b2}$ 7
11 I_b $\overline{Y}_{b3}$ 9
19 $\overline{OE}_b$
2 I_{a0} Y_{a0} 18
4 I_{a1} Y_{a1} 16
6 I_{a2} Y_{a2} 14
8 I_{a3} Y_{a3} 12
1 $\overline{OE}_a$
17 I_b Y_{b0} 3
15 I_b Y_{b1} 5
13 I_b Y_{b2} 7
11 I_b Y_{b3} 9
19 OE_b

LS03090S

LOGIC SYMBOL (IEEE/IEC)



'F1240
'F1241
1 EN1
19 EN2
2 1▽ 18
4 16
6 14
8 12
17 2▽ 3
15 5
13 7
11 9

LS03101S

FUNCTION TABLE for 'F1240

INPUTS				OUTPUTS	
$\overline{OE}_a$	I_a	$\overline{OE}_b$	I_b	$\overline{Y}_{an}$	$\overline{Y}_{bn}$
L	L	L	L	H	H
L	H	L	H	L	L
H	X	H	X	Z	Z

FUNCTION TABLE for 'F1241

INPUTS				OUTPUTS	
$\overline{OE}_a$	I_a	OE_b	I_b	Y_{an}	Y_{bn}
L	L	H	L	L	L
L	H	H	H	H	H
H	X	L	X	Z	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High-impedance (OFF) state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	128	mA
T_A	Operating free-air temperature range	0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−15	mA
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]			74F1240, 74F1241			UNIT
							Min	Typ[2]	Max	
V_{OH}	High-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = −3mA	± 10%V_{CC}	2.4			V
						± 5%V_{CC}	2.7	3.4		V
					I_{OH} = −15mA	± 10%V_{CC}	2.0			V
						± 5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 48mA	± 10%V_{CC}		0.35	0.50	V
					I_{OL} = 64mA	± 5%V_{CC}		0.40	0.55	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, I_I = I_{IK}				−0.73	−1.2	V
I_I	Input current at maximum input voltage			V_{CC} = 0.0V, V_I = 7.0V					100	μA
I_{IH}	High-level input current			V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	Low-level input current			V_{CC} = MAX, V_I = 0.5V					−20	μA
I_{OZH}	OFF-state output current High-level voltage applied			V_{CC} = MAX, V_O = 2.7V					50	mA
I_{OZL}	OFF-state output current Low-level voltage applied			V_{CC} = MAX, V_O = 0.5V					−50	mA
I_{OS}	Short-circuit output current[3]			V_{CC} = MAX			−100		−225	mA
I_{CC}	Supply current (total)	I_{CCH}	'F1240	V_{CC} = MAX				22	30	mA
		I_{CCL}						58	75	mA
		I_{CCZ}						44	58	mA
		I_{CCH}	'F1241					33	44	mA
		I_{CCL}						62	80	mA
		I_{CCZ}						45	60	mA

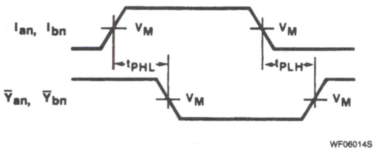
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

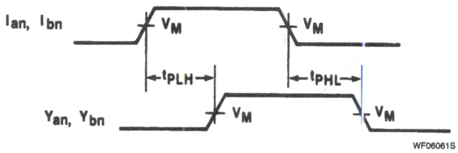
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	74F1240, 74F1241					UNIT
				$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0$ to $+70°C$ $V_{CC} = +5.0V$ $\pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay Data to output	'F1240	Waveform 1	3.0 1.5	4.5 2.5	6.5 4.5	2.5 1.5	7.5 5.0	ns
t_{PZH} t_{PZL}	Output enable time To High or Low		Waveform 3 Waveform 4	3.0 4.0	5.5 7.0	7.5 9.0	3.0 4.0	8.0 9.5	ns
t_{PHZ} t_{PLZ}	Output disable time From High or Low		Waveform 3 Waveform 4	2.0 2.0	4.0 4.0	6.0 5.5	2.0 2.0	6.5 6.0	ns
t_{PLH} t_{PHL}	Propagation delay Data to output	'F1241	Waveform 2	2.5 2.5	4.0 5.0	5.5 6.5	2.5 2.5	6.0 7.0	ns
t_{PZH} t_{PZL}	Output enable time To High or Low		Waveform 3 Waveform 4	3.0 3.0	5.5 6.5	7.0 8.0	3.0 3.0	7.5 8.5	ns
t_{PHZ} t_{PLZ}	Output disable time From High or Low		Waveform 3 Waveform 4	3.0 3.0	5.5 6.0	7.5 8.0	3.0 3.0	8.5 8.5	ns

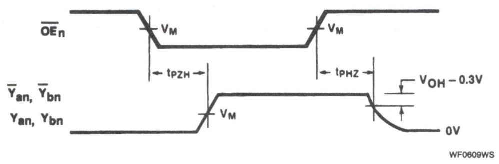
AC WAVEFORMS


Ian, Ibn
VM
VM
tPHL
tPLH
Ȳan, Ȳbn
VM
VM
WF06014S

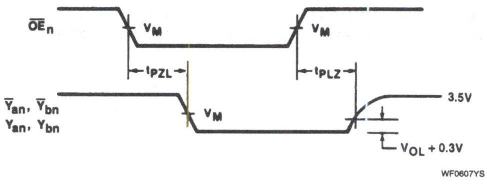
Waveform 1. Propagation Delay Data to Output for 'F1240


Ian, Ibn
VM
VM
tPLH
tPHL
Yan, Ybn
VM
VM
WF06061S

Waveform 2. Propagation Delay Data to Output for 'F1241


OEn
VM
VM
tPZH
tPHZ
VOH − 0.3V
Ȳan, Ȳbn
Yan, Ybn
VM
0V
WF0609WS

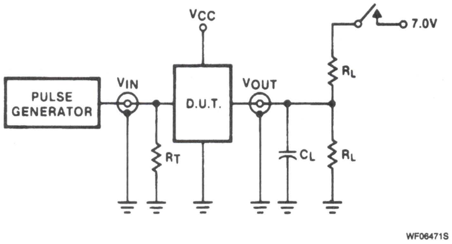
Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time From High Level


OEn
VM
VM
tPZL
tPLZ
3.5V
Ȳan, Ȳbn
Yan, Ybn
VM
VOL + 0.3V
WF0607YS

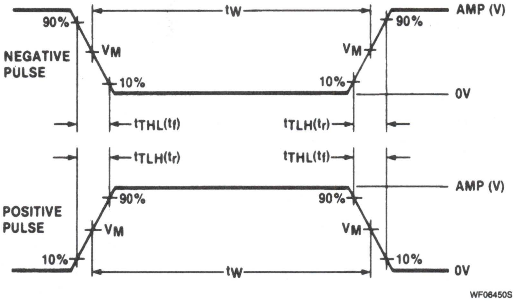
Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORMS


VCC
7.0V
RL
PULSE GENERATOR
VIN
D.U.T.
VOUT
RT
CL
RL
WF06471S

Test Circuit for 3-State Outputs


tw
90%
AMP (V)
NEGATIVE PULSE
VM
10%
0V
tTHL(tf)
tTLH(tr)
tTLH(tr)
tTHL(tf)
AMP (V)
POSITIVE PULSE
90%
VM
10%
0V
tw
WF06450S

$V_M = 1.5V$

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor to GND; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F1242, F1243
Transceivers

'F1242 Quad Inverting Transceiver (3-State)
'F1243 Quad Transceiver (3-State)
Product Specification

FAST Products

FEATURES

- High-impedance NPN base inputs for reduced loading (70µA in High and Low states)
- Low-power, light-bus loading
- Functional pin for pin equivalent of 'F242 and 'F243
- 1/30th the bus loading of 'F242 or 'F243
- Provides ideal interface and increases fan-out of MOS Microprocessors
- 3-State outputs sink 64mA and source 15mA

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F1242	3.5ns	43mA
74F1243	4.5ns	44mA

ORDERING INFORMATION

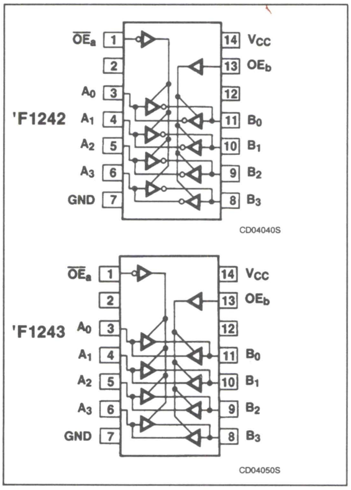
PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
20-Pin Plastic DIP	N74F1242N, N74F1243N
20-Pin Plastic SOL	N74F1242D, N74F1243D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

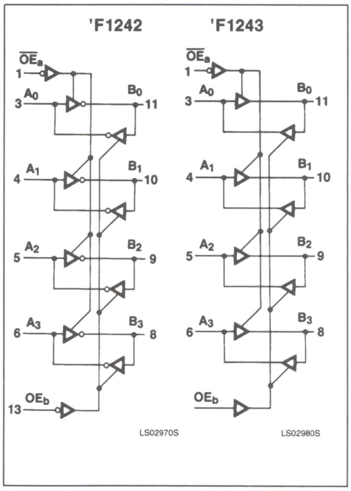
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_n, B_n	Data inputs	3.5/0.117	70µA/70µA
$\overline{OE}_a$	3-State output enable input (active-Low)	1.0/0.033	20µA/20µA
OE_b	3-State output enable input (active-High)	1.0/0.033	20µA/20µA
A_n, B_n	Data outputs	750/106.7	15mA/64mA

NOTE:
1. One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

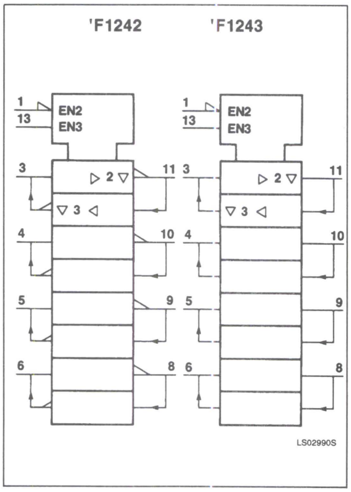
PIN CONFIGURATION


'F1242
$\overline{OE}_a$ 1
2
A_0 3
A_1 4
A_2 5
A_3 6
GND 7
14 V_{CC}
13 OE_b
12
11 B_0
10 B_1
9 B_2
8 B_3
CD04040S
'F1243
$\overline{OE}_a$ 1
2
A_0 3
A_1 4
A_2 5
A_3 6
GND 7
14 V_{CC}
13 OE_b
12
11 B_0
10 B_1
9 B_2
8 B_3
CD04050S

LOGIC SYMBOL


'F1242
'F1243
$\overline{OE}_a$ 1
A_0 3
B_0 11
A_1 4
B_1 10
A_2 5
B_2 9
A_3 6
B_3 8
OE_b 13
LS02970S
LS02980S

LOGIC SYMBOL (IEEE/IEC)


'F1242
'F1243
1
13
EN2
EN3
3
11
▷ 2 ▽
▽ 3 ◁
4
10
5
9
6
8
LS02990S

FUNCTION TABLE for 'F1242

INPUTS		INPUT/OUTPUT	
$\overline{OE}_a$	OE_b	A_n	B_n
L	L	INPUT	B = A
H	L	Z	Z
L	H	a	a
H	H	A = B	INPUT

FUNCTION TABLE for 'F1243

INPUTS		INPUT/OUTPUT	
$\overline{OE}_a$	OE_b	A_n	B_n
L	L	INPUT	B = A
H	L	Z	Z
L	H	a	a
H	H	A = B	INPUT

H = High voltage level
L = Low voltage level
Z = High-impedance (OFF) state
a = This condition is not allowed due to excessive currents.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	128	mA
T_A	Operating free-air temperature range	0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−15	mA
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]			74F1242/74F1243			UNIT
							Min	Typ[2]	Max	
V_{OH}	High-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = −3mA	±10%V_{CC}	2.4			V
						±5%V_{CC}	2.7	3.4		V
					I_{OH} = −15mA	±10%V_{CC}	2.0			V
						±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 48mA	±10%V_{CC}		0.35	0.50	V
					I_{OL} = 64mA	±5%V_{CC}		0.40	0.55	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, $I_I = I_{IK}$				−0.73	−1.2	V
I_I	Input current at maximum input voltage	$A_0 - A_3$, $B_0 - B_3$		V_{CC} = 5.5V, V_I = 5.5V					1.0	mA
		$\overline{OE}_a$, OE_b		V_{CC} = 0.0V, V_I = 7.0V					100	μA
I_{IH}	High-level input current for $\overline{OE}_a$ and OE_b inputs only			V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	Low-level input current for $\overline{OE}_a$ and OE_b inputs only			V_{CC} = MAX, V_I = 0.5V					−20	μA
I_{IH} + I_{OZH}	OFF-state output current High-level voltage applied			V_{CC} = MAX, V_O = 2.7V					70	μA
I_{IL} + I_{OZL}	OFF-state output current Low-level voltage applied			V_{CC} = MAX, V_O = 0.5V					−70	μA
I_{OS}	Short-circuit output current[3]			V_{CC} = MAX			−100		−225	mA
I_{CC}	Supply current (total)	'F1242	I_{CCH}	V_{CC} = MAX				35	46	mA
			I_{CCL}					50	72	mA
			I_{CCZ}					45	60	mA
		'F1243	I_{CCH}					40	50	mA
			I_{CCL}					52	65	mA
			I_{CCZ}					44	55	mA

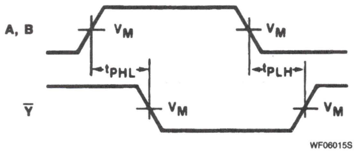
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

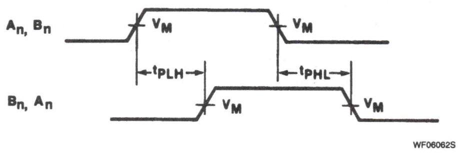
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	74F1242/74F1243					UNIT
				$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay data to output	'F1242	Waveform 1	3.0 1.5	4.5 2.5	6.0 4.0	3.0 1.5	6.5 4.5	ns
t_{PZH} t_{PZL}	Output enable time to High or Low		Waveform 3 Waveform 4	3.5 3.0	5.5 5.5	7.5 7.5	3.0 3.0	8.0 8.0	ns
t_{PHZ} t_{PLZ}	Output disable time from High or Low		Waveform 3 Waveform 4	3.5 3.0	6.0 5.0	8.0 7.5	3.5 3.0	9.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay data to output	'F1243	Waveform 2	2.0 3.0	4.0 5.0	5.5 6.5	2.0 3.0	6.0 7.0	ns
t_{PZH} t_{PZL}	Output enable time to High or Low		Waveform 3 Waveform 4	2.5 2.5	5.5 5.0	8.0 7.5	2.5 2.5	8.5 8.0	ns
t_{PHZ} t_{PLZ}	Output disable time from High or Low		Waveform 3 Waveform 4	3.5 2.0	6.5 5.0	8.5 7.5	3.0 2.0	9.0 8.0	ns

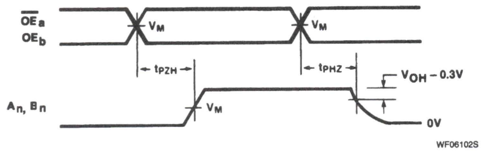
AC WAVEFORMS


A, B
V_M
V_M
tPHL
tPLH
Ȳ
V_M
V_M
WF06015S

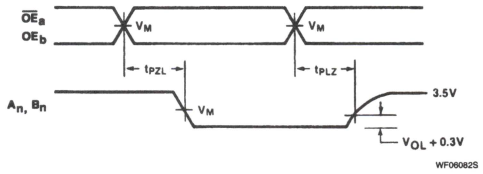
Waveform 1. Propagation Delay Data to Output for 'F1242


A_n, B_n
V_M
V_M
tPLH
tPHL
B_n, A_n
V_M
V_M
WF06062S

Waveform 2. Propagation Delay Data to Output for 'F1243


OE̅_a
OE_b
V_M
V_M
tPZH
tPHZ
V_OH − 0.3V
A_n, B_n
V_M
0V
WF06102S

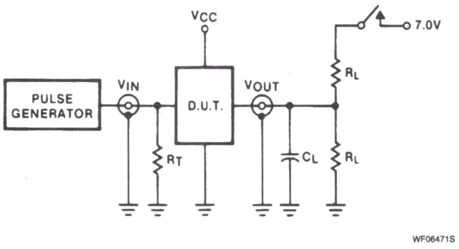
Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time From High Level


OE̅_a
OE_b
V_M
V_M
tPZL
tPLZ
A_n, B_n
V_M
3.5V
V_OL + 0.3V
WF06082S

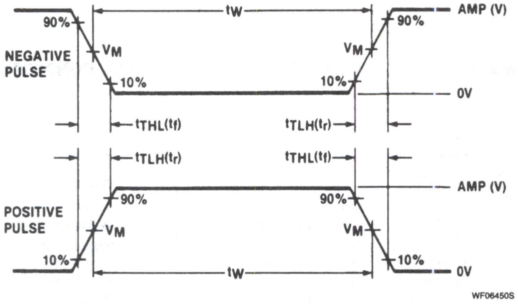
Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORMS


VCC
7.0V
RL
VIN
VOUT
PULSE GENERATOR
D.U.T.
RT
CL
RL
WF06471S

Test Circuit for 3-State Outputs


tW
90%
AMP (V)
NEGATIVE PULSE
VM
10%
0V
tTHL(tf)
tTLH(tr)
tTLH(tr)
tTHL(tf)
90%
AMP (V)
POSITIVE PULSE
VM
10%
0V
tW
WF06450S

$V_M = 1.5V$

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH 1
t_{PZH}	open
t_{PZL}	closed
t_{PHZ}	open
t_{PLZ}	closed

DEFINITIONS

R_L = Load resistor to GND; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F1244
Buffer

Octal Buffer (3-State)
Product Specification

FAST Products

FEATURES

- **High-impedance NPN base inputs for reduced loading (20µA in High and Low states)**
- **Functional pin for pin equivalent of 'F244**
- **1/30th the bus loading of 'F244**
- **Low-power, light-bus loading**
- **Provides ideal interface and increases fan-out of MOS Microprocessors**
- **Octal bus interface**
- **3-State buffer outputs sink 64mA and source 15mA**

DESCRIPTION

The 'F1244 is an octal buffer that is ideal for driving bus lines or buffer memory address registers. The outputs are capable of sinking 64mA and sourcing up to 15mA, producing very good capacitive drive characteristics. The device features two output enables, $\overline{OE}_n$, each controlling four of the 3-State outputs. The 'F1244 is pin and functional compatible with the 'F244. The lower power and light bus loading features make it an ideal part to interface directly with MOS Microprocessors.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F1244	4.5ns	43mA

ORDERING INFORMATION

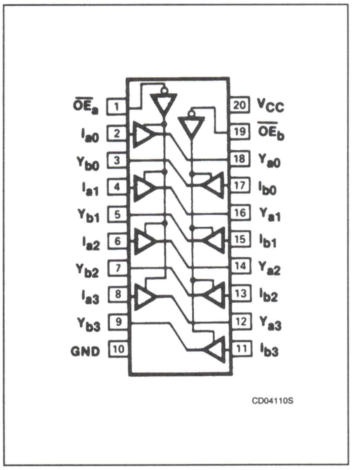
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F1244N
20-Pin Plastic SOL	N74F1244D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$I_{a0}-I_{a3}$, $I_{b0}-I_{b3}$	Data inputs	1.0/0.033	20µA/20µA
$\overline{OE}_a$	3-State output enable input (active-Low)	1.0/0.033	20µA/20µA
$\overline{OE}_b$	3-State output enable input (active-Low)	1.0/0.033	20µA/20µA
$Y_{a0}-Y_{a3}$, $Y_{b0}-Y_{b3}$	Data outputs	750/106.7	15mA/64mA

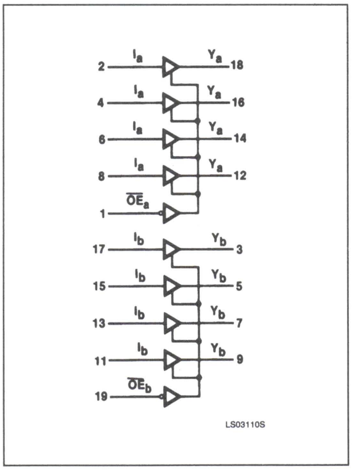
NOTE:
1. One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



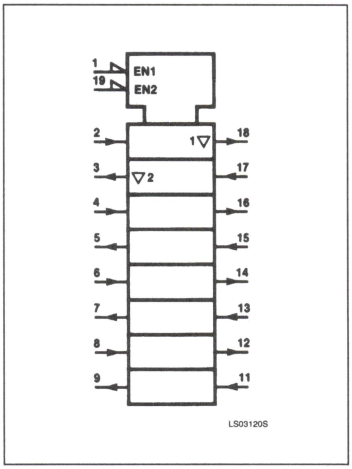
$\overline{OE}_a$ 1
I_{a0} 2
Y_{b0} 3
I_{a1} 4
Y_{b1} 5
I_{a2} 6
Y_{b2} 7
I_{a3} 8
Y_{b3} 9
GND 10
20 V_{CC}
19 $\overline{OE}_b$
18 Y_{a0}
17 I_{b0}
16 Y_{a1}
15 I_{b1}
14 Y_{a2}
13 I_{b2}
12 Y_{a3}
11 I_{b3}
CD04110S

LOGIC SYMBOL



2 I_a Y_a 18
4 I_a Y_a 16
6 I_a Y_a 14
8 I_a Y_a 12
1 $\overline{OE}_a$
17 I_b Y_b 3
15 I_b Y_b 5
13 I_b Y_b 7
11 I_b Y_b 9
19 $\overline{OE}_b$
LS03110S

LOGIC SYMBOL (IEEE/IEC)



1 EN1
19 EN2
2 1▽ 18
3 ▽2 17
4 16
5 15
6 14
7 13
8 12
9 11
LS03120S

FUNCTION TABLE for 'F1244

INPUTS				OUTPUTS	
$\overline{OE}_a$	I_a	$\overline{OE}_b$	I_b	Y_{an}	Y_{bn}
L	L	L	L	L	L
L	H	L	H	H	H
H	X	H	X	Z	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High-impedance (OFF) state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	128	mA
T_A	Operating free-air temperature range	0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−15	mA
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature	0		70	°C

Buffer

FAST 74F1244

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			74F1244			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = −3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.4		V
				I_{OH} = −15mA	±10%V_{CC}	2.0			V
					±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 48mA	±10%V_{CC}		0.35	0.50	V
				I_{OL} = 64mA	±5%V_{CC}		0.40	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = 0.0V, V_I = 7.0V					100	μA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					−20	μA
I_{OZH}	OFF-state output current High-level voltage applied		V_{CC} = MAX, V_O = 2.7V					50	μA
I_{OZL}	OFF-state output current Low-level voltage applied		V_{CC} = MAX, V_O = 0.5V					−50	μA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX			−100		−255	mA
I_{CC}	Supply current[4] (total)	I_{CCH}	V_{CC} = MAX				30	40	mA
		I_{CCL}					57	75	mA
		I_{CCZ}					43	58	mA

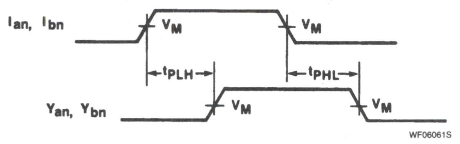
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. I_{CC} is measured with outputs open.

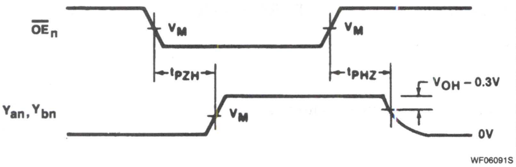
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F1244					UNIT
			T_A = +25°C V_{CC} = +5.0V C_L = 50pF R_L = 500Ω			T_A = 0 to +70°C V_{CC} = +5.0V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_{an}, I_{bn} to Y_{an}, Y_{bn}	Waveform 1	2.5 2.0	4.0 5.0	5.5 7.0	2.5 2.0	7.5 6.0	ns
t_{PZH} t_{PZL}	Output enable time to High or Low	Waveform 2 Waveform 3	3.0 3.0	6.0 6.5	7.5 8.0	3.0 3.0	8.5 8.5	ns
t_{PHZ} t_{PLZ}	Output disable time from High or Low	Waveform 2 Waveform 3	2.0 2.0	4.0 4.0	5.5 5.5	2.0 2.0	6.0 6.0	ns

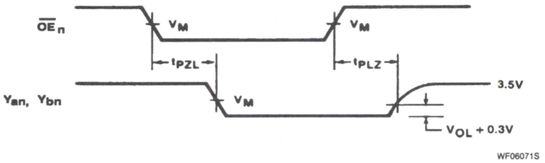
AC WAVEFORMS


Ian, Ibn
VM
VM
tPLH
tPHL
Yan, Ybn
VM
VM
WF06061S

Waveform 1. Propagation Delay Data to Output


OEn
VM
VM
tPZH
tPHZ
VOH − 0.3V
Yan, Ybn
VM
0V
WF06091S

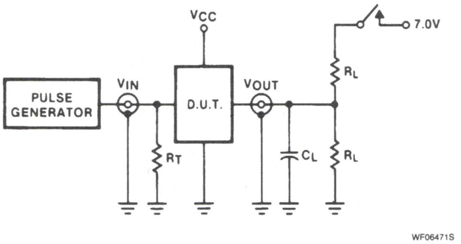
Waveform 2. 3-State Output Enable Time to High Level and Output Disable Time From High Level


OEn
VM
VM
tPZL
tPLZ
Yan, Ybn
VM
3.5V
VOL + 0.3V
WF06071S

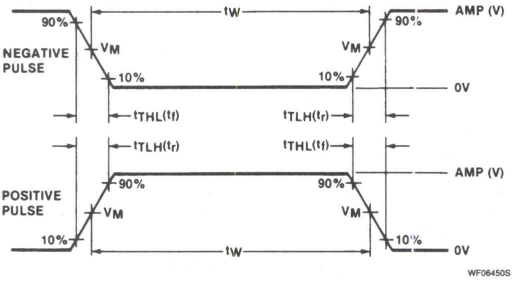
Waveform 3. 3-State Output Enable Time to Low Level and Output Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORMS


VCC
7.0V
RL
PULSE GENERATOR
VIN
D.U.T.
VOUT
RT
CL
RL
WF06471S

Test Circuit for 3-State Outputs


90%
tW
AMP (V)
90%
NEGATIVE PULSE
VM
VM
10%
10%
0V
tTHL(tf)
tTLH(tr)
tTLH(tr)
tTHL(tf)
AMP (V)
POSITIVE PULSE
90%
90%
VM
VM
10%
10%
0V
tW
WF06450S

$V_M = 1.5V$

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor to GND; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F1245
Transceiver

Octal Transceiver (3-State)
Product Specification

FAST Products

FEATURES

- Same function and pinout as 74F1245
- High-impedance NPN base inputs for reduced loading (70μA in High and Low states)
- Useful in applications where light bus-loading or direct interface with output of a MOS microprocessor is desired
- Octal bidirectional bus interface
- Glitch free during 3-State power up and power down
- 3-State buffer outputs sink 64mA
- 15mA source current

DESCRIPTION

The 'F1245 is octal transceiver featuring non-inverting 3-State bus compatible outputs in both transmit and receive directions. The B port outputs are all capable of sinking 64mA and sourcing up to 15mA, producing very good capacitive drive characteristics. The device features an Ouput Enable ($\overline{OE}$) input for easy cascading and a Transmit/Receive (T/$\overline{R}$) input for direction control. The 3-State ouputs, $B_0 - B_7$, have been designed to prevent ouput bus loading if the power is removed from the device.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F1245	5.0ns	115mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
20-Pin Plastic DIP	N74F1245N
20-Pin Plastic SOL[1]	N74F1245D

NOTE:

1. Thermal mounting techniques are recommended. See App Note AN SMD-100 for a discussion of thermal considerations for surface mounted devices.

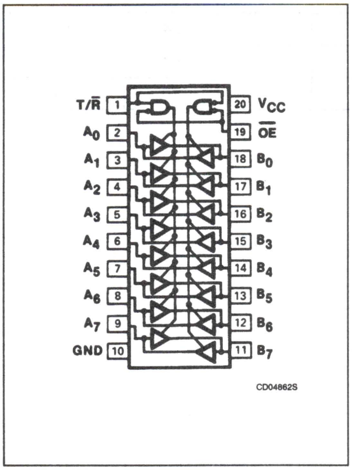
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$A_0 - A_7$	Data inputs	3.5/0.117	70μA/70μA
$B_0 - B_7$	Data inputs	3.5/0.117	70μA/70μA
T/$\overline{R}$	Transmit/Receive input	2.0/0.066	40μA/40μA
$\overline{OE}$	Output Enable input	2.0/0.066	40μA/40μA
$A_0 - A_7$	Data outputs	150/40	3mA/24mA
$B_0 - B_7$	Data outputs	750/106.7	15mA/64mA

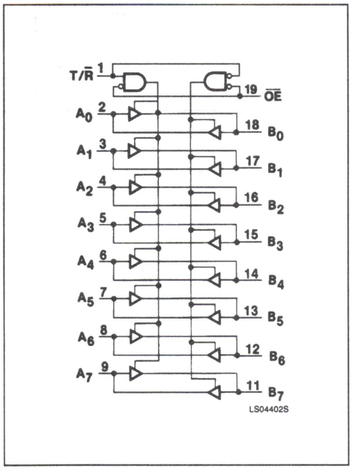
NOTE:

1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

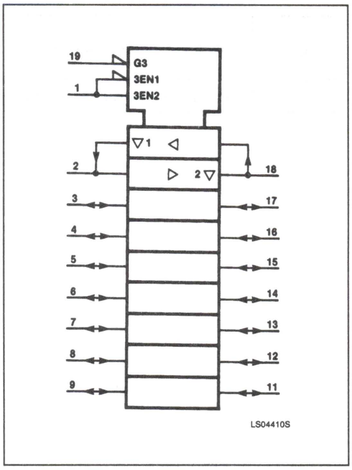
PIN CONFIGURATION


T/R̄ 1
A0 2
A1 3
A2 4
A3 5
A4 6
A5 7
A6 8
A7 9
GND 10
20 VCC
19 OE
18 B0
17 B1
16 B2
15 B3
14 B4
13 B5
12 B6
11 B7
CD04862S

LOGIC SYMBOL


T/R̄ 1
A0 2
A1 3
A2 4
A3 5
A4 6
A5 7
A6 8
A7 9
19 OE
18 B0
17 B1
16 B2
15 B3
14 B4
13 B5
12 B6
11 B7
LS04402S

LOGIC SYMBOL (IEEE/IEC)


19
1
G3
3EN1
3EN2
▽1
◁
▷
2▽
2
3
4
5
6
7
8
9
18
17
16
15
14
13
12
11
LS04410S

FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS	
$\overline{OE}$	T/$\overline{R}$	A_n	B_n
L	L	A = B	INPUT
L	H	INPUT	B = A
H	X	Z	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High-impedance (OFF) state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		−0.5 to +7.0	V
V_{IN}	Input voltage		−0.5 to +7.0	V
I_{IN}	Input current		−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		−0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	$A_0 - A_7$	48	mA
		$B_0 - B_7$	128	mA
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature range		−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Typ	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	High-level output current	$A_0 - A_7$			−3	mA
		$B_0 - B_7$			−15	mA
I_{OL}	Low-level output current	$A_0 - A_7$			24	mA
		$B_0 - B_7$			64	mA
T_A	Operating free-air temperature		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			74F1245			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage	$A_0 - A_7$ $B_0 - B_7$	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = −3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.4		V
		$B_0 - B_7$		I_{OH} = −15mA	±10%V_{CC}	2.0			V
					±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage	$A_0 - A_7$	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 24mA			0.35	0.50	V
							0.35	0.50	V
		$B_0 - B_7$		I_{OL} = 64mA	±5%V_{CC}		0.40	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$				−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = 0.0V, V_I = 7.0V					100	μA
I_{IH}	High-level input current $\overline{OE}$ and S/$\overline{R}$ only		V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	Low-level input current $\overline{OE}$ and S/$\overline{R}$ only		V_{CC} = MAX, V_I = 0.5V					−20	μA
$I_{OZH} + I_{IH}$	OFF-state current High-level voltage applied		V_{CC} = MAX, V_O = 2.7V					70	μA
$I_{OZL} + I_{IL}$	OFF-state current Low-level voltage applied		V_{CC} = MAX, V_O = 0.5V					−600	μA
I_{OS}	Short-circuit output current[3]	$A_0 - A_7$	V_{CC} = MAX			−60		−150	mA
		$B_0 - B_7$	V_{CC} = MAX			−100		−225	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_{IN} = 4.5V			120	155	mA
		I_{CCL}		V_{IN} = GND			116	150	mA
		I_{CCZ}		$V_{IN} = \overline{OE}$ = 4.5V			110	165	mA

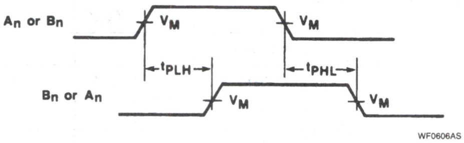
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

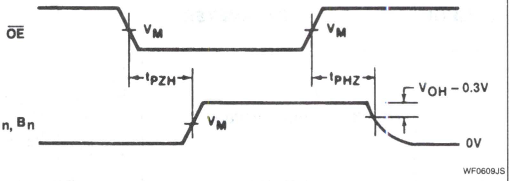
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F1245					UNIT
			T_A = +25°C V_{CC} = +5.0V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = +5.0V± 10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n or B_n to B_n or A_n	Waveform 1	2.0 2.5	4.0 5.0	6.5 7.5	1.5 2.0	7.0 8.0	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}$ to A_n or B_n	Waveform 2 Waveform 3	3.0 4.0	6.0 7.5	8.0 10.0	2.5 3.5	9.0 11.0	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}$ to A_n or B_n	Waveform 2 Waveform 3	2.0 4.0	5.0 7.0	8.0 10.0	1.5 4.0	9.0 11.0	ns

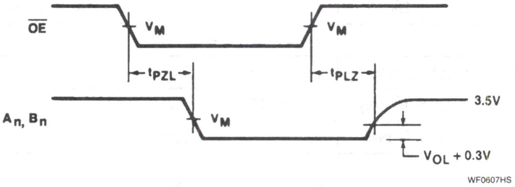
AC WAVEFORMS


An or Bn
VM
VM
tPLH
tPHL
Bn or An
VM
VM
WF0606AS

Waveform 1. Propagation Delay for Input to Output


OE
VM
VM
tPZH
tPHZ
VOH − 0.3V
An, Bn
VM
0V
WF0609JS

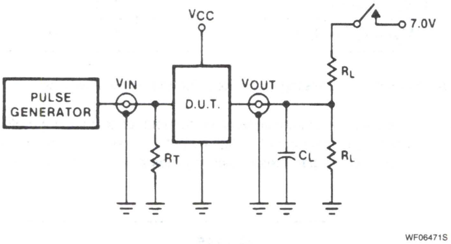
Waveform 2. 3-State Output Enable Time to High Level and Output Disable Time From High Level


OE
VM
VM
tPZL
tPLZ
3.5V
An, Bn
VM
VOL + 0.3V
WF0607HS

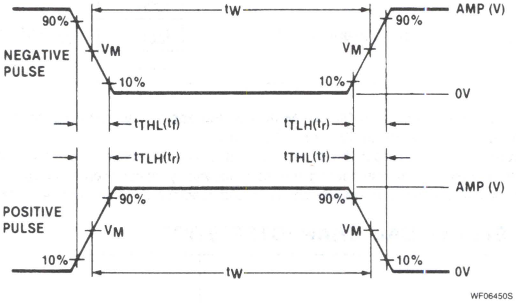
Waveform 3. 3-State Output Enable Time to Low Level and Output Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORMS


VCC
7.0V
RL
PULSE GENERATOR
VIN
D.U.T.
VOUT
RT
CL
RL
WF06471S

Test Circuit for 3-State Outputs


tW
AMP (V)
90%
90%
NEGATIVE PULSE
VM
VM
10%
10%
0V
tTHL(tf)
tTLH(tr)
tTLH(tr)
tTHL(tf)
AMP (V)
90%
90%
POSITIVE PULSE
VM
VM
10%
10%
0V
tW
WF06450S

$V_M = 1.5V$

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor to GND; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Signetics

FAST 74F1761

DRAM and Interrupt Vector Controller

Preliminary Specification

FAST Products

FEATURES

- **Programmable DRAM signal timing generator**
- **Automatic refresh circuitry**
- **Provides byte selection for 16- and 32-bit buses**
- **Interrupt Priority Encoder included**
- **Interrupt Acknowledge vector generator on-chip**

DESCRIPTION

The Signetics DRAM and Interrupt Vector Controller (DIVC) is a high-performance bipolar device designed to reduce board space and improve performance in microprocessor-based systems. The DIVC's functions include a DRAM signal interface with user programmable timing to match the performance of specific DRAMs used in a system. With a maximum clock frequency of 100MHz, this means a timing resolution of 10ns. The DRAM Controller section also includes automatic refresh arbitration, with the duration and frequency of refresh totally programmable by the user. When used with the 74F1762 Memory Address Controller, the DIVC provides a complete system solution for DRAM and Interrupt Control. For Interrupt Control, the DIVC contains an Interrupt Priority Decoder with latched inputs controlled by the Interrupt Latch Enable (ILE) input. In addition, the DIVC contains an Interrupt Acknowledge Controller which passes a programmable 8-bit vector on the system data bus upon receipt of an interrupt acknowledge. There are 7 interrupt acknowledge vectors; each accessible by placing the priority number of the Interrupt Acknowledge on the A1 – A3 signal inputs while acknowledging an interrupt.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F1761	100MHz	200mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $70°C$
Plastic DIP	N74F1761N
PLCC 44	N74F1761A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

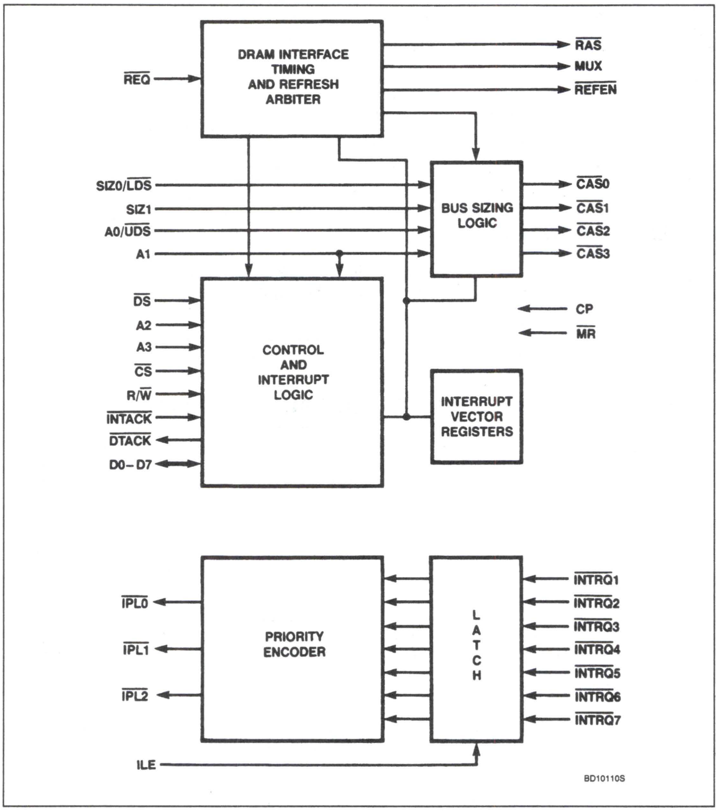
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$\overline{\text{REQ}}$	DRAM request input	1.0/1.0	20μA/0.6mA
SIZ0/$\overline{\text{LDS}}$, SIZ1, A0/$\overline{\text{UDS}}$, A1	Byte Select inputs	1.0/1.0	20μA/0.6mA
A2, A3	Register Select inputs	1.0/1.0	20μA/0.6mA
$\overline{\text{CS}}$, $\overline{\text{DS}}$	Chip Select, Data Strobe	1.0/1.0	20μA/0.6mA
R/$\overline{\text{W}}$	Read/Write input	1.0/1.0	20μA/0.6mA
$\overline{\text{INTACK}}$	Interrupt Acknowledge input	1.0/1.0	20μA/0.6mA
ILE	Interrupt Latch Enable input	1.0/1.0	20μA/0.6mA
CP	Clock input	1.0/1.0	20μA/0.6mA
$\overline{\text{MR}}$	Master Reset input	1.0/1.0	20μA/0.6mA
$\overline{\text{INTRQ1-7}}$	Interrupt Request inputs	1.0/1.0	20μA/0.6mA
$\overline{\text{DTACK}}$	Data Transfer Acknowledge output	(OC)/80	24mA
D0 – D7	Data Bus	50/80 (1.0/1.0)	1.0mA/24mA
$\overline{\text{IPL0-2}}$	Interrupt Priority outputs	50/80	1.0mA/24mA
$\overline{\text{RAS}}$, MUX, $\overline{\text{REFEN}}$, $\overline{\text{CAS0-3}}$	DRAM Control outputs	1750/100	35mA/60mA

NOTE:

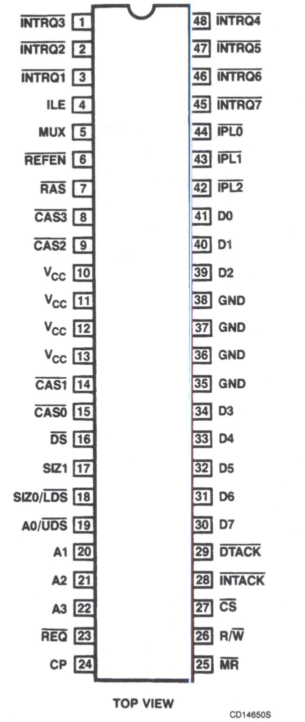
1. One (1.0) FAST Unit Load is defined as 20μA in the High state and 0.6mA in the Low state. O.C. = Open-Collector

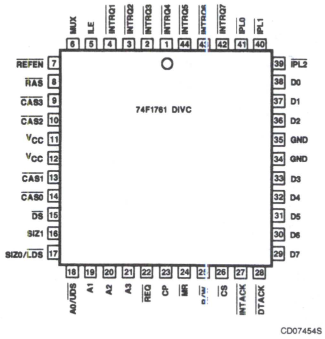
DRAM and Interrupt Vector Controller FAST 74F1761

BLOCK DIAGRAM


REQ
DRAM INTERFACE TIMING AND REFRESH ARBITER
RAS
MUX
REFEN
SIZ0/LDS
SIZ1
A0/UDS
A1
BUS SIZING LOGIC
CAS0
CAS1
CAS2
CAS3
DS
A2
A3
CS
R/W
INTACK
DTACK
D0 – D7
CONTROL AND INTERRUPT LOGIC
CP
MR
INTERRUPT VECTOR REGISTERS
IPL0
IPL1
IPL2
PRIORITY ENCODER
LATCH
INTRQ1
INTRQ2
INTRQ3
INTRQ4
INTRQ5
INTRQ6
INTRQ7
ILE
BD10110S

PIN CONFIGURATION


INTRQ3 1
INTRQ2 2
INTRQ1 3
ILE 4
MUX 5
REFEN 6
RAS 7
CAS3 8
CAS2 9
VCC 10
VCC 11
VCC 12
VCC 13
CAS1 14
CAS0 15
DS 16
SIZ1 17
SIZ0/LDS 18
A0/UDS 19
A1 20
A2 21
A3 22
REQ 23
CP 24
48 INTRQ4
47 INTRQ5
46 INTRQ6
45 INTRQ7
44 IPL0
43 IPL1
42 IPL2
41 D0
40 D1
39 D2
38 GND
37 GND
36 GND
35 GND
34 D3
33 D4
32 D5
31 D6
30 D7
29 DTACK
28 INTACK
27 CS
26 R/W
25 MR
TOP VIEW
CD14650S


MUX 6
ILE 5
INTRQ1 4
INTRQ2 3
INTRQ3 2
INTRQ4 1
INTRQ5 44
INTRQ6 43
INTRQ7 42
IPL0 41
IPL1 40
REFEN 7
RAS 8
CAS3 9
CAS2 10
VCC 11
VCC 12
CAS1 13
CAS0 14
DS 15
SIZ1 16
SIZ0/LDS 17
74F1761 DIVC
39 IPL2
38 D0
37 D1
36 D2
35 GND
34 GND
33 D3
32 D4
31 D5
30 D6
29 D7
18 A0/UDS
19 A1
20 A2
21 A3
22 REQ
23 CP
24 MR
25 R/W
26 CS
27 INTACK
28 DTACK
CD07454S

FAST 74F1762
Memory Address Controller

Preliminary Specification

FAST Products

FEATURES

- **Provides DRAM Refresh and multiplexed addresses**
- **Direct Addressing of up to 4Mb**
- **Compatible with 74F1761 DIVC and other DRAM controllers**
- **High-performance outputs**
- **High-speed multiplexing**
- **Internal 11-bit refresh counter**

DESCRIPTION

The Signetics Memory Address-Controller is designed for use in very high-performance dynamic RAM applications. In addition to multiplexing row and column addresses, the device also generates and multiplexes refresh addresses. Though specifically designed to be used with the 74F1761 DRAM and Interrupt Vector Controller, it may be used with any other custom or standard DRAM timing controller chip.

The F1762 contains 22 address inputs ($RA_0 - RA_{10}$ and $CA_0 - CA_{10}$), an 11-bit refresh counter, and eleven 3-to-1 multiplexers. The multiplexed row, column, or refresh address is output on the eleven high-performance outputs ($MA_0 - MA_{10}$). This enables direct addressing of up to 4Mb dynamic RAMs.

Combined with the F1761, the F1762 provides a complete 4Mb DRAM and Interrupt Control solution. This solution can control dynamic RAMs with access times down to 40ns.

TYPE	TYPICAL DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F1762	5.3ns	70mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $70°C$
Plastic DIP	N74F1762N
PLCC 44	N74F1762A

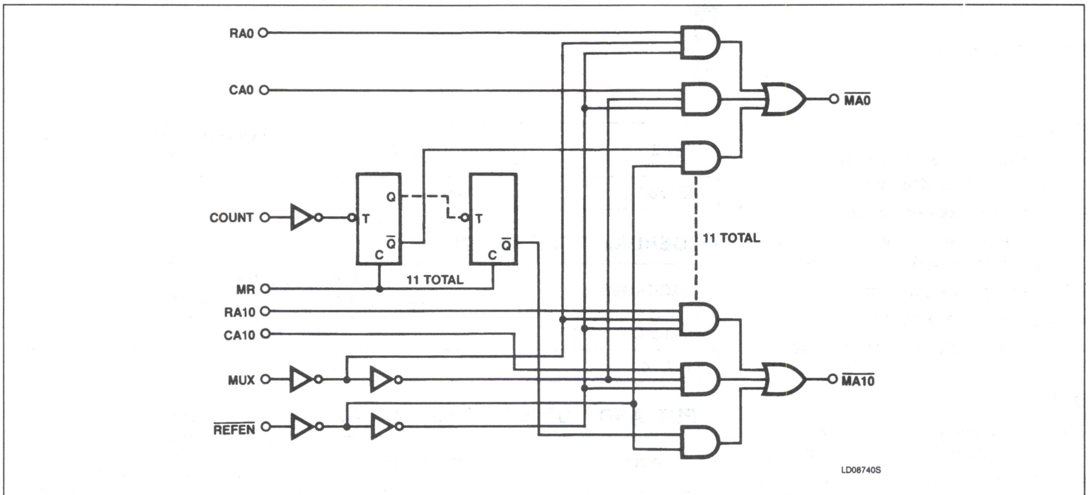
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
RA0 – RA10	Row Address inputs	1.0/1.0	20μA/0.6mA
CA0 – CA10	Column Address inputs	1.0/1.0	20μA/0.6mA
$\overline{MA0}$ – $\overline{MA10}$	DRAM Address outputs	N/A	35mA/60mA
$\overline{REFEN}$	Refresh Select input (active-Low)	1.0/1.0	20μA/0.6mA
MUX	Row/Column Select input	1.0/1.0	20μA/0.6mA
COUNT	Refresh Address Count input	1.0/1.0	20μA/0.6mA
MR	Refresh Counter Reset input	1.0/1.0	20μA/0.6mA

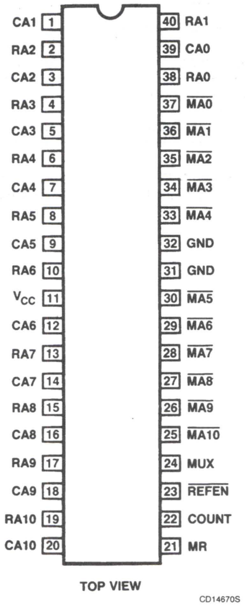
NOTE:

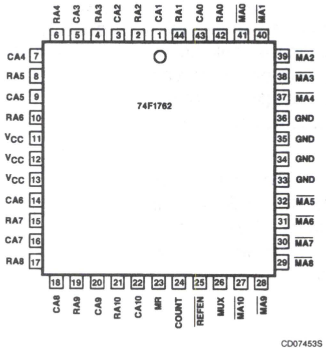
1. One (1.0) FAST Unit Load is defined as 20μA in the High state and 0.6mA in the Low state. FAST Unit Loads do not correspond to DRAM Input Loads. See Functional Description for details.

EQUIVALENT LOGIC DIAGRAM


RA0
CA0
COUNT
MR
RA10
CA10
MUX
REFEN
T
Q
C
Q̄
11 TOTAL
11 TOTAL
MA0
MA10
LD08740S

PIN CONFIGURATION


CA1 1
RA2 2
CA2 3
RA3 4
CA3 5
RA4 6
CA4 7
RA5 8
CA5 9
RA6 10
VCC 11
CA6 12
RA7 13
CA7 14
RA8 15
CA8 16
RA9 17
CA9 18
RA10 19
CA10 20
40 RA1
39 CA0
38 RA0
37 MA0
36 MA1
35 MA2
34 MA3
33 MA4
32 GND
31 GND
30 MA5
29 MA6
28 MA7
27 MA8
26 MA9
25 MA10
24 MUX
23 REFEN
22 COUNT
21 MR
TOP VIEW
CD14670S


RA4 6
CA3 5
RA3 4
CA2 3
RA2 2
CA1 1
RA1 44
CA0 43
RA0 42
MA0 41
MA1 40
CA4 7
RA5 8
CA5 9
RA6 10
VCC 11
VCC 12
VCC 13
CA6 14
RA7 15
CA7 16
RA8 17
39 MA2
38 MA3
37 MA4
36 GND
35 GND
34 GND
33 GND
32 MA5
31 MA6
30 MA7
29 MA8
18 CA8
19 RA9
20 CA9
21 RA10
22 CA10
23 MR
24 COUNT
25 REFEN
26 MUX
27 MA10
28 MA9
74F1762
CD07453S

Signetics

FAST 74F1763
Intelligent DRAM Controller

Preliminary Specification

FAST Products

FEATURES

- **DRAM signal timing generator**
- **Automatic refresh circuitry**
- **Programmable row address hold and $\overline{\text{RAS}}$ precharge Time**
- **Supports Page Mode accesses**
- **Controls 1Mb DRAMs**
- **Intelligent Burst-Mode Refresh after Page-Mode access cycles**

DESCRIPTION

The Signetics Intelligent Dynamic RAM Controller is a 1Mb, single-port version of the popular 74F764 Dynamic RAM Dual-Ported Controller. It contains automatic signal timing, address multiplexing, and refresh control required for interfacing with dynamic RAMs. Additional features have been added to this device to take advantage of technological advances in Dynamic RAMs. A Page-Mode access pin allows the user to assert $\overline{\text{RAS}}$ for the entire access cycle rather than the predefined four-clock-cycle pulse width used for normal random access cycles. In addition, the user has the ability to program the $\overline{\text{RAS}}$ precharge time and Row-Address-Hold time to fit the particular DRAMs being used. $\overline{\text{DTACK}}$ has been modified from previous family parts to become a negative true, tri-stated output. The options for latched or unlatched address are contained on a single device by the addition of an Address Latch Enable (ALE) input. Finally, a burst refresh monitor has been added to ensure complete refreshing after lengthy page-mode access cycles. With a maximum clock frequency of 100MHz, the F1763 is capable of driving DRAM arrays with access times down to 40ns.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F1763	100MHz	150mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $70°C$
Plastic DIP	N74F1763N
PLCC 44	N74F1763A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

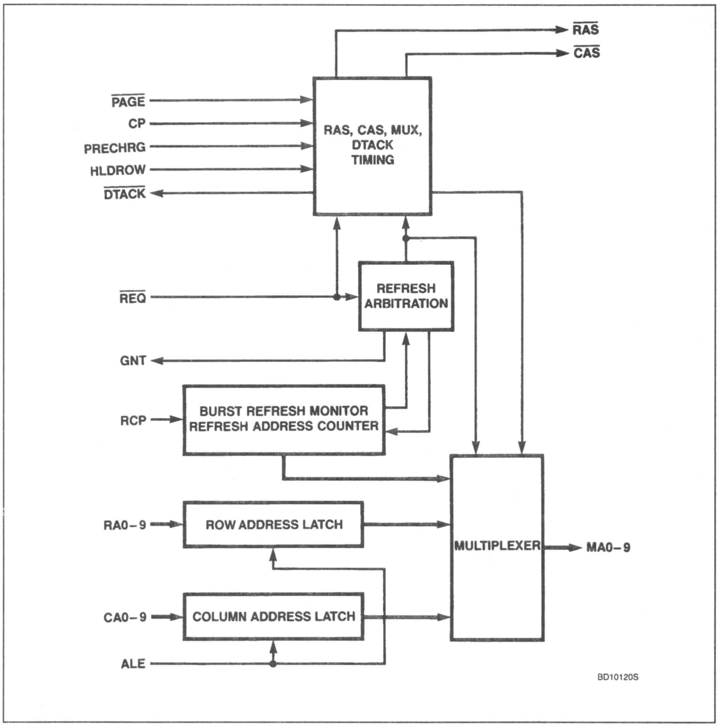
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$\overline{\text{REQ}}$	DRAM Request input	1.0/1.0	20μA/0.6mA
CP	Clock input	1.0/1.0	20μA/0.6mA
$\overline{\text{PAGE}}$	Page Mode Select input	1.0/1.0	20μA/0.6mA
PRECHRG	RAS Precharge Select input	1.0/1.0	20μA/0.6mA
HLDROW	Row Hold Select input	1.0/1.0	20μA/0.6mA
$\overline{\text{DTACK}}$	Data Transfer Ack. output	50/80	35mA/60mA
GNT	Access Grant output	50/80	35mA/60mA
RCP	Refresh Clock input	1.0/1.0	20μA/0.6mA
RA0 – RA9	Row Address inputs	1.0/1.0	20μA/0.6mA
CA0 – CA9	Column Address inputs	1.0/1.0	20μA/0.6mA
ALE	Address Latch Enable input	1.0/1.0	20μA/0.6mA
$\overline{\text{RAS}}$	Row Address Strobe output	N/A	35mA/60mA
$\overline{\text{CAS}}$	Column Address Strobe output	N/A	35mA/60mA
MA0 – MA9	DRAM Address outputs	N/A	35mA/60mA

NOTE:

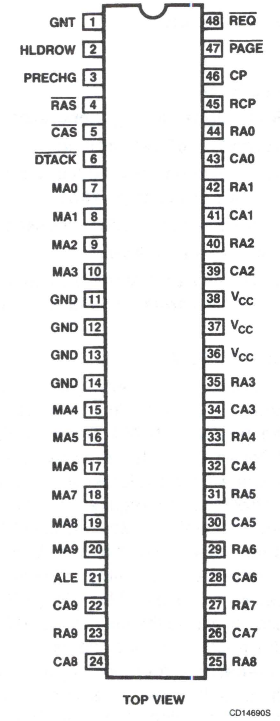
1. One (1.0) FAST Unit Load is defined as 20μA in the High state and 0.6mA in the Low state. FAST Unit Loads do not correspond to DRAM Input Loads. See Functional Description for details.

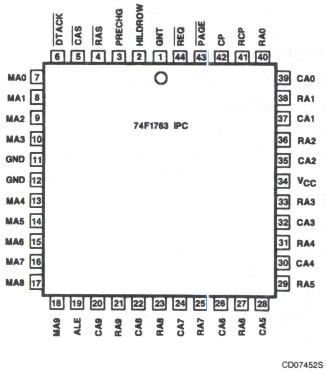
Intelligent DRAM Controller FAST 74F1763

BLOCK DIAGRAM


$\overline{\text{RAS}}$
$\overline{\text{CAS}}$
$\overline{\text{PAGE}}$
CP
PRECHRG
HLDROW
$\overline{\text{DTACK}}$
RAS, CAS, MUX, DTACK TIMING
$\overline{\text{REQ}}$
REFRESH ARBITRATION
GNT
RCP
BURST REFRESH MONITOR
REFRESH ADDRESS COUNTER
RA0–9
ROW ADDRESS LATCH
MULTIPLEXER
MA0–9
CA0–9
COLUMN ADDRESS LATCH
ALE
BD10120S

PIN CONFIGURATION


GNT 1
HLDROW 2
PRECHG 3
$\overline{\text{RAS}}$ 4
$\overline{\text{CAS}}$ 5
$\overline{\text{DTACK}}$ 6
MA0 7
MA1 8
MA2 9
MA3 10
GND 11
GND 12
GND 13
GND 14
MA4 15
MA5 16
MA6 17
MA7 18
MA8 19
MA9 20
ALE 21
CA9 22
RA9 23
CA8 24
48 $\overline{\text{REQ}}$
47 $\overline{\text{PAGE}}$
46 CP
45 RCP
44 RA0
43 CA0
42 RA1
41 CA1
40 RA2
39 CA2
38 V_{CC}
37 V_{CC}
36 V_{CC}
35 RA3
34 CA3
33 RA4
32 CA4
31 RA5
30 CA5
29 RA6
28 CA6
27 RA7
26 CA7
25 RA8
TOP VIEW
CD14690S


$\overline{\text{DTACK}}$ 6
$\overline{\text{CAS}}$ 5
$\overline{\text{RAS}}$ 4
PRECHG 3
HLDROW 2
GNT 1
$\overline{\text{REQ}}$ 44
$\overline{\text{PAGE}}$ 43
CP 42
RCP 41
RA0 40
MA0 7
MA1 8
MA2 9
MA3 10
GND 11
GND 12
MA4 13
MA5 14
MA6 15
MA7 16
MA8 17
39 CA0
38 RA1
37 CA1
36 RA2
35 CA2
34 V_{CC}
33 RA3
32 CA3
31 RA4
30 CA4
29 RA5
74F1763 IPC
18 MA9
19 ALE
20 CA9
21 RA9
22 CA8
23 RA8
24 CA7
25 RA7
26 CA6
27 RA6
28 CA5
CD07452S

Signetics

FAST 74F1764/1765, 74F1764-1/1765-1
1 Megabit DRAM Dual-Ported Controllers

FAST Products

Preliminary Specification

FEATURES

- **Allows two microprocessors to access the same bank of dynamic RAM**
- **Performs arbitration, signal timing, address multiplexing, and refresh**
- **10 address output pins allow direct control of up to 1Mbit dynamic RAMS**
- **External address multiplexing enables control of 4Mbit (or greater) dynamic RAMs**
- **Separate refresh clock allows adjustable refresh timing**
- **F1764/F1764-1 have on-chip 20-bit address input latch**
- **Allows control of dynamic RAMs with row access times down to 40ns**
- **F1764/1765 output drivers designed for incident wave switching**
- **F1764-1/1765-1 output drivers designed for first reflected wave switching**

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F1764/1765	150MHz	150mA
74F1764-1/1765-1	150MHz	125mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ± 10%, T_A = 0°C to +70°C
Plastic DIP	74F1764N, 74F1765N, 74F1764-1N, 74F1765-1N
PLCC-44	74F1764A, 74F1765A, 74F1764-1A, 74F1765-1A

DESCRIPTION

The 74F1764/1765 DRAM Dual-ported Controller is a high-speed synchronous dual-port arbiter and timing generator that allows two microprocessors, microcontrollers, or any other memory accessing device to share the same block of DRAM. The device performs arbitration, signal timing, address multiplexing, and refresh address generation, replacing up to 25 discrete devices.

74F1764 vs 74F1765

The F1764 though functionally and pin to pin compatible with the F1765 differs from the later in that it has an on-chip address input latch. This is useful in systems that have unlatched or multiplexed address and data bus.

74F1764/1765 vs 74F1764-1/1765-1

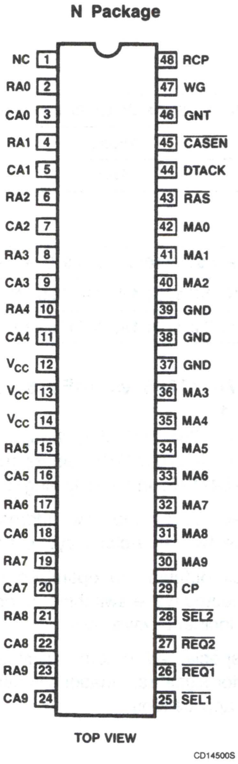
The 74F1764-1/1765-1, though as fast as the 74F1764/1765, differs from the 74F1764/1765 in the following respects:

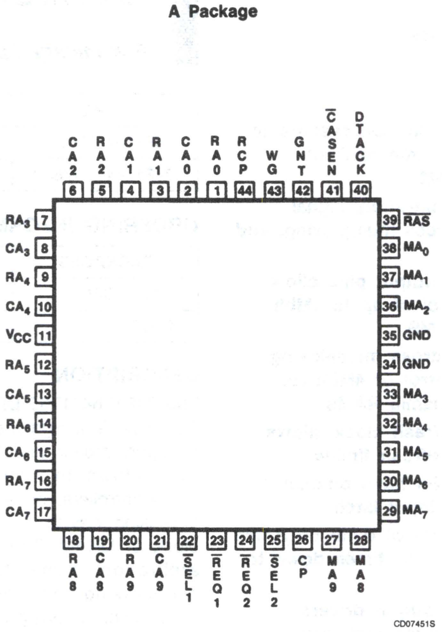
a) they reduce the row address hold time by half-a-clock cycle, and

b) their outputs are optimized for first reflected wave switching as opposed to incident wave switching.

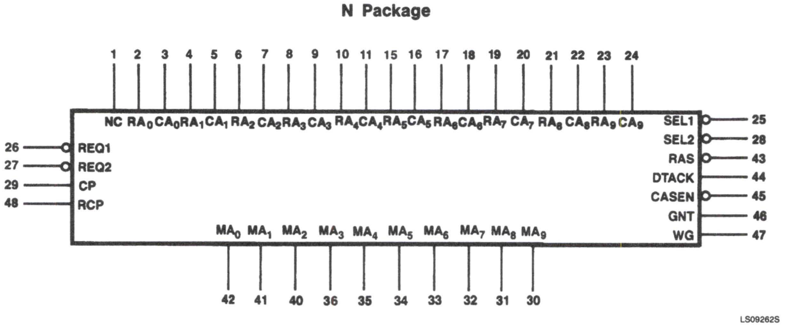
The specialized outputs eliminate the need for signal terminations in essentially all applications.

PIN CONFIGURATION


N Package
NC 1
RA0 2
CA0 3
RA1 4
CA1 5
RA2 6
CA2 7
RA3 8
CA3 9
RA4 10
CA4 11
V_{CC} 12
V_{CC} 13
V_{CC} 14
RA5 15
CA5 16
RA6 17
CA6 18
RA7 19
CA7 20
RA8 21
CA8 22
RA9 23
CA9 24
48 RCP
47 WG
46 GNT
45 $\overline{CASEN}$
44 DTACK
43 $\overline{RAS}$
42 MA0
41 MA1
40 MA2
39 GND
38 GND
37 GND
36 MA3
35 MA4
34 MA5
33 MA6
32 MA7
31 MA8
30 MA9
29 CP
28 $\overline{SEL2}$
27 $\overline{REQ2}$
26 $\overline{REQ1}$
25 $\overline{SEL1}$
TOP VIEW
CD14500S


A Package
CA2 6
RA2 5
CA1 4
RA1 3
CA0 2
RA0 1
RCP 44
WG 43
GNT 42
$\overline{CASEN}$ 41
DTACK 40
RA_3 7
CA_3 8
RA_4 9
CA_4 10
V_{CC} 11
RA_5 12
CA_5 13
RA_6 14
CA_6 15
RA_7 16
CA_7 17
39 $\overline{RAS}$
38 MA_0
37 MA_1
36 MA_2
35 GND
34 GND
33 MA_3
32 MA_4
31 MA_5
30 MA_6
29 MA_7
18 RA8
19 CA8
20 RA9
21 CA9
22 $\overline{SEL1}$
23 $\overline{REQ1}$
24 $\overline{REQ2}$
25 $\overline{SEL2}$
26 CP
27 MA9
28 MA8
CD07451S

LOGIC SYMBOL


N Package
1 2 3 4 5 6 7 8 9 10 11 15 16 17 18 19 20 21 22 23 24
NC RA_0 CA_0 RA_1 CA_1 RA_2 CA_2 RA_3 CA_3 RA_4 CA_4 RA_5 CA_5 RA_6 CA_6 RA_7 CA_7 RA_8 CA_8 RA_9 CA_9
26 REQ1
27 REQ2
29 CP
48 RCP
SEL1 25
SEL2 28
RAS 43
DTACK 44
CASEN 45
GNT 46
WG 47
MA_0 MA_1 MA_2 MA_3 MA_4 MA_5 MA_6 MA_7 MA_8 MA_9
42 41 40 36 35 34 33 32 31 30
LS09262S

V_{CC} = Pin 12 – 14
GND = Pin 37 – 39

1 Megabit DRAM Dual-Ported Controllers

FAST 74F1764/1765, 74F1764-1/1765-1

PIN DESCRIPTION

SYMBOL	PINS		TYPE	NAME AND FUNCTION
	DIP	PLCC		
RA$_0$	2	1	I	Address inputs used to generate memory row address
RA$_1$	4	3	I	
RA$_2$	6	5	I	
RA$_3$	8	7	I	
RA$_4$	10	9	I	
RA$_5$	15	12	I	
RA$_6$	17	14	I	
RA$_7$	19	16	I	
RA$_8$	21	18	I	
RA$_9$	23	20	I	
CA$_0$	3	2	I	Address inputs used to generate memory column address
CA$_1$	5	4	I	
CA$_2$	7	6	I	
CA$_3$	9	8	I	
CA$_4$	11	10	I	
CA$_5$	16	13	I	
CA$_6$	18	15	I	
CA$_7$	20	17	I	
CA$_8$	22	19	I	
CA$_9$	24	21	I	
$\overline{REQ}_1$	26	23	I	Memory access request from Microprocessor 1
$\overline{REQ}_2$	27	24	I	Memory access request from Microprocessor 2
CP	29	26	I	Clock input which determines the master timing
RCP	48	44	I	Refresh clock determines the period of refresh for each row after it is internally divided by 64
$\overline{SEL}_1$	25	22	O	Select signal is activated in response to active $\overline{REQ}_1$ input, indicating selection of Microprocessor 1
V$_{CC}$	12 – 14	11		Power supply +5V± 10%
GND	37 – 39	34 35		Ground
$\overline{SEL}_2$	28	25	O	Select signal is activated in response to active $\overline{REQ}_2$ input, indicating selection of Microprocessor 2
MA$_0$	42	38	O	Memory address output pins, designed to drive address lines of the DRAM
MA$_1$	41	37	O	
MA$_2$	40	36	O	
MA$_3$	36	33	O	
MA$_4$	35	32	O	
MA$_5$	34	31	O	
MA$_6$	33	30	O	
MA$_7$	32	29	O	
MA$_8$	31	28	O	
MA$_9$	30	27	O	
GNT	46	42	O	Grant output, activated upon start of a memory access cycle
$\overline{RAS}$	43	39	O	Row address strobe, used to latch the row address into the bank of DRAM (to be connected directly to the $\overline{RAS}$ inputs of the DRAMs)
WG	47	43	O	Write Gate may be gated with the microprocessor's write strobe to perform an early write cycle
$\overline{CASEN}$	45	41	O	Column Address Strobe Enable is used to latch the column address into the bank of DRAMs
DTACK	44	40	O	Data Transfer Acknowledge indicates that data on the DRAM output lines is valid or the proper access time has been met

ARCHITECTURE

The 74F1764/1765 1 Megabit DRAM dual-ported controller is a synchronous device, with all signal generation being a function of the input clock (CP).

The 'F1764/1765 arbitration logic is divided into two stages. The first stage controls which one of the two $\overline{REQ}$ inputs will be serviced by activating the corresponding $\overline{SEL}$ output. This arbitration takes place irrespective of whether or not a refresh cycle is in progress. The arbitration is accomplished by sampling the $\overline{REQ}_1$ and $\overline{REQ}_2$ inputs on different edges of the CP clock. $\overline{REQ}_1$ is sampled on the rising edge and $\overline{REQ}_2$ on the falling edge (refer to Figures 1 – 4).

Therefore, if access to the DRAM is requested by both processors at the same time, the contention is automatically resolved. The internal flip-flops of the device used in the arbitration process have been chosen for their immunity to metastable conditions.

The second stage of arbitration selects between the selected processor and any internal refresh request. Refresh always has priority and is serviced immediately after the current cycle is completed (if needed). This arbitration stage also indicates the start of an access cycle by asserting the GNT output.

The Refresh Clock (RCP) input determines the period for each row. This clock may be held in the High state for external or no refresh applications. When used, a refresh request is internally generated every 64 RCP cycles. The refresh counter is incremented at the end of every refresh cycle, and provides the refresh address.

Since $\overline{SEL}$ outputs indicate which one of the two memory accessing devices has been selected to be serviced, these provide an indication of which processor's address bus should be asserted at the controller address inputs. A Data Transfer Acknowledge (DTACK) signal is generated by the timing logic and either this signal or GNT may be used with the $\overline{SEL}$ outputs to indicate the end or beginning of an access cycle for each processor.

FUNCTIONAL DESCRIPTION

As described earlier, the timing, arbitration, refresh and multiplexing functions provided by the controller are all derived from the CP input. The period of this clock should be set equal to:

(Tras (of the DRAM) + 16 – 5)/4 plus any system guard-band required.

For the F1764-1/1765-1 the CP clock input period should be equal to:

(Tras (of the DRAM) + 22 – 10)/4 plus any system guard-band required.

A microprocessor requests access to the DRAM by activating the appropriate $\overline{REQ}$ input. If a refresh cycle is not in process and the other request input is not active, the $\overline{SEL}$ output corresponding to the active $\overline{REQ}$ input will be asserted to indicate the selected processor. The GNT output then goes High to indicate the start of a memory access cycle. If however, a refresh cycle is in process, and there is only one active $\overline{REQ}$ input, the $\overline{SEL}$ output corresponding to the active input $\overline{REQ}$ will be asserted but the GNT output will not go High until after the completion of the refresh cycle (see Figures 10, 11 & 14, 15).

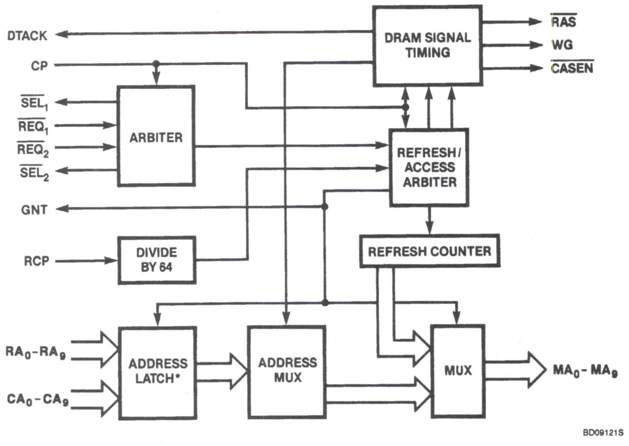
When the device is servicing a memory access cycle and a memory access is also requested by the other processor before the current cycle is completed, the $\overline{SEL}$ output for the other processor will not be issued, though GNT is asserted at that time, because the other processor is performing an access cycle. This will ensure that there is no contention on the address bus, i.e., the address bus is not driven by both processors at the same time.

Following the completion of the current memory access cycle, the $\overline{SEL}$ output corresponding to the awaiting $\overline{REQ}$ input will be asserted, followed by the GNT output. If however, there were any pending refresh requests, assertion of the GNT output will be held OFF until the refresh request has been serviced.

When GNT goes High, the $RA_0 - RA_9$ and $CA_0 - CA_9$ address input to the 'F1764/F1764-1 are latched internally and the $RA_0 - RA_9$ signals are propagated to the $MA_0 - MA_9$ outputs. The address inputs are not latched by the F1765/F1765-1 and therefore, $RA_0 - RA_9$ inputs propagate directly to the $MA_0 - MA_9$ outputs.

A half-clock cycle is allowed for the address signals to propagate through to the outputs, after which the $\overline{RAS}$ output is asserted.

BLOCK DIAGRAM



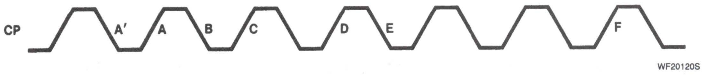
NOTE:
* The address input latch is available only on the 74F1764/F1764-1.

One clock cycle later, the $CA_0 - CA_9$ latch outputs on the 'F1764 or $CA_0 - CA_9$ inputs to the 'F1765 are selected and propagated to the $MA_0 - MA_9$ outputs. This occurs half a clock cycle earlier on the F1764-1/1765-1 (refer to Figures 3 & 4). The Write Gate (WG) output becomes valid at this time to indicate the proper time to gate the Write signal from the selected processor to the DRAM to perform an Early Write cycle.

A half-clock cycle is again allowed for the $CA_0 - CA_9$ signals to propagate and stabilize. $\overline{\text{CASEN}}$ then becomes valid. $\overline{\text{CASEN}}$ can be used as $\overline{\text{CAS}}$ output or decoded with Higher-order address signals to produce multiple $\overline{\text{CAS}}$ signals. After $\overline{\text{CASEN}}$ is valid, the controller will wait for $2\frac{1}{2}$ clock cycles before negating $\overline{\text{RAS}}$, making a total $\overline{\text{RAS}}$ pulse width of approximately 4 clock cycles. Since this width matches the standard DRAM access time, the controller next asserts DTACK output, indicating that valid data is on the DRAM data lines or that a memory access cycle is complete. DTACK may be used to assert valid data transfer acknowledge for processors requiring this signal (i.e., the 68000 family of processors).

All controller output signals are held in this final state until the selected processor withdraws its request by driving its $\overline{\text{REQ}}$ input High. When the request is withdrawn, internal synchronization takes place, the controller output signals become inactive, and any pending memory access or refresh cycles are serviced.

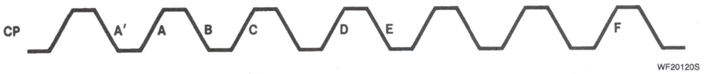
A refresh cycle is serviced by propagating the 10 refresh counter address signals to the $MA_0 - MA_9$ outputs. After a half-clock cycle the $\overline{\text{RAS}}$ output is asserted for four cycles and then negated for three clock cycles to meet the $\overline{\text{RAS}}$ precharge requirements of the DRAMs (see Figures 5 & 6).



A'	$\overline{\text{REQ}}_2$ sampled
A	$\overline{\text{REQ}}_1$ sampled $\overline{\text{SEL}}_1$ triggered ($\overline{\text{SEL}}_1$ triggered by $\overline{\text{REQ}}_1$ sample circuitry) ($\overline{\text{REQ}}_2$ disabled by $\overline{\text{SEL}}_1$ circuitry)
B	GNT triggered $RA_0 - RA_9$ and $CA_0 - CA_9$ latched (Input address latch triggered by GNT circuitry)* $RA_0 - RA_9$ propagate to $MA_0 - MA_9$ outputs
C	$\overline{\text{RAS}}$ triggered
D	WG triggered $CA_0 - CA_9$ selected and propagated to $MA_0 - MA_9$ outputs
E	$\overline{\text{CASEN}}$ triggered
F	$\overline{\text{RAS}}$ negated DTACK triggered

* Only on the 'F1764.

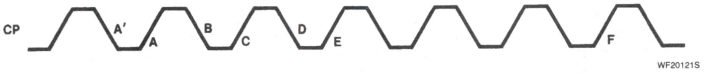
Figure 1. Sequence of Events for $\overline{\text{REQ}}_1$ Memory Access Cycle for F1764/1765



A'	$\overline{\text{REQ}}_2$ sampled $\overline{\text{SEL}}_2$ triggered ($\overline{\text{SEL}}_2$ triggered by $\overline{\text{REQ}}_2$ sampling circuitry)
A	$\overline{\text{REQ}}_1$ is not sampled (disabled by $\overline{\text{SEL}}_2$ circuitry)
B	GNT triggered $RA_0 - RA_9$ and $CA_0 - CA_9$ latched (Input address latch triggered by GNT circuitry)* $RA_0 - RA_9$ propagate to $MA_0 - MA_9$ outputs
C	$\overline{\text{RAS}}$ triggered
D	WG triggered $CA_0 - CA_9$ selected and propagated to $MA_0 - MA_9$ outputs
E	$\overline{\text{CASEN}}$ triggered
F	$\overline{\text{RAS}}$ negated DTACK triggered

* Only on the 'F1764.

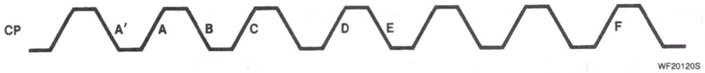
Figure 2. Sequence of Events for $\overline{\text{REQ}}_2$ Memory Access Cycle for F1764/1765



A'	$\overline{REQ}_2$ sampled
A	$\overline{REQ}_1$ sampled $\overline{SEL}_1$ triggered ($\overline{SEL}_1$ triggered by $\overline{REQ}_1$ sample circuitry) ($\overline{REQ}_2$ disabled by $\overline{SEL}_1$ circuitry)
B	GNT triggered $RA_0 - RA_9$ and $CA_0 - CA_9$ latched (Input address latch triggered by GNT circuitry)* $RA_0 - RA_9$ propagate to $MA_0 - MA_9$ outputs
C	$\overline{RAS}$ triggered
D	WG triggered $CA_0 - CA_9$ selected and propagated to $MA_0 - MA_9$ outputs
E	$\overline{CASEN}$ triggered
F	$\overline{RAS}$ negated DTACK triggered

* Only on the F1764-1.

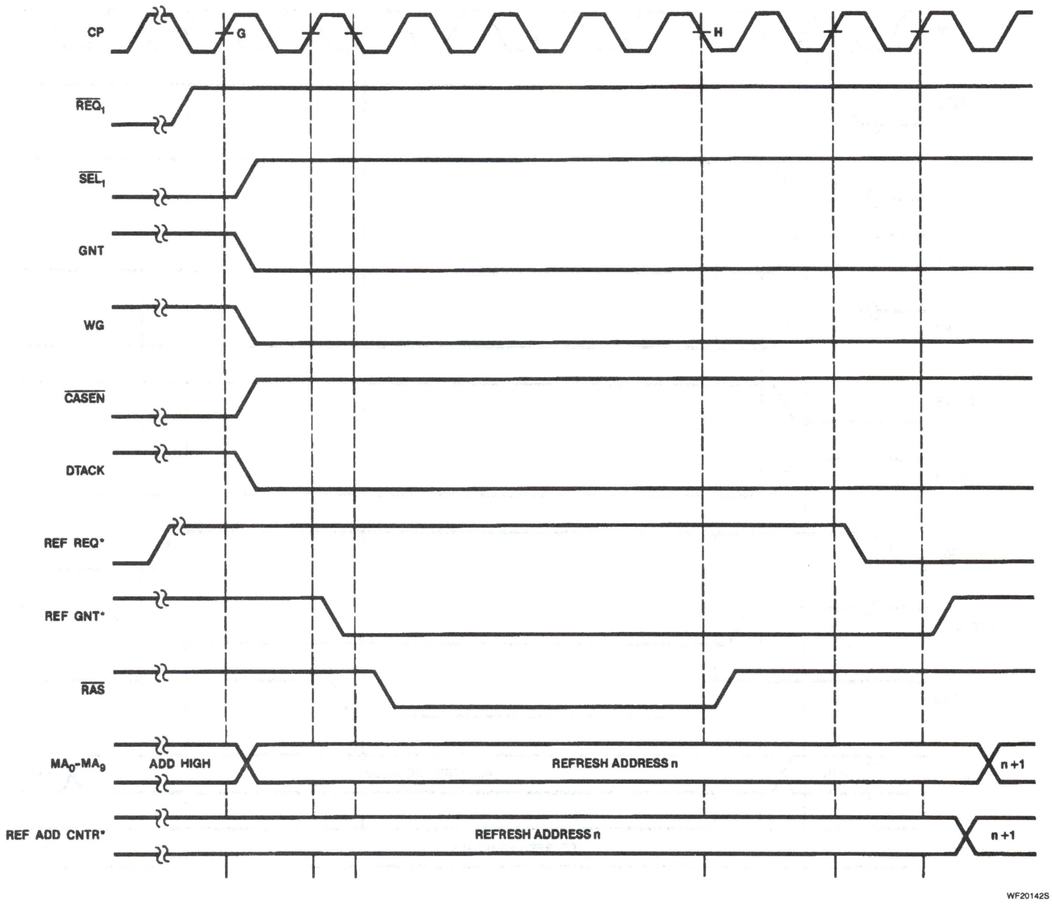
Figure 3. Sequence of Events for $\overline{REQ}_1$ Memory Access Cycle for F1764-1/1765-1



A'	$\overline{REQ}_2$ sampled $\overline{SEL}_2$ triggered ($\overline{SEL}_2$ triggered by $\overline{REQ}_2$ sampling circuitry)
A	$\overline{REQ}_1$ is not sampled (disabled by $\overline{SEL}_2$ circuitry)
B	GNT triggered $RA_0 - RA_9$ and $CA_0 - CA_9$ latched (Input address latch triggered by GNT circuitry)* $RA_0 - RA_9$ propagate to $MA_0 - MA_9$ outputs
C	$\overline{RAS}$ triggered
D	WG triggered $CA_0 - CA_9$ selected and propagated to $MA_0 - MA_9$ outputs
E	$\overline{CASEN}$ triggered
F	$\overline{RAS}$ negated DTACK triggered

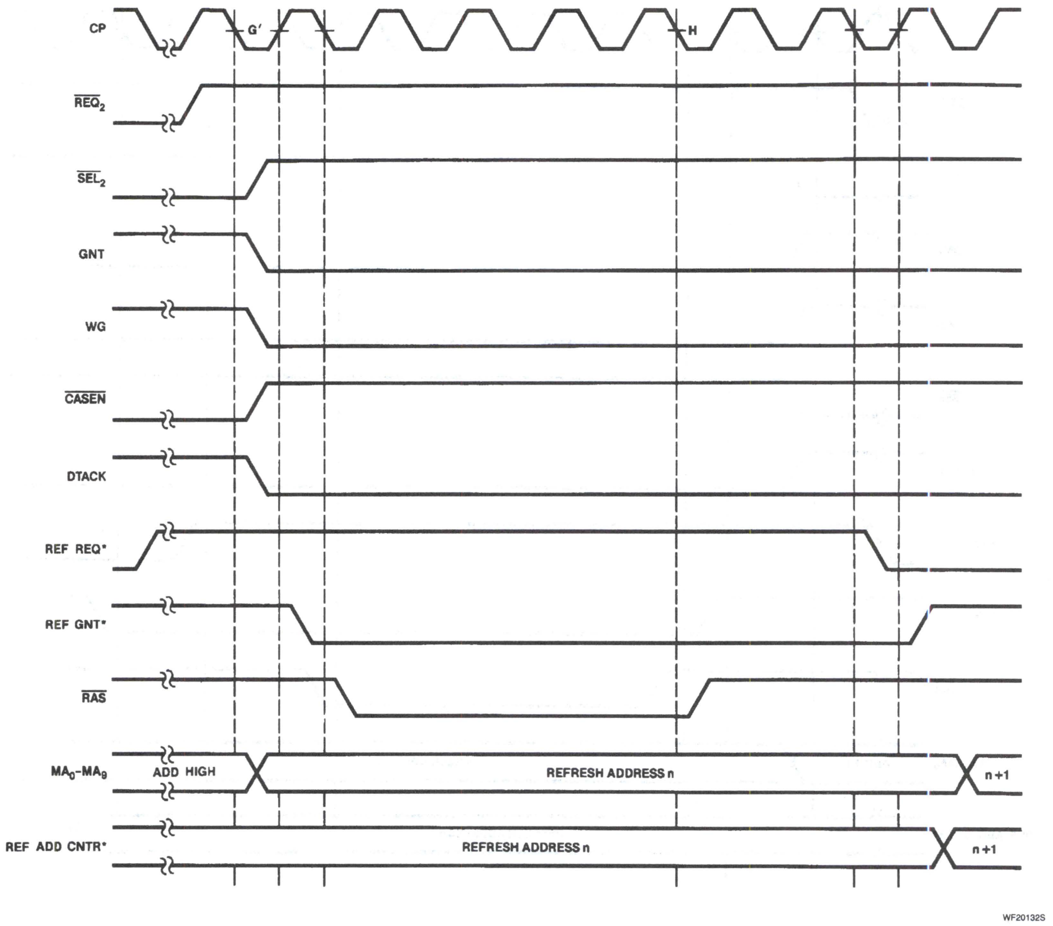
* Only on the F1764-1.

Figure 4. Sequence of Events for $\overline{REQ}_2$ Memory Access Cycle for F1764-1/1765-1


CP
G
H
$\overline{REQ_1}$
$\overline{SEL_1}$
GNT
WG
$\overline{CASEN}$
DTACK
REF REQ*
REF GNT*
$\overline{RAS}$
MA_0-MA_9
ADD HIGH
REFRESH ADDRESS n
n+1
REF ADD CNTR*
REFRESH ADDRESS n
n+1
WF20142S

NOTE:
* These are internal signals only.

Figure 5. Refresh Cycle Timing Following a $\overline{REQ_1}$ Memory Access Cycle


CP
G′
H
$\overline{REQ_2}$
$\overline{SEL_2}$
GNT
WG
$\overline{CASEN}$
DTACK
REF REQ*
REF GNT*
$\overline{RAS}$
MA_0-MA_9
ADD HIGH
REFRESH ADDRESS n
n+1
REF ADD CNTR*
REFRESH ADDRESS n
n+1
WF20132S

NOTE:
* These are internal signals only.

Figure 6. Refresh Cycle Timing Following a $\overline{REQ_2}$ Memory Access Cycle

1 Megabit DRAM Dual-Ported Controllers

FAST 74F1764/1765, 74F1764-1/1765-1

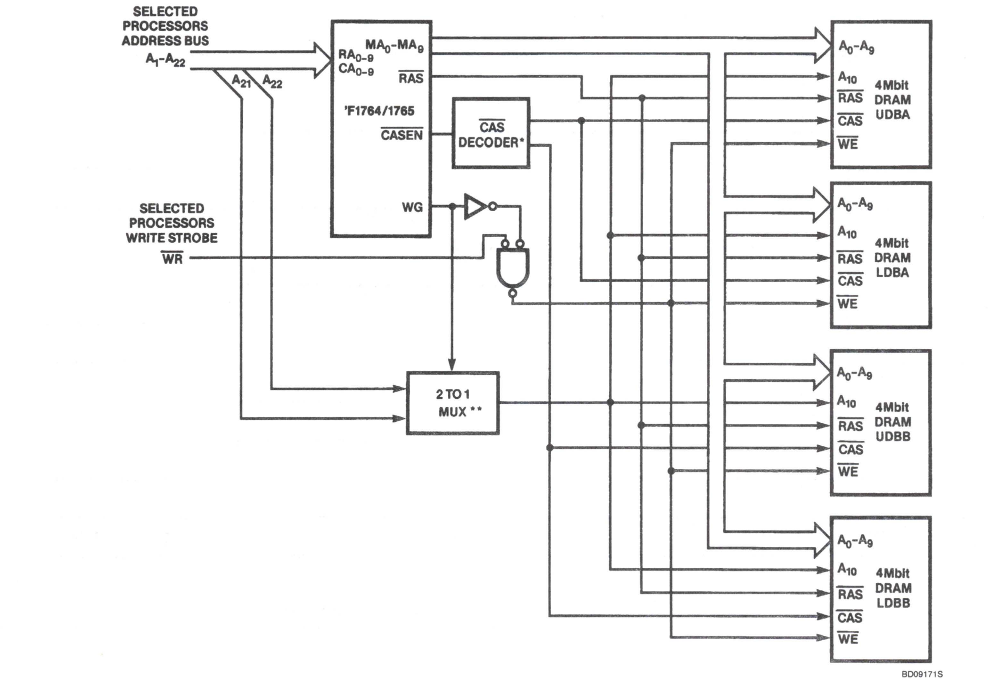
USING 74F1764/1765 AND 74F1764-1/1765-1 TO ADDRESS 4MBIT DRAMS

The addressing capabilities of the 1 Megabit DRAM dual-ported controllers can be extended to address 4Mbit (or greater) DRAMs by using an external multiplexer to multiplex additional address bits.

Figure 7 shows an application, using an external 2-to-1 multiplexer to address 4Mbit dynamic RAMs. The 10-bit internal refresh counter of the controller provides 1024 row addresses which more than meet the refreshing needs for most industry standard 4Mbit DRAMs. Therefore, it is unnecessary to provide for any additional refresh address bits for DRAMs with up to 1024 rows.

Additional address bits (for larger DRAMs) may also be multiplexed externally as long as the DRAM refreshing requirements do not exceed 1024 row addresses.

The WG output of the controller should be used to multiplex between the external row and column addresses. However it is important that the propagation delay through the external multiplexer does not cause column address setup violations on the dynamic RAM.


SELECTED PROCESSORS ADDRESS BUS
A_1-A_{22}
A_{21}
A_{22}
RA_{0-9}
CA_{0-9}
MA_0-MA_9
$\overline{RAS}$
'F1764/1765
$\overline{CASEN}$
$\overline{CAS}$ DECODER*
WG
SELECTED PROCESSORS WRITE STROBE
$\overline{WR}$
2 TO 1 MUX **
A_0-A_9
A_{10}
$\overline{RAS}$
$\overline{CAS}$
$\overline{WE}$
4Mbit DRAM UDBA
4Mbit DRAM LDBA
4Mbit DRAM UDBB
4Mbit DRAM LDBB
BD09171S

NOTES:

* The $\overline{CAS}$ decode logic is not necessary if multiple $\overline{CAS}$ signals are not required. The application also does not show further decoding of multiple $\overline{CAS}$ signals to distinguish between Upper and Lower data bytes. If required, multiple $\overline{CAS}$ signal generation and Upper and Lower byte decoding can be accomplished as shown in Figures 16 – 18.

** Propagation delay through the multiplexer should be considered when using the controller for 4Mbit addressing.

Figure 7. Using the Controller to Address 1Mbit DRAMs

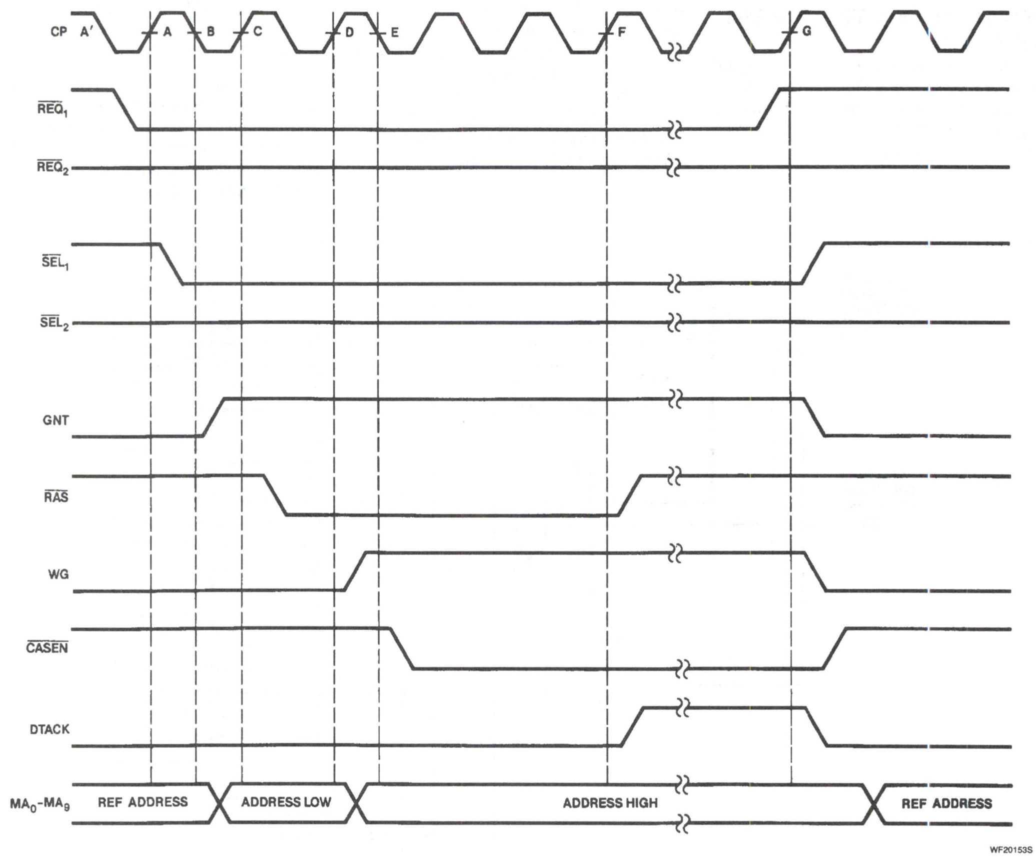

CP
A′
A
B
C
D
E
F
G
$\overline{REQ}_1$
$\overline{REQ}_2$
$\overline{SEL}_1$
$\overline{SEL}_2$
GNT
$\overline{RAS}$
WG
$\overline{CASEN}$
DTACK
MA_0-MA_9
REF ADDRESS
ADDRESS LOW
ADDRESS HIGH
REF ADDRESS
WF20153S

Figure 8. Request 1 ($\overline{REQ}_1$) Memory Access Cycle Timing for F1764/1765

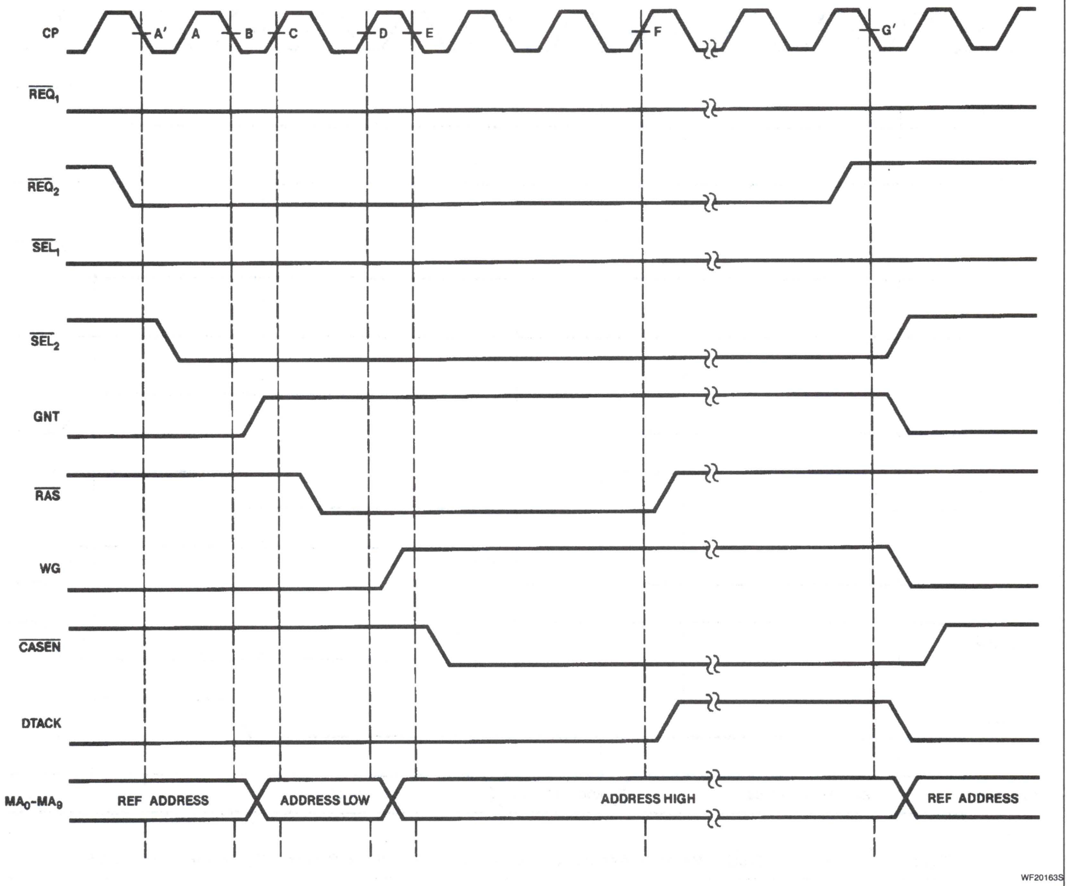

CP
A'
A
B
C
D
E
F
G'
$\overline{REQ_1}$
$\overline{REQ_2}$
$\overline{SEL_1}$
$\overline{SEL_2}$
GNT
$\overline{RAS}$
WG
$\overline{CASEN}$
DTACK
MA_0-MA_9
REF ADDRESS
ADDRESS LOW
ADDRESS HIGH
REF ADDRESS
WF20163S

Figure 9. Request 2 ($\overline{REQ_2}$) Memory Access Cycle Timing for F1764/1765

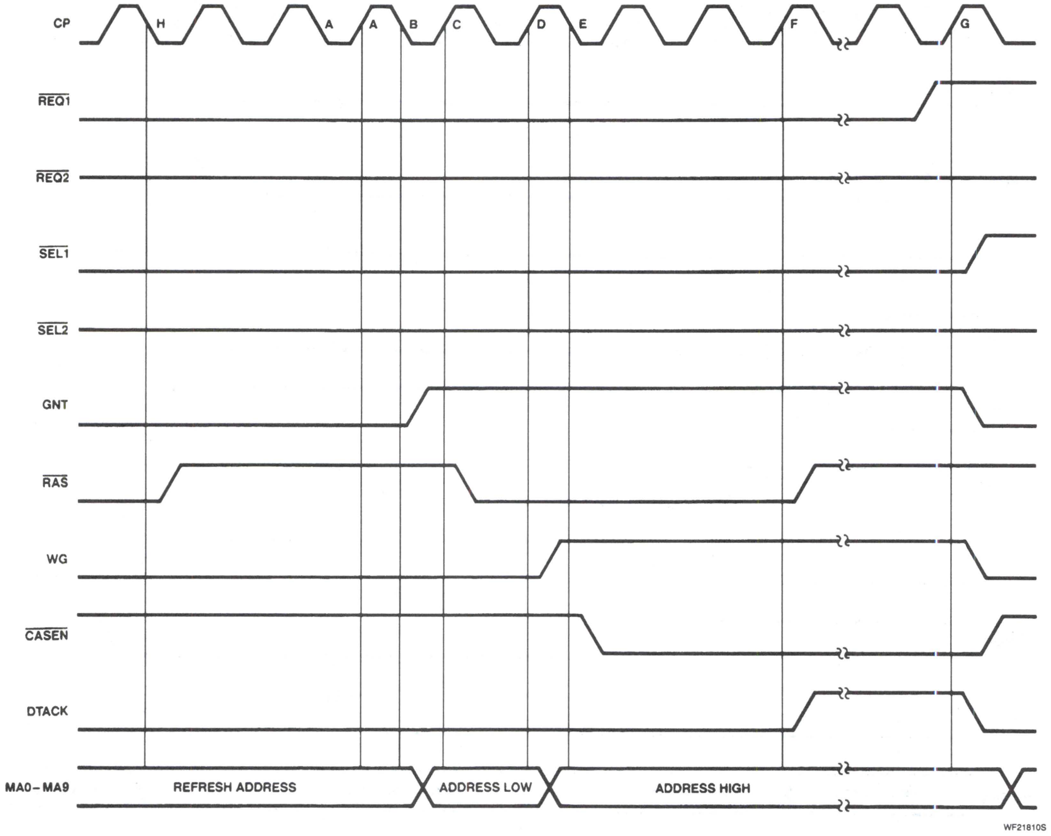

CP
H
A
A
B
C
D
E
F
G
$\overline{REQ1}$
$\overline{REQ2}$
$\overline{SEL1}$
$\overline{SEL2}$
GNT
$\overline{RAS}$
WG
$\overline{CASEN}$
DTACK
MA0 – MA9
REFRESH ADDRESS
ADDRESS LOW
ADDRESS HIGH
WF21810S

Figure 10. Request 1 ($\overline{REQ_1}$) Memory Access Cycle Timing Following a Refresh Cycle for F1764/1765

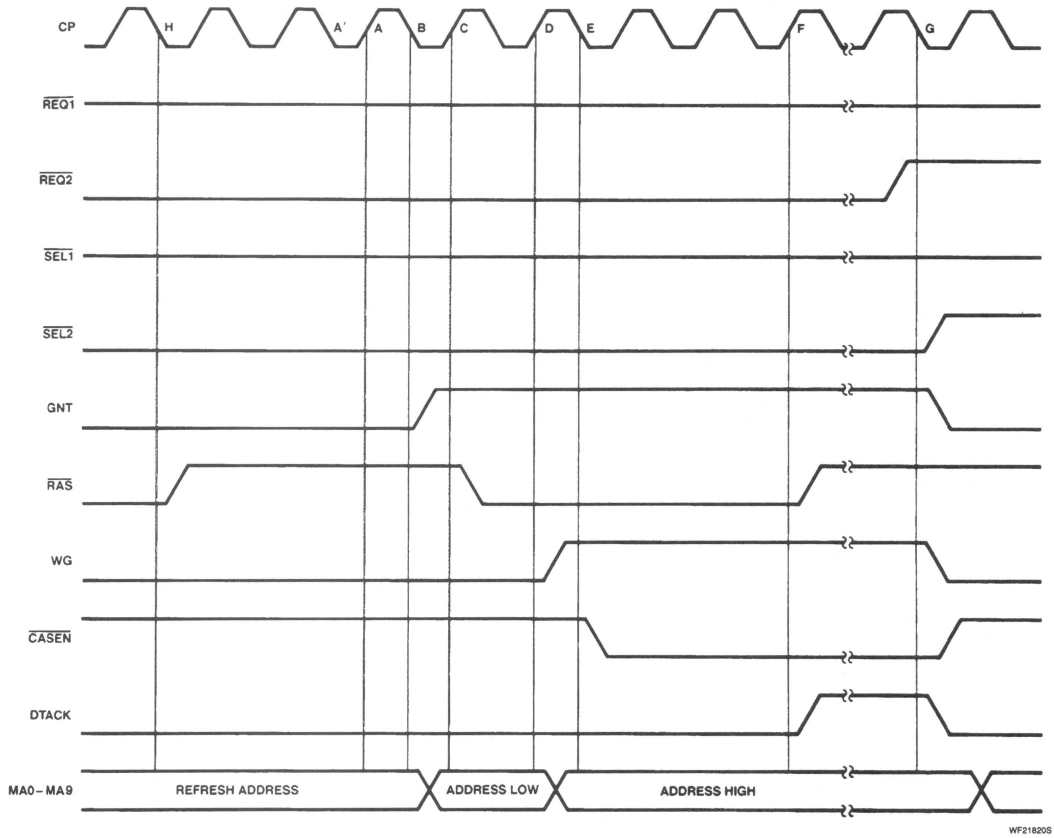

CP
H
A′
A
B
C
D
E
F
G
$\overline{REQ1}$
$\overline{REQ2}$
$\overline{SEL1}$
$\overline{SEL2}$
GNT
$\overline{RAS}$
WG
$\overline{CASEN}$
DTACK
MA0 – MA9
REFRESH ADDRESS
ADDRESS LOW
ADDRESS HIGH
WF21820S

Figure 11. Request 2 ($\overline{REQ_2}$) Memory Access Cycle Timing Following a Refresh Cycle for F1764/1765

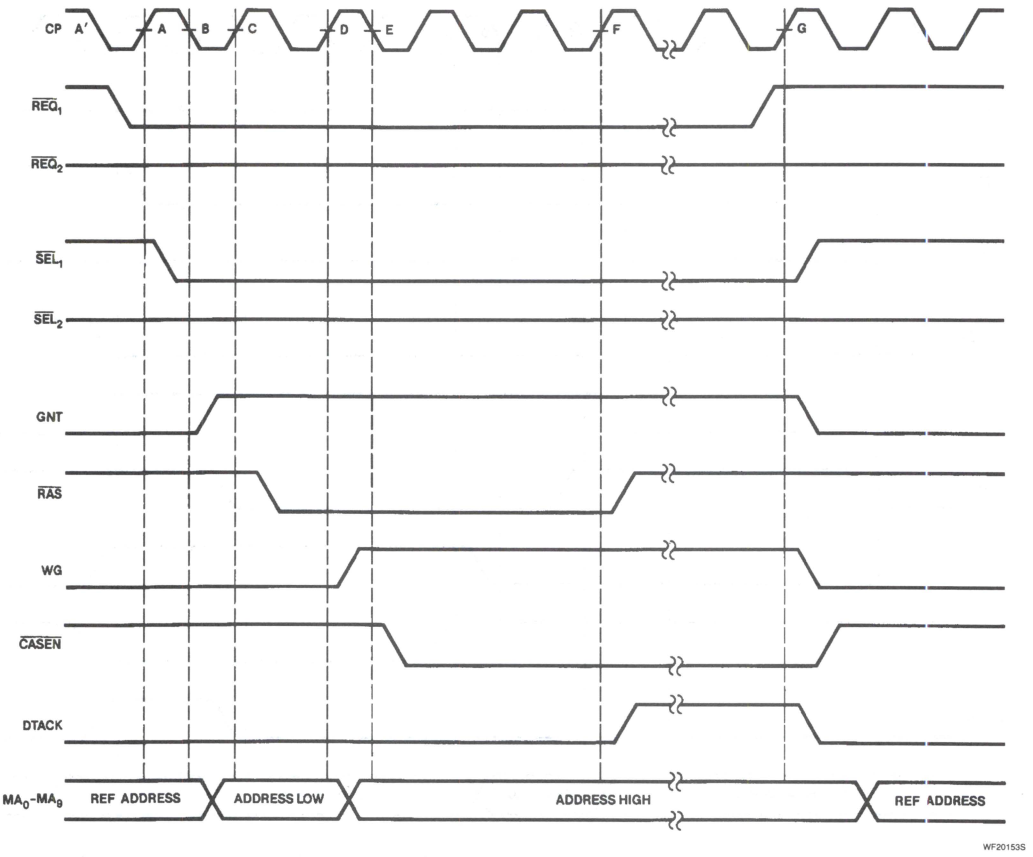

CP
A'
A
B
C
D
E
F
G
$\overline{REQ_1}$
$\overline{REQ_2}$
$\overline{SEL_1}$
$\overline{SEL_2}$
GNT
$\overline{RAS}$
WG
$\overline{CASEN}$
DTACK
MA_0-MA_9
REF ADDRESS
ADDRESS LOW
ADDRESS HIGH
REF ADDRESS
WF20153S

Figure 12. Request 1 ($\overline{REQ_1}$) Memory Access Cycle Timing for F1764-1/1765-1

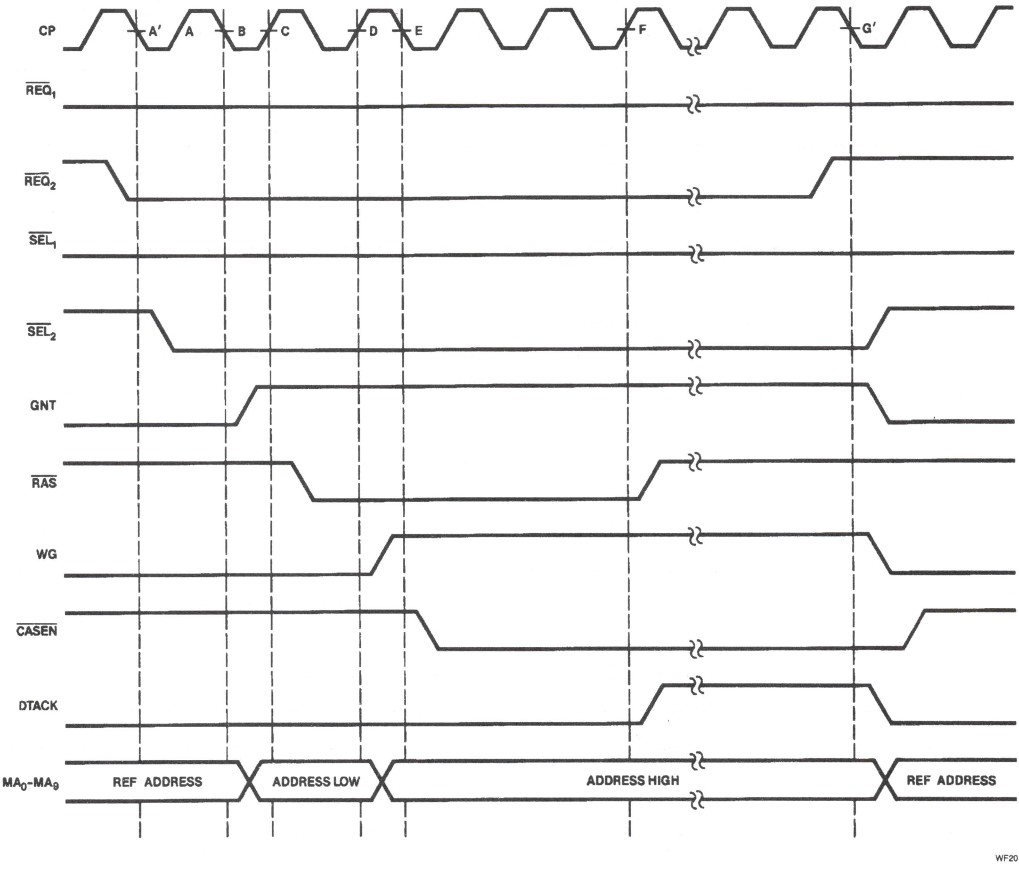

CP
A'
A
B
C
D
E
F
G'
$\overline{REQ_1}$
$\overline{REQ_2}$
$\overline{SEL_1}$
$\overline{SEL_2}$
GNT
$\overline{RAS}$
WG
$\overline{CASEN}$
DTACK
MA_0-MA_9
REF ADDRESS
ADDRESS LOW
ADDRESS HIGH
REF ADDRESS
WF20163S

Figure 13. Request 2 ($\overline{REQ_2}$) Memory Access Cycle Timing for F1764-1/1765-1

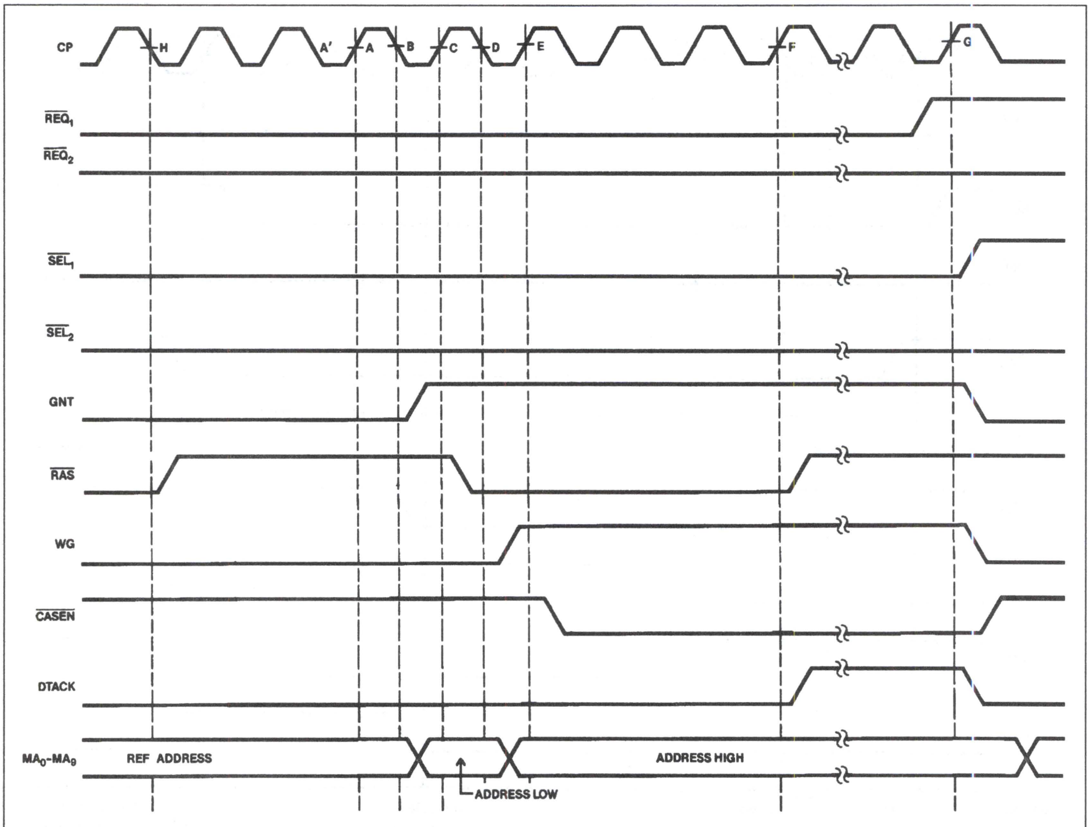

CP
H
A'
A
B
C
D
E
F
G
REQ1
REQ2
SEL1
SEL2
GNT
RAS
WG
CASEN
DTACK
MA0-MA9
REF ADDRESS
ADDRESS HIGH
ADDRESS LOW
WF20166S

Figure 14. Request 1 ($\overline{REQ}_1$) Memory Access Cycle Timing Following a Refresh Cycle for F1764-1/1765-1

1 Megabit DRAM Dual-Ported Controllers

FAST 74F1764/1765, 74F1764-1/1765-1

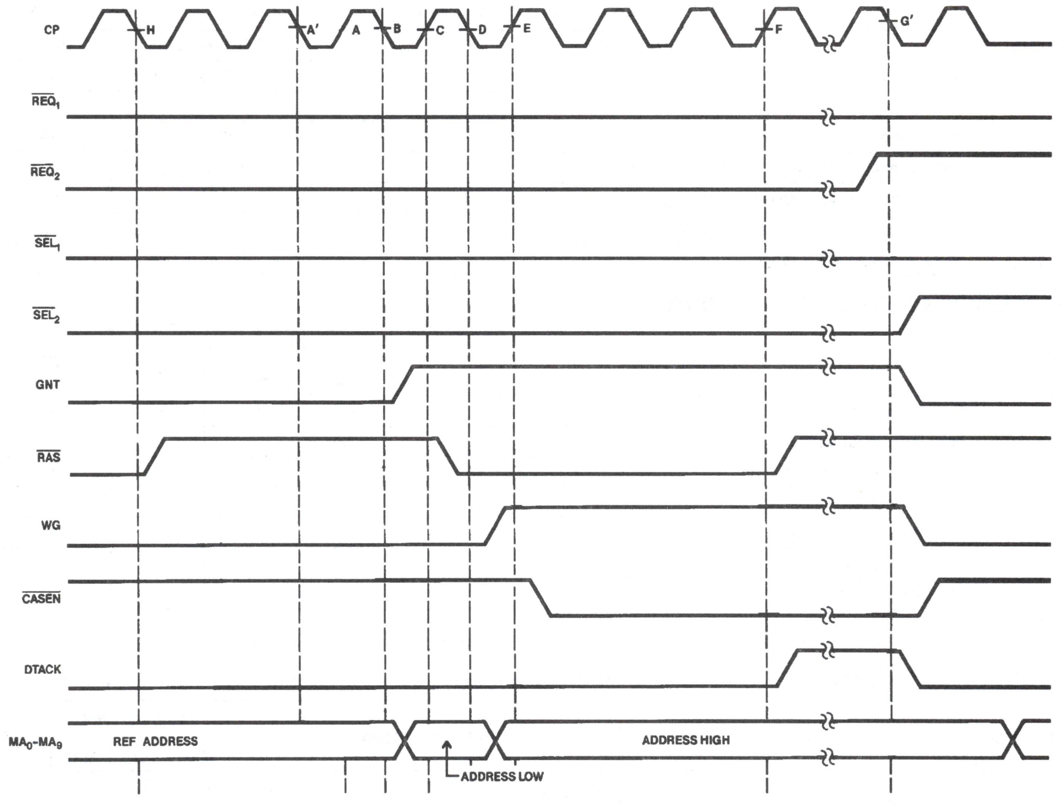

CP
H
A'
A
B
C
D
E
F
G'
REQ1
REQ2
SEL1
SEL2
GNT
RAS
WG
CASEN
DTACK
MA0-MA9
REF ADDRESS
ADDRESS HIGH
ADDRESS LOW
WF20165S

Figure 15. Request 2 ($\overline{REQ_2}$) Memory Access Cycle Timing Following a Refresh Cycle for F1764-1/1765-1

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range).

SYMBOL	PARAMETER	74F1764/1765	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	500	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature range	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74F1764/1765			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current[1]			−15	mA
I_{OL}	Low-level output current[1]			24	mA
T_A	Operating free-air temperature	0		70	°C

NOTE:

1. Transient currents will exceed these values in actual operation. Please refer to Appendix A for a detailed discussion.

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]			74F1764/1765			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	$I_{OH} = -15mA$	±10%V_{CC}	2.5	3.2		V
				±5%V_{CC}	2.7	3.4		V
V_{OH2}[3]	High-level output voltage		I_{OH2}[3] = −35mA	±5%V_{CC}	2.4			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 24mA	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{OL2}[4]	Low-level output voltage		I_{OL2}[4] = 60mA	±5%V_{CC}		0.45	0.80	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, $I_I = I_{IK}$				−0.73	−1.2	V
I_I	Input current at maximum input voltage	V_{CC} = 0.0V, V_I = 7.0V					100	μA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V					−0.6	mA
I_{OS}	Short-circuit output current[5]	V_{CC} = MAX			−100		−225	mA
I_{CC}	Supply current (total) I_{CCH}	V_{CC} = MAX				150	200	mA
	I_{CCL}					165	210	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value under the recommended operating conditions for the applicable conditions.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Refer to Appendix A.
4. Refer to Appendix A.
5. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well over the normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER[1]	74F1764/1765					UNIT
		$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 300pF$ $R_L = 70\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 300pF$ $R_L = 70\Omega$		
		Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	100	150		100		MHz
t_{PLH}	Propagation delay CP(G) to $\overline{SEL}_1$	5	10	14	5	16	ns
t_{PHL}	Propagation delay CP(A) to $\overline{SEL}_1$	5	10	14	5	16	ns
t_{PLH}	Propagation delay CP(G′) to $\overline{SEL}_2$	5	10	14	5	16	ns
t_{PHL}	Propagation delay CP(A′) to $\overline{SEL}_2$	5	10	14	5	16	ns
t_{PLH}	Propagation delay CP(B) to GNT	5	10	14	5	16	ns
t_{PHL}	Propagation delay CP(G or G′) to GNT	5	10	15	5	16	ns
t_{PLH} t_{PHL}	Propagation delay CP(B) to MA(row address)	5 5	12 11	17 15	5 5	18 16	ns
t_{PLH}	Propagation delay CP(F or H) to $\overline{RAS}$	5	10	14	5	16	ns
t_{PHL}	Propagation delay CP(C) to $\overline{RAS}$	5	10	14	5	16	ns
t_{PLH}	Propagation delay CP(D) to WG	5	10	14	5	16	ns
t_{PHL}	Propagation delay CP(G or G′) to WG	8	13	17	8	18	ns
t_{PLH} t_{PHL}	Propagation delay CP(D) to MA(column address)	5 5	12 10	17 15	5 5	18 16	ns
t_{PLH}	Propagation delay CP(G or G′) to $\overline{CASEN}$	7	17	23	7	25	ns
t_{PHL}	Propagation delay CP(E) to $\overline{CASEN}$	5	10	14	5	16	ns
t_{PLH}	Propagation delay CP(F) to DTACK	5	10	14	5	16	ns
t_{PHL}	Propagation delay CP(G or G′) to DTACK	6	13	17	5	18	ns
74F1765 Only							
t_{PLH} t_{PHL}	Propagation delay RA_0-RA_9, CA_0-CA_9 to MA_0-MA_9	4 2	7 5	12 8	4 4	13 9	ns

NOTE:
1. For test conditions, see the AC waveforms.

AC SETUP AND HOLD REQUIREMENTS

SYMBOL	PARAMETER[2]	74F1764/1765					UNIT
		$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 300pF$ $R_L = 70\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 300pF$ $R_L = 70\Omega$		
		Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{REQ}_1$, $\overline{REQ}_2$ to CP	2 2			2 2		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low CP to $\overline{REQ}_1$, $\overline{REQ}_2$	2 2			3 3		ns
$t_w(H)$ $t_w(L)$	CP pulse width High or Low	5 5			5 5		ns
$t_w(H)$ $t_w(L)$	RCP pulse width High or Low	10 10			10 10		ns
74F1764 Only							
$t_s(H)$ $t_s(L)$	Setup time, High or Low RA_0-RA_9, CA_0-CA_9 to CP(↓)	−4[1] −4			−5 −5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low CP(↓) to RA_0-RA_9, CA_0-CA_9	5 5			5 5		ns

NOTES:
1. These numbers indicate that the address inputs have a negative setup time and could be valid 4ns after the falling edge of the CP clock. It is suggested that $\overline{SEL}_2$ be used to enable Address Bus 2 and the opposite polarity of the same be used, instead of $\overline{SEL}_1$ to enable Address Bus 1. This will insure that setup time for Address Bus 1 is not violated.
2. For the test conditions, see the AC waveforms.

1 Megabit DRAM Dual-Ported Controllers

FAST 74F1764/1765, 74F1764-1/1765-1

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range).

SYMBOL	PARAMETER	74F1764-1/1765-1	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	500	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature range	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74F1764-1/1765-1			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current[1]			−20	mA
I_{OL}	Low-level output current[1]			8	mA
T_A	Operating free-air temperature	0		70	°C

NOTE:

1. Transient currents will exceed these values in actual operation. Please refer to Appendix A for a detailed discussion.

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			74F1764-1/1765-1			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = −20mA	±10%V_{CC}	2.4	2.7		V
					±5%V_{CC}	2.6	3.0		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 8mA	±10%V_{CC}		0.30	0.50	V
					±5%V_{CC}		0.30	0.50	V
V_{OL2}[3]	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL2}[3] = 75mA	±5%V_{CC}		2.1	2.5	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$				−0.7	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = 0.0V, V_I = 7.0V					100	μA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				−0.2	−0.6	mA
I_{OS}	Short-circuit output current[4]		V_{CC} = MAX			−80	−150	−225	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				120	165	mA
		I_{CCL}					125	170	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value under the recommended operating conditions for the applicable conditions.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Refer to Appendix A.
4. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well over normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	74F1764-1/1765-1					UNIT
		$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 300pF$ $R_L = 70\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 300pF$ $R_L = 70\Omega$		
		Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	150	175		100		MHz
t_{PLH}	Propagation delay CP(G) to $\overline{SEL}_1$	9	12	15	8	17	ns
t_{PHL}	Propagation delay CP(A) to $\overline{SEL}_1$	13	16	20	12	22	ns
t_{PLH}	Propagation delay CP(G′) to $\overline{SEL}_2$	9	12	15	8	17	ns
t_{PHL}	Propagation delay CP(A′) to $\overline{SEL}_2$	13	16	20	12	22	ns
t_{PLH}	Propagation delay CP(B) to GNT	9	12	14	8	16	ns
t_{PHL}	Propagation delay CP(G or G′) to GNT	20	23	26	17	28	ns
t_{PLH} t_{PHL}	Propagation delay CP(B) to MA(row address)	11 14	14 18	17 22	10 13	19 24	ns
t_{PLH}	Propagation delay CP(F or H) to $\overline{RAS}$	11	14	16	10	18	ns
t_{PHL}	Propagation delay CP(C) to $\overline{RAS}$	13	17	20	12	22	ns
t_{PLH}	Propagation delay CP(D) to WG	9	11	14	8	16	ns
t_{PHL}	Propagation delay CP(G or G′) to WG	20	23	26	19	26	ns
t_{PLH} t_{PHL}	Propagation delay CP(D) to MA(column address)	12 14	14 18	17 21	11 13	19 23	ns
t_{PLH}	Propagation delay CP(G or G′) to $\overline{CASEN}$	14	17	20	12	22	ns
t_{PHL}	Propagation delay CP(E) to $\overline{CASEN}$	14	16	19	13	21	ns
t_{PLH}	Propagation delay CP(F) to DTACK	10	12	15	9	17	ns
t_{PHL}	Propagation delay CP(G or G′) to DTACK	20	23	26	19	28	ns
74F1765-1 Only							
t_{PLH} t_{PHL}	Propagation delay $RA_0 - RA_9$, $CA_0 - CA_9$ to $MA_0 - MA_9$	9 9	11 12	14 15	8 8	16 17	ns

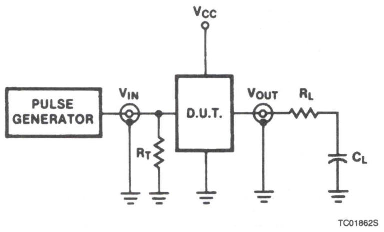
AC SETUP AND HOLD REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	74F1764-1/1765-1					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 300pF$ $R_L = 70\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 300pF$ $R_L = 70\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{REQ}_1$, $\overline{REQ}_2$ to CP	AC Waveforms	3	1		4		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low CP to $\overline{REQ}_1$, $\overline{REQ}_2$		2	0		3		ns
$t_w(H)$ $t_w(L)$	CP pulse width High or Low		5	3		5		ns
$t_w(H)$ $t_w(L)$	RCP pulse width High or Low		5			5		ns
74F1764-1 Only								
$t_s(H)$ $t_s(L)$	Setup time, High or Low $RA_0 - RA_9$, $CA_0 - CA_9$ to CP(↓)	AC Waveforms	0	−1[1]		1		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low CP(↓) to $RA_0 - RA_9$, $CA_0 - CA_9$		5	3		6		ns

NOTE:

1. These numbers indicate that the address inputs have a negative setup time and could be valid 1ns after the falling edge of the CP clock. It is suggested that $\overline{SEL}_2$ be used to enable Address Bus 2 and the opposite polarity of the same be used, instead of $\overline{SEL}_1$ to enable Address Bus 1. This will insure that setup time for Address Bus 1 is not violated.

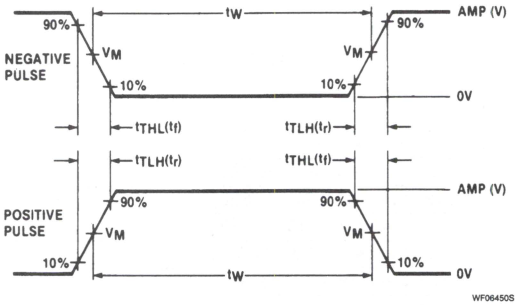
TEST CIRCUIT AND WAVEFORMS



Test Circuit Simulating RAM Boards

DEFINITIONS

R_L = Load resistor to GND; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

APPLICATIONS

The 1 Megabit DRAM dual-ported controller can be designed into a wide range of single and dual-port interface configurations. The processors could be general or special-purpose (microcontrollers) and the data bus may differ in size.

Figure 16 shows two 68000 processors sharing a 4Meg × 8 (two banks each consisting of sixteen 1Meg × 1 devices) memory. Since the 68000 does not have a multiplexed address and data bus, the 'F1765/F1765-1 is appropriate.

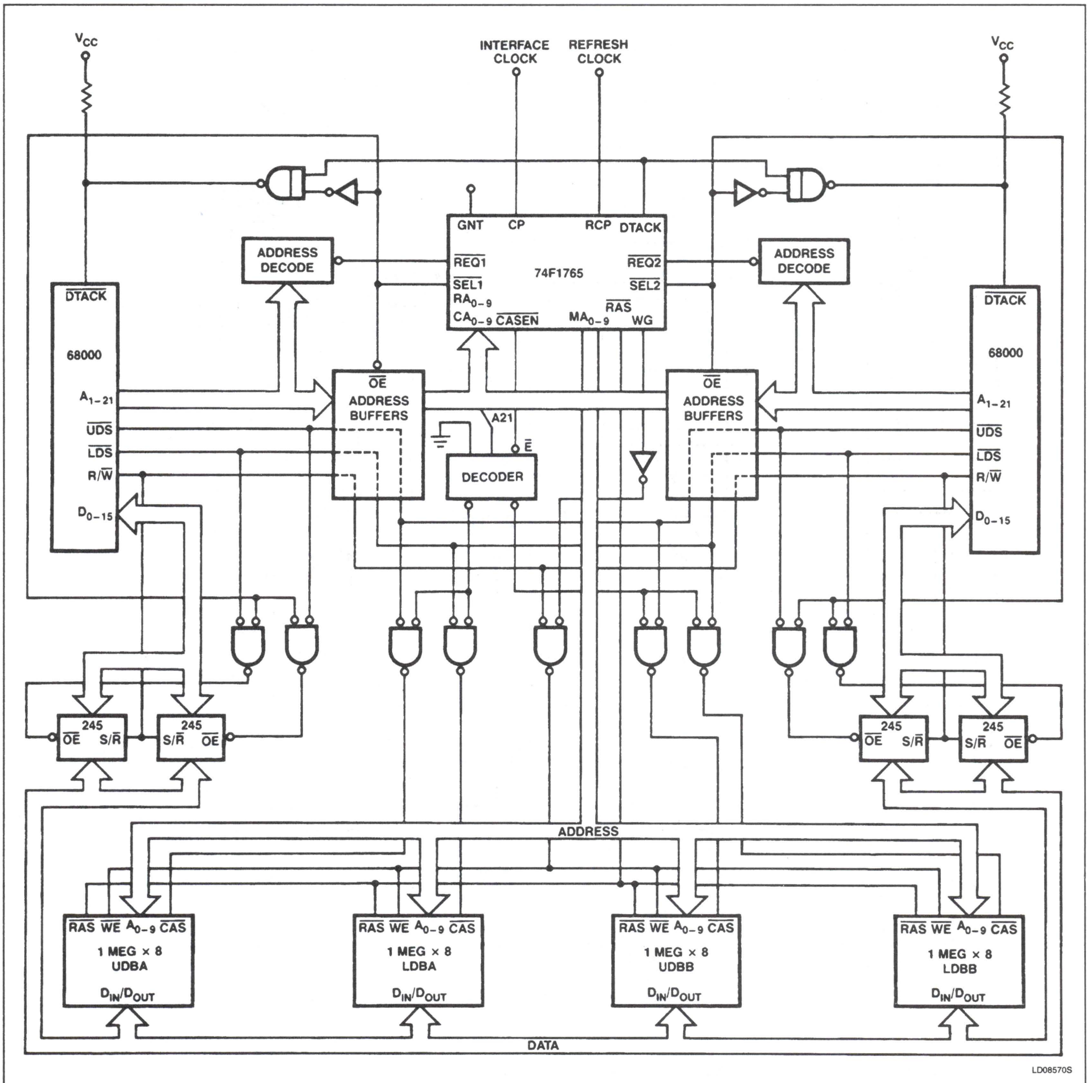
Address bit (A_{21}) from either of the two 68000 processors distinguishes between Memory Banks A and B. Where Bank A consists of Upper Data Byte A (UDBA) and Lower Data Byte A (LDBA) and Bank B consists of Upper Data Byte B (UDBB) and Lower Data Byte B (LDBB).

Upper and Lower Data Strobes ($\overline{\text{UDS}}$ and $\overline{\text{LDS}}$) from either of the two 68000 determine processors determine whether a byte or word transfer will take place. The additional circuitry is to ensure that $\overline{\text{DTACK}}$ to the 68000 is asserted only when it is selected.

Figure 17 shows two 8086 processors sharing 1MByte (two banks each consisting of sixteen 256K × 1 devices) of dynamic RAM. Using 'F1764/1764-1 in this application may eliminate the need for an external address latch.

Similarly, Figure 18 shows two 68020 processors sharing 4Mbyte of memory.

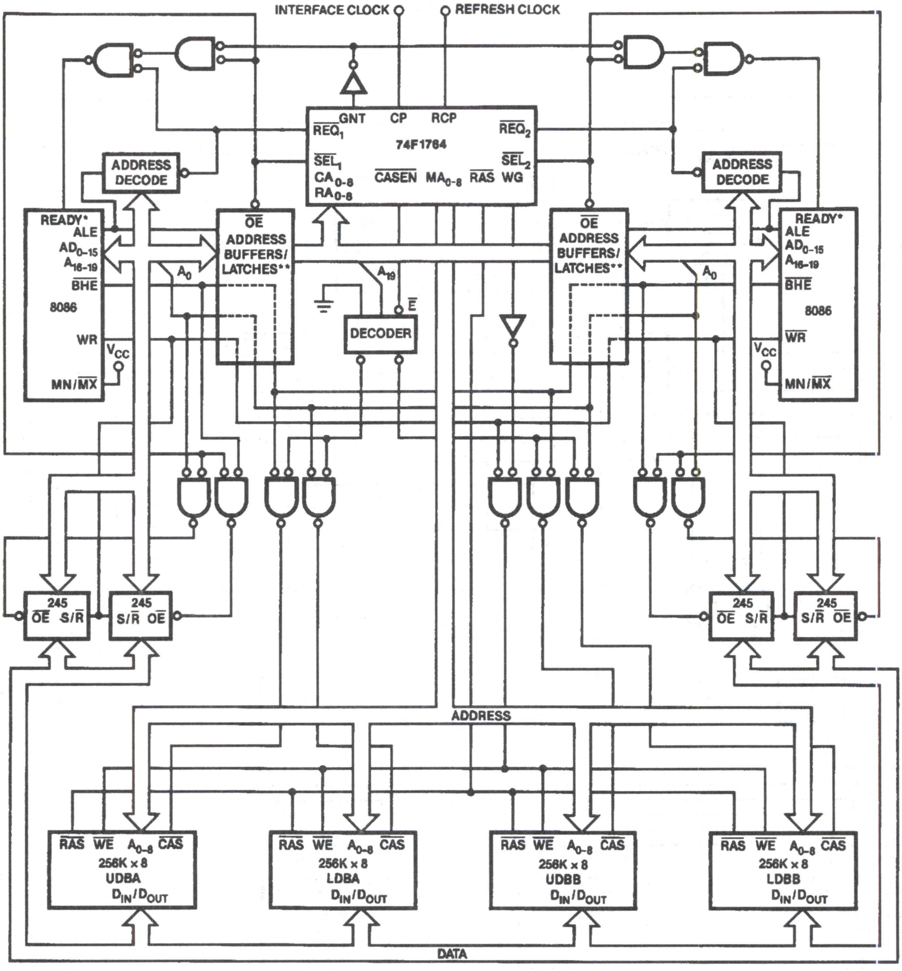
APPLICATIONS



V_{CC}
INTERFACE CLOCK
REFRESH CLOCK
V_{CC}
GNT
CP
RCP
DTACK
REQ1
74F1765
REQ2
SEL1
SEL2
RA_{0-9}
RAS
CA_{0-9} CASEN
MA_{0-9}
WG
ADDRESS DECODE
ADDRESS DECODE
DTACK
68000
A_{1-21}
UDS
LDS
R/W
D_{0-15}
OE
ADDRESS BUFFERS
A21
E
DECODER
OE
ADDRESS BUFFERS
DTACK
68000
A_{1-21}
UDS
LDS
R/W
D_{0-15}
245
OE S/R
245
S/R OE
245
OE S/R
245
S/R OE
ADDRESS
RAS WE A_{0-9} CAS
1 MEG × 8
UDBA
D_{IN}/D_{OUT}
RAS WE A_{0-9} CAS
1 MEG × 8
LDBA
D_{IN}/D_{OUT}
RAS WE A_{0-9} CAS
1 MEG × 8
UDBB
D_{IN}/D_{OUT}
RAS WE A_{0-9} CAS
1 MEG × 8
LDBB
D_{IN}/D_{OUT}
DATA
LD08570S

Figure 16. Two 68000 Processor Sharing 4 Mega-Byte DRAM

APPLICATIONS


INTERFACE CLOCK
REFRESH CLOCK
GNT
CP
RCP
REQ1
74F1764
REQ2
SEL1
CA0-8
RA0-8
CASEN
MA0-8
RAS
WG
SEL2
ADDRESS DECODE
ADDRESS DECODE
READY*
ALE
AD0-15
A16-19
BHE
8086
WR
VCC
MN/MX
OE
ADDRESS BUFFERS/ LATCHES**
A0
A19
E
DECODER
OE
ADDRESS BUFFERS/ LATCHES**
A0
READY*
ALE
AD0-15
A16-19
BHE
8086
WR
VCC
MN/MX
245
OE S/R
245
S/R OE
245
OE S/R
245
S/R OE
ADDRESS
RAS WE A0-8 CAS
256K x 8
UDBA
DIN/DOUT
RAS WE A0-8 CAS
256K x 8
LDBA
DIN/DOUT
RAS WE A0-8 CAS
256K x 8
UDBB
DIN/DOUT
RAS WE A0-8 CAS
256K x 8
LDBB
DIN/DOUT
DATA
BD09142S

NOTES:

* It might be necessary to synchronize READY by the 8284A. Please refer to the 8086 data sheet.

** Whether or not the 8086 address bus needs to be latched externally, should be determined by the relative speeds of the 8086 and the controller.

Figure 17. Two 8086 Processors Sharing 1MBYTE of DRAM

APPLICATIONS

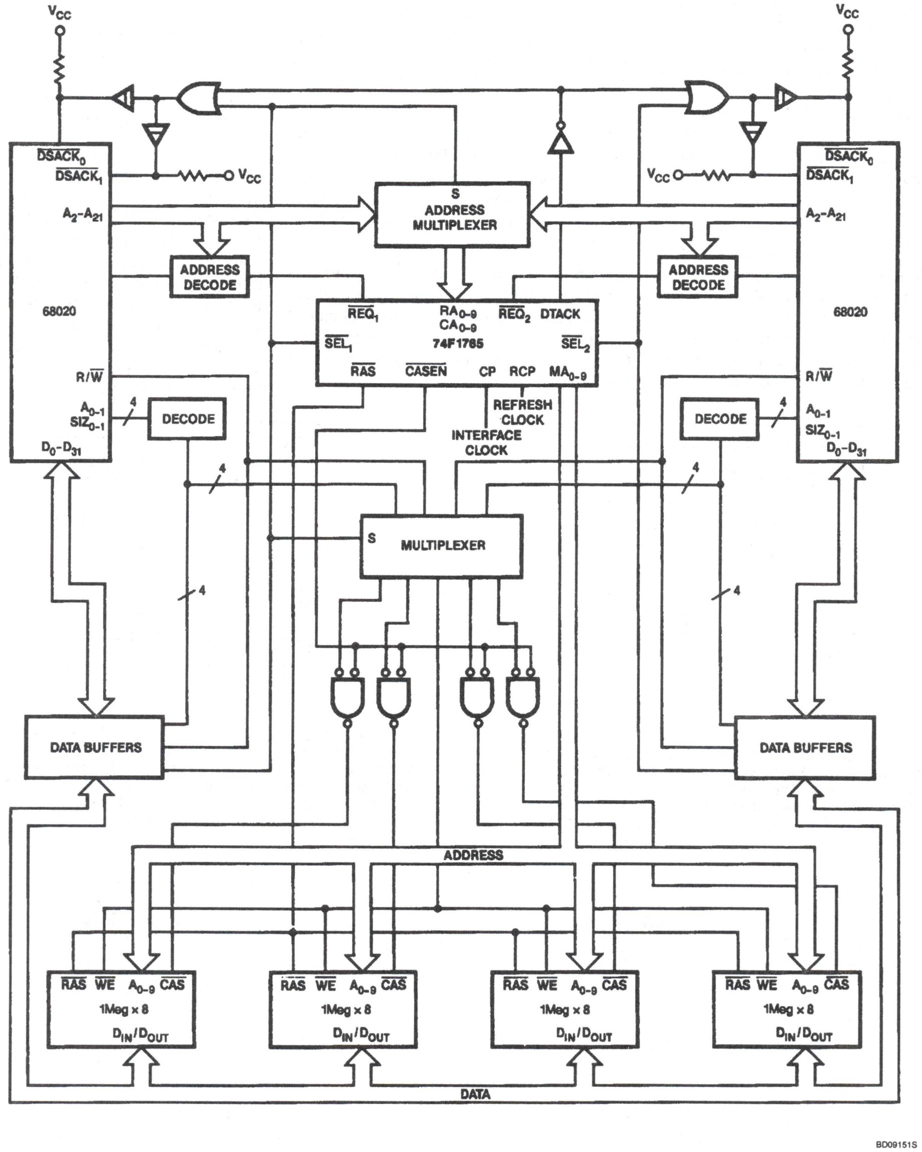

V_{CC}
V_{CC}
$\overline{DSACK_0}$
$\overline{DSACK_1}$
V_{CC}
V_{CC}
$\overline{DSACK_0}$
$\overline{DSACK_1}$
A_2-A_{21}
S
ADDRESS MULTIPLEXER
A_2-A_{21}
ADDRESS DECODE
ADDRESS DECODE
68020
68020
$\overline{REQ_1}$
RA_{0-9}
CA_{0-9}
$\overline{REQ_2}$
DTACK
$\overline{SEL_1}$
74F1765
$\overline{SEL_2}$
$\overline{RAS}$
$\overline{CASEN}$
CP
RCP
MA_{0-9}
R/$\overline{W}$
R/$\overline{W}$
A_{0-1}
SIZ_{0-1}
4
DECODE
REFRESH CLOCK
INTERFACE CLOCK
DECODE
4
A_{0-1}
SIZ_{0-1}
D_0-D_{31}
D_0-D_{31}
4
4
S
MULTIPLEXER
4
4
DATA BUFFERS
DATA BUFFERS
ADDRESS
$\overline{RAS}$ $\overline{WE}$ A_{0-9} $\overline{CAS}$
1Meg x 8
D_{IN}/D_{OUT}
$\overline{RAS}$ $\overline{WE}$ A_{0-9} $\overline{CAS}$
1Meg x 8
D_{IN}/D_{OUT}
$\overline{RAS}$ $\overline{WE}$ A_{0-9} $\overline{CAS}$
1Meg x 8
D_{IN}/D_{OUT}
$\overline{RAS}$ $\overline{WE}$ A_{0-9} $\overline{CAS}$
1Meg x 8
D_{IN}/D_{OUT}
DATA
BD09151S

Figure 18. Two 68020 Processors Sharing 4MBYTE of DRAM

74F1764 FAMILY LINE DRIVING CHARACTERISTICS

The 74F1764/1765 are designed to provide incident wave switching in Dual-Inline-Package (DIP) or Zig-zag-Inline-Package (ZIP) housed memory arrays and first reflected wave switching in Single-Inline-Package (SIP) or Single-Inline-Module (SIM) housed arrays. The 74F1764-1/1765-1, on the other hand, are designed to provide first reflected wave switching with as wide a range of characteristic impedances as possible.

The I_{OL2}/V_{OL2} and I_{OH2}/V_{OH2} parameters are included in the product specifications to assist engineers in designing systems which will switch memory array signal lines in the above mentioned manner. For example, the characteristic impedance of signal lines in DIP housed memory arrays is usually around 70Ω. If a signal line has settled out in a High state at 4 volts and must be pulled down to 0.8 volts or less on the incident wave, the DRAM Controller output must sink (4-0.8)/70A or 46mA at 0.8 volts. The I_{OL2}/V_{OL2} parameter indicates that the signal line in question will always be switched on the incident wave over the full commercial operating range.

It should be noted here that I_{OL2}/V_{OL2} and I_{OH2}/V_{OH2} are intended for transient use only and that steady state operation at I_{OH2} or I_{OL2} is not recommended (long term, steady state operation at these currents may result in electromigration).

Figures 1 – 4 show the output I/V characteristics of the DRAM Controller family of devices. These figures also demonstrate a graphical method for determining the incident wave (and first reflected wave) characteristics of the devices.

The suggested line termination for the 74F1764/1765 driving dual-in-line packaged or zig-zag packaged DRAMs is shown in Figure 8a. When driving single-in-line modules using the 74F1764/1765 or when driving any type of memory arrays with the 74F1764-1/1765-1, the schottky diode termination shown in Figure 8b can be used (most of these will need no termination at all).

Figures 5 – 7 are double exposures showing the High to Low and Low to High transitions while driving four banks of eight Dual-Inline-Packaged DRAMs. The signal line is unterminated in Figures 5 and 6, allowing the 74F1764/1765 to ring two volts below ground while the 74F1764-1/1765-1 make nice clean transitions. In Figure 7 the 74F1764/1765 is driving the same signal line but with one of its four branches terminated with its characteristic impedance in series with 300pF to ground (the worst of the four branches is shown).

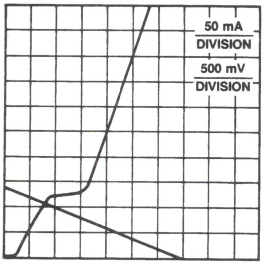


Figure 1. I-V Output Characteristics of the 74F1764/1765 in the Low State. Light Line is the I-V Curve of a 25Ω Transmission Line Settled to 3.5V (Typical for Recommended Termination). The High to Low Incident Wave on This Line Will Typically be to 0.8V

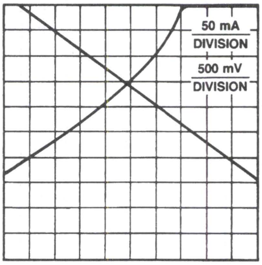


Figure 2. I-V Output Characteristics of the 74F1764/1765 in the High State. Light Line is the I-V Curve of a 35Ω Transmission Line Settled to 0.25V. The Incident Wave on the Low to High Transition Will Typically be to 2.4V on This Line. Any Line Over 35Ω Will Typically be Switched on the Incident Wave

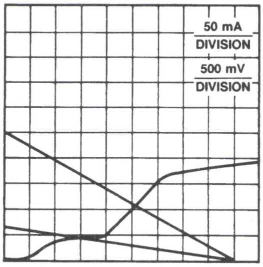


Figure 3. I-V Output Characteristics of the 74F1764-1/1765-1 in the Low State. Any Unterminated Line Impedance Between 18Ω and 70Ω (Both Shown) Will Typically Switch on the First Reflected Wave Without Violating the −1V Minimum Input Voltage Specification Typical of DRAMs

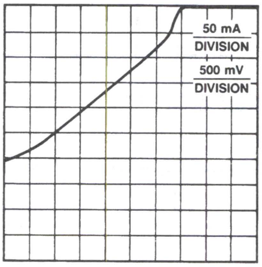


Figure 4. I-V Output Characteristics of the 74F1764-1/1765-1 While in the High State

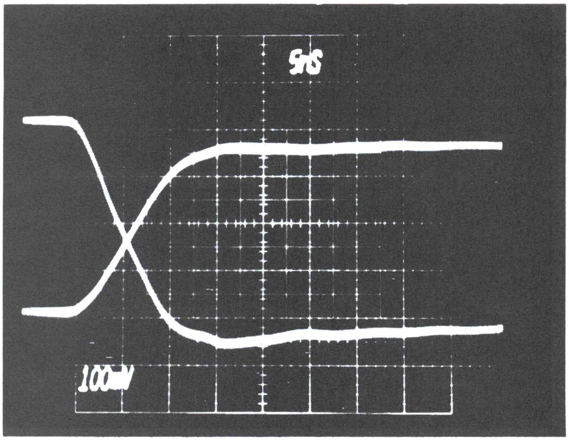


Figure 5. 74F1764-1/1765-1 Driving 32 DRAMs (Unterminated)

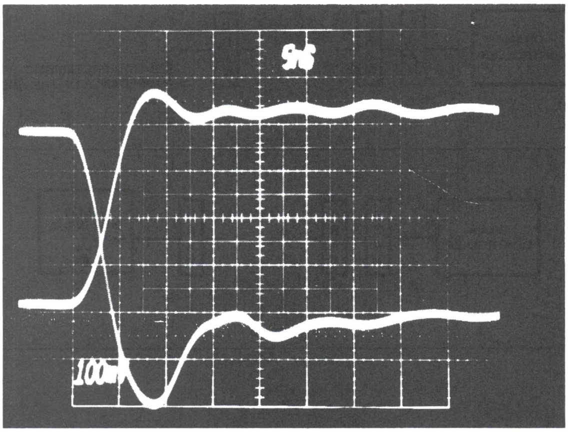


Figure 6. 74F1764/1765/1764-1/1765-1 Driving 32 DRAMs (Unterminated)

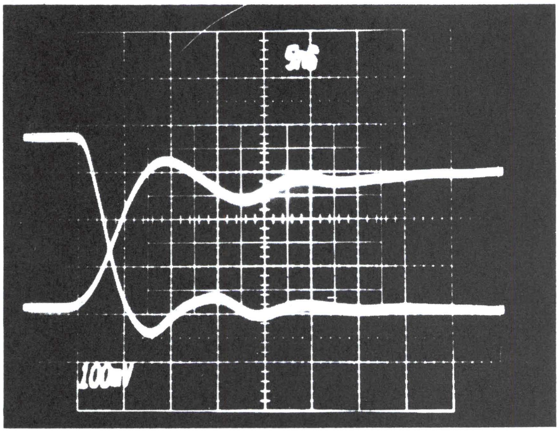
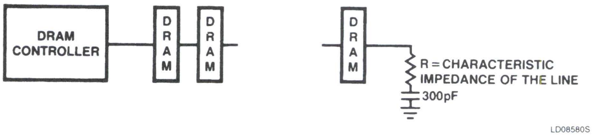


Figure 7. 74F1764/1765/1764-1/1765-1 Driving 32 DRAMs (Terminated as in Figure 8a)

(a)


DRAM CONTROLLER
DRAM
DRAM
DRAM
R = CHARACTERISTIC IMPEDANCE OF THE LINE
300pF
LD08580S

(b)

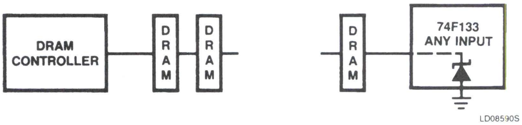

DRAM CONTROLLER
DRAM
DRAM
DRAM
74F133 ANY INPUT
LD08590S

Figure 8

Signetics

74F2952, 74F2953
Registered Transceivers

'F2952 8-Bit Registered Transceivers, Non-Inverting (3-State)
'F2953 8-Bit Registered Transceivers, Inverting (3-State)
Preliminary Specification

FAST Products

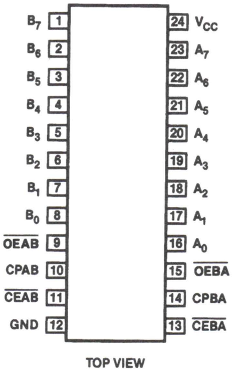
FEATURES

- 8-bit registered transceivers
- Two 8-bit, back to back registers store data moving in both directions between two bidirectional busses
- Separate Clock, Clock Enable and 3-State Output Enable provided for each register
- 'F2952 Non-inverting
- 'F2953 Inverting
- AM2952/2953 functional equivalent
- A Outputs sinks 24mA
- B Outputs sinks 64mA
- 24-pin 300mil-wide Slim DIP package

DESCRIPTION

The 'F2952 and 'F2953 are 8-bit registered transceivers. Two 8-bit back to back registers store data fLowing in both directions between two bidirectional busses. Data applied to the A inputs is entered and stored on the rising edge of the clock (CPAB), provided that the Clock Enable ($\overline{CEAB}$) is Low; simultaneously, the status flip-flop is set and the A-to-B flag (FAB) output goes High.

PIN CONFIGURATION



B7 1
B6 2
B5 3
B4 4
B3 5
B2 6
B1 7
B0 8
OEAB 9
CPAB 10
CEAB 11
GND 12
24 VCC
23 A7
22 A6
21 A5
20 A4
19 A3
18 A2
17 A1
16 A0
15 OEBA
14 CPBA
13 CEBA

TOP VIEW

CD08031S

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F2952 74F2953	12ns 12ns	56mA 65mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
24-Pin Plastic Slim DIP (300mil)	N74F2952N, N74F2953N
24-PIn Plastic SOL	N74F2952D, N74F2953D

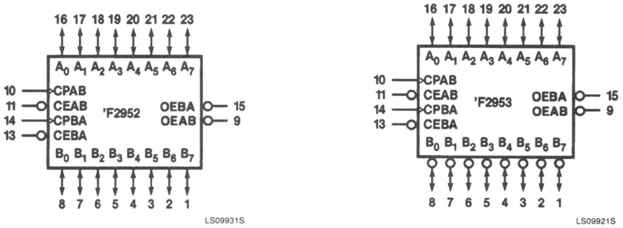
NOTE:
1. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$A_0 - A_3$, $B_0 - B_7$	A and B inputs	1.0/1.0	20µA/0.6mA
CPAB, CPBA	Clock inputs	1.0/0.033	20µA/20µA
$\overline{CEAB}$, $\overline{CEBA}$	Clock enable inputs	1.0/0.033	20µA/20µA
$\overline{OEBA}$, $\overline{OEAB}$	Output enable inputs	1.0/0.033	20µA/20µA
$A_0 - A_7$	A Outputs	150/40	3mA/24mA
$B_0 - B_7$	B Outputs	750/106.7	15mA/64mA

NOTE:
1. One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

LOGIC SYMBOL



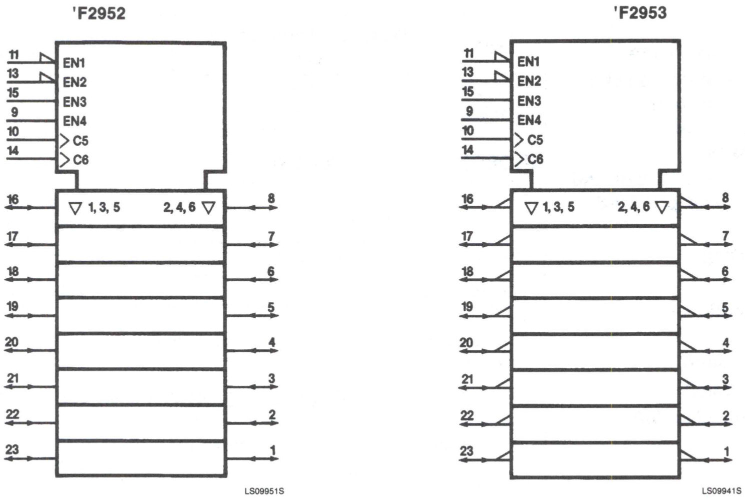
16 17 18 19 20 21 22 23
A0 A1 A2 A3 A4 A5 A6 A7
10 CPAB
11 CEAB
14 CPBA
13 CEBA
'F2952
OEBA 15
OEAB 9
B0 B1 B2 B3 B4 B5 B6 B7
8 7 6 5 4 3 2 1
16 17 18 19 20 21 22 23
A0 A1 A2 A3 A4 A5 A6 A7
10 CPAB
11 CEAB
14 CPBA
13 CEBA
'F2953
OEBA 15
OEAB 9
B0 B1 B2 B3 B4 B5 B6 B7
8 7 6 5 4 3 2 1

'F2952 LS09931S

'F2953 LS09921S

Data thus entered from the A inputs is present at the inputs to the B output buffers, but only appears on the B I/O pins when the B Output Enable ($\overline{OEAB}$) is made Low. Data fLow from B inputs to A outputs proceeds in the same manner as described for A inputs to B outputs fLow.

LOGIC SYMBOL (IEEE/IEC)


'F2952
11
13
15
9
10
14
EN1
EN2
EN3
EN4
C5
C6
▽ 1, 3, 5
2, 4, 6 ▽
16
17
18
19
20
21
22
23
8
7
6
5
4
3
2
1
LS09951S
'F2953
11
13
15
9
10
14
EN1
EN2
EN3
EN4
C5
C6
▽ 1, 3, 5
2, 4, 6 ▽
16
17
18
19
20
21
22
23
8
7
6
5
4
3
2
1
LS09941S

Registered Transceivers 74F2952, 74F2953

FUNCTION TABLE for Register A or B

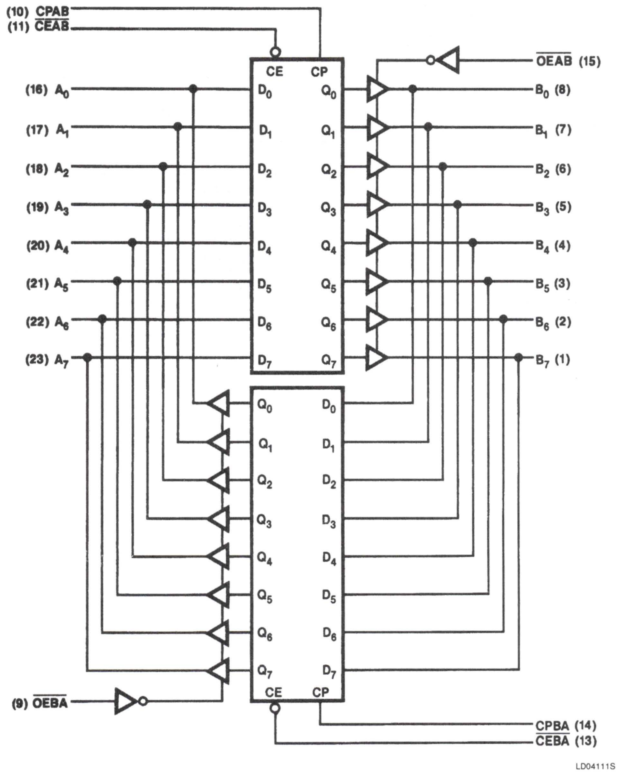
INPUTS			INTERNAL Q	OPERATING MODE
A_n or B_n	CP	CE		
X	X	H	NC	Hold data
L	↑	L	L	Load data
H	↑	L	H	

H = High voltage level
L = Low voltage level
X = Don't care
Z = High-impedance (OFF) state
↑ = Low-to-High transition
NC = No change

FUNCTION TABLE for Output Enable

$\overline{OE}$	INTERNAL Q	A OR B OUTPUTS		OPERATING MODE
		F2952	F2953	
H	X	Z	Z	Disable Outputs
L	L	L	H	Enable Outputs
L	H	H	L	

LOGIC DIAGRAM


(10) CPAB
(11) $\overline{CEAB}$
$\overline{OEAB}$ (15)
CE CP
(16) A_0
(17) A_1
(18) A_2
(19) A_3
(20) A_4
(21) A_5
(22) A_6
(23) A_7
D_0 D_1 D_2 D_3 D_4 D_5 D_6 D_7
Q_0 Q_1 Q_2 Q_3 Q_4 Q_5 Q_6 Q_7
B_0 (8)
B_1 (7)
B_2 (6)
B_3 (5)
B_4 (4)
B_5 (3)
B_6 (2)
B_7 (1)
(9) $\overline{OEBA}$
CE CP
CPBA (14)
$\overline{CEBA}$ (13)
LD04111S

V_{CC} = Pin 24
GND = Pin 12
( ) = Pin Numbers

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		−0.5 to +7.0	V
V_{IN}	Input voltage		−0.5 to +7.0	V
I_{IN}	Input current		−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		−0.5 to +5.5	
I_{OUT}	Current applied to output in Low output state	$A_0 - A_7$	48	mA
		$B_0 - B_7$	128	mA
T_A	Operating free-air temperature range		0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.75	5.0	5.25	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	High-level output current	$A_0 - A_7$			−3	mA
		$B_0 - B_7$			−15	mA
I_{OL}	Low-level output current	$A_0 - A_7$			24	mA
		$B_0 - B_7$			64	mA
T_A	Operating free-air temperature		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			74F00			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage	$A_0 - A_7$ $B_0 - B_7$	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	$I_{OH} = -3mA$	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.4		V
		$B_0 - B_7$		$I_{OH} = -15mA$	±10%V_{CC}	2.0			V
					±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage	$A_0 - A_7$	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	$I_{OL} = 20mA$	±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
		$B_0 - B_7$		$I_{OL} = 48mA$	±10%V_{CC}		0.40	0.55	V
				$I_{OL} = 64mA$	±5%V_{CC}		0.40	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$				−0.73	−1.2	V
I_I	Input current at maximum input voltage	CPAB, CPBA, $\overline{OEAB}$ $\overline{OEBA}$, $\overline{CEAB}$, $\overline{CEBA}$	$V_{CC} = 0.0V$, $V_I = 7.0V$					100	µA
		A_n, B_n	$V_{CC} = 5.5V$, $V_I = 5.5V$					1	mA
I_{IH}	High-level input current	CPAB, CPBA, $\overline{OEAB}$ $\overline{OEBA}$, $\overline{CEAB}$, $\overline{CEBA}$	V_{CC} = MAX, $V_I = 2.7V$					20	µA
I_{IL}	Low-level input current	CPAB, CPBA, $\overline{OEAB}$ $\overline{OEBA}$, $\overline{CEAB}$, $\overline{CEBA}$	V_{CC} = MAX, $V_I = 0.5V$					−0.6	mA
I_{OZH} $+I_{IH}$	OFF-state output current, High-level voltage applied	A_n, B_n	V_{CC} = MAX, $V_O = 2.7V$					70	µA
I_{OZL} $+I_{IL}$	OFF-state output current, Low-level voltage applied	A_n, B_n	V_{CC} = MAX, $V_O = 0.5V$					−70	µA
I_{OS}	Short-circuit output current[3]	$A_0 - A_7$	V_{CC} = MAX			−60		−100	mA
		$B_0 - B_7$	V_{CC} = MAX			−150		−225	mA
I_{CC}	Supply current (total)		V_{CC} = MAX				130	190	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at $V_{CC} = 5V$, $T_A = 25°C$.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of High-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

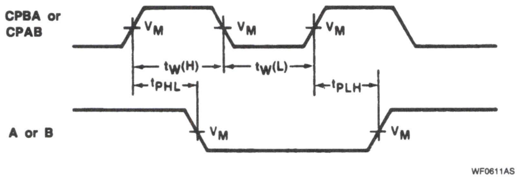
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F2952, 74F2953					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	110	130		100		MHz
t_{PLH}	Propagation delay CPBA or CPAB to A_n or B_n	Waveform 1	3.0	5.5	7.5	2.5	8.5	ns
t_{PHL}			4.0	7.0	9.0	3.5	10.0	
t_{PZH}	Output enable time $\overline{OEAB}$ or $\overline{OEBA}$ to A_n or B_n	Waveform 3	2.5	5.5	7.5	2.0	8.5	ns
t_{PZL}		Waveform 4	3.5	7.0	9.5	3.0	10.0	
t_{PHZ}	Output disable time $\overline{OEAB}$ or $\overline{OEBA}$ to A_n or B_n	Waveform 3	3.0	6.5	9.0	2.5	10.0	ns
t_{PLZ}		Waveform 4	2.5	5.5	7.5	2.0	8.5	

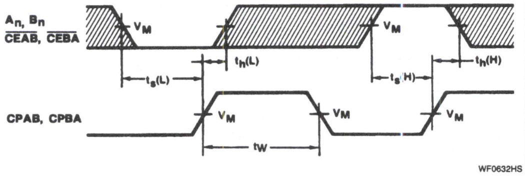
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	74F2952, 74F2953					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_s(H) t_s(L)	Setup time, High or Low A_n or B_n to CPBA or CPAB	Waveform 2	4.0 4.0			4.0 4.0		ns
t_h(H) t_h(L)	Hold time, High or Low A_n or B_n to CPBA or CPAB	Waveform 2	2.0 2.0			2.0 2.0		ns
t_s(H) t_s(L)	Setup time, High or Low $\overline{CEAB}$, $\overline{CEBA}$ to CPAB, CPBA	Waveform 2	1.0 4.0			1.0 4.0		ns
t_h(H) t_h(L)	Hold time, High or Low $\overline{CEAB}$, $\overline{CEBA}$ to CPAB, CPBA	Waveform 2	2.0 2.0			2.0 2.0		ns
t_w(H) t_w(L)	CPAB, CPBA pulse width High or Low	Waveform 1	3.0 3.0			3.0 3.0		ns

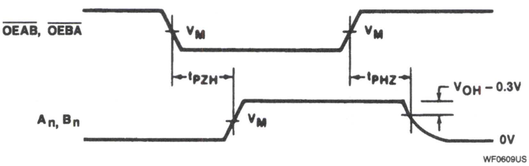
AC WAVEFORMS


CPBA or CPAB
V_M
V_M
V_M
t_W(H)
t_W(L)
t_PHL
t_PLH
A or B
V_M
V_M
WF0611AS

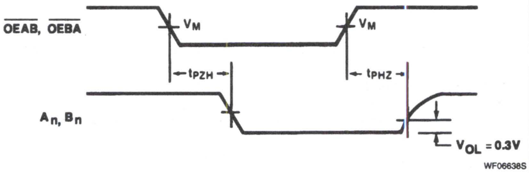
Waveform 1. Propagation Delay Clocks to Outputs and Clock Pulse Widths


A_n, B_n
CEAB, CEBA
V_M
V_M
t_h(L)
t_s(L)
t_s(H)
t_h(H)
CPAB, CPBA
V_M
V_M
V_M
tw
WF0632HS

Waveform 2. Data and Select Setup and Hold Times


OEAB, OEBA
V_M
V_M
t_PZH
t_PHZ
V_OH − 0.3V
A_n, B_n
V_M
0V
WF0609US

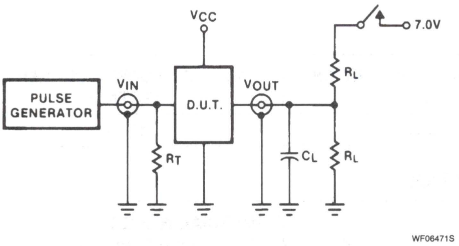
Waveform 3. 3-State Enable Time to High Level and Output Disable Time From High Level


OEAB, OEBA
V_M
V_M
t_PZH
t_PHZ
A_n, B_n
V_OL = 0.3V
WF06638S

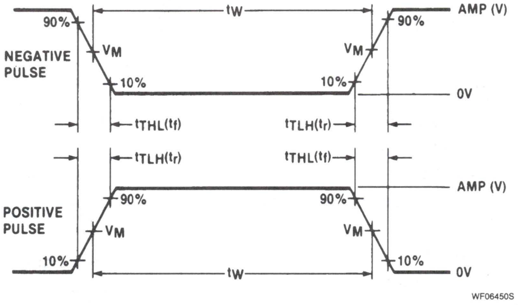
Waveform 4. 3-State Enable Time to Low Level and Output Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predicatable output performance.

TEST CIRCUIT AND WAVEFORMS


VCC
7.0V
RL
PULSE GENERATOR
VIN
D.U.T.
VOUT
RT
CL
RL
WF06471S

Test Circuit for 3-State Outputs


90%
tW
AMP (V)
NEGATIVE PULSE
VM
10%
0V
tTHL(tf)
tTLH(tr)
POSITIVE PULSE
tTLH(tr)
tTHL(tf)
90%
VM
10%
tW
0V
WF06450S

$V_M = 1.5V$

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F3037
30Ω Line Driver

Quad 2-Input NAND 30Ω Line Driver
Product Specification

FAST Products

FEATURES

- **30Ω line driver**
- **160mA output drive capability in the Low state**
- **67mA output drive capability in the High state**
- **High-speed**
- **Facilitates incident wave switching**
- **3nh lead inductance each on V_{CC} and GND when both side pins are used**

DESCRIPTION

The F3037 is a high current Line driver composed of four 2-input NAND gates. It has been designed to deal with the transmission line effects of PC boards which appear when fast edge rates are used.

The drive capability of the F3037 is 67mA source and 160mA sink with a V_{CC} as low as 4.5 volts. This guarantees incident wave switching with V_{OH} not less than 2.0V and V_{OL} not more than 0.8V while driving impedances as low as 30Ω. This is applicable with any combination of outputs using continuous duty.

The propagation delay of the part is minimally affected by reflections when terminated only by the TTL inputs of other devices. Performance may be improved by full or partial line termination.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F3037	3.8ns	15mA

ORDERING INFORMATION

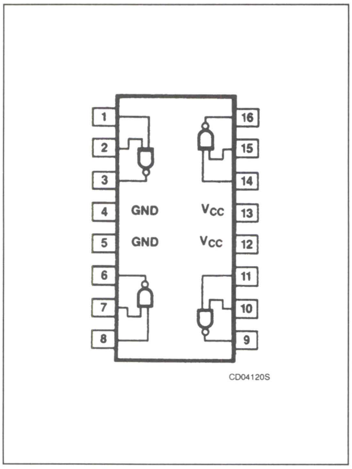
PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
Plastic DIP	N74F3037N

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

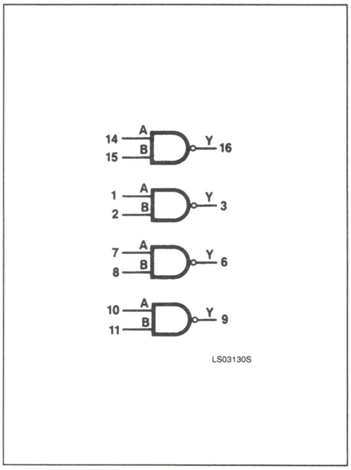
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A, B	Data inputs	1.0/1.0	20μA/0.6mA
$\overline{Y}$	Data output	3350/266	67mA/160mA

NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

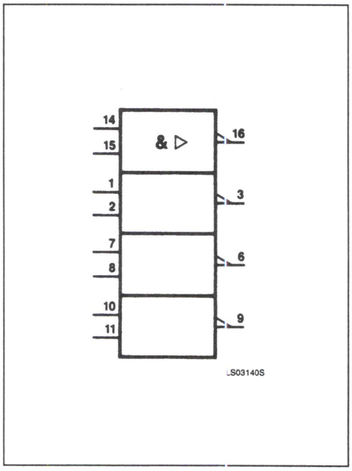
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



30Ω Line Driver FAST 74F3037

FUNCTION TABLE

INPUTS		OUTPUT
A	B	$\overline{Y}$
L	L	H
L	H	H
H	L	H
H	H	L

H = High voltage level
L = Low voltage level

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	320	mA
T_A	Operating free-air temperature range	0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High level input voltage	2.0			V
V_{IL}	Low level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High level output current			−67	mA
I_{OL}	Low level output current			160	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			74F3037			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = −45mA	±10%V_{CC}	2.5			V
					± 5%V_{CC}	2.7	3.4		V
				I_{OH1} = −67mA[3]	±10%V_{CC}	2.0			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 100mA	±10%V_{CC}		0.40	0.55	V
				I_{OL1} = 160mA[4]	±10%V_{CC}			0.80	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$				−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V					100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					−0.6	mA
I_O[5]			V_{CC} = MAX, V_O = 2.25V			−60		−160	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				3.5	6.0	mA
		I_{CCL}					27	40	mA

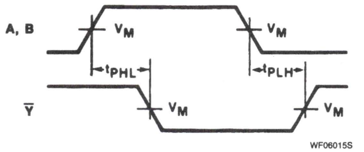
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OH1} is the current necessary to guarantee the Low to High transition in a 30Ω transmission line on the incident wave.
4. I_{OL1} is the current necessary to guarantee the High to Low transition in a 30Ω transmission line on the incident wave.
5. I_O is tested under conditions that produce current approximately one half of the true short-circuit output current (I_{OS}).

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F3037					UNIT
			T_A = +25°C V_{CC} = +5.0V C_L = 50pF R_L = 500Ω			T_A = 0 to +70°C V_{CC} = +5.0V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A, B to $\overline{Y}$	Waveform 1	3.0 1.5	4.5 3.0	6.0 5.0	2.5 1.5	6.5 5.5	ns

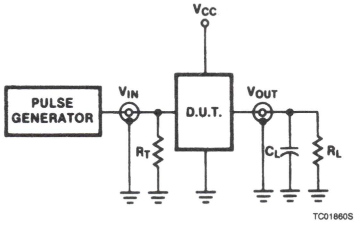
AC WAVEFORM


A, B
V_M
V_M
tPHL
tPLH
Ȳ
V_M
V_M
WF06015S

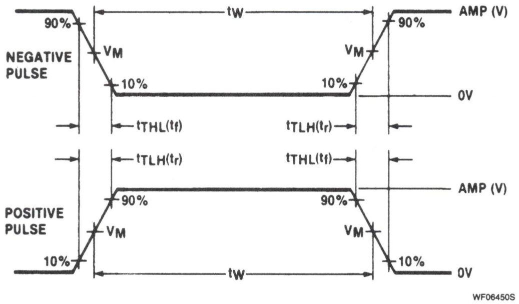
NOTE: $V_M = 1.5V$.

Waveform 1. Propagation Delay for Inputs to Output

TEST CIRCUIT AND WAVEFORMS


V_CC
PULSE GENERATOR
V_IN
D.U.T.
V_OUT
R_T
C_L
R_L
TC01860S

Test Circuit for Totem-Pole Outputs


tw
AMP (V)
90%
90%
NEGATIVE PULSE
VM
VM
10%
10%
0V
tTHL(tf)
tTLH(tr)
tTLH(tr)
tTHL(tf)
AMP (V)
90%
90%
POSITIVE PULSE
VM
VM
10%
10%
tw
0V
WF06450S

$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS

R_L = Load resistor to GND; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F3038
30Ω Line Driver

Quad 2-Input NAND 30Ω Line Driver (Open-Collector)
Product Specification

FAST Products

FEATURES

- **30Ω line driver**
- **160mA output drive capability**
- **High speed**
- **Facilitates incident wave switching**
- **3nh lead inductance each on V_{CC} and GND when both side pins are used**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F3038	9.0ns	17mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
Plastic DIP	N74F3038N

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A, B	Data inputs	1.0/1.0	20μA/0.6mA
$\overline{Y}$	Data output	OC*/266	OC*/160mA

NOTES:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.
2. OC* = Open Collector

DESCRIPTION

The F3038 is a high current Open-Collector Line Driver composed of four 2-input NAND gates.

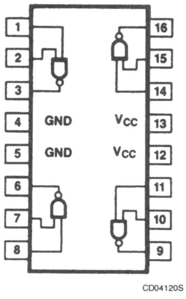
It has been designed to deal with the transmission line effects of PC boards which appear when fast edge rates are used.

The F3038 can sink 160mA with a V_{CC} as low as 4.5V. This guarantees incident wave switching with V_{OL} not more than 0.8V while driving impedances as low as 30Ω. This is applicable with any combination of outputs using continuous duty.

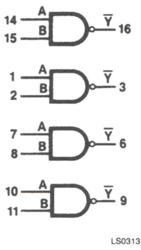
The AC specifications for the F3038 were determined using the standard Fast load for Open-Collector parts of 50pF capacitance, a 500Ω pull-up resistor and a 500Ω pull-down. (See Test Circuit).

Reducing the load resistors to 100Ω will decrease the T_{PLH} propagation delay by approximately 50% while increasing T_{PHL} only slightly. The graph of Typical Propagation Delay vs Load Resistor shows a spline fit curve from four measured data points: $R_L = 30Ω$, $R_L = 100Ω$, $R_L = 300Ω$, and $R_L = 500Ω$.

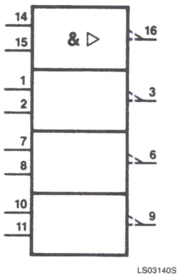
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = High voltage level
L = Low voltage level

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	320	mA
T_A	Operating free-air temperature range	0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
V_{OH}	High-level output voltage			4.5	V
I_{OL}	Low-level output current			160	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			74F3038			UNIT
						Min	Typ[2]	Max	
I_{OH}	High-level output current		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, V_{OH} = MAX					250	μA
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 100mA	±10%V_{CC}			0.55	V
				I_{OL1} = 160mA[3]	±10%V_{CC}			0.80	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V					100	μA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					−0.6	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX		V_{IN} = GND		3.5	6.0	mA
		I_{CCL}			V_{IN} = 4.5V		30	40	mA

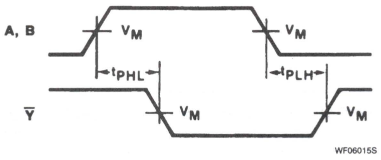
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OL1} is the current necessary to guarantee the High to Low transition in a 30Ω transmission line on the incident wave.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F3038					UNIT
			T_A = +25°C V_{CC} = +5.0V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = +5.0V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A, B to $\overline{Y}$	Waveform 1	6.0 1.5	9.5 3.0	12.0 5.0	5.5 1.5	12.5 5.5	ns

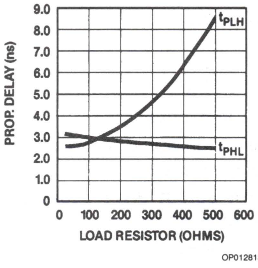
AC WAVEFORM


A, B
VM
VM
tPHL
tPLH
Y̅
VM
VM
WF06015S

NOTE: For all waveforms, $V_M = 1.5V$.

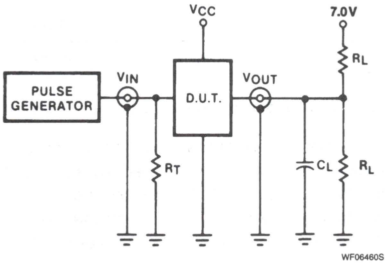
Waveform 1. Propagation Delay for Input to Output

AC CHARACTERISTICS

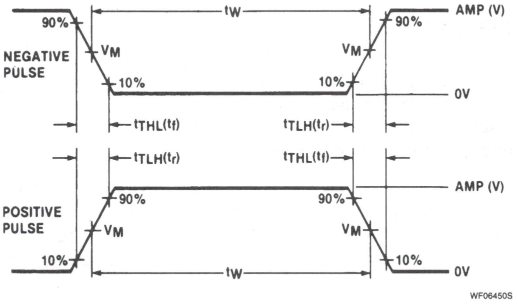


Typical Prop. Delay vs. Load Resistor

TEST CIRCUIT AND WAVEFORMS


VCC
7.0V
RL
PULSE GENERATOR
VIN
D.U.T.
VOUT
RT
CL
RL
WF06460S

Test Circuit for Open-Collector Outputs


tW
AMP (V)
90%
90%
NEGATIVE PULSE
VM
VM
10%
10%
0V
tTHL(tf)
tTLH(tr)
tTLH(tr)
tTHL(tf)
AMP (V)
90%
90%
POSITIVE PULSE
VM
VM
10%
10%
tW
0V
WF06450S

$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F3040
30Ω Line Driver

Dual 4-Input NAND 30Ω Line Driver
Product Specification

FAST Products

FEATURES

- **30Ω line driver**
- **160mA output drive capability in the Low state**
- **67mA output drive capability in the High state**
- **High-speed**
- **Facilitates incident wave switching**
- **3nh lead inductance each on V_{CC} and GND when both side pins are used**

DESCRIPTION

The F3040 is a high-current Line driver composed of two 2-Input NAND gates. It has been designed to deal with the transmission line effects of PC boards which appear when fast edge rates are used.

The drive capability of the F3040 is 67mA source and 160mA sink with a V_{CC} as low as 4.5V. This guarantees incident wave switching with V_{OH} not less than 2.0V and V_{OL} not more than 0.8V while driving impedances as low as 30Ω. This is applicable with any combination of outputs using continuous duty. The propagation delay of the part is minimally affected by reflections when terminated only by the TTL inputs of other devices. Performance may be improved by full or partial line termination.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F3040	3.7ns	7.5mA

ORDERING INFORMATION

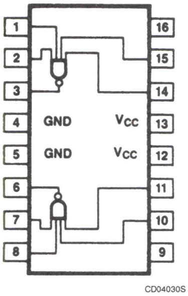
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ± 10%; T_A = 0°C to +70°C
Plastic DIP	N74F3040N

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

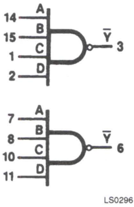
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A, B, C, D	Data inputs	1.0/1.0	20µA/0.6mA
$\overline{Y}$	Data output	3350/266	67mA/160mA

NOTE:
1. One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

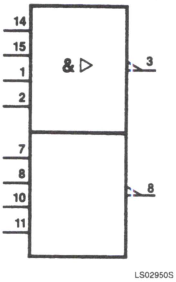
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



FUNCTION TABLE

INPUT				OUTPUT
A	B	C	D	Y
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	320	mA
T_A	Operating free-air temperature range	0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−67	mA
I_{OL}	Low-level output current			160	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]			74F3040			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = −45mA	±10%V_{CC}	2.5			V
			I_{OH1} = −67mA[3]	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 100mA	±10%V_{CC}		0.4	0.55	V
			I_{OL1} = 160mA[4]	±10%V_{CC}			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, $I_I = I_{IK}$				−0.73	−1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V					100	μA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V					−0.6	mA
I_O[5]		V_{CC} = MAX, V_O = 2.25V			−60		−160	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			2.0	4.0	mA
		I_{CCL}				14	20	mA

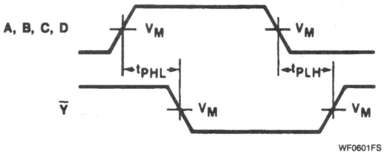
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OH1} is the current necessary to guarantee the Low to High transition in a 30Ω transmission line on the incident wave.
4. I_{OL1} is the current necessary to guarantee the the High to Low transition in a 30Ω transmission line on the incident wave.
5. I_O is tested under conditions that produce current approximately one half of the true short-circuit output current (I_{OS}).

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F3040					UNIT
			T_A = +25°C V_{CC} = +5.0V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A, B, C, D to $\overline{Y}$	Waveform 1	2.5 1.0	4.5 2.5	6.5 4.5	2.5 1.0	7.0 5.0	ns

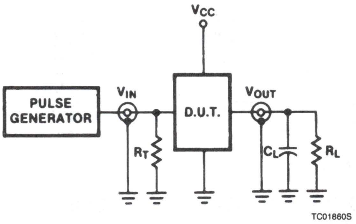
AC WAVEFORM


A, B, C, D
V_M
V_M
t_{PHL}
t_{PLH}
$\overline{Y}$
V_M
V_M
WF0601FS

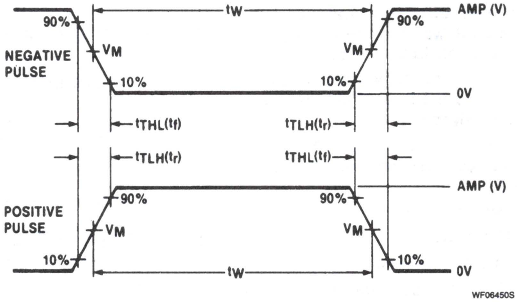
Waveform 1. Propagation Delays for Inputs to Output

NOTE: For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORMS


V_{CC}
PULSE GENERATOR
V_{IN}
D.U.T.
V_{OUT}
R_T
C_L
R_L
TC01860S

Test Circuit for Totem-Pole Outputs


NEGATIVE PULSE
90%
V_M
10%
tw
90%
V_M
10%
AMP (V)
0V
$t_{THL}(t_f)$
$t_{TLH}(t_r)$
$t_{TLH}(t_r)$
$t_{THL}(t_f)$
POSITIVE PULSE
90%
90%
V_M
V_M
10%
10%
tw
AMP (V)
0V
WF06450S

$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS

R_L = Load resistor to GND; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F30240, 74F30244
30Ω Line Drivers

Product Specification

FAST Products

'F30240 Octal 30Ω Line Driver With Enable, INV (Open-Collector)
'F30244 Octal 30Ω Line Driver With Enable, NINV (Open-Collector)

FEATURES

- **Ideal for driving transmission lines or backplanes. 160mA I_{OL} ideal for applications with impedance as low as 30Ω.**
- **Guaranteed threshold voltages on the incident wave while driving line impedance as low as 30Ω.**
- **High-impedance NPN base inputs for reduced loading (20μA in High and Low states)**
- **Ideal for applications which require high output drive and minimal bus loading**
- **Octal bus interface**
- **'F30240A Inverting**
- **'F30244A Non-Inverting**
- **Open-Collector outputs sink 160mA**
- **160mA I_{OL} ideal for low-impedance applications and transmission line effects with impedance as low as 30Ω**
- **Multiple side pins are used for V_{CC} and GND to reduce lead inductance (improves speed and noise immunity)**
- **24-pin 300mil-wide Slim DIP package**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74F30240	9.5ns	62.5mA
74F30244	10.5ns	69mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
Plastic SLIM DIP (300mil)	74F30240AN, 74F30244AN
*Cerdip (300mil)	74F30240AN, 74F30244AN

NOTE:
* Thermal mounting techniques are recommended.

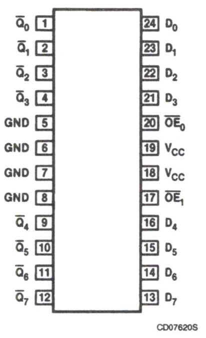
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$D_0 - D_7$	Data inputs	1.0/0.033	20μA/20μA
$\overline{OE}_0$, $\overline{OE}_1$	Output Enable inputs (active-Low)	1.0/0.033	20μA/20μA
$\overline{Q}_0 - \overline{Q}_7$	Data outputs (OC*)'F30240A	OC*/266.7	OC*/160mA
$Q_0 - Q_7$	Data outputs (OC*)'F30244A	OC*/266.7	OC*/160mA

NOTES:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.
2. OC* = Open-Collector

PIN CONFIGURATION

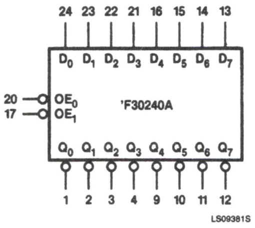
'F30240



Q̄0 1
Q̄1 2
Q̄2 3
Q̄3 4
GND 5
GND 6
GND 7
GND 8
Q̄4 9
Q̄5 10
Q̄6 11
Q̄7 12
24 D0
23 D1
22 D2
21 D3
20 OE̅0
19 VCC
18 VCC
17 OE̅1
16 D4
15 D5
14 D6
13 D7
CD07620S

LOGIC SYMBOL

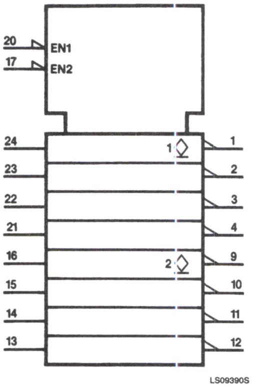
'F30240



24 23 22 21 16 15 14 13
D0 D1 D2 D3 D4 D5 D6 D7
20 OE0
17 OE1
'F30240A
Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
1 2 3 4 9 10 11 12
LS09381S

LOGIC SYMBOL (IEEE/IEC)

'F30240

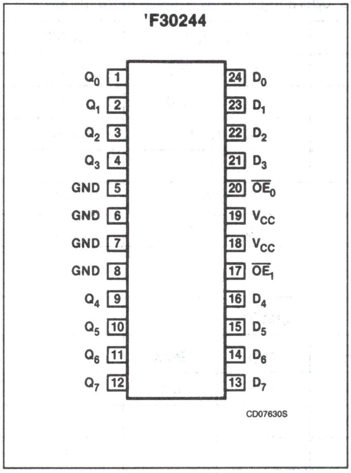


20 EN1
17 EN2
24
23
22
21
16
15
14
13
1
2
1
2
3
4
9
10
11
12
LS09390S

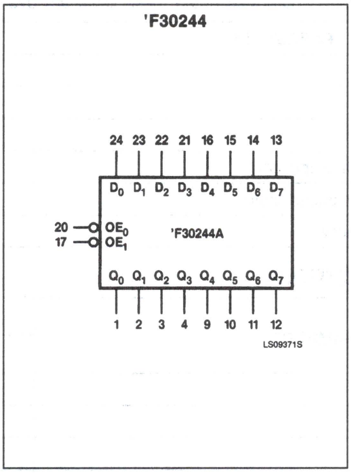
30Ω Line Drivers

FAST 74F30240, 74F30244

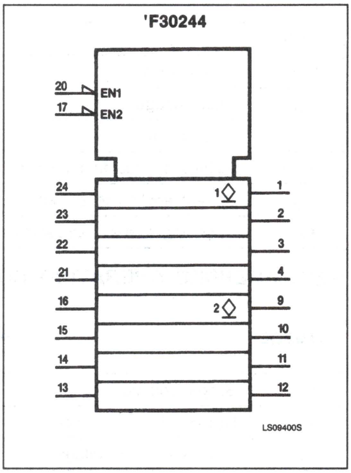
PIN CONFIGURATION


'F30244
Q0 1
Q1 2
Q2 3
Q3 4
GND 5
GND 6
GND 7
GND 8
Q4 9
Q5 10
Q6 11
Q7 12
24 D0
23 D1
22 D2
21 D3
20 OE0
19 VCC
18 VCC
17 OE1
16 D4
15 D5
14 D6
13 D7
CD07630S

LOGIC SYMBOL


'F30244
24 23 22 21 16 15 14 13
D0 D1 D2 D3 D4 D5 D6 D7
20 OE0
17 OE1
'F30244A
Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
1 2 3 4 9 10 11 12
LS09371S

LOGIC SYMBOL (IEEE/IEC)


'F30244
20 EN1
17 EN2
24 23 22 21 16 15 14 13
1
2
1 2 3 4 9 10 11 12
LS09400S

DESCRIPTION

The 'F30240/'F30244 are high current Open-Collector Octal Buffers composed of eight inverters.

The 'F30240 has inverting data paths and the 'F30244 has non-inverting paths. Each device has eight inverters with two Output Enables ($\overline{OE}_0$, $\overline{OE}_1$) each controlling four outputs. Both drivers are designed to deal with the low-impedance transmission line effects found on printed circuit boards when fast edge rates are used.

The 160mA I_{OL} provides ample power to achieve TTL switching voltages on the incident wave.

FUNCTION TABLE

INPUTS		OUTPUTS	
		'F30240	'F30244
$\overline{OE}_n$	D_n	$\overline{Q}_n$	Q_n
L	L	H	L
L	H	L	H
H	X	OFF	OFF

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to 5.5	V
I_{OUT}	Current applied to output in Low output state	320	mA
T_A	Operating free-air temperature range	0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
V_{OH}	High-level output voltage			4.5	V
I_{OL}	Low-level output current			160	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]			74F30240 74F30244			Unit
							Min	Typ[2]	Max	
I_{OH}	High–level output current			V_{CC} = MIN, V_{IL} = MAX,V_{IH} = MIN,V_{OH} = MAX					250	μA
V_{OL}	Low-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 100mA	±10%V_{CC}			.55	V
					I_{OL1} = 160mA[3]	±5%V_{CC}			.80	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, I_I = I_{IK}				−0.73	−1.2	V
I_I	Input current at maximum input voltage			V_{CC} = 0.0V, V_I = 7.0V					100	μA
I_{IH}	High-level input current			V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	Low-level input current			V_{CC} = MAX, V_I = 0.5V					−20	μA
I_{CC}	Supply current (total)	I_{CCH}	'F30240	V_{CC} = MAX				13	23	mA
		I_{CCL}						70	95	
		I_{CCH}	'F30244					19	27	mA
		I_{CCL}						70	100	

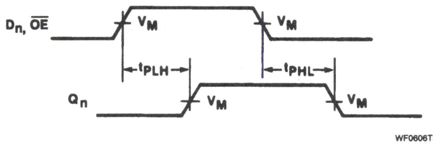
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OL1} is the current necessary to guarantee the High to Low transition in a 30Ω transmission line on the incident wave.

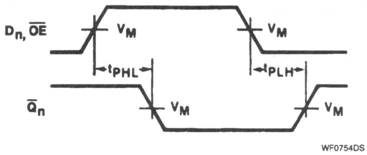
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	74F30240, 74F30244					UNIT
				$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_n to $\overline{Q}_n$	'F30240	Waveform 2	4.0 1.0	10.0 2.0	14.5 5.0	4.0 1.0	15.0 5.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{OE}$ to $\overline{Q}_n$		Waveform 1, 2	4.0 3.5	10.0 6.0	14.0 9.0	4.0 3.5	14.5 10.5	ns
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	'F30244	Waveform 1	4.0 3.0	10.5 5.5	14.5 9.0	4.0 3.0	15.0 9.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{OE}$ to Q_n		Waveform 1, 2	4.0 3.5	9.5 6.0	14.0 9.0	4.0 3.5	14.5 10.5	ns

AC WAVEFORMS



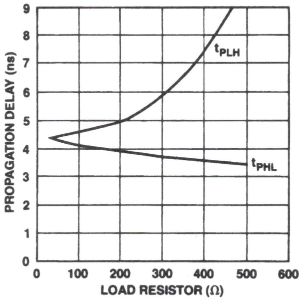
Waveform 1. Propagation Delay for Data to Output



Waveform 2. Propagation Delay for Data to Output

NOTE: For all waveforms, $V_M = 1.5V$.

TYPICAL PROPAGATION DELAYS VERSUS LOAD RESISTOR FOR OPEN-COLLECTOR OUTPUTS

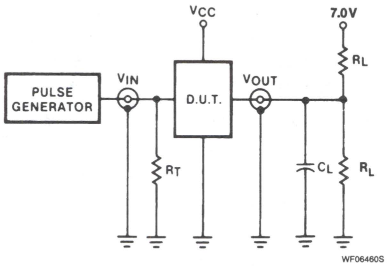


NOTES:
When using open-collector parts, the value of the pull-up resistor greatly affects the value of the t_{PLH}. For example, changing the specified pull-up resistor value from 500 ohms to 100 ohms will improve the t_{PLH} up to 50% with only a slight increase in the t_{PHL}. However, if the value of the pull-up resistor is changed, the user must make certain that the total I_{OL} current through the resistor and, thus the total I_{IL}s of the receiver, does not exceed the I_{OL} maximum specification.

30Ω Line Drivers

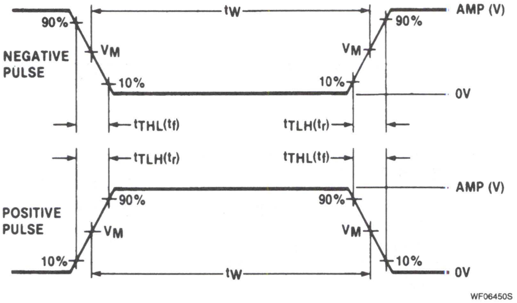
FAST 74F30240, 74F30244

TEST CIRCUIT AND WAVEFORMS



V_{CC}
7.0V
R_L
PULSE GENERATOR
V_{IN}
D.U.T.
V_{OUT}
R_T
C_L
R_L
WF06460S

Test Circuit for Open-Collector Outputs



tw
90%
AMP (V)
NEGATIVE PULSE
V_M
V_M
10%
10%
0V
$t_{THL}(t_f)$
$t_{TLH}(t_r)$
$t_{TLH}(t_r)$
$t_{THL}(t_f)$
AMP (V)
90%
90%
POSITIVE PULSE
V_M
V_M
10%
10%
0V
tw
WF06450S

$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	**Rep. Rate**	**Pulse Width**	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST Products

FAST 74F30245, 74F30640
Transceivers

Product Specification

'F30245 Octal 30Ω Transceivers, NINV (Open-Collector With Enable + 3-State)
'F30640 Octal 30Ω Transceivers, INV (Open-Collector With Enable + 3-State)

FEATURES

- High-impedance NPN base inputs for reduced loading (20μA in High and Low states)
- Ideal for applications which require High output drive and minimal bus loading
- Octal bidirectional bus interface
- 'F30245 Non-inverting
- 'F30640 Inverting
- Choice of outputs: Open-Collectors ($B_0 - B_7$) and 3-States ($A_0 - A_7$)
- Open-Collector outputs sink 160mA
- 160mA I_{OL} ideal for low-impedance applications and transmission line effects with impedance as low as 30Ω
- 3-State outputs sink 24mA
- Multiple side pins are used for V_{CC} and GND to reduce lead inductance (improves speed and noise immunity)
- Available in 24-pin standard Slim DIP (300mil) plastic or Cerdip packages
- Flow through pinout structure facilitates PC board layout

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F30245	5.5ns	90mA
74F30640	5.0ns	85mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
Cerdip (300mil)	N74F30245F, N74F30640F
Plastic Slim DIP	N74F30245N, N74F30640N

NOTE: Thermal mounting techniques are recommended.

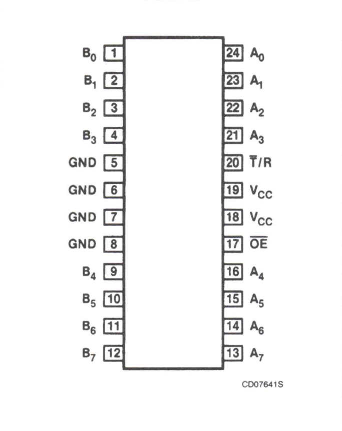
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$A_0 - A_7$	Data inputs	3.5/0.1167	70μA/70μA
$B_0 - B_7$	Data inputs	1.0/1.0	20μA/0.6mA
$\overline{OE}$	Output Enable input (active-Low)	2.0/0.0667	40μA/40μA
$\overline{T}$/R	Transmit/Receive input	2.0/0.0667	40μA/40μA
$A_0 - A_7$	Data outputs (3-State)	150/40	3mA/24mA
$B_0 - B_7$	Data outputs (OC*)	OC*/266.7	OC*/160mA

NOTES:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.
2. OC* = Open-Collector

PIN CONFIGURATION

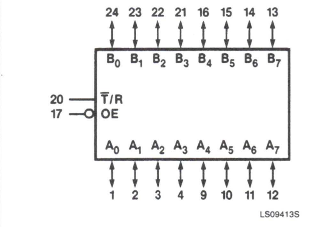
'F30245



B0 1
B1 2
B2 3
B3 4
GND 5
GND 6
GND 7
GND 8
B4 9
B5 10
B6 11
B7 12
24 A0
23 A1
22 A2
21 A3
20 T̄/R
19 VCC
18 VCC
17 OE
16 A4
15 A5
14 A6
13 A7
CD07641S

LOGIC SYMBOL

'F30245

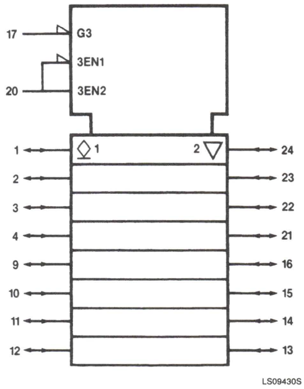


24 23 22 21 16 15 14 13
B0 B1 B2 B3 B4 B5 B6 B7
20 T̄/R
17 OE
A0 A1 A2 A3 A4 A5 A6 A7
1 2 3 4 9 10 11 12
LS09413S

V_{CC} = Pin 18, 19
GND = Pin 5, 6, 7, 8

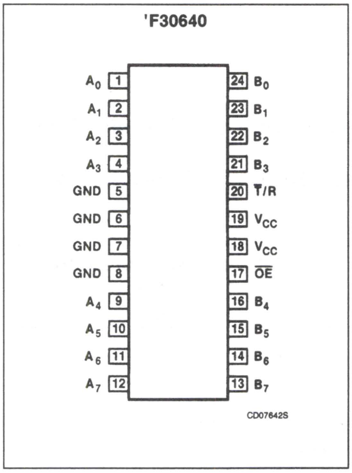
LOGIC SYMBOL (IEEE/IEC)

'F30245

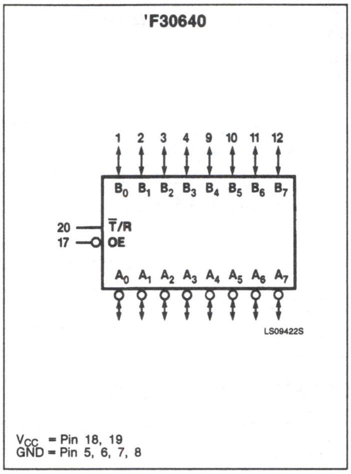


17
G3
3EN1
20
3EN2
1
2
1
2
3
4
9
10
11
12
24
23
22
21
16
15
14
13
LS09430S

PIN CONFIGURATION

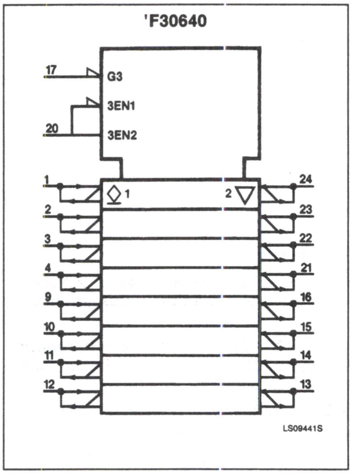

'F30640
A0 1
A1 2
A2 3
A3 4
GND 5
GND 6
GND 7
GND 8
A4 9
A5 10
A6 11
A7 12
24 B0
23 B1
22 B2
21 B3
20 T/R
19 VCC
18 VCC
17 OE
16 B4
15 B5
14 B6
13 B7
CD07642S

LOGIC SYMBOL


'F30640
1 2 3 4 9 10 11 12
B0 B1 B2 B3 B4 B5 B6 B7
20 T/R
17 OE
A0 A1 A2 A3 A4 A5 A6 A7
LS09422S

V_{CC} = Pin 18, 19
GND = Pin 5, 6, 7, 8

LOGIC SYMBOL (IEEE/IEC)


'F30640
17
G3
3EN1
20
3EN2
1
2
3
4
9
10
11
12
1
2
24
23
22
21
16
15
14
13
LS09441S

DESCRIPTION

The 'F30245/'F30640 are high-current Octal Transceivers.

The 'F30245 has non-inverting data paths and the 'F30640 has inverting paths. The B outputs are Open-Collectors with 160mA I_{OL} while the A outputs are 3-State with 24mA I_{OL}. Both transceivers are designed to deal with the Low-impedance transmission line effects found on printed circuit boards when fast edge rates are used.

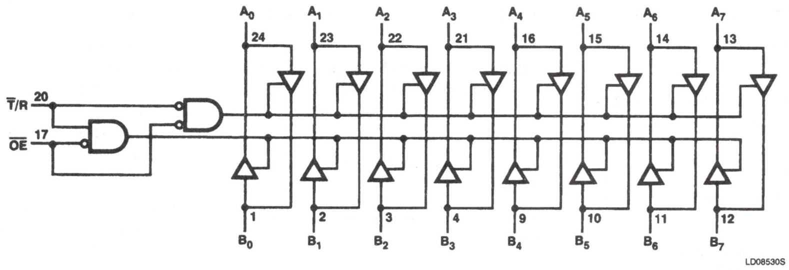
The 160mA I_{OL} provides ample power to achieve TTL switching voltages on the incident wave.

FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS			
		'F30245		'F30640A	
$\overline{OE}$	$\overline{T}$/R	A_n	B_n	A_n	B_n
L	H	A = B	Inputs	$A = \overline{B}$	Inputs
L	L	Inputs	B = A	Inputs	$B = \overline{A}$
H	X	Z	Z	Z	Z

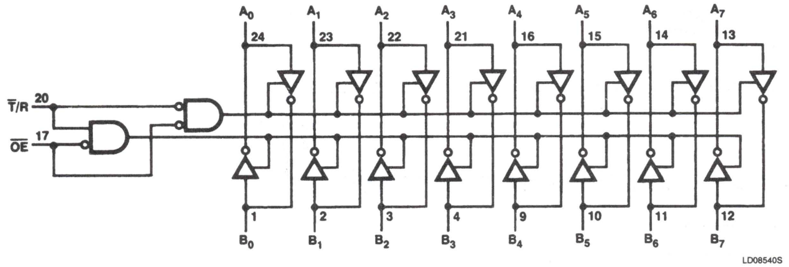
H = High voltage level
L = Low voltage level
X = Don't care
Z = High-impedance

LOGIC DIAGRAM 'F30245


A0
A1
A2
A3
A4
A5
A6
A7
24
23
22
21
16
15
14
13
T/R 20
OE 17
1
2
3
4
9
10
11
12
B0
B1
B2
B3
B4
B5
B6
B7
LD08530S

NOTES:
V_{CC} = Pin 18, 19
GND = Pin 5, 6, 7, 8

LOGIC DIAGRAM 'F30640


A0
A1
A2
A3
A4
A5
A6
A7
24
23
22
21
16
15
14
13
T/R 20
OE 17
1
2
3
4
9
10
11
12
B0
B1
B2
B3
B4
B5
B6
B7
LD08540S

NOTES:
V_{CC} = Pin 18, 19
GND = Pin 5, 6, 7, 8

PACKAGE OUTLINES for HERMETIC CERDIP

1. Controlling dimensions are given in inches and millimeters in parentheses.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.

2.1 ⊕ is a geometric characteristic symbol meaning the accuracy of a position.

2.2 "T", "D", and "E" are reference datums on the body and include allowance for glass overrun and meniscus on the seal line and lid to mismatch.

2.3 "S" is a modifying symbol and means "regardless of features".

2.4 "M" is a modifying symbol and means "at a maximum material condition".

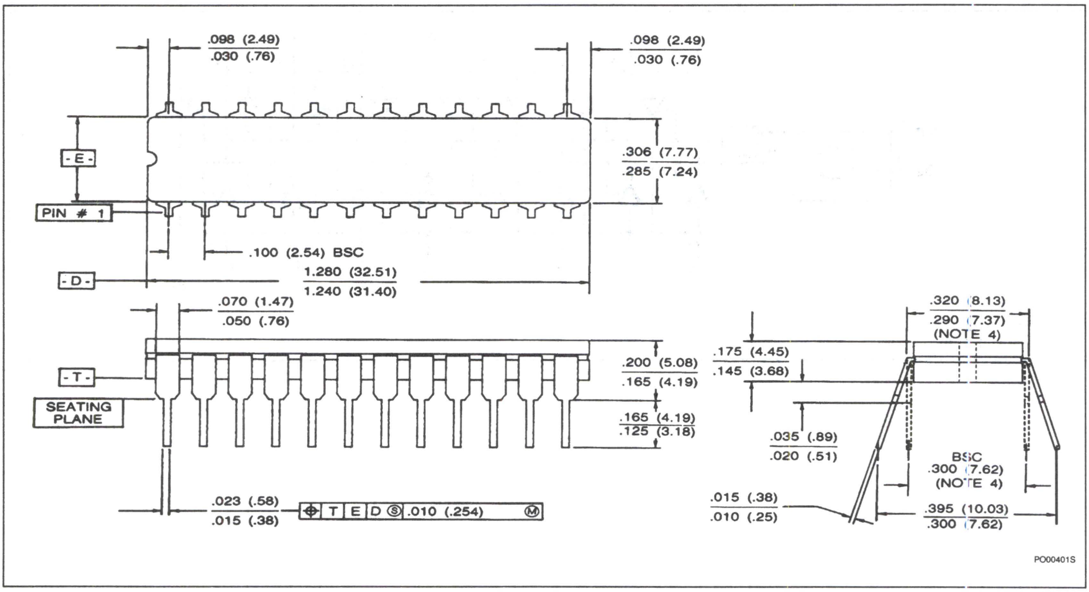
4. These dimensions measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with pin #1 and continue counter-clockwise when viewed from the top.
6. Lead material: ASTM Alloy F-30 (Alloy 42) or equivalent-tin plated or solder dipped.
7. Body Material: Ceramic with glass seal at leads.
8. Thermal resistance values for N74F30245F/N74F30640F in 24-pin CERDIP (300mil) package:

θ_{JA} = 70°C/W
θ_{JC} = 11°C/W

Test conditions:
Test ambient – still air
Power dissipation – 1.0W
Test fixture
θ_{JA} = Textool ZIF socket with .040" stand-OFF
θ_{JC} = water cooled heat sink

Thermal resistance values are determined by temperature sensitive parameter (TSP) method. This method uses the forward voltage drop of a calibrated diode to measure the change in junction temperature due to a known power application.

FN 24-PIN CERDIP (300MIL)


.098 (2.49)
.030 (.76)
.098 (2.49)
.030 (.76)
-E-
.306 (7.77)
.285 (7.24)
PIN # 1
.100 (2.54) BSC
-D-
1.280 (32.51)
1.240 (31.40)
.070 (1.47)
.050 (.76)
-T-
SEATING PLANE
.200 (5.08)
.165 (4.19)
.165 (4.19)
.125 (3.18)
.023 (.58)
.015 (.38)
⊕ T E D Ⓢ .010 (.254) Ⓜ
.175 (4.45)
.145 (3.68)
.035 (.89)
.020 (.51)
.015 (.38)
.010 (.25)
.320 (8.13)
.290 (7.37)
(NOTE 4)
BSC
.300 (7.62)
(NOTE 4)
.395 (10.03)
.300 (7.62)
PO00401S

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		−0.5 to +7.0	V
V_{IN}	Input voltage		−0.5 to +7.0	V
I_{IN}	Input current		−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		−0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	$A_0 - A_7$	320	mA
		$B_0 - B_7$	48	mA
T_A	Operating free-air temperature range		0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		74F30245, 74F30640			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
V_{OH}	High-level output voltage	$A_0 - A_7$			4.5	V
I_{OH}	High-level output current	$B_0 - B_7$			−3	mA
I_{OL}	Low-level output current	$A_0 - A_7$			160	mA
		$B_0 - B_7$			24	mA
T_A	Operating free-air temperature		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]			74F30245, 74F30640			UNIT
							Min	Typ[2]	Max	
I_{OH}	High-level output current		B_0–B_7	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, V_{OH} = MAX					250	μA
V_{OH}	High-level output voltage		$A_0 - A_7$ $R/\overline{T}$, $\overline{OE}$	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = −3mA	±10%V_{CC}	2.4			V
						±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		$A_0 - A_7$ $R/\overline{T}$, $\overline{OE}$	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 24mA	±10%V_{CC}		0.35	0.50	V
						±5%V_{CC}		0.35	0.50	V
			$B_0 - B_7$		I_{OL} = 100mA	±10%V_{CC}		0.40	0.55	V
					I_{OL1} = 160mA[4]	±5%V_{CC}			0.80	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, $I_I = I_{IK}$				−0.73	−1.2	V
I_I	Input current at maximum input voltage		$\overline{T}/R$, $\overline{OE}$	V_{CC} = 0.0V, V_I = 7.0V					100	μA
			A_n, B_n	V_{CC} = 5.5V, V_I = 5.5V					1.0	mA
I_{IH}	High-level input current		$\overline{T}/R$, $\overline{OE}$	V_{CC} = MAX, V_I = 2.7V					40	μA
			$B_0 - B_7$						20	μA
I_{IL}	Low-level input current		$\overline{T}/R$, $\overline{OE}$	V_{CC} = MAX, V_I = 0.5V					−40	μA
			$B_0 - B_7$						−600	μA
$I_{OZH} + I_{IH}$	OFF-state output current, High-level voltage applied		$A_0 - A_7$	V_{CC} = MAX, V_O = 2.7V					70	μA
$I_{OZL} + I_{IL}$	OFF-state current, Low-level voltage applied		$A_0 - A_7$	V_{CC} = MAX, V_O = 0.5V					−70	μA
I_{OS}	Short-circuit output current[3]		$A_0 - A_7$	V_{CC} = MAX			−60		−150	mA
I_{CC}	Supply current (total)	I_{CCH}	'F30245	V_{CC} = MAX				45	70	mA
		I_{CCL}						85	135	mA
		I_{CCZ}						55	75	mA
		I_{CCH}	'F30640	V_{CC} = MAX				40	60	mA
		I_{CCL}						75	130	mA
		I_{CCZ}						45	65	mA

NOTES:

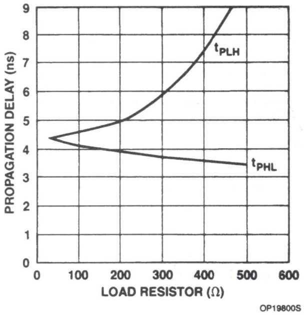
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of High-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and to more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. I_{OL1} is the current necessary to guarantee the High to Low transition in a 30Ω transmission line on the incident wave.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	74F30245, 74F30640					UNIT
				$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
				Min	Typ	Max	Min	Max	
*t_{PLH} t_{PHL}	Propagation delay A_n to B_n	'F30245	Waveform 1, 2	7.5 3.0	9.5 5.5	13.5 8.5	7.0 3.0	13.5 9.5	ns
t_{PLH} t_{PHL}	Propagation delay B_n to A_n		Waveform 1, 2	2.0 1.0	3.5 2.5	6.5 5.5	1.5 1.0	7.0 5.5	ns
*t_{PLH} t_{PHL}	Propagation delay A_n to B_n	'F30640	Waveform 1, 2	7.5 1.0	10.0 2.0	13.0 5.0	7.5 1.0	13.5 5.5	ns
t_{PLH} t_{PHL}	Propagation delay B_n to A_n		Waveform 1, 2	1.0 1.0	2.5 2.0	5.5 5.0	1.0 1.0	6.0 5.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{OE}$ to B_n	B_n outputs	Waveform 1, 2	7.0 3.5	9.5 5.5	12.5 8.5	7.0 3.5	13.0 9.5	ns
t_{PZH} t_{PZL}	Output Enable time from High to Low	A_n outputs	Waveform 3 Waveform 4	2.5 2.0	4.5 4.0	7.5 8.0	2.0 1.5	8.0 8.5	ns
t_{PHZ} t_{PLZ}	Output Enable time to High or Low	A_n outputs	Waveform 3 Waveform 4	1.5 1.0	3.5 3.5	6.5 6.5	1.0 1.0	7.5 7.0	ns

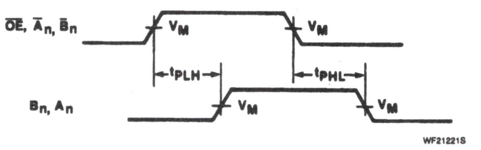
* See Figure A for Open-Collector Output Information

TYPICAL PROPAGATION DELAYS VERSUS LOAD RESISTOR FOR OPEN-COLLECTOR OUTPUTS

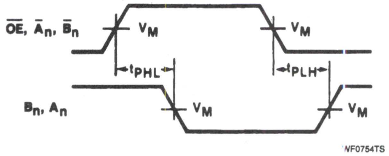


NOTES:
When using Open-Collector parts, the value of the pull-up resistor greatly affects the value of the t_{PLH}. For example, changing the specified pull-up resistor value from 500Ω to 100Ω will improve the t_{PLH} up to 50% with only a slight increase in the t_{PHL}. However, if the value of the pull-up resistor is changed, the user must make certain that the total I_{OL} current through the resistor and, thus the total I_{IL}s of the receivers does not exceed the I_{OL} maximum specification.

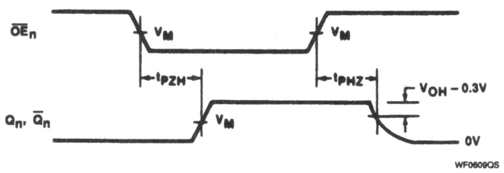
AC WAVEFORMS


OE, An, Bn
VM
VM
tPLH
tPHL
Bn, An
VM
VM
WF21221S

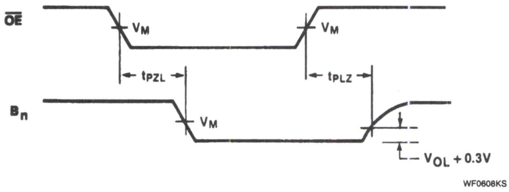
Waveform 1. Propagation Delay for Data to Output


OE, An, Bn
VM
VM
tPHL
tPLH
Bn, An
VM
VM
WF0754TS

Waveform 2. Propagation Delay for Data to Output


OEn
VM
VM
tPZH
tPHZ
VOH – 0.3V
Qn, Qn
VM
0V
WF0609QS

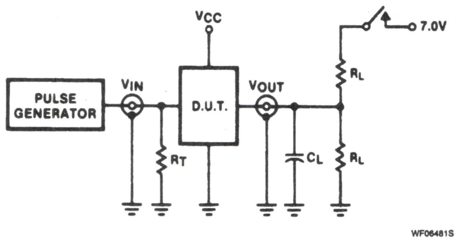
Waveform 3. 3-State Enable Time to High Level and Disable Time From High Level


OE
VM
VM
tPZL
tPLZ
Bn
VM
VOL + 0.3V
WF0608KS

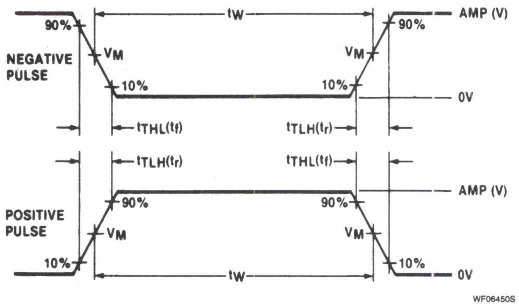
Waveform 4. 3-State Enable Time to Low Level and Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORMS


VCC
7.0V
RL
PULSE GENERATOR
VIN
D.U.T.
VOUT
RT
CL
RL
WF06481S

Test Circuit for 3-State and Open-Collector (OC) Outputs


90%
tW
90%
AMP (V)
NEGATIVE PULSE
VM
VM
10%
10%
0V
tTHL(tf)
tTLH(tr)
tTLH(tr)
tTHL(tf)
AMP (V)
90%
90%
POSITIVE PULSE
VM
VM
10%
tW
10%
0V
WF06450S

$V_M = 1.5V$

Input Pulse Definitions

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
OC	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Section 7
FAST Application Notes

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Signetics

AN202

Testing And Specifying FAST Logic

Application Note

FAST Products

INTRODUCTION

FAST^{TM} is a second generation Schottky logic family that utilizes advanced oxide-isolation techniques to increase the speed and decrease the power dissipation beyond the levels achievable with conventional junction-isolated families. The improved performance of the family is exhibited in two ways — first, the speed and power characteristics of the devices are improved, and second, the conditions under which speed and power are specified are much tighter. For instance, LS and S TTL families offer AC limits only at a nominal +5.00V V_{CC} supply voltage and at room temperature, 25°C. By contrast, FAST guarantees improved AC performance and specifies that performance over a supply variation of +5.00V ±10% and at temperatures from 0°C to 70°C. Thus the designer no longer needs to derate his propagation delays from the data sheet limits to compensate for speed degradation over the temperature range.

With every advance of this magnitude, there arise new considerations that must be kept in mind both by the system designer and the user setting up test procedures. FAST is no exception, and it is these considerations that will be addressed in this application note. This paper represents an attempt to describe the way the FAST logic parts are specified, why they are spec'd in the way they are, and how the parts may be tested in the qualification lab and at incoming inspection to verify their performance.

THE FAST DATA SHEET PHILOSOPHY

Signetics FAST data sheets have been configured with an eye to quick useability . . . they are self contained and should require no reference to other sections for information. The typical propagation delays listed at the top of the page are the average between t_{PLH} and t_{PHL} for the most significant data path through the part. In the case of clocked products, this is sometimes the max frequency of operation, but in any event this number is a 5.00V - 25°C typical specification. The I_{CC} typical current shown in that same specification block is the average current (in the case of a gate, this will be the average of the I_{CCH} and I_{CCL} currents) at room temperature and V_{CC} = 5.00V. It represents the total current through the package, not the *current through individual functions.*

Other considerations are the Fanout And Loading tables. Some manufacturers relate these numbers in terms of 7400 gate loads . . . Signetics feels that FAST is unlikely to be mixed with other logic families and so gives the loading factors in terms of FAST unit loads. A FAST unit load is defined to be 0.6mA in the Low state and 20μA in the High state. Thus in the case of the 74F00 gate, the inputs are specified as 1 Ful (FAST unit load) each . . . the outputs need a little explanation. The standard FAST output is specified with an I_{OL} sink current of 20mA and an I_{OH} of +1.0mA. Thus the fanout of this gate in the Low state is 20mA/0.6mA or 33 FAST unit loads. In the High state the fanout is 1mA/20μA or 50 FAST unit loads. In each case, the Fanout and Loading Table on the Signetics data sheets states the High/Low fanout numbers . . . thus the 74F00 output fanout is specified as 50/33 Ful.

ABSOLUTE MAXIMUM RATINGS

The Absolute Maximum Ratings table carries the maximum limits to which the part can be subjected without damaging it . . . there is no implication that the part will function at these extreme conditions. Thus, specifications such as the most negative voltage that may be applied to the outputs only guarantees that if less than -0.5V is applied to the output pin, after that voltage is removed the part will still be functional and its useful life will not have been shortened — it is difficult to imagine the meaning of the term "functionality" WHILE that voltage is applied to the output.

Input voltage and output voltage specification in this table reflect the device breakdown voltages in the positive direction (+7.0V) and the effect of the clamping diodes in the negative direction (-0.5V).

RECOMMENDED OPERATING CONDITIONS

The Recommended Operating Conditions table has a dual- purpose. In one sense, it sets some environmental conditions (operating free-air temperature), and in another, it sets the conditions under which the limits set forth in the DC Electrical Characteristics table and AC Electrical Characteristics table will be met. Another way of looking at this table is to think of it, not as a set of limits guaranteed by Signetics, but as the conditions Signetics uses to test the parts and guarantee that they will then meet the limits set forth in the DC and AC Electrical Characteristics tables.

Some care must be used in interpreting the numbers in this table. Signetics feels strongly that the specifications set forth in a data sheet should reflect as accurately as possible the operation of the part in an actual system. In particular, the input threshold values of V_{IH} and V_{IL} can be tested by the user with parametric test equipment . . . if V_{IH} and V_{IL} are applied to the inputs, the outputs will be at the voltages guaranteed by the DC Electrical Characteristics table providing that there is adequate grounding and the input voltages are free from noise, otherwise a guardbanded V_{IH} and V_{IL} should be used, ie., 2.5V instead of 2.0V and .5V instead of .8V. There is a tendency on the part of some users to use V_{IH} and V_{IL} as conditions applied to the inputs to test the part for functionality in a "truth-table exerciser" mode. This frequently causes problems because of the noise present at the test head of automated test equipment. Parametric tests, such as those used for the output levels under the V_{IH} and V_{IL} conditions are done fairly slowly, on the order of milliseconds, and any noise present at the inputs has settled out before the outputs are measured. (This is not the case with clocked or enabled parts and poor or moderate fixturing may induce oscillations or severe ground bounce if noise is present.) But in functionality testing, the outputs are examined much faster, before the noise on the inputs are settled out and the part has assumed its final and correct output state. Since these are unloaded outputs, having faster edge rates, this causes more noise. If the outputs are loaded, the 50pF per output pin can cause substantial ground bounce. Thus V_{IH} and V_{IL} should never be used in testing the functionality of any TTL part including FAST. For these types of tests input voltages of +4.5V and 0.0V should be used for the High and Low states respectively.

In no way does this imply that the devices are noise sensitive in the final system. The use of "hard" Highs and Lows during functional testing is done primarily to (1) reduce the effects of the large amounts of noise typically present at the test heads of automated test

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TMFAST is a trademark of Fairchild Camera and Instrument Corporation.

equipment with cables that may at times reach several feet and (2) deal with testing parts exhibiting fast edge rates and 50pF per output pin. The situation in a system on a PC board is less severe than in a noisy production environment.

DC ELECTRICAL CHARACTERISTICS

This table reflects the DC limits used by Signetics during its testing operations and conducted under the conditions set forth under the Recommended Operating Conditions table. V_{OH}, for example, is guaranteed to be no less than 2.7V when tested with $V_{CC} = +4.75V$, $V_{IH} = 2.0V$, $V_{IL} = 0.8V$, across the temperature range from 0° to 70°C, and with an output current of $I_{OH} = -1.0mA$. In this table, one sees the heritage of the original junction isolated Schottky family . . . $V_{OL} = 0.5V$ at $I_{OL} = 20mA$. This gives the user a guaranteed worst-case Low state noise immunity of 0.3V. In the High state the noise immunity is 0.7V worst case. Although at first glance it would seem one-sided to have greater noise immunity in the High state than in the Low, this is a useful state of affairs. Because the impedance of an output in the High state is generally much higher than in the Low state, more noise immunity in the High state is needed. This is because the noise source couples noise onto the output connection of the device — that output tries to pull the noise source down by sinking the energy to ground or to V_{CC} depending on the state. The ability of the output to do that is determined by its output impedance. The lower half of the output stage is a very low-impedance transistor which can effectively pull the noise source down. Because of the higher impedance of the upper stage of the output, it is not as effective in shunting the noise energy to V_{CC}, so that an extra 0.4V of noise immunity in the High state compensates for the higher impedance. The result is a nice balance of sink and drive current capabilities with the optimum amount of noise immunity in both states.

I_I, the maximum input current at maximum input voltage, is a measure of the input leakage current at the guaranteed minimum input breakdown voltage of 7.0V. Although some users consider this to be a test of the input breakdown itself, that voltage is typically over 15V. At room temperature, this leakage current should be less than 10μA. (This is not the case with NPN input designed parts.)

Short-Circuit Output Current is a parameter that has appeared on digital data sheets since the inception of integrated circuit logic devices, but the meaning and implications of that *specification* have totally changed. Originally I_{OS} was an attempt to reassure the user that if a stray oscilloscope probe accidentally shorted an output to ground the device would not be damaged. In this manner, an extremely long time was associated with the I_{OS} test. However, thermally induced malfunctions could occur after several seconds of sustained test. Over a period of time, I_{OS} became a measure of the ability of an output to charge line capacitance. Assume a device is driving a long line and is in the Low state. When the output is switched High, the rise time of the output waveform is limited by the rate at which the line capacitance can be charged to its new state of V_{OH}. At the instant that the output switches, the line capacitance looks like a short to ground. I_{OS} is the current demanded by the capacitive load as the voltage begins to rise and the demand decreases. The full value of I_{OS} need only be supplied for a few hundred microseconds at most, even with 1.0μFd of line capacitance tied to the output, a load that is unrealistically high by several orders of magnitude.

The effective of a large I_{OS} surge through the relatively small transistors that make up the upper part of the output stage is not serious, AS LONG AS THAT CURRENT IS LIMITED TO A SHORT DURATION. If the hard short is allowed to remain, the full I_{OS} current will flow through that output state and may cause functional failure or damage to the structure. A test induced failure may occur if the I_{OS} test time is excessive. As long as the I_{OS} condition is very brief, typically 50ms or less with ATE equipment, the local heating does not reach the point where damage or functional failures might occur. As we have already seen, this is considerably longer than the time of the effective current surge that must be supplied by the device in the case of charging line capacitance. The Signetics data sheet limits for I_{OS} reflect the conditions that the part will see in the system — full I_{OS} spikes for extremely short periods of time. Problems could occur if slow test equipment or test methods ground an output for too long a time causing functional failure or damage.

AC TESTING

FAST data sheets carry several types of AC information. The AC Characteristics table contains the guaranteed limits when tested under the conditions set forth under the AC Test Circuits And Waveforms. In some cases, the test conditions are further defined by the AC Setup Conditions — this is generally the case with counters and flip-flops where setup and hold times are involved. All of the AC Characteristics are guaranteed with 50pF load capacitances and with the fewest number possible of outputs switching, depending upon the functionality of the device. One of the sets of limits is spec'd at 25°C and +5.00V V_{CC} — these relate closely to the standard Schottky specifications which are under similar conditions but use only 15pF load capacitances. While these numbers are convenient for comparing the two families, keep in mind that using full 50pF loads with the Schottky devices would add several nanoseconds to their propagation delays. These numbers are ideal for checking out test jigs and correlating data since they do not involve temperature or supply voltage spreads. For system design, full specifications are included that include temperature and supply voltage variations — in one case the military ranges and in the other, the commercial ranges.

AC TEST JIGS AND SETUPS

Each FAST data sheet spells out the test circuit used to check AC performance, the waveforms, measurement points, rep rate, test loads, etc. But there are only the quantifiable variables involved in this testing. There is another more complex side to the issue — test jigs and equipment setups.

To get an appreciation for the problems involved in testing FAST, consider these facts. The output rise and fall times on FAST outputs are very sharp. Translating these edge rates into the effective sine wave equivalents generates frequencies on the order of several hundred MHz. At these frequencies, attention to RF phenomena is required.

Because of these RF frequencies, it is necessary to have an AC test jig that has minimal modifying effect on the input and output waveforms. To do this the jig must be constructed properly. The following items are key in dealing with AC jig construction.

BYPASSING CAPACITORS

Signetics uses high quality capacitors that have good RF qualities to decouple the power supply lines on the test jig, right at the V_{CC} pin to the ground plane. Four capacitors with absolute minimum lead length are used. Microwave chip capacitors are recommended. (Note: In some sensitive test environments it is advisable to decouple the V_{CC}, as well as bypass. This is done by passing the V_{CC} through a wire wrapped around a ferrite core 6 – 8 times. The inductor created helps decouple the noise from V_{CC} and reduces dramatically, the tendency for feedback oscillations through the V_{CC} and ground current loop. This is a key problem on clocked parts since the ground bounce created by the fast edge rates and high currents will effect V_{CC} and ground substantially and thereby effect internal thresholds.) These are one each, 10μFd dipped tantalum, 0.1μFd dipped tantalum or chip, .001μFd chip and 100pF chip.

Testing And Specifying FAST Logic AN202

GROUNDING

One of the biggest contributors to waveform degradation is improper grounding. In reference up to the test jig, the grounding is best done with one or more large ground planes that are directly connected to the ground pin of the test socket. The Signetics AC Test Jigs, both DIP and SO styles, are constructed as a four layer PC board with the 2 internal layers as ground planes. Ground planes are also interdigitated between all signal lines to decrease crosstalk. There are holes drilled in these and they are plated through to connect with the internal 2 layers and the top and bottom layers. See Figure 3 to see the interdigitated ground planes on the PCB layout of the SO jig. This grounding scheme has been used with great success in 10k and 100k ECL fixturing. The board is laid out so that the characteristic impedance of the signal lines is 50Ω. This is done by using industry standard stripline techniques. The ground plane also passes down through the center of the part on the bottom side of the board and ground pin is soldered to it using copper wire to connect the pin and the ground plane. On the top side of the board, the V_{CC} plane goes through the center of the part too, and connects to the V_{CC} pin in like manner as the ground pin. See Figure 1. The bypass capacitors are attached on the bottom side to the V_{CC} pin from the ground plane, see Figure 1. As the V_{CC} is brought on board, the V_{CC} wire is wrapped around a ½ inch ferrite core, 6-8 times, then makes connection with the V_{CC} plane on the top side.

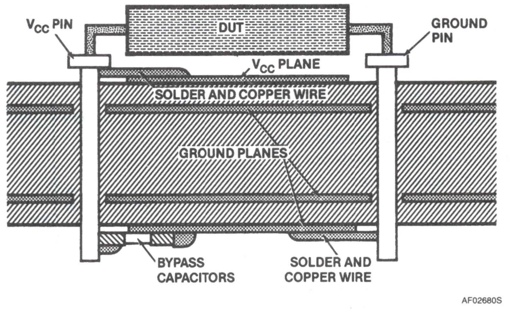


Figure 1

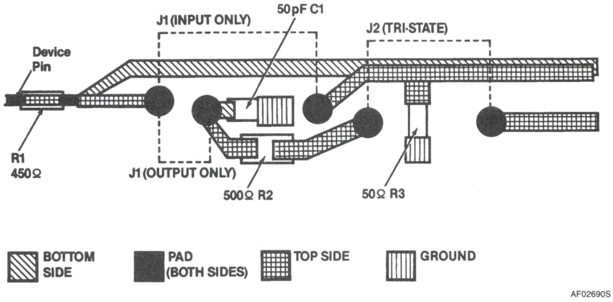


Figure 2a. FAST AC Test Fixture — Board Layout

INTERCONNECTS

The next concern is getting the input signal to the part and the output signal to the measurement system. As stated before, the Signetics jig is laid out for a 50Ω characteristic impedance. We recommend that the user maintain a 50Ω environment for the input signal as close as possible to the input pin and then terminate in 50Ω. On our jig, we terminate with a 50Ω chip resistor. The signal is brought on board through an SMB connector to the 50Ω trace on the top side of the board. The signal is terminated by the chip resistor, R3, see Figure 2a and 2b. The signal proceeds to the DUT pin, a distance of about .5 inches, through Jumper 1 (in the Input Only position), and the rest of the trace. The same pin on the opposite side of the board has a 450Ω chip resistor soldered to it. The other side of this resistor, R1, is soldered to a 50Ω trace on the bottom side of the board that runs to an SMB connector on the edge of the jig. This connects to the 50Ω input of the Sampling Oscilloscope. This 450Ω resistor in series with the 50Ω input of the scope creates a 10X divided 500Ω probe for the scope and provides impedance matching for the scope. See Figure 2b. This circuit also doubles as the resistive portion of the FAST AC Output Load and thereby allows the output to be sensed in the same fashion. When the input is not used for a signal or generator input, the line may be switched to one of three voltage sources. V_S 1 – V_S 3, by the use of a DIP switch on each pin. It may also be left open and then the 50Ω pull-down resistor that is used for an input terminator, pulls the line to ground and can be used as a hard low level. See Figure 2b. This scheme eliminates excessive cabling to each input to provide static input levels and thereby reduces parasitic inductances and cross-talk. It also eliminates the need for bulky and sometimes unreliable high impedance probes by using the 50Ω input of the Sampling Scope. With the designed-in flexibility of Jumper 1 and Jumper 2, and the selectable nature of V_{CC} and Ground pin designations, one can configure this board for any V_{CC} and Ground pin designations, select which pins are outputs or inputs and even provide the proper pull-up for 3-state outputs. This makes the board entirely universal for designated V_{CC}/Ground configurations. To explain this, the output of the device is connected to its capacitive load by Jumper 1 in the Output Only position. This means that no pin can be both output and input at the same time, but can be either. Jumper 2 allows an output to be connected to the 3-state pull-up resistor, R2, and have that connected to the needed 7V. See Figure 2a and 2b. The scope is connected in the same way as the input, with the 450Ω resistor and the 50Ω of the scope comprising the 500Ω needed for the FAST load. One other consideration exists. In small part quantity testing, the elimination of a socket is very desirable, using inserted pins that are flush with the jig. In larger quantity testing, sockets may be needed, however. If this is the case, some degradation in the performance will occur due to the increased lead inductance for each pin, which is observable, and the addition of group delay through the socket may alter or affect the readings obtained.

HIGH-FREQUENCY DESIGN

The exact jig delay time is determined by the size of the universal jig that is being used. It is important to know that the frequency response of the jig must be High to prevent any delay factor from varying with the edge rates. The frequency response of the jig indicates how constant the impedance remains over frequency. The characteristic impedance of a transmission line is expressed as . . .

$$Z_o = \frac{V}{I} = \sqrt{\frac{L_o}{C_o}}$$

Where L_o is the inductance per unit length, C_o is the capacitance per unit length, Z_o is in Ohms, L_o in Henrys, and C_o in Farads. Propagation velocity and its inverse, delay per unit length d, are also expressed in L_o and C_o. . .

$$V = \frac{1}{\sqrt{L_o\ C_o}} \qquad \delta = \sqrt{L_o\ C_o}$$

where δ is expressed in nanoseconds, L_o is in microhenrys per unit length, and C_o in microfarads per unit length. From this, it is clear that if the Z_o changes over frequency, then the delay per unit length will vary as well. Therefore, it is imperative to know how the jig responds over frequency and that all measurement line lengths are identical.

Frequency response also depends on the phase as well as the magnitude of the impedance. If the phase changes so does the delay, since delay is the derivative of phase change with frequency. An S-parameter analysis is needed in evaluating jig performance.

UNIVERSAL JIG CONSTRUCTION

Jig universality is with respect to chip pin count and V_{CC} and ground pin placements and as such, separate universal test jigs are built for 14, 16, 20, 24, and 28 pin parts.

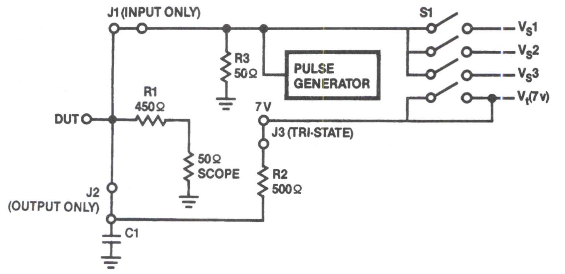


Figure 2b. FAST AC Test Fixture — Schematic

An S-parameter analysis was performed in a network analyzer to optimize the jig layout. This assured that the jig had a flat frequency response over the spectrum of interest for FAST products. Figure 2b shows the schematic of the fixture and Figure 2a shows a drawing of the board layout, component placement and signal paths. The equipment used to analyze the jigs and loads was: HP8505A Network Analyzer, HP8503A S-Parameter Test Set, HP8501A Storage Normalizer. In some measurements the equipment was driven by an HP9845B desk-top computer.

Jigs produced in this way should have minimal lead length to reduce the characteristic inductance. This in turn minimizes reflections with their accompanying waveform distortions and measurement inaccuracies.

AC TEST LOADS FOR THE SIGNETICS UNIVERSAL JIG

As stated previously, the Network Analyzer was also used to design and optimize AC test loads to be used with the universal jig. FAST product loads require 50pF load capacitance and 500Ω resistance to ground.

Signetics meets the 50pF requirement through the use of a 45pF load, 4pF jig capacitance, and 3pF probe capacitance. The result, 52pF, is slightly more stringent than required.

A few words about load capacitors are in order. All capacitors have an associated inductance. Due to this inductance, a capacitor will form a series resonant circuit at some frequency. For single 50pF capacitors, this typically occurs between 200 and 600MHz depending on the type of capacitor. Above this resonant frequency, the capacitor has inductive characteristics and does not present a capacitive load. This is very important with FAST because harmonics due to the sharp edge transition rates occur at 600MHz and above.

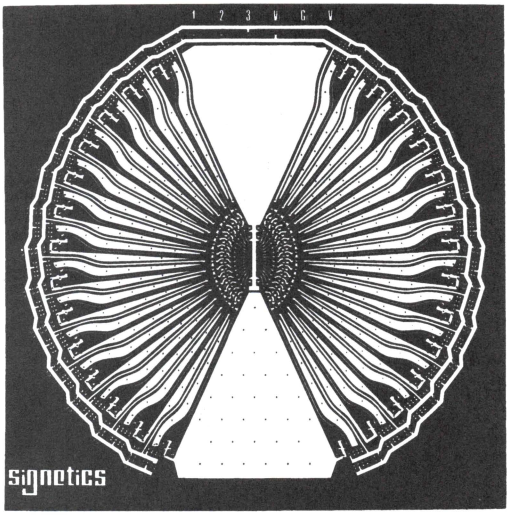
The Signetics FAST loads solve this problem by reducing the load capacitor lead inductance by paralleling three 15pF chip capacitors. The resulting load is 45pF. At the same time, since smaller value caps are used to build up the capacitive load, the associated series resonant point is above 1.2GHz.

The load resistors are 1/8W selected 510Ω ± 10Ω chip resistors.

The entire load assembly is constructed on the jig PCB along with the input termination, and the jumpers with select an input or output path. The load circuit is detailed on the FAST data sheets for 3-state parts.

CORRELATION

While numerous ATE systems are available and are very efficient, it is imperative that the ATE correlate to a user's bench setup. Since the Signetics FAST parts are all characterized on the setup described in this note, it is just as important that the user bench jigs meet the same performance criteria. Without similar jigs, it will be very difficult to correlate AC data.


1 2 3 V G V
signetics

CD07580S

Figure 3

Signetics

AN203
Test Fixtures for High-Speed Logic

Application Note

FAST Products

INTRODUCTION

The Signetics Standard Products Division (SPD) operates a Characterization Laboratory in Orem, Utah. This Lab maintains the capability of testing the 11 logic product families the Division supports. These include: AuTTL-74XXX, Schottky-74SXXX, Low-Power Schottky-74LSXXX, FAST-74FXXX, ALS-74ALSXXX, High-Speed CMOS-74HCXXX, High-Speed CMOS/TTL-74HCTXXX, Advanced CMOS/TTL (ACL)-74ACT11XXX, Advanced CMOS (ACL)-74AC11XXX, and both 10K and 100K ECL.

Due to the great diversity of product families and the different testing requirements and complexity of the product types of each family, Signetics SPD Characterization has designed and built a bench test AC fixture that is specifically designed to address to only the High-speed logic families. It has the advantages of being very versatile, has high bandwidth capability (⩾750MHz), is 50Ω system compatible, and is manually programmable for the input static voltages. This provides the ability to have one fixture that addresses many product types across families. The extent of this versatility is explained in the following Application Note. The families that this fixture is intended to support are: FAST, ALS, ACL, 10K ECL, and 100K ECL (Note: This fixture is compatible with any 500Ω pull-down load.)

THEORY OF OPERATION

There are several key points in testing the faster edge-rate logic families. They are:

- Very good by-passing and decoupling (they are different).
- Large ground and V_{CC} planes
- Low-impedance signal lines (i.e., 50Ω)
- Signal lines that are uniform in impedance over frequency
- Signal lines must have high bandwidth (> 500MHz)
- Low-inductance paths for the DUT leads, including V_{CC} and GND
- Output AC load close to the DUT
- Measurement point close to the DUT
- Avoidance of ground loops (especially on inputs at DC levels)

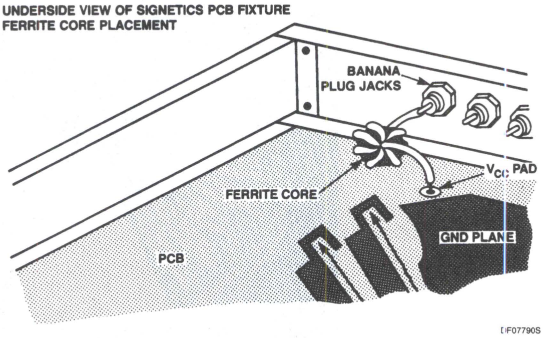


Figure 1. Ferrite Core Placement

Also of concern to the test engineer and the manager are:

- Versatility and/or ease of use (there are tradeoffs)
- Cost
- The number of fixtures needed to support products

Each of these concerns have merit and must be understood by the user of these logic families if valid and correlatable results are to be found.

V_{CC} and GND

The secret in V_{CC} and GND use in fixturing is to do the things that reduce the noise that can: 1) get to your part, and 2) come from your part. This is done by reducing the noise of the V_{CC} as it arrives to the fixture, by judicious application of frequency dependant by-passing at the DUT V_{CC} pin to GND and reducing inductance from the V_{CC} and GND pins of the DUT to the point where good contact of the by-passing and V_{CC} and GND planes occur. All of these are techniques used in good RF and microwave board design. By reducing parasitic inductances and cleaning up any sources of noise, good signal integrity is better maintained.

These points are evident in the fixture Signetics has designed. Part of the noise reduction of the power supply as it arrives is done by by-passing the power supply at its terminals. The power is then brought to the fixture via banana cables, (as short as possible), to jacks on the chassis of the fixture. An 18 gauge wire, attached to the jack, is wrapped through a ¾ inch ferrite core 8 – 12 times for decoupling of any spikes. (Details of the cores used are included in the parts list.) This acts as a Low-pass filter. The wire is then soldered to the bottom of the PC board onto the large V_{CC} plane that narrows to the V_{CC} bus running between the pins of the DUT. See Figures 1 and 2 for detail.

Triangle-shaped, the V_{CC} plane provides a Low inductive path for the V_{CC} to the DUT pin. See Figure 2 for the board layouts. The V_{CC} bus from this plane travels down between the DUT pins to that connection. This is so connection to the V_{CC} bus is easy and very short. The DUT may have V_{CC} located on any pin with this configuration. The pin is connected to the V_{CC} bus by soldering small copper braid or similar Low-inductance wire capable of carrying the current for the device, see Figure 3.

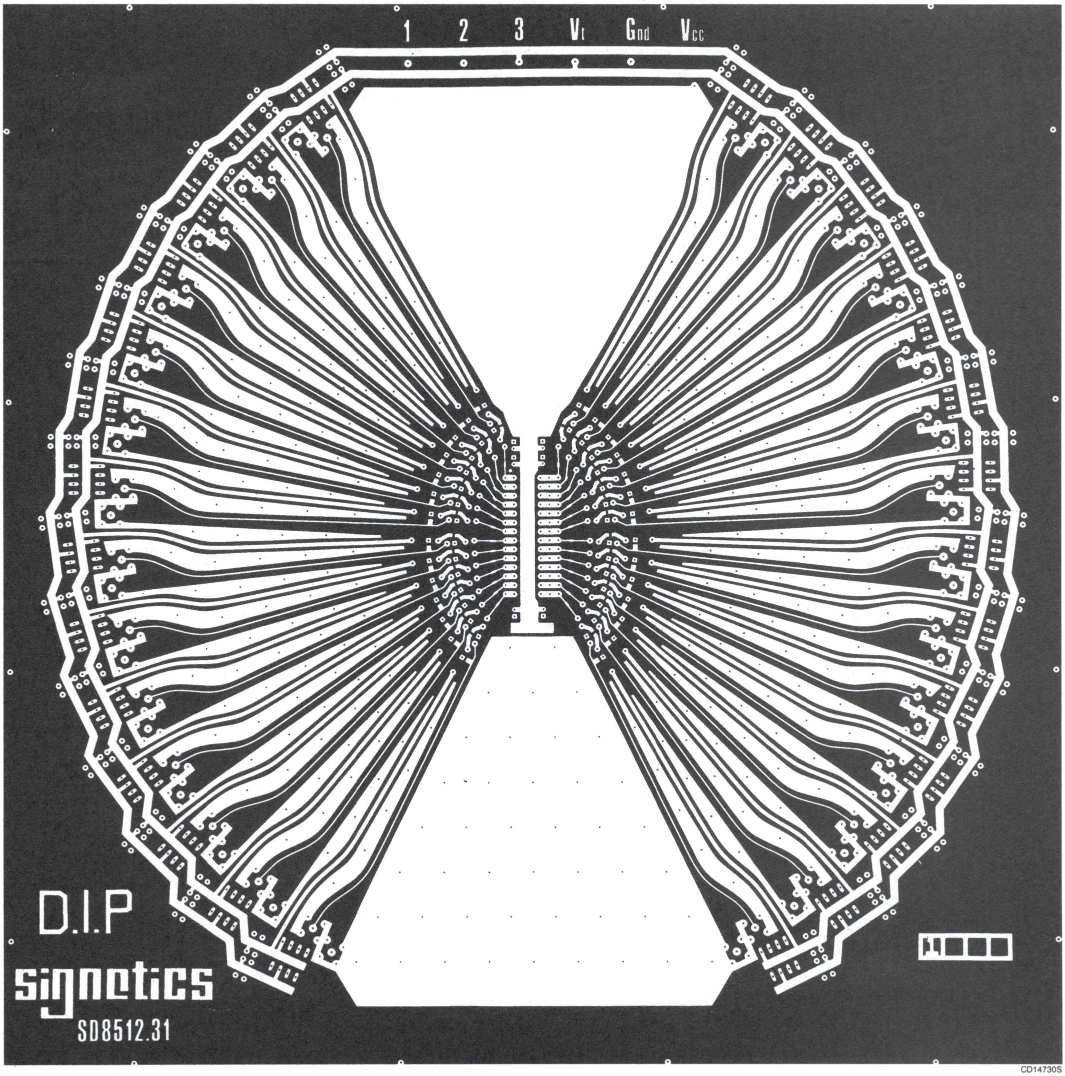

1
2
3
Vt
Gnd
Vcc
D.I.P
signetics
SD8512.31
CD14730S

Figure 2a. Board Layout - Top Side

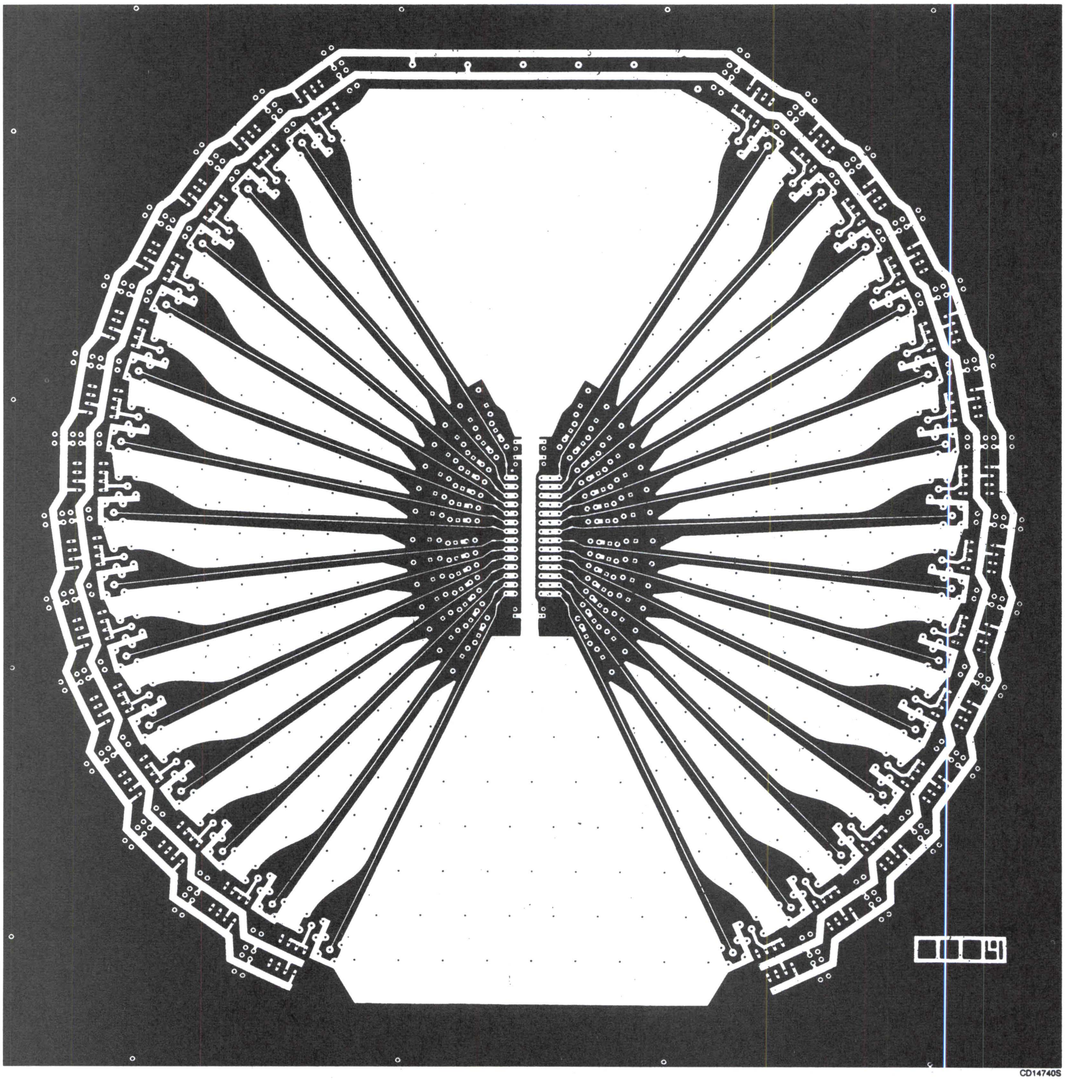


Figure 2b. Board Layout - Bottom Side

On the opposite side of the top layer of the board is a triangle-shaped ground plane. Ground planes are also located on the bottom layer of the board in the same places as the V_{CC} and ground planes of the top layer. Since this fixture is laid out for 50Ω stripline, layers 2 and 3 are almost total ground plane, with holes in them for feed-throughs and components. Also found between the signal lines, on the top and bottom layers, are ground plane "fingers" that are connected to all 4 layers by plated-through holes. This provides good separation of the signal lines resulting in lower cross-talk.

The bottom layer ground plane consists of two triangle-shaped planes connected by a bus strip that runs between the DUT pins. This was done for 3 reasons: First, this allows connection of any ground pin of the DUT to the ground, regardless of location; like the V_{CC} connection on the top layer. Second, it allows the connection of the by-pass capacitors from the V_{CC} pin to the ground with the shortest possible lead length. Characterization uses typically 2 or 3 ceramic chip capacitors and 1 or 2 dipped tantalum capacitors (35V) to by-pass the V_{CC} pin. It is important to keep the dipped tantalum capacitor's leads as short as possible to reduce series inductance. The recommended values of capacitors are: 100pf, .01μf, .1μf. and 10μf. We have found at times, the need to adjust these values depending upon the product type and its performance. Some noise sensitive circuits need more by-passing in the lower and extreme higher values of capacitance. And third, the connection of the two planes eliminates possible ground loops and the feed-throughs create a ground mesh and give an excellent ground plane for the circuit. Figure 3 illustrates the by-pass connections.

BY-PASS AND DECOUPLING

It is important to understand the difference between decoupling, as with the ferrite core, and by-passing, as with capacitors. Decoupling occurs as High-frequency signals are removed by saturation of the ferrite core. This prevents "noise" that may be on the V_{CC} power supply from getting on the V_{CC} plane. The action of the by-passing capacitors is to: 1) "pass" any non-DC signals that occur on the V_{CC} (due to the part's operation) to ground, and 2) be able to provide the "instantaneous" current demands of the part as it switches.

The various values of capacitors are intended to provide a Low-impedance path at all operating frequencies. Since real-world capacitors have resonance points at a given frequency, depending upon their value and type of capacitor (and actually turn inductive above the resonance point), using different values that have different resonance points allows an across-frequency Low-impedance path for V_{CC} noise.

An important point in the use of by-pass capacitors is the minimization of lead length. Lead length represents inductance; inductance in series with the capacitance. If it is too much, it can cause resonance and oscillation problems with the part and/or power supplies and nullify the benefit of the capacitors. It also plays a major part in inhibiting the effect of the "instantaneous" current response needed by the part from the by-pass capacitors. It actually can cause the ground of the device to track the change in current to the degree of the lead inductance. The lower the inductance, the lower the "ground bounce" effect. Hence, short or no lead lengths on capacitors are needed to help prevent the effects of ground bounce.

SIGNAL LINES

A signal line is defined as a line that carries the input stimulus, either DC or AC, or output response, to or from the device. Since these signals are measured and determine the data which characterizes the part, it is critical that they are of the highest integrity and represent, as far as physically possible, the action of the part; not the nuances of the fixture. To achieve this, the line must not be able to change the signal over the measureable frequencies of the device, nor affect the delay of the part.

The fixture as designed, has 50Ω signal lines determined by a stripline layout method. The 50Ω value was selected for several reasons: 1) the 50Ω value matches impedance with the pulse generators that are used as input stimulus. 2) The output loads specified for this fixture are either a 500Ω pull-down or a 50Ω pull-down (ECL), in parallel with a capacitive load. This allows the 50Ω signal line to be terminated into this load for either a 10:1 or a 1:1 match. 3) A Low-impedance line will have better characteristics with regards to cross-talk and resisting external noise.

There are two types of signal lines on this fixture: input and output; both of which are 50Ω transmission lines. The input line is on the top side of the board and is always terminated in 50Ω. It is connected to the DUT via a .3″ jumper, Jumper #1 for input. When this jumper is installed, the DUT pin is available only as an input. To allow this line to be used as an output, a .1″ jumper, Jumper #1 for output, is used instead of the .3″ jumper. This connects the DUT pin to the AC load when the DUP pin is an output. See Figure 5.

The output signal line can be dedicated two different ways. The first method, used for ECL, is to leave shorted the 50Ω trace and have it run directly into the SMB connector into the 50Ω sampling system. The second method is to cut the trace at the DUT pin and solder the 450Ω chip resistor, R1, across the cut. This, combined with the 50Ω scope, then appears to the part as either a 500Ω probe for the input signal or the 500Ω output AC load for the output signal.

The signal lines are equal length and therefore do not introduce any extraneous delay from pin to pin. We also characterized the impedance of the lines over frequency to ensure minimal distortion over the frequency range and any effective change in propagation delay caused by the relationship of inductance and group delay, see Ap Note 202. Figure 4 illustrates the frequency response of the signal lines in impedance.

This is considered to be high bandwith and encompasses the frequency range exhibited by ALS, ACL, ELC, and FAST logic families.

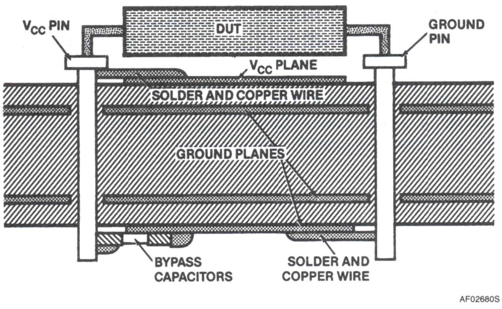


Figure 3. Decoupling Connections

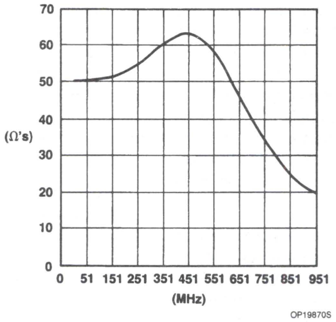


Figure 4. Signal Line Frequency Response

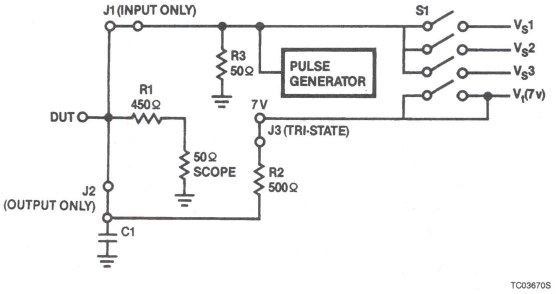


Figure 5. Signetics PCB Fixture Schematic

LOADING

The explanation of the two types of AC loads that may be used will be covered in two parts. First the ALS, ACL, and FAST implementation will be discussed, then the ECL implementation.

ALS. ACL, and FAST Implementation

The FAST, ALS, and ACL product families AC load is specified as a 50pF capacitor and a 500Ω resistor in parallel. This load has the advantage of being adaptable to both a High-impedance (A.T.E.) or a Low-impedance (bench) measurement environment. The Signetics fixture uses a Low-impedance environment primarily for two reasons. The first reason is that experience of the last 5 years has told us that High-impedance probes represent a reliability concern and can introduce hard to detect errors into the waveform. The second reason being that most suppliers of these technologies provide data based upon the Low-impedance approach and most large users of these products do so as well. This also allows the fixture to be used for ECL testing since that product uses a totally 50Ω environment. Figure 5 illustrates how this test fixture implements the 50pF/500Ω load schematically.

The fixture was laid out to present the load as close as possible to the device, and yet allow for flexibility in deciding if a certain pin is an output or an input. This distance is critical due to its inductive effect upon ground bounce phenomena. *It is acknowledged here that a fixture dedicated to a single device type without jumpers, and therefore placing the load virtually on the pin of the device, would show the ground bounce phenomena for simultaneous switching to be less than that of this fixture. However, this fixture can be so dedicated by not using the pads as provided, but rather by using the ground bus, like the by-pass capacitors used. The flexibility of this fixture substantially reduces the cost of fixturing for these families. Studies on simultaneous switching with this fixture have shown dramatically favorable results to previous fixtures. Those studies continue. For work other than that of simultaneous switching, there will be no appreciable difference with a dedicated fixture.*

As illustrated in Figure 5, the load is shared with the 50Ω input of the measurement system; a 50Ω sampling oscilloscope. The 450Ω resistor: R1, is soldered to the socket pin of the device and is in series with the 50Ω input of the scope. Figure 6 illustrates this on the board layout of one input/output pin. This allows virtually a probe tip on the device pin. The load capacitor: C1, is a 33pF ceramic chip capacitor. This is added to the measured value of 17pF of board capacitance, achieving the 50pF value specified for the load. The distance from the pin to the capacitor is .5 inches and is adequate for the testing of these product families.

For testing 3-State parameters, the 500Ω resistor: R2, is connected to it's pull-up supply. V_t via a .3″ jumper: Jumper #2. The V_t supply is bussed to each pin and may or may not be connected with that jumper. See Figures 5 and 6.

ECL Implementation

When testing ECL product, the 450Ω resistor: R1, is not used, Rather, this point is left shorted together in the construction process. Also for ECL, the load chip capacitor: C1, the tri-state pull-up resistor: R2, the 50Ω terminator: R3, and the "output only" jumper: Jumper #1, are not used. The input signal travels down the input path, is jumpered using the "input only" (Jumper #1), goes to the device, travels out the output path (left shorted, no R1), and proceeds to the scope. When the signal is an output, the "input only" jumper: Jumper #1, is removed and a 50Ω terminator is connected to the SMB connector as the load or the 50Ω input of the scope. See Figure 7.

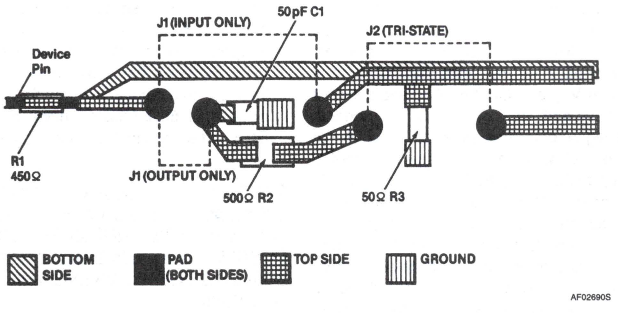

J1 (INPUT ONLY)
50pF C1
J2 (TRI-STATE)
Device Pin
R1 450Ω
J1 (OUTPUT ONLY)
500Ω R2
50Ω R3
BOTTOM SIDE
PAD (BOTH SIDES)
TOP SIDE
GROUND
AF02690S

Figure 6. Signetics Fixture - Board

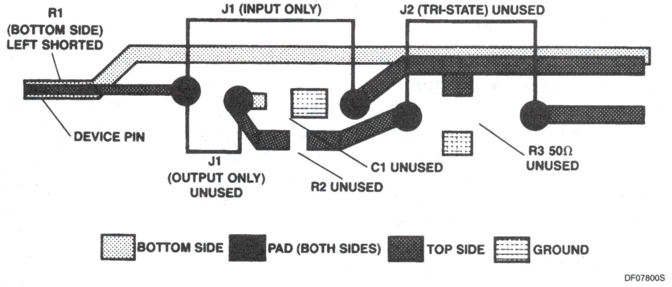

R1 (BOTTOM SIDE) LEFT SHORTED
J1 (INPUT ONLY)
J2 (TRI-STATE) UNUSED
DEVICE PIN
J1 (OUTPUT ONLY) UNUSED
R2 UNUSED
C1 UNUSED
R3 50Ω UNUSED
BOTTOM SIDE
PAD (BOTH SIDES)
TOP SIDE
GROUND
DF07800S

Figure 7. ECL Configuration

INPUT STIMULUS AND MEASUREMENT

When the input is not used for a signal input, the line may be switched to one of three voltage sources: V_s 1 through V_s 3, by the use of a DIP switch on each pin. It may also be left open and then the 50Ω pull-down resistor: R1, pulls the line to ground and can be used as a hard low level. See Figure 5. These voltage levels are brought in from external supplies through banana connectors like V_{CC}. This scheme eliminates excessive cabling to each input to provide the static input levels and thereby reduces parasitic inductances and cross-talk. Each of the 3 busses and the V_t bus all have places for by-pass capacitors in the event of noise on the static levels. Figure 8 illustrates the DIP switch and SMB connectors and how they control the input stimulus and output measurement.

As stated previously, the measurements are made with 50Ω sampling systems. The connections to these systems are made via SMB connectors. This was chosen since it is compatible with SMC; it is push-on, it is small for easy configuration, and it is capable of high bandwidth operation. Figure 8 illustrates where the connections are made, where the pulse generators connect to the input and an SMB connector. Since the 450Ω resistor: R1, is soldered directly to the pin of the device, the actual probe tip is at that point. See Figure 6. This has the advantage of eliminating any distance from the device to the probe tip, thus guaranteeing accurate results.

VERSATILITY AND COST

At some point, there is a choice between the most technically attractive options and the cost of options. This fixture has been primarily designed to optimize the cost effectiveness of test fixturing yet yielding a technically sound tool. To do this, a compromise has been made between the ease of use and the versatility.

In the construction of the fixture, a choice is made as to where the V_{CC} and GND pins are to be located. This then dedicates this particular fixture to part types with this V_{CC} and GND configurations. This is alos done with a dedicated fixture. However, on a dedicated fixture, the pins are individually constructed to be either an input or an output, and in so doing, the fixture is usable for 1-to-4 devices. The Signetics fixture, once dedicated to a particular V_{CC} and GND configuration, is built up to have both input and output components on all signal pins. The selection of which pin is an output or an input is made by inserting the appropriate jumper, See Figures 5 and 6. The same applies in doing tri-state testing. The tradeoff here is that it would probably take less time to setup the dedicated fixture than the Signetics fixture. To help compensate for that tradeoff, we have the three Vs supplies that may be switched into any pin to provide input static levels and eliminate the need to bus input High or Low levels by external cabling. For the user that means the only connections being made to the fixture are:

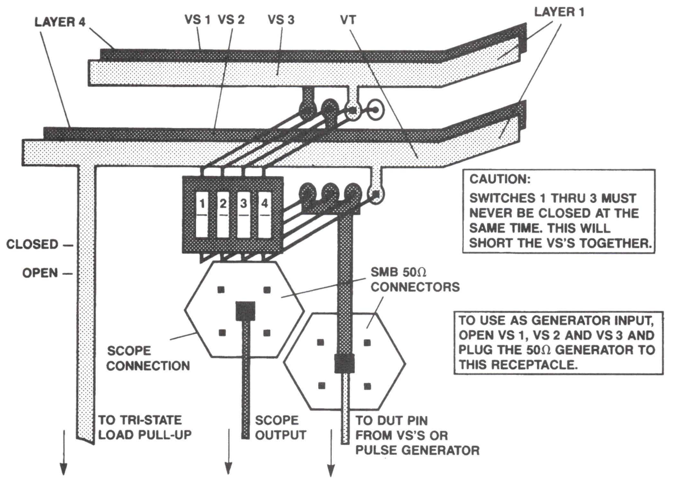
- the V_{CC} (banana jack)
- the (GND) (banana jack): this is the common ground of all input supplies.
- the V_S 1, V_S 2, and V_S 3 supplies (banana jack): these may be any voltage and are switchable. Signetics connects programmable supplies to these connectors.
- the V_t supply (banana jack): this is the tri-state pull-up voltage and is permanently connected to the bus to each pin. It is selectable by Jumper #2, see Figures 5 and 6. For FAST and ALS products this is 7V. For ACL products this is $V_{CC} \times 2$ and it is not used for ECL applications.
- Input Stimulus (inside SMB connector: this is found on every input/output pin. More than one pin may be used in this manner. **CAUTION:** When using this connector as an input stimulus, make sure V_s 1 – 3 are disconnected. This will short the power supplies to the generator if they are not disconnected.
- Output Measurement or Scope Connection (outside SMB connector: this is also found on every input/output pin. More than one pin may be used in this manner. Remember, if this pin is not connected to a scope and is an output, a 50Ω resistor must be connected here to ground to complete the 50Ω resistive load. Signetics has constructed 50Ω load by soldering a high-quality (High-frequency) 50Ω resistor inside a female SMB cable connector. See Figure 9.

CAUTION: V_S 1.2 and 3 are all on the same DIP switch. Since they connect to the same bus per pin, **ONLY ONE SUPPLY MAY BE CONNECTED AT ONE TIME.** Otherwise, this will result in a short between power supplies connected.

With these 6 connections, the fixture is capable of testing the product lines as mentioned.

The cost of this fixture ranges from 550 per fixture, dedicated to a 20-pin device in quantities of 1 – 10, to as low as 385 per fixture of the same type in quantities over 100. This is not substantially higher than the cost of a dedicated fixture; which is estimated at 200 – 500. The factor to consider would be the quantity of fixtures for the number of products to be tested. To have a dedicated fixture for every 2 – 3 product types versus a "universal" test fixture for 20 – 30 product types is worth considering from a cost standpoint.

Included in Appendix 1 is the parts list for this fixture and the supplies used by Signetics. This in no way constitutes Signetics endorsements of these suppliers and the customer may select their own supplier if they so desire. This fixture is offerd to the public to duplicate and use within their own environments. Signetics will not provide any materials but will allow the manufacturers of the board and materials to build and/or supply for any requesting party. Pricing and availability are left to the vendors and Signetics has no control over those issues. The intent is to provide something for users of High-speed logic that has been proven and tested in a true High-speed use, and provide a characterization of these products prior to their introduction to the market place.


LAYER 4
VS 1
VS 2
VS 3
VT
LAYER 1
1
2
3
4
CLOSED
OPEN
SMB 50Ω CONNECTORS
SCOPE CONNECTION
TO TRI-STATE LOAD PULL-UP
SCOPE OUTPUT
TO DUT PIN FROM VS'S OR PULSE GENERATOR
DF07810S

CAUTION:
SWITCHES 1 THRU 3 MUST NEVER BE CLOSED AT THE SAME TIME. THIS WILL SHORT THE VS'S TOGETHER.

TO USE AS GENERATOR INPUT, OPEN VS 1, VS 2 AND VS 3 AND PLUG THE 50Ω GENERATOR TO THIS RECEPTACLE.

Figure 8. DIP Switch Connections for V_s 1, V_s 2, V_s 3, and V_t and the SMB Connectors for Input Signals and Output Measurement

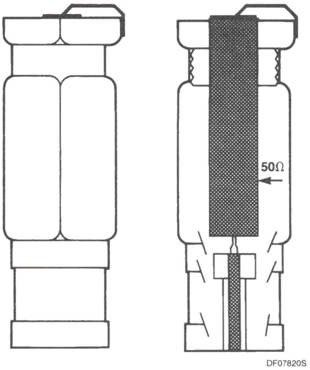

50Ω
DF07820S

Figure 9. 50Ω Load Resistors Using Output Pin SMB Cable Connectors

5. APPENDIX I - Component and Vendor List

The following prices are quoted for a 30 piece build of a 24 pin test fixture and are not binding in any way.

1. Printed circuit mother board.
    - SO and SOL -#SD8512.28 **$195.00**
    - DIP -#SD8512.31 **$195.00**
    - Requirement: 1 per part configuration
    - Supplier: Prototype and Production Circuits
      8040 S. 1444 W.
      West Jordan, UT 84084
      (801) 566-5431

2. SO and SOL sockets.

#_PINS	PART_#
14	001-014
16	001-016
16L	001-116
20	001-120
24	001-124
28	001-128

All sockets are the same price. **$3.00**
SOIC through hole socket
Requirement: 1 per board
Supplier: Surface Mount Devices, Inc.
PO Box 16818
Stamford, CT. 06903
(203) 322-8290

3. L$G-1AG14-1 Socket Terminal Pins.
    - For DIP boards - number of pins equal to the part pin count times by (7) seven.
      24 × 7 = 160 × .20 = **$33.60**
    - For SO and SOL boards - number of pins equal to the part pins count times by (5) five.
      24 × 5 = 120 × .20 = **$24.00**
    - cost per pin is $ .20

4. Shorting Blocks (Jumpers).
    - .3 inch 8136-475G1 Requirement: 1 per pin
      $.25 each × 24 = **$6.00**
    - .1 inch 8136-651P2 Requirement: 1 per pin
      $.05 each × 24 = **$1.20**
    - Supplier: Augat

5. Chip Resistors.
    - 50Ω 1% CRCW 1210 Requirement: 1 per pin
      $.168 each × 24 = **$4.03**
    - 450Ω 1% CRCW 1206 Requirement: 1 per pin
      $.037 each × 24 = **$.91**
    - 500Ω 1% CRCW 1206 Requirement: 1 per pin
      $.037 each × 24 = **$.91**
    - Supplier: Dale Electronics, Inc.
      2300 Riverside Blvd.
      Norfolk, Nebraska 68701
      (402) 371-0080

6. Chip Capacitors.

Ceramic Part_#	Requirement	
33pf 500R15N330JP	1 per bin	
$.17 each × 24 =		$4.08
15pf 500R15N150JP4	1 per board	
$.50 each × 1 =		$.50
.015μf 500$41W103KP4	1 per board	
$1.00 each × 1 =		$1.00
.1μf 500$41W104KP4	1 per board	
$1.00 each × 1 =		$1.00

Supplier: Johanson Dielectrics

7. Dipped Tantalum.

Ceramic	Requirement	
10μf 106k025NLF	1 per board	
$1.00 each × 1 =		$1.00
47μf 476K020WLG	1 per board	
$2.18 each × 1 =		$2.18

Supplier: Mallory

8. Ferrite Core.

T80-1	Requirement: 1 per board	
$1.00 each × 1 =		$1.00

Supplier:
Amidon Associates
12033 Otsego Street
North Hollywood, CA 91607
(818) 760-4429

9. Mounting Screw.

4-40 × 1/4 Phillips pan head machine screw	Requirement: 16 per board.	
$.02 × 16 =		$.32

Supplier:
Bonneville Industry Supply Co.
45 So. 1500 W.
Orem, Utah
(801) 225-7770

10. Bannana Plug Jack.

H.H._Smith_Type		Order_#	Requirement	
White	1509-101	28F1178	6/board-color your choice	
Red	1509-102	35F870	6/board-color your choice	
Black	1509-103	35F869	6/board-color your choice	
Green	1509-104	28F1179	6/board-color your choice	
Blue	1509-105	28F1180	6/board-color your choice	
Yellow	1509-107	28F1182	6/board-color your choice	
$.35 × 6 =				$2.10

Supplier: Newark Electronics

11. Switch.

76P$B04 4-bit side actuated piano-dip	Requirement: 1 per pin	
$1.39 × 24 =		$33.36

Supplier: Grayhill Co.

12. Connectors - Snap-on SMB.

51-051-0000-220 - Straight jack receptacle	Requirement: 2 per pin	
$2.25 × 48 =		$108.00

Supplier: Sealectro

13. Mounting frame.

Signetic's number CB-1.0	Requirement: 1 per test fixture	$21.50

Supplier:
Electronic Chassis Corp.
468 North 1200 West
Lindon, Utah 84062
(801) 785-9113

14. Hookup wire.
No. 18/20 gauge Teflon coated — about 24 inches per test fixture. $1.00

The approximate cost for 1-of-30, 24-pin fixtures is $418.73 each.

The following components may be needed in use of the test fixtures but are not part of the test fixtures.

61-001-0000-89	50Ω terminator plug	As required or hand built with 50Ω resistor and 51-007-0000
51-007-0000	Straight Cable Clamp Type	As required
51-083-0000-222	"T" adaptor J-J-J	As required
51-085-0000	"T" adaptor J-P-J	As required
51-072-0000	Adaptor J-J	As required
51-073-0000	Adaptor P-P	As required
51-001-0020	Shorting plug	As required
61-002-0000-89	50Ω terminator jack	As required
Supplier:	Sealectro Corp (415) 965-1212	

6. APPENDIX II-Construction Hints

A suggested order of assembly is as follows:

1. Cut traces for 450Ω resistor. (Not needed for ECL)
2. Install SMB Connectors. Elevate base from board .05″.
3. Install DIP Switches. Note: Numbers on switches may not correlate to Vs supply numbers.
4. Install Augat socket pin.
5. Install load/termination resistors and capacitors.
6. Strap V_{CC} and GND pins to appropriate bus strips.
7. Install by-pass capacitors.
8. Clean flux off of board and components.
9. Check for lead to frame shorts on PLCC board. (Not discussed in App Note.)
10. Install banana jacks on frame.
11. Attach board to frame with 1/4 Phillips pan head machine screws.
12. Wrap wire 8-12 times around ferrite core. Leave enough wire to connect to frame and board. See Figure 1.
13. Connect V_{CC}, GND, and voltage supplies from banana jacks to board.
14. Remove all remaining flux. Keep "flux-off" from banana jacks.

Hints on construction:

— A .05″ shim that fits under the SMB connector base helps elevate it during construction.

— Mount the SMB connector with flat side out rather that point side out. See Figure 8.

— Solder Augat socket pins in with a part inserted to hold the pins steady.

— "Piano DIP" switches have the numbers reversed from the Board notation. Taping a new number on the board designations will help match the switches.

— Hint for solder chip components: apply a small amount of solder on one side of the pads on the board.

— Keep DIP switches and SMB connectors spaced as far away from each other as the holes will permit, ie., push the SMBs in and the DIP switches out.

Signetics

FAST Products

AN205

Using FAST ICs For μP-To-Memory Interfaces

Application Note

INTRODUCTION

Most microprocessor-based systems use some form of bipolar interface between the processor and memory; only a very primitive system does not require such interface support. TTL devices in quad, hex, or octal configurations are used to meet functional and circuit-interface requirements of the system. For complex systems, the interface support may be extensive while, for simple systems, only a few devices may be required to ensure operational integrity. In a majority of system designs, one or more of the following interface requirements must be addressed.

- Buffering and Demultiplexing of Data/ Address Buses
- Signal Timing and Signal Isolation
- Address Decoding
- Bank Switching
- Handling of Wait States
- Adjusting Read/ Write Data Rates
- Refreshing Dynamic RAM
- Unique Interface Requirements such as Multi-Processor Networks, Data Communication Links, etc.

Interface support is an important part of the overall design job; when implemented with the proper parts, system efficiency can be dramatically improved, higher reliability can be obtained and the design can be executed with minimum parts. This Application Note shows how common interface problems can be solved by using a minimum of high-performance bipolar devices from Signetics.

BUFFERING AND DEMULTIPLEXING

Microprocessor outputs are inherently fanout-limited; thus, some form of buffering is required to drive multiple loads such as those found on address and data buses. Extended bus configurations coupled with MOS loads tend to produce large capacitive sinks which degrade waveforms and also increase propagation delays. The use of TTL buffers provides an easy and economical way of overcoming or, at least, minimizing these harmful effects. In those systems that use shared memories and direct memory access (DMA), buffers are frequently used for isolation and as a method for switching between multiple buses. Buffers are also commonly used to optimize signal-to-noise ratios and to drive multicard bus interfaces. For the most part, buffer and latch-control functions can be summarized as follows:

- Latch the address information in systems that use multiplexed buses.
- During read operations, avoid bus contention by preventing the system from driving the multiplexed address/ data bus until the address information is removed.
- Control the direction of data transceivers according to processor operation while preserving write-data and read-data hold times and avoiding bus contention when switching direction.
- Isolate the microprocessor from the system bus during DMA and multiprocessor operations.

With the use of 16-bit microprocessors, systems have become more sophisticated; likewise, buffer control and interface circuits have become somewhat more complex. Many of the 16-bit machines use multiplexed address/data buses to reduce I/O pin count; as a result, latches are required to demultiplex, hold, and buffer the address bus. Not only must the address information be latched at the correct time but the date bus must usually be buffered with bidirectional transceivers to provide the necessary drive. As previously indicated, the interface circuits must be able to avoid bus contention and, when required, to isolate the processor from the system bus.

Buffers and latch-control signals for three popular 16-bit microprocessors — the 8086, the Z8001, and the 68000 — are shown in Figure 1. For each processor, the buffer and interface functions are summarized at the bottom of the figure. Although the timing-and-control functions of the interface support circuits are fairly complex, these internal complexities are transparent to the user; only the bus connections and a few control lines are required to achieve the management goals of the system.

INTERFACE FUNCTIONS (8086 SYSTEM)

- Multiplexed address/data bus ($AD_0 - AD_{15}$)
- 3-State latches (74F373) used for demultiplexing; latches are continuously enabled by ALE until data is stable on the bus and a timing pulse is delivered by the microprocessor.
- HLDA is used to float address bus during DMA operation.
- Data bus buffered by 74F1245 or 74F245 Transceivers; data direction controlled by DT/$\overline{\text{R}}$ in minimum mode.
- Bus control and DMA isolation controlled by $\overline{\text{DEN}}$ is minimum mode.

INTERFACE FUNCTIONS (Z8001 SYSTEM)

- Address bus ($AD_0 - AD_{15}$) latched with 74F373s using $\overline{\text{AS}}$ for latch enable and $\overline{\text{BUSAK}}$ for isolation. (Note: The segmented outputs are designed to drive a Memory Management Unit with internal latches; however, in this application, the address outputs are prelatched since they are not stable for the entire cycle.)
- Data bus buffered with 74F1245s or 74F245s; $\overline{\text{DS}}$ and R/$\overline{\text{W}}$, respectively, control data direction and bus contention.
- BUSAK controls DMA isolation.

Using FAST ICs For μP-To-Memory Interfaces

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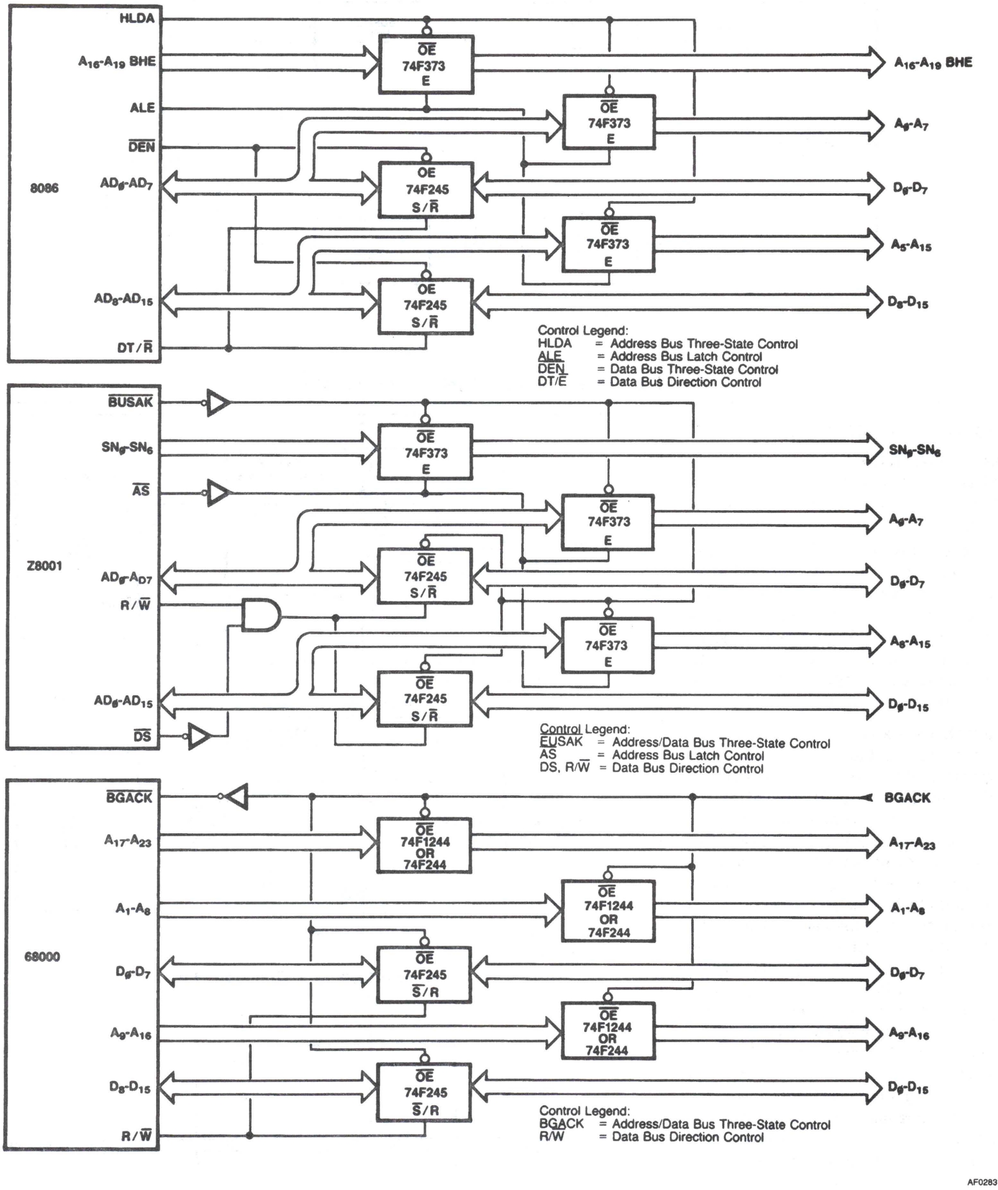

8086
HLDA
A_{16}-A_{19} BHE
ALE
DEN
AD_0-AD_7
AD_8-AD_{15}
DT/R
OE
74F373
E
74F245
S/R
A_{16}-A_{19} BHE
A_0-A_7
D_0-D_7
A_8-A_{15}
D_8-D_{15}
Z8001
BUSAK
SN_0-SN_6
AS
AD_0-AD_7
R/W
AD_8-AD_{15}
DS
SN_0-SN_6
A_0-A_7
D_0-D_7
A_8-A_{15}
D_8-D_{15}
68000
BGACK
A_{17}-A_{23}
A_1-A_8
D_0-D_7
A_9-A_{16}
D_8-D_{15}
R/W
74F1244
OR
74F244
S/R
BGACK
A_{17}-A_{23}
A_1-A_8
D_0-D_7
A_9-A_{16}
D_8-D_{15}
AF02831S

Control Legend:
HLDA = Address Bus Three-State Control
ALE = Address Bus Latch Control
DEN = Data Bus Three-State Control
DT/E = Data Bus Direction Control

Control Legend:
EUSAK = Address/Data Bus Three-State Control
AS = Address Bus Latch Control
DS, R/W = Data Bus Direction Control

Control Legend:
BGACK = Address/Data Bus Three-State Control
R/W = Data Bus Direction Control

Figure 1. Examples of Processor-to-Bus Interfaces

Using FAST ICs For μP-To-Memory Interfaces AN205

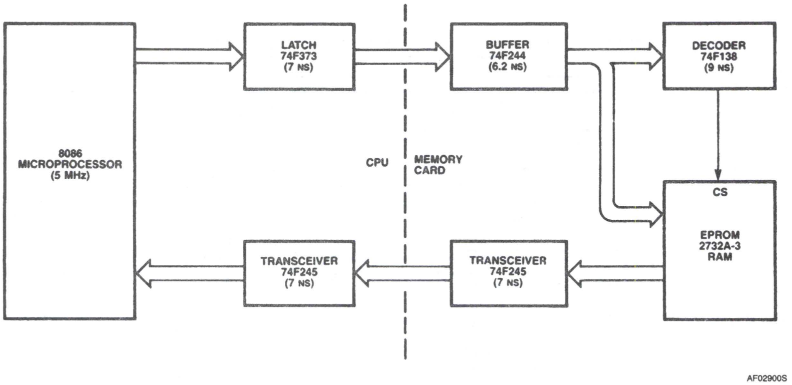

8086
MICROPROCESSOR
(5 MHz)
LATCH
74F373
(7 NS)
BUFFER
74F244
(6.2 NS)
DECODER
74F138
(9 NS)
CPU
MEMORY
CARD
CS
EPROM
2732A-3
RAM
TRANSCEIVER
74F245
(7 NS)
TRANSCEIVER
74F245
(7 NS)
AF02900S

Figure 2. System Showing Typical Interface Delays

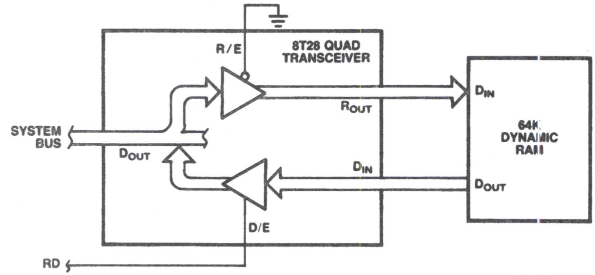
INTERFACE FUNCTIONS (68000 SYSTEM)

- Address bus buffered by 74F1244s or 74F244s and DMA isolation controlled by BGACK.
- Data bus buffered by 74F1245 or 74F245 Transceivers with R/W and BGACK, respectively, controlling data direction and bus isolation. (Note: In this configuration, a larger processor package is required since the address and data buses are separate; some advantage in speed and simplified timing are to be gained.)

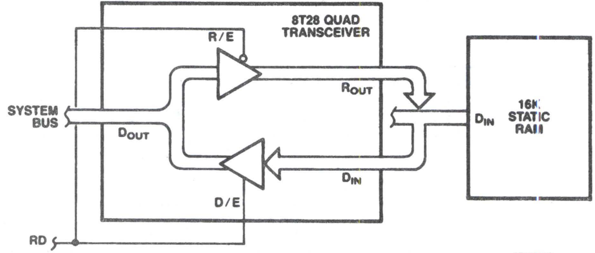
Figure 2 shows the effects of buffers and an address decoder on the memory access time in a system configuration. The access time of the 8086 microprocessor is defined as the time from which a valid address appears at the output of the processor assuming that there are no wait states. Observe that each buffer and the decoding function adds a specific delay to the data-processing chain. In addition to these propagation delays, the system designer must consider capacitive loading, buffer access delays, (that is, are buffers enabled when valid data appears at input) and any other delay parameters that would extend the memory access time. (Note: The normal 8086 buffer control does not affect access time.) The delay should be calculated using maximum propagation delays over the operating temperature range of the system. Based on these considerations, the memory access time for the system shown in Figure 2 can be approximated as follows:

8086 READ CYCLE — Address Valid Output to Data Valid Input 460ns

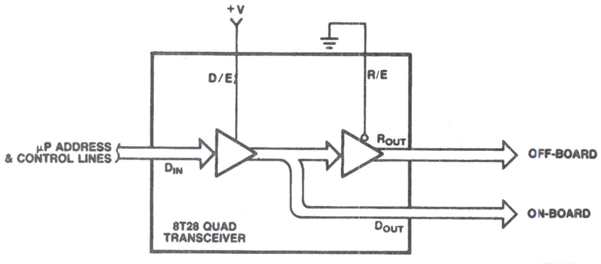
2732 MEMORY ACCESS TIME (T_{CE})-T_{CE} = 460ns-3 (7ns) — 6.2ns-9ns = 423.8ns


R/E
8T28 QUAD
TRANSCEIVER
SYSTEM
BUS
D_{OUT}
R_{OUT}
D_{IN}
D/E
RD
D_{IN}
64K
DYNAMIC
RAM
D_{OUT}
AF02910S

a. Interface to Separate Buses


R/E
8T28 QUAD
TRANSCEIVER
SYSTEM
BUS
D_{OUT}
R_{OUT}
D_{IN}
D/E
RD
D_{IN}
16K
STATIC
RAM
AF02920S

b. Interface to a Common Bus


+V
D/E
R/E
µP ADDRESS
& CONTROL LINES
D_{IN}
R_{OUT}
OFF-BOARD
ON-BOARD
D_{OUT}
8T28 QUAD
TRANSCEIVER
AF02930S

c. Driving a Multi-Card Interface

Figure 3. Using 8T28 Transceive to Obtain Optimum Interface Flexibility

Using FAST ICs For μP-To-Memory Interfaces

AN205

BIDIRECTIONAL BUS INTERFACES

Virtually all microprocessor-based systems use a bidirectional bus interface between the processor and I/O peripherals; the memory interface may require separate-or-common bus connections. In either case, the 8T28 Quad Transceiver is well suited to this type of application. The 8T28 is able to drive a capacitive load of 300-picofarads without waveform degradation and the three-state outputs provide the switching speeds of TTL while offering the drive capabilities of open-collector gates. Typical bus interfaces are shown in Figure 3.

In Figure 3a, the transceiver provides a bidirectional interface between the system bus and separate input/output buses of the dynamic RAM. The D_{IN} bus is continuously driven while the D_{OUT} bus is gated onto the system bus via D/E.

Figure 3b shows a static RAM interface implemented by tying R_{OUT} and D_{IN} together. Here, the 8T28 functions as a normal bidirectional transceiver, providing buffered drive between the system bus on one hand and the memory I/O bus on the other. The bottom panel shows how the 8T28 can be used in the dual capacity of an on-board/off-board buffer/driver. To prevent signal degradation in such multi-board systems, the address/data/control buses must be buffered if off-board extensions are to be driven. Furthermore, the on-board/off-board buses should be buffer-isolated to prevent down-stream noise and/or failures from feeding back to the mother board. In Figure 3, observe that driver gates of the 8T28 are used to drive the on-board bus and receiver gates are used for the off-board bus. Low cost and minimum component count make the 8T28 ideally suited for such double-buffered applications.

MEMORY ADDRESS DECODING

In any computer system, information on the address bus must be decoded to generate select signals for memory and any I/O peripherals. There are numerous decoding schemes and a variety of implementation techniques. Generally, the methods used depend on system complexity which, in turn, depends on memory size, mapping parameters, access time, the particular technology, etc. Although simple decoders are frequently used in uncomplicated systems, the more sophisticated applications use PROMs to provide the required flexibility and to satisfy the mapping complexities that are usually encountered.

To develop trouble-free decoding circuits, the designer must be aware of those areas that can degrade system performance. For instance, caution is advised when using decoder outputs to terminate date write cycles. When read/write strobes (such as "E" on the 6801) are used to enable the address decoder, the data hold time is reduced because the trailing edge of the address decoder output now follows the trailing edge of the strobe signal to which the "hold time" is referenced. In systems that are sensitive to hold time, read and write strobes should not be used to enable address decoding circuits. Instead, the strobes should be gated with the decoder outputs to reduce the hold time.

Signetics makes a wide range of decoders, demultiplexers, and PROMs that are suitable for both simple and complex decoding functions. Some of the more common decoding applications are summarized in Figures 4 through 7.

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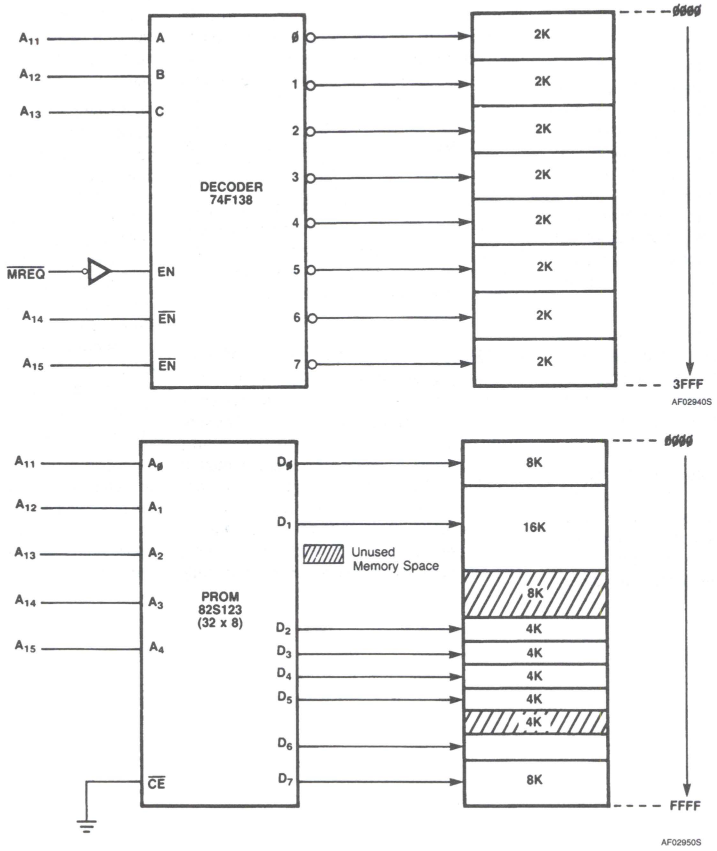
A11
A12
A13
MREQ
A14
A15
A
B
C
EN
EN
EN
DECODER
74F138
0
1
2
3
4
5
6
7
2K
2K
2K
2K
2K
2K
2K
2K
0000
3FFF
AF02940S
A11
A12
A13
A14
A15
A0
A1
A2
A3
A4
CE
PROM
82S123
(32 x 8)
D0
D1
D2
D3
D4
D5
D6
D7
Unused
Memory Space
8K
16K
8K
4K
4K
4K
4K
4K
8K
0000
FFFF
AF02950S

Figure 4. Two Simple Decoding Methods

OPERATION & APPLICATIONS SUMMARY

For small uncomplicated systems, the 74F138 decoder provides a cost-effective interface between the system address bus and memory. The configuration shown above is not only economical, it is fast, uses very little power, and requires no programming. Such systems are commonly used to generate contiguous memory addresses and to decode memory segments of equal size. With additional decoding circuits, the memory mapping capabilities of the system can be expanded.

Where speed is not a critical factor, the PROM decoder shown below adds considerable flexibility with no increase in chip count. The 82S123 can generate contiguous or non-contiguous address space and can be memory-mapped to satisfy the requirements of most applications. Although the PROM decoder is a bit more expensive and uses slightly more power, it has the advantage of being field programmable.

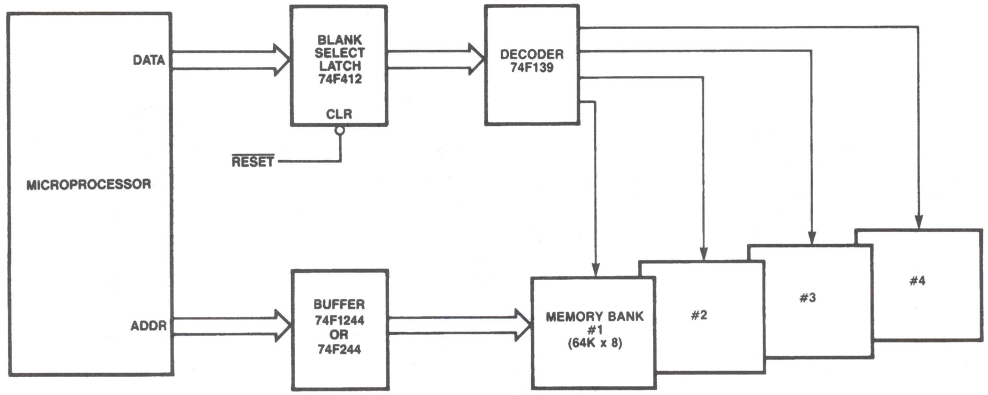
MICROPROCESSOR
DATA
ADDR
BLANK SELECT LATCH 74F412
CLR
RESET
DECODER 74F139
BUFFER 74F1244 OR 74F244
MEMORY BANK #1 (64K x 8)
#2
#3
#4
AF02851S

Figure 6. Extending the Logical Address Space Via Bank Switching

OPERATION & APPLICATIONS SUMMARY

In some applications, it is desirable for the system memory to extend beyond the logical address space of the processor. As shown, such a system can be easily implemented with a few interface parts and a bit of software. The four memory banks are wired in parallel; each bank can be as large as the logical memory space of the microprocessor — 512 bytes for 8-bits of address and 64K for a 16-bit address bus. An output port under software control selects the active bank; the bank address is decoded to ensure that only the appropriate memory bank is enabled. In this way, the possibility of bank contention is eliminated.

Memory allocation schemes such as these are frequently used in multiprocessor environments and, in this type of application, a copy of the operating system kernel must reside in each memory bank. The system can be enhanced by providing direct switching between the memory banks; however, additional hardware is required for such operations.

Using FAST ICs For μP-To-Memory Interfaces

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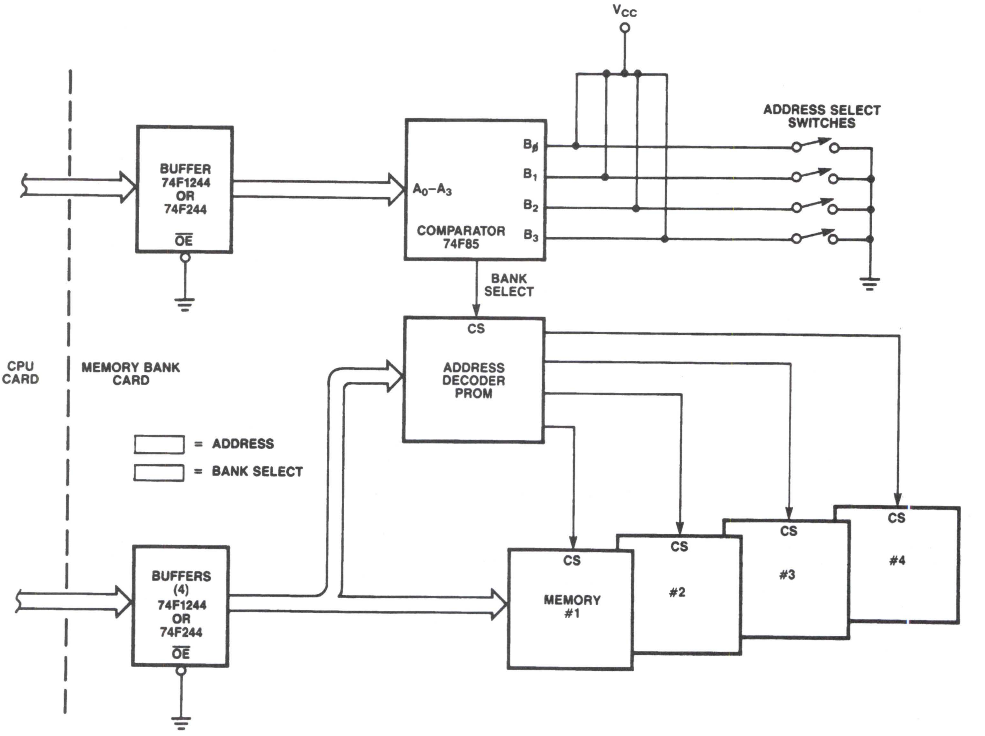
V_{CC}
ADDRESS SELECT SWITCHES
BUFFER 74F1244 OR 74F244
OE
A0–A3
B0
B1
B2
B3
COMPARATOR 74F85
BANK SELECT
CS
ADDRESS DECODER PROM
CPU CARD
MEMORY BANK CARD
= ADDRESS
= BANK SELECT
BUFFERS (4) 74F1244 OR 74F244
OE
MEMORY #1
#2
#3
#4
AF02861S

Figure 7. Multi-Board Decoding System With Extended Address Space

OPERATION & APPLICATIONS SUMMARY

In a multi-board system, the address decoding and memory-bank select functions can be implemented as shown here. The bank address on the memory card is identified by setting the address select switches of the comparator to a predetermined configuration. When the bank select signals from the CPU card match the present bank address, the PROM is enabled and the appropriate memory bank is placed on-line. Data bus control for the system is not shown.

The system show in Figure 6 and the one shown here are similar in that the four memory banks are wired in parallel and each bank can be as large as the logical address space of the microprocessor.

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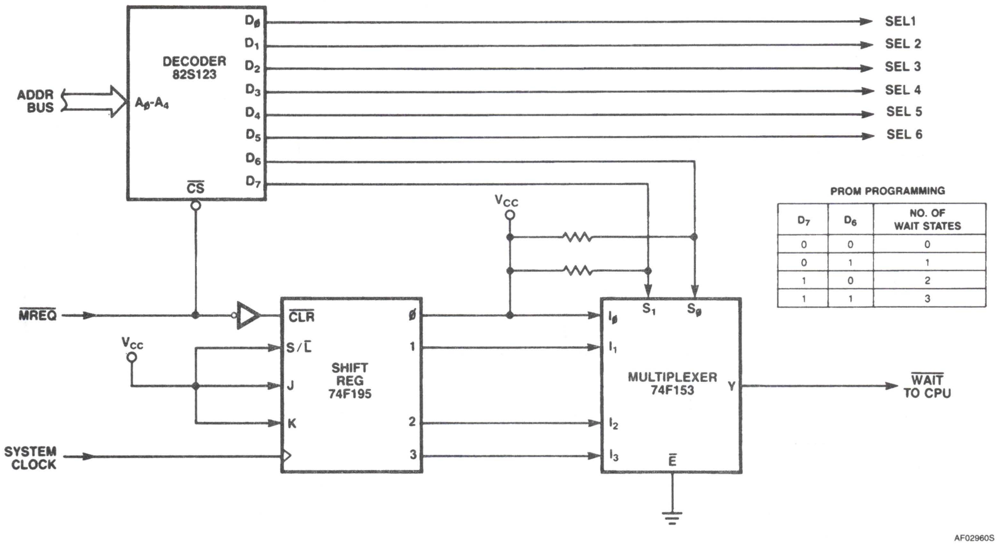
DECODER
82S123
ADDR BUS
A0-A4
D0
D1
D2
D3
D4
D5
D6
D7
CS
SEL1
SEL 2
SEL 3
SEL 4
SEL 5
SEL 6
VCC
MREQ
CLR
S/L
J
K
SHIFT REG 74F195
0
1
2
3
SYSTEM CLOCK
VCC
I0
I1
I2
I3
S1
S0
MULTIPLEXER 74F153
Y
E
WAIT TO CPU
AF02960S

PROM PROGRAMMING

D_7	D_6	NO. OF WAIT STATES
0	0	0
0	1	1
1	0	2
1	1	3

Figure 8. Programming Wait States to Optimize Data Throughput

SPECIAL MEMORY-INTERFACE CIRCUITS

In some applications, the memory interface circuits must be adapted to the unique requirements of the system. For instance, a system may use devices whose response time and wait-state requirements are vastly different, necessitating programmed wait states for optimum throughput.

Other examples include capturing a high-speed bit stream without the use of high-speed (high cost) memories, refreshing dynamic RAM via interleaving, and minimizing leakage problems when driving open-collector buses. Figures 8 through 11 show how Signetics ICs can be used to solve interface problems of this type.

OPERATION & APPLICATIONS SUMMARY

Using the "slowest" device in the system as a reference for data through-put is a gross waste of processor time. ROM is usually slower than RAM, and I/O devices are generally slowest of all. One way of reducing the harmful effects of these diverse characteristics is to program wait states for each device such that inactive periods for the CPU will be minimized. With the PROM decoder in the system shown above programmed in this manner, the multiplexer selects the appropriate tap of the shift register to initiate the required number of wait states. The wait cycle is terminated when a "1" is shifted to the selected tap; the shift register is cleared at the end of each wait state cycle.

Using FAST ICs For µP-To-Memory Interfaces

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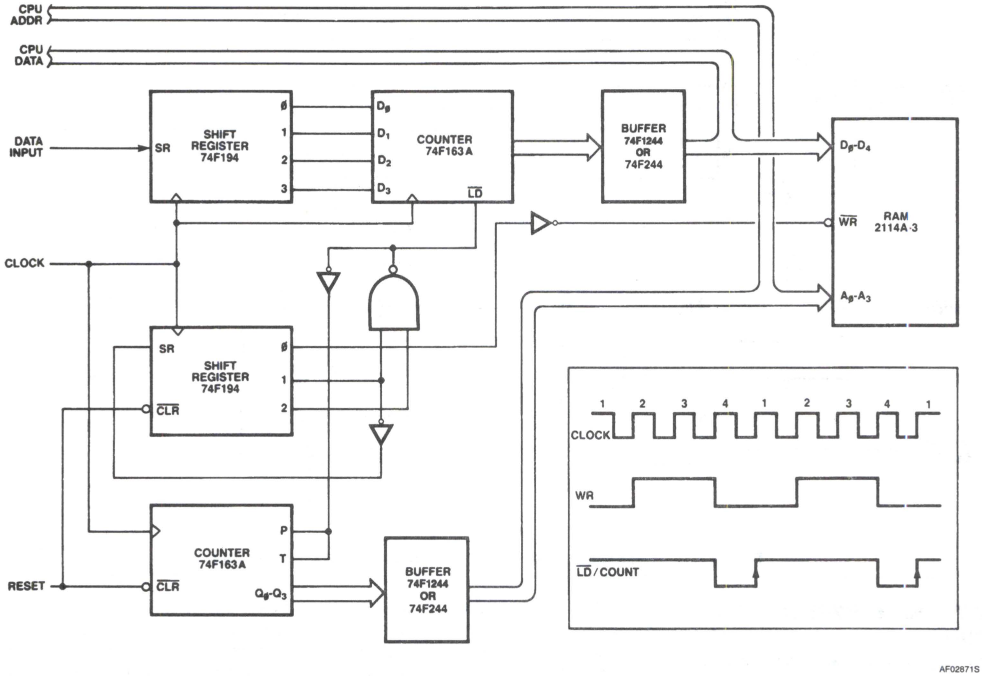

CPU ADDR
CPU DATA
DATA INPUT
SR
SHIFT REGISTER 74F194
0
1
2
3
D0
D1
D2
D3
COUNTER 74F163A
LD
BUFFER 74F1244 OR 74F244
D0-D4
WR
RAM 2114A-3
A0-A3
CLOCK
SR
SHIFT REGISTER 74F194
CLR
0
1
2
COUNTER 74F163A
P
T
Q0-Q3
CLR
RESET
BUFFER 74F1244 OR 74F244
1 2 3 4 1 2 3 4 1
CLOCK
WR
LD/COUNT
AF02871S

Figure 9. Storing High-Speed Serial Bit Stream With Low-Speed RAM

OPERATION & APPLICATIONS SUMMARY

In the design and use of logic analyzers, disk media, modems, and other similar equipment, a high-speed serial bit stream must be stored in memory. The above system shows how a 20MHz serial data stream can be captured and stored in a relatively low-speed RAM that has a 5MHz (200ns) cycle rate. The system uses a simple parallel to serial converter, thus, saving the cost of high-speed memory devices. Other than the synchronizing clock being supplied by the serial-input system and the setup/hold times of the shift registers being met, operation is simple and straightforward.

- Incoming serial data is clocked into shift register.
- After each fourth bit, data is transferred in parallel to a 4-bit counter (74F163) used as a latch.
- Data is written into RAM while four new bits enter shift register.
- Memory addressing is performed by incrementing the 74F163s and timing is controlled by a simple ring counter.

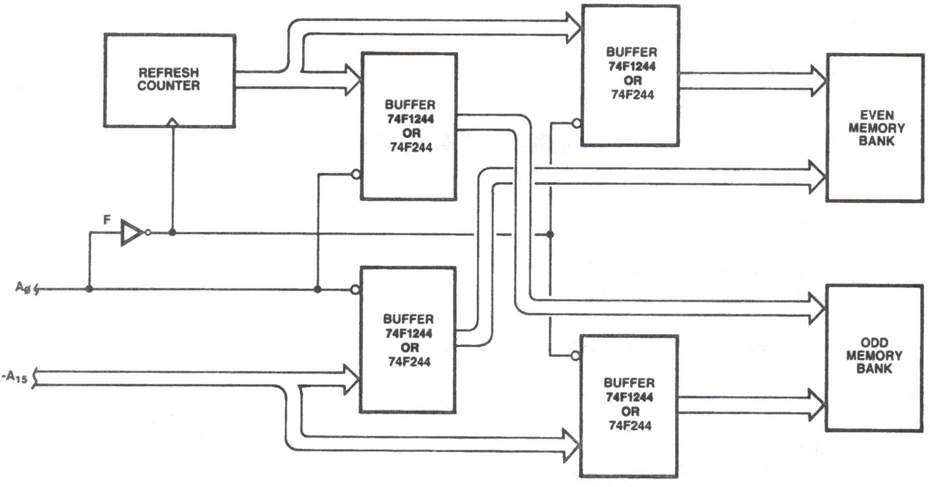

REFRESH COUNTER
BUFFER 74F1244 OR 74F244
BUFFER 74F1244 OR 74F244
BUFFER 74F1244 OR 74F244
BUFFER 74F1244 OR 74F244
EVEN MEMORY BANK
ODD MEMORY BANK
F
A0
A1-A15
AF02881S

Figure 10. Using Interleaving Technique to Refresh Dynamic RAM Memories

OPERATION & APPLICATIONS SUMMARY

Most dynamic RAMs must be refreshed at least every 2-milliseconds to ensure retention of valid data. One method of memory refresh is shown in the above example. This system uses interleaving and relies on the premise that, during normal program execution, A_0 toggles frequently enough to refresh the RAM without slowing the microprocessor with wait-states or DMA cycles to refresh the counter. If the system program uses wait-states, halt instructions, or address incrementing is otherwise limited, A_0 may not toggle at a rate sufficient to accomplish refresh. For such situations, additional circuits or special programming may be required to prevent loss of data. Operation of the system can be summarized as follows:

- When even bank is addressed by CPU, odd bank is refreshed by address counter.
- Even bank is refreshed when CPU addresses the odd bank.
- A_0 increments the refresh counter before each odd-bank refresh.

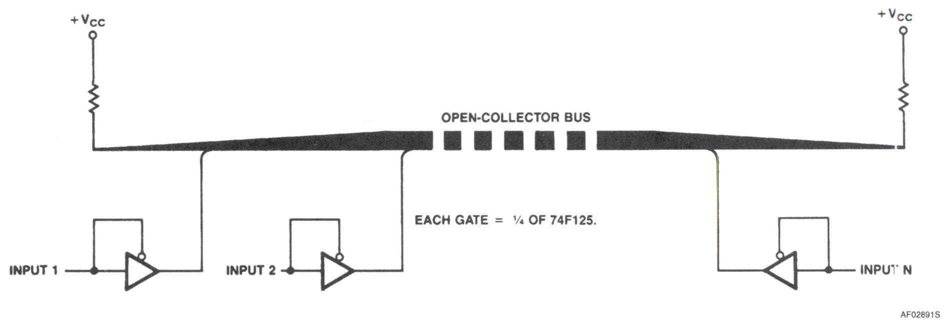


Figure 11. Reducing Leakage Current When Driving Open-Collector Buses

OPERATION & APPLICATIONS SUMMARY

The number of buffers (7406 type) that can share an open-collector bus is often limited by device leakage or by the increased power consumption caused by lowering the values of the pullup resistors. A method of reducing the leakage current is shown in the above example. Here, the logic input and output enable of each gate are tied together; thus, the gate output is floated High to drive the open-collector bus. Floating the gate outputs provides a significant reduction in leakage current which allows the use of more gates and/or reduced power consumption by the pullups.

SUMMARY

Many of the applications and concepts provided in this document were direct contributions or heavily influenced by entries in the Signetics' Interface Circuit Design contest. Our special thanks to those individuals whose entries are referenced in whole or in part.

As integrated circuits become more and more complex, fewer and fewer parts are required to implement a functional system; thus, interface support is a major consideration in the overall design process. To produce a competitive and cost effective product, the user must choose interface components that are efficient, reliable, and those that reflect the best features of current technologies. Signetics has met these challenges in the past and will continue to meet them in the future, providing silicon solutions that are truly state of the art — be it logic, memories, gate arrays, or other. For further documentation and/or applications assistance, call or write to your nearest Signetics Sales and Service Office — there is one near you.

Signetics

AN206
Using μP I/O Ports With FAST Logic

Application Note

FAST Products

INTRODUCTION

Signetics interface ICs are most often used to implement input and output ports in microprocessor based systems. This application note illustrates the effective use of Signetics FAST devices to interface microprocessor data and address buses to general purpose I/O ports. Topics illustrated include handshaking, multiplexing, arbitration, and bit manipulating. More complex circuits involving memory interfacing, shared memory, and multiple processors are covered in other application notes.

Simple I/O Ports

The simple Input/Output ports shown in Figure 1 use 74F374 octal flip-flops and 74F244 octal 3-State buffers to interface to a microprocessor's data bus. The input port is enabled by $\overline{RD}$ AND $\overline{PORTSEL}$. The output is enabled by $\overline{WR}$ and $\overline{PORTSEL}$.

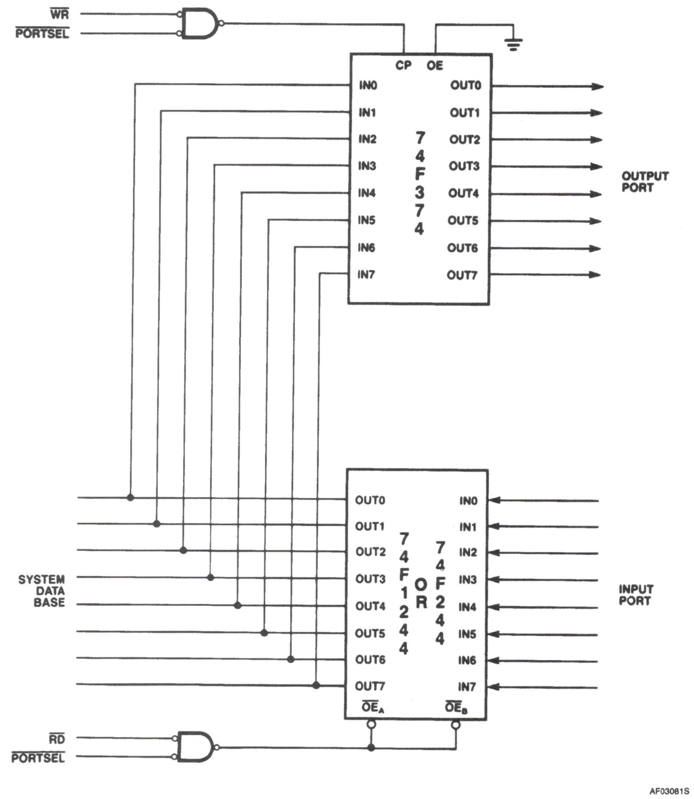


Figure 1. Simple Input/Output Ports Interface With Microprocessor Data Bus

When 16 pin packages are preferable to 20 pin packages for physical design considerations, 3-State multiplexers may be used as input ports. In Figure 2, 74F257 quad two-input multiplexers are used. A_0 selects between port A and port B.

In Figure 3, a 74F373 octal transparent latch is used to drive a light emitting diode annunciator array. The output follows the data bus while E is High, and the display freezes when E goes Low. The 20mA sink current of the 74F373 permits interface to most LED devices.

A potential hazard exists when using transparent latches as output ports. The timing diagram of Figure 4 shows that data may not be valid when E is brought High, causing invalid data to be present on the output for a brief period. This will not cause a problem when driving LEDs because the duration of the invalid data is too short to be seen. But, problems will occur if the outputs are used to trigger other circuits that cannot tolerate glitches. Flip-flops should be used instead of transparent latches when these conditions exist.

Interfacing microprocessors to slow peripherals, such as printers, usually requires handshaking logic. In Figure 5, the 74F374, 3-State octal flip-flop acts as an output port for the microprocessor and as an input port for peripheral. The microprocessor writes data to the output port which sets /data available Low. The peripheral then reads input port which sets /data accepted Low and /data available back to High. The Low /data accepted line interrupts microprocessor indicating that peripheral is ready for another data transfer.

Bit Manipulation

In Figure 6, the 74F251, 3-State 8 to 1 multiplexer provides a bit-oriented input port. This technique permits processors which do not have built-in bit manipulating capability to examine single bits at input ports efficiently. In addition, parallel inputs may be read bit-serially over a single data line. Address lines A_0, A_1, and A_2 select the bit to be read, and data bus line D_7 is selected to permit a simple software decision based on JUMP-ON-SIGN or SHIFT-LEFT & JUMP-ON-CARRY.

A versatile bit-oriented output port may be implemented with a 74F259, eight-bit addressable latch as shown in Figure 7. With this technique single output bits may be manipulated without maintaining a copy of the output port contents in memory. This is useful in bit-oriented control applications. The addressable latch effectively performs serial to parallel conversion on data supplied from the system bus. Data is written to 1 of 8 output bit locations specified by address lines A_0, A_1, and A_2.

Caution: Address inputs must be stable before latch is enabled or data can be entered into incorrect locations. If output glitches cannot be tolerated, data input must also be stable before the latch is enabled.

A similar technique is used in Figure 8, to accomplish bit manipulation without using the data bus. Each bit is associated with two addresses. If A_0 is High, the bit is set High; if A_0 is Low, the bit is set Low. With this approach bit-manipulation is faster and requires less program memory because data does not have to be loaded and output from the accumulator. Also PCB layout complexity is reduced by removing the data bus from the output port.

I/O Timing

In many applications it is necessary to adjust timing to match microprocessor specifications to bus specifications. For example, the MC6809 microprocessor has data write hold time of 30ns, making it difficult to interface to peripheral chips such as floppy disk controllers that have longer hold time requirements.

Figure 9 extends this hold time for interface to slow peripheral devices. A 74F373 3-State octal transparent latch is used to freeze data on I/O bus during write operations. During read operations, the 74F373 outputs are floated and data is read through the 74F244 3-State octal buffer.

Figure 10 shows the timing diagram for an I/O bus with extended hold time. During the write cycle, data is latched by 74F373 on the falling edge of E. Data remains on the outputs of the 74F373 until the rising edge of Q at the beginning of the next cycle, when the outputs are floated. The read cycle is unaffected. Data hold time is extended to ¼ cycle – from 30ns to 250ns for a 1MHz cycle rate. Note that a latch is used instead of a flip-flop to preserve the data setup time of the 6809.

A dedicated hardware solution is faster in systems requiring High throughput rates where the required function is performed frequently. In Figure 11, a 74F374 3-State octal flip-flop is used as both input and output port. By jumpering the output data lines of the 74F374 to different system data bus lines, various dedicated functions can be realized – examples are nibble swapping, bit transposing, and data encryption. The software to perform data manipulation is simple – data is written to the octal flip-flop, and manipulated data is read back into the processor using the following instructions: OUT (DATA MANIPULATOR), A IN A, (DATA MANIPULATOR)

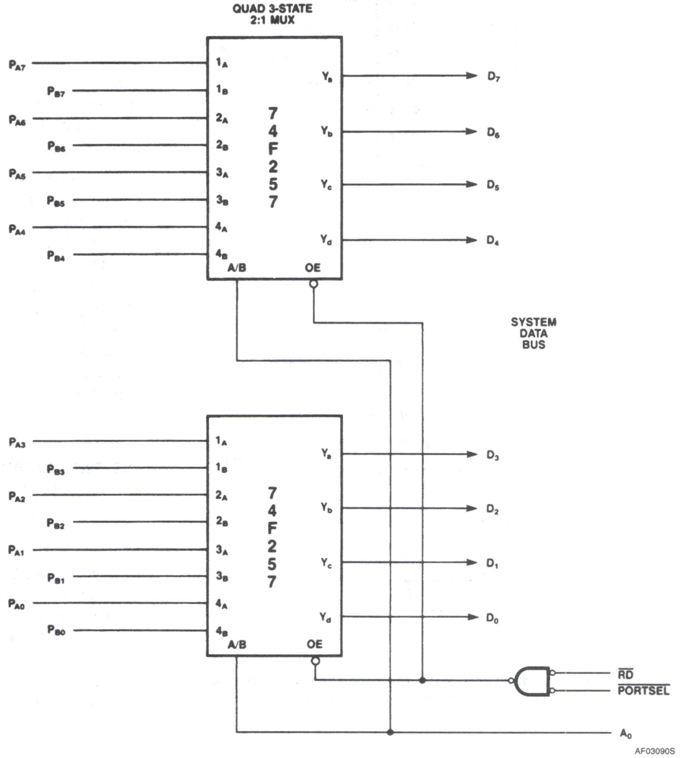


Figure 2. Use of 3-State Multiplexers As Input Ports

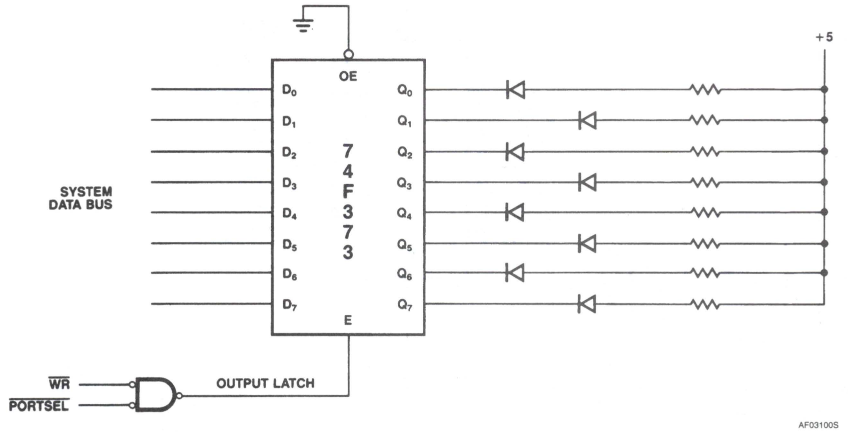

SYSTEM DATA BUS
OE
D_0
D_1
D_2
D_3
D_4
D_5
D_6
D_7
74F373
Q_0
Q_1
Q_2
Q_3
Q_4
Q_5
Q_6
Q_7
E
+5
WR
PORTSEL
OUTPUT LATCH
AF03100S

Figure 3. Output Port Driving LEDs Using 74F373 Octal Transparent Latch

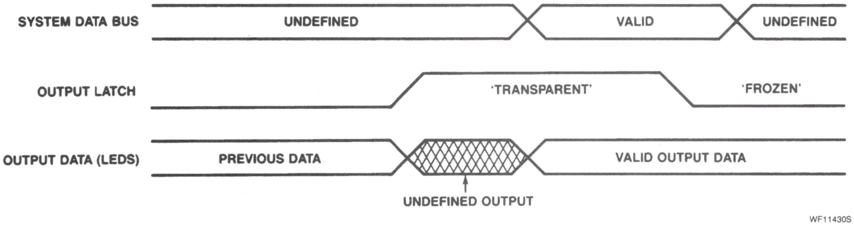

SYSTEM DATA BUS
UNDEFINED
VALID
UNDEFINED
OUTPUT LATCH
'TRANSPARENT'
'FROZEN'
OUTPUT DATA (LEDS)
PREVIOUS DATA
VALID OUTPUT DATA
UNDEFINED OUTPUT
WF11430S

Figure 4. Potential Hazard Exists When Using Transparent Latch as Output Port

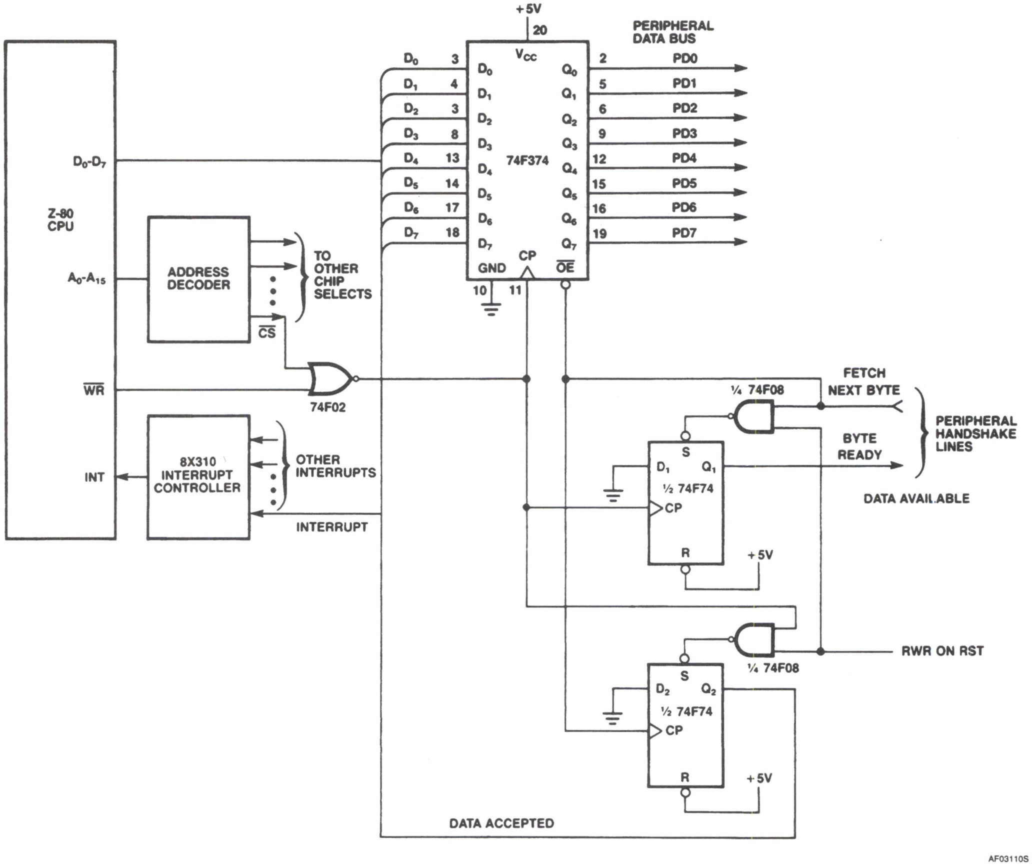

+5V
20
V_{CC}
PERIPHERAL DATA BUS
Z-80 CPU
D_0-D_7
A_0-A_{15}
$\overline{WR}$
INT
ADDRESS DECODER
TO OTHER CHIP SELECTS
$\overline{CS}$
74F02
8X310 INTERRUPT CONTROLLER
OTHER INTERRUPTS
INTERRUPT
D_0 3
D_1 4
D_2 3
D_3 8
D_4 13
D_5 14
D_6 17
D_7 18
74F374
Q_0 2 PD0
Q_1 5 PD1
Q_2 6 PD2
Q_3 9 PD3
Q_4 12 PD4
Q_5 15 PD5
Q_6 16 PD6
Q_7 19 PD7
GND
CP
$\overline{OE}$
10
11
FETCH NEXT BYTE
¼ 74F08
S
D_1
Q_1
½ 74F74
CP
R
+5V
BYTE READY
PERIPHERAL HANDSHAKE LINES
DATA AVAILABLE
¼ 74F08
RWR ON RST
S
D_2
Q_2
½ 74F74
CP
R
+5V
DATA ACCEPTED
AF03110S

Figure 5. Interfacing Microprocessors to Slow Peripherals, Such as Printers, Using Handshaking Logic

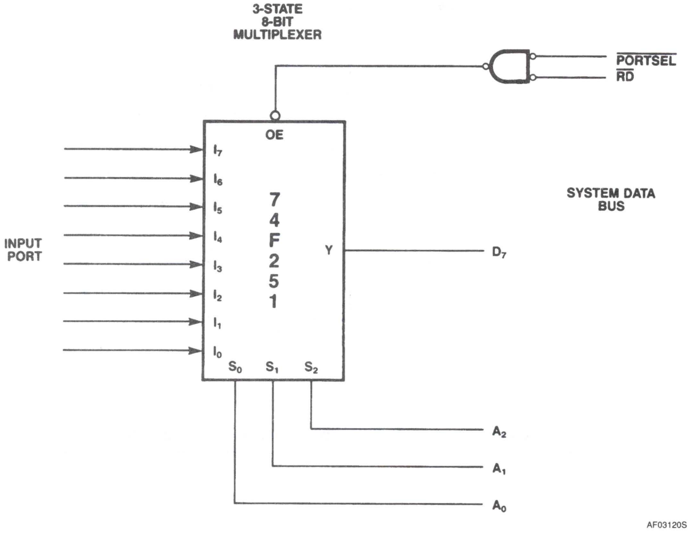

3-STATE
8-BIT
MULTIPLEXER
PORTSEL
RD
OE
I_7
I_6
I_5
I_4
I_3
I_2
I_1
I_0
74F251
Y
D_7
SYSTEM DATA BUS
INPUT PORT
S_0
S_1
S_2
A_2
A_1
A_0
AF03120S

Figure 6. 3-State 8 to 1 Multiplexer Provides Versatile Bit-Oriented Input Port

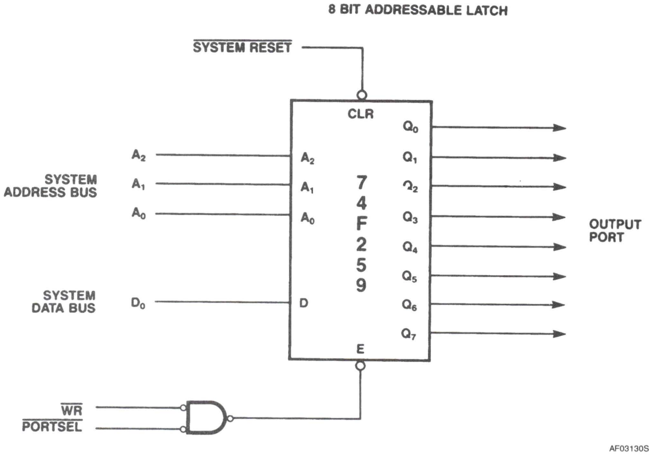

8 BIT ADDRESSABLE LATCH
SYSTEM RESET
CLR
SYSTEM ADDRESS BUS
A_2
A_1
A_0
74F259
Q_0
Q_1
Q_2
Q_3
Q_4
Q_5
Q_6
Q_7
OUTPUT PORT
SYSTEM DATA BUS
D_0
D
E
WR
PORTSEL
AF03130S

Figure 7. 8-Bit Addressable Latch Provides Versatile Bit-Oriented Output Port

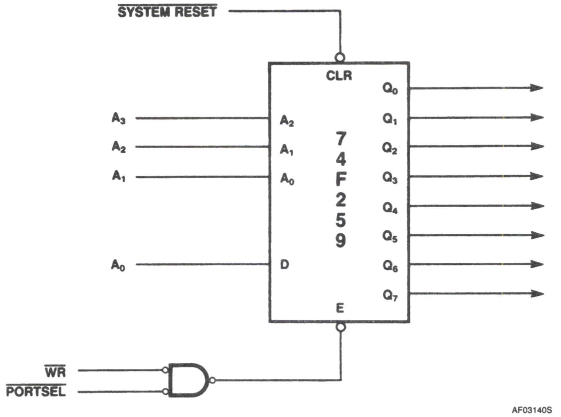

SYSTEM RESET
CLR
74F259
A3
A2
A1
A0
A2
A1
A0
D
E
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
WR
PORTSEL
AF03140S

Figure 8. Bit Addressable Output Port Does Not Require Data Bus

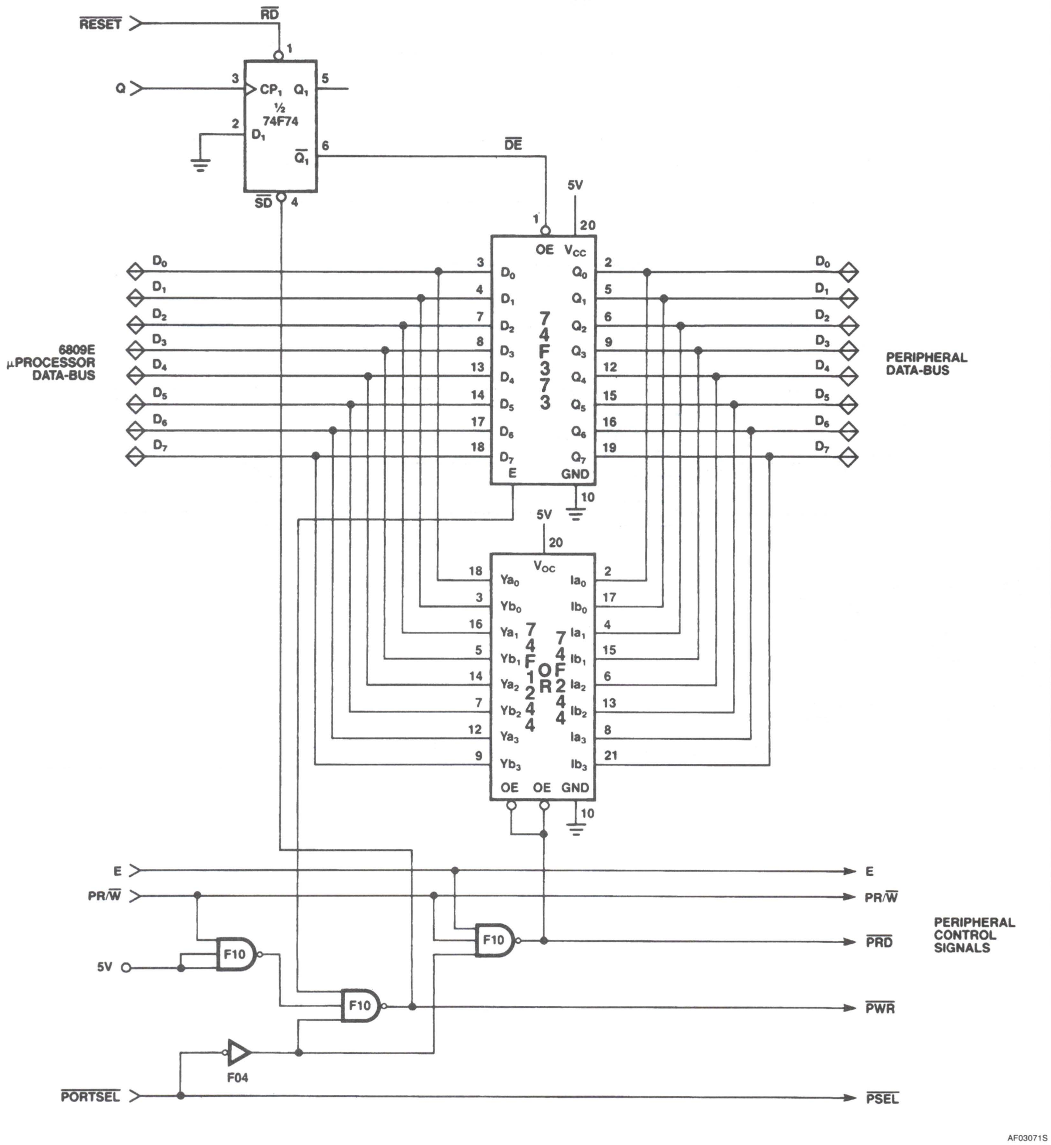
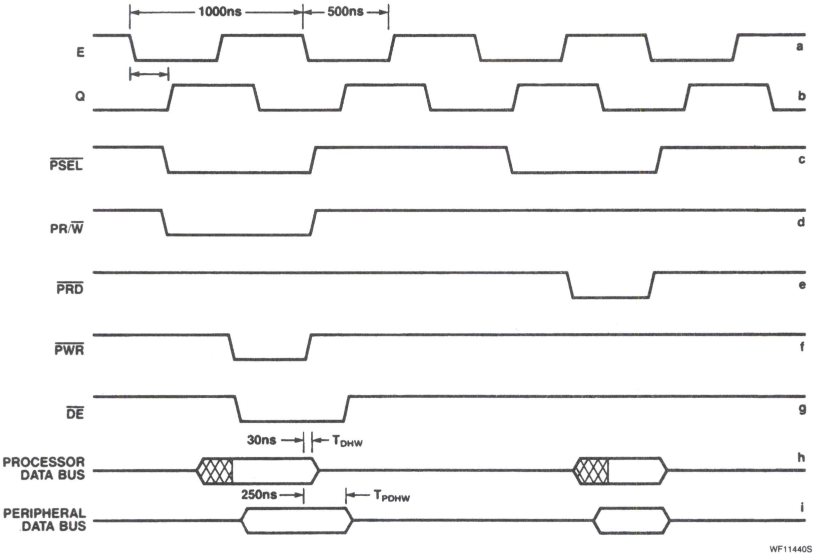

RESET
RD
1
Q
3
CP1
Q1
5
½
74F74
2
D1
Q1
6
DE
SD
4
5V
1
20
OE
VCC
D0
D1
D2
D3
D4
D5
D6
D7
6809E
µPROCESSOR
DATA-BUS
74F373
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
E
GND
10
PERIPHERAL
DATA-BUS
5V
20
VCC
Ya0
Yb0
Ya1
Yb1
Ya2
Yb2
Ya3
Yb3
74F1244
74F0R244
Ia0
Ib0
Ia1
Ib1
Ia2
Ib2
Ia3
Ib3
OE
OE
GND
10
E
PR/W
5V
F10
F10
F10
F04
PORTSEL
E
PR/W
PRD
PWR
PSEL
PERIPHERAL
CONTROL
SIGNALS
AF03071S

Figure 9. Hold Time Extended for Interface to Slow Peripheral With MC6809 Microprocessor


1000ns
500ns
E
Q
$\overline{\text{PSEL}}$
PR/$\overline{\text{W}}$
$\overline{\text{PRD}}$
$\overline{\text{PWR}}$
$\overline{\text{DE}}$
PROCESSOR DATA BUS
PERIPHERAL DATA BUS
30ns
T_{DHW}
250ns
T_{PDHW}
a
b
c
d
e
f
g
h
i
WF11440S

NOTES:

1. RESET	-Power on reset
2. Q	-6809E processor clock (1MHz shown)
3. O	-Quadrature clock for 5809?
4. DE	-Peripheral bus driver enable
5. PR/$\overline{\text{W}}$	-Peripheral READ/$\overline{\text{WRITE}}$
6. PSEL	-Peripheral select
7. PRD	-Peripheral read
8. PWR	-Peripheral write
9. T_{DHW}	-6809E output data hold time
10. T_{PDHW}	-Peripheral write data hold time

Figure 10. Timing Diagram for I/O Bus With Extended Hold Time

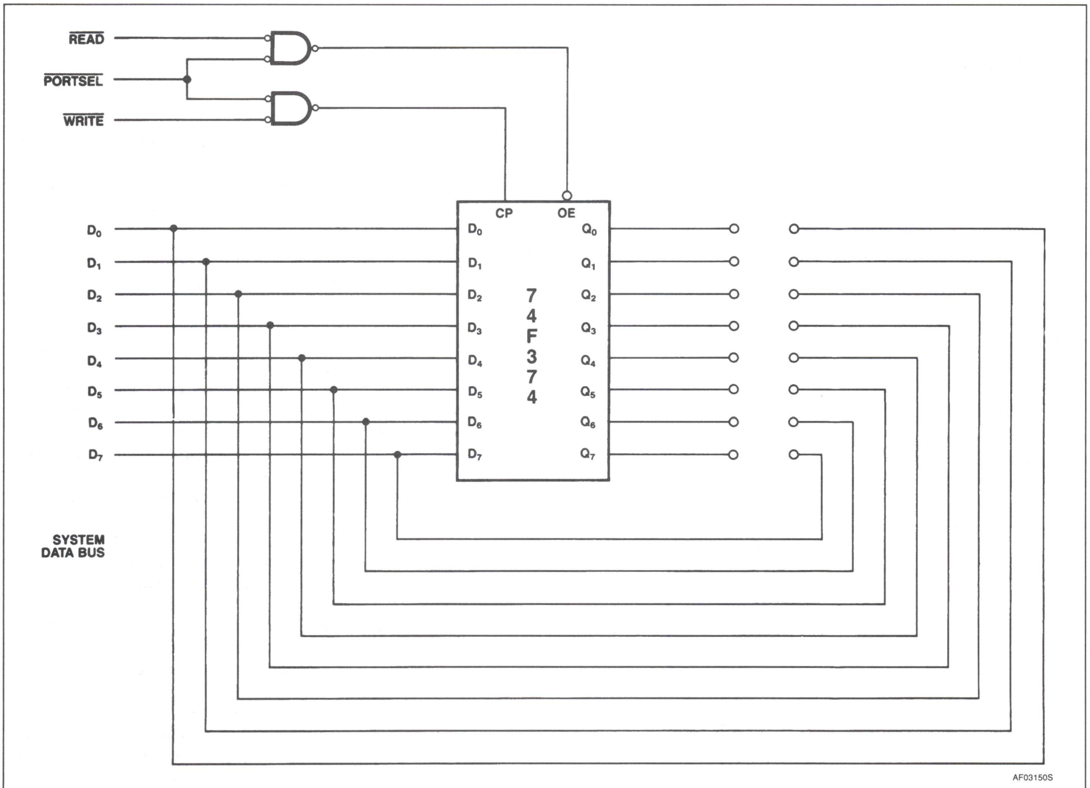

READ
PORTSEL
WRITE
CP
OE
D0
D1
D2
D3
D4
D5
D6
D7
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
74F374
SYSTEM DATA BUS
AF03150S

Figure 11. Data Manipulator Uses Dedicated Hardware

BIBLIOGRAPHY

Many of the applications illustrated in this note were contributed or influenced by entries in Signetics' Interface Circuit design contest. Special thanks are due to the following individuals whose entries were referenced in whole or in part in this note:

V.K. Agrawal
Timothy Anderson
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Loren H. Johnson
Prakash R. Kollaram
G.B. Livingston
Joseph Mastroieni
Jonathan A. Titus
Eugene M. Zumchak

Signetics

AN207
Multiple μP Interfacing With FAST ICs

Application Note

FAST Products

INTRODUCTION

As microprocessor costs continue to decrease and the demands on product performance continue to increase, designers are increasingly turning to multiple microprocessor systems to meet the performance challenge. The introduction of many ''peripheral controller'' type processors has made this choice even more attractive. This application note addresses typical problems associated with interfacing multiple microprocessors, and illustrates the use of Signetics Interface Circuits in solving these problems.

A multi-processor system contains two or more processors communicating through parallel ports, multi-port memories, serial data links, and/or shared buses. The most popular multi-processor architectures are ''loosely coupled'' systems. In loosely coupled systems each processor operates asynchronously with the other processors, usually performing a separate function. Communication is not continuous, and occurs only when necessary.

A special application for multiple microprocessor systems is in redundant systems. As the price of microprocessors dropped, it became economically feasible to achieve greatly increased reliability by employing several processors operating in parallel, performing identical functions. After each operation a vote is taken on the result. If there is disagreement, a fault has been detected, and appropriate corrective action can be taken. Appropriate action might be switching in a third processor, repeating the process, or activating an error sequence and/or an alarm.

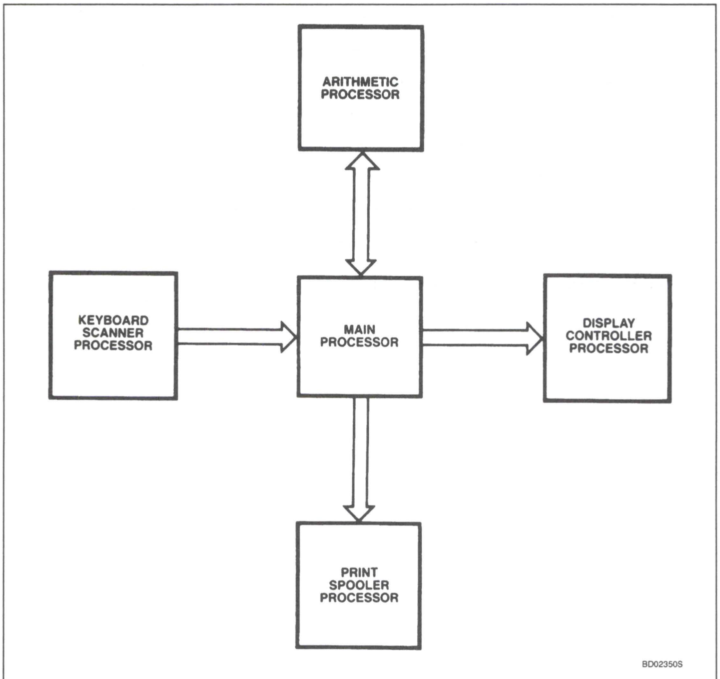

Figure 1. Typical Multi-processor System

In the typical loosely coupled multiple processor system of Figure 1, a main processor ''delegates'' processing work to four other processors. A keyboard scanner microprocessor scans the keyboard continuously, debounces key closures, performs code conversions, and transmits key codes to the main processor in a format that it can easily assimilate. A separate arithmetic processor accepts parameters from the main processor, performs arithmetic calculations, and provides the results for the main processor to read when it is not busy with other tasks. The display controller accepts data and commands from the main processor, then displays and manipulates data on CRT or other displays. The display controller refreshes the display and supports graphic displays without tying up the main processor. The print spooler is a separate processor that accepts files to be printed from the main processor using high-speed data transfers. Then the print spooler stores and feeds data to the printer at the printer's lower data rate, freeing the main processor for other chores. Each processor module contains its own ''local'' ROM, RAM, or I/O, so that it performs its task independently, and communicates with other processors only when necessary. As a result, the system as a whole operates closer to its maximum speed.

Some of the advantages of multiple microprocessor systems are:

- Each processor performs a relatively independent task.
  - Design is easily split among team members.
  - Testing is easily performed on a modular level.
  - Modules can be added or modified without affecting other modules.
- Multi-processing allows distributed processing where modules may be physically separated from the main system.

Multiple μP Interfacing With FAST ICs

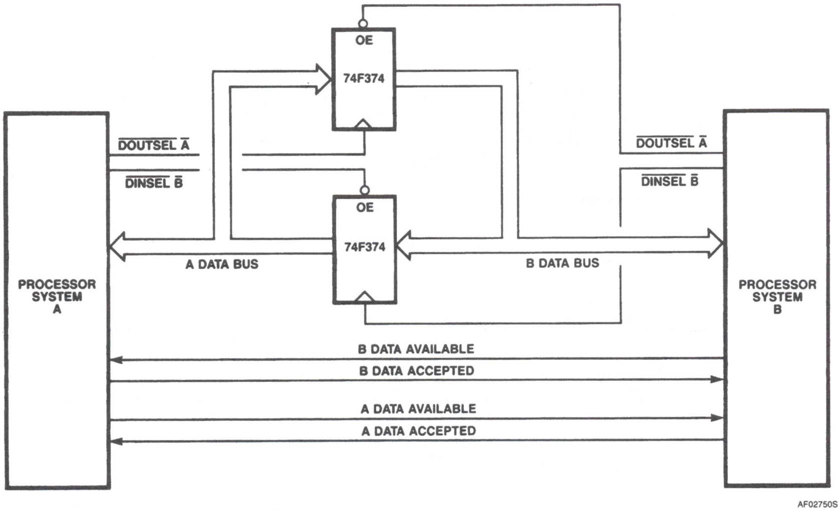

Figure 2. Basic Inter-processor Communication Using Parallel I/O Ports

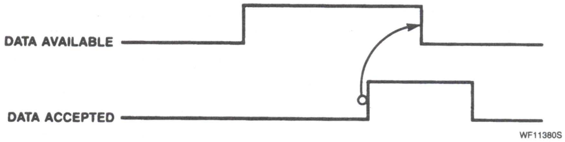

Figure 3. Handshake for Parallel Port Communication

- Parallel processing greatly increases system performance and throughput.
- Hardware cost is less than single-processor systems with similar performance.
- Reliability can be increased easily by redundant processing.

The following application examples illustrate the use of Signetics FAST Interface Circuits in multiple-processor systems.

PARALLEL I/O PORT COMMUNICATIONS

Figure 2 illustrates how parallel I/O ports using Signetics FAST Interface devices are used to accomplish simple 2-processor communications. Two 74F374 octal 3-State registers are used to implement bi-directional parallel data communication. Each 74F374 acts as output port to one processor and input port to the other. The handshake lines are needed when the processors operate asynchronously to ensure that data has been received before new data is transmitted. A handshake timing protocol (Figure 3) implemented in software acts as a traffic cop to assure valid data communications. The transmitting processor starts the handshake by setting Data Available to indicate that data is valid. The receiving processor sets Data Accepted to indicate data has been read. The transmitter then resets Data Available allowing the receiver to reset Data Accepted. The transmitter will not send new data until Data Accepted is reset.

COMMUNICATIONS VIA MULTI-PORT MEMORY

Figure 4 illustrates the logic required for two processors to communicate through a multi-port memory. The RAM is accessible from both processor A and processor B via 74F157 multiplexers used to select one processor's bus at a time. Multi-byte messages and data blocks may be written into the memory by one processor and read out by the other at a later time. No byte-by-byte handshake is required. The multi-port memory provides increased system performance at somewhat higher cost compared to a parallel port technique. Because of the use of multi-port memories in microprocessor systems, these systems can become quite complex. Another application note in this series covers interfacing to multi-port memories in greater depth.

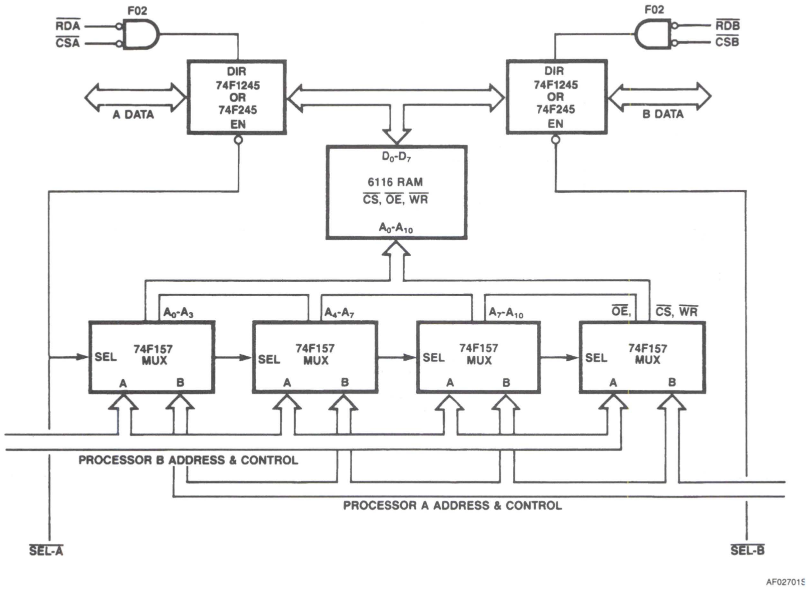

Figure 4. Multiport Memory Provides High-performance Multi-processor Communications

SERIAL COMMUNICATIONS

Although serial communications between multiple processors is slower than the parallel methods examined above, it is usually less expensive and very useful for communicating with remote units. Serial communications via RS-232 or RS-422 links can provide reliable communications over great distances. Implementation of serial communications is simplified by the availability of Universal Asynchronous Receiver Transmitter (UART) devices and well established standards for circuit interfaces and protocols. Figure 5 illustrates local/remote processor communication using Signetics SC2681 UART devices. In many cases additional interface lines are required for handshaking.

SHARED BUS ARCHITECTURE

One of the most powerful multiple processor architectures uses the popular shared bus concept. In Figure 6, each processor has its own local bus with some combination of RAM, ROM, and I/O available locally. The shared bus permits use of "global resources" such as global memory and global I/O which are accessible to all processors on the shared bus. Common interfaces such as printer ports do not have to be implemented for each processor, and may be connected to the shared bus. Multiple processors communicate indirectly with one another through the global RAM. This technique provides highest throughput when interconnecting more than two processors. It also reduces cost through sharing of global resources.

Any processor permitted to drive the system address, data, and control buses is known as a "master." Processors not having this capability are "slaves." A useful attribute of shared bus systems is the ability to add whole new functions by connecting a new master to the bus. Figure 7 illustrates a typical shared system bus interface using Signetics Interface circuits. Three 74F244 octal 3-State buffers are used to drive the 24 bit system address bus (16 bits in some cases). Two 74F245 octal bidirectional 3-State buffers are used to drive the 16 bit data bus (8 bits in some cases). In addition, half a 74F244 is used to drive the system command bus, composed of the signals $\overline{\text{IORD}}$, $\overline{\text{IOWR}}$, $\overline{\text{MEMRD}}$, and $\overline{\text{MEMWR}}$.

Multiple local processors may request use of the shared bus by setting $\overline{\text{BUS REQUEST}}$ active and waiting for the arbitration logic to assert $\overline{\text{BUS GRANT}}$. The arbitration logic indicates to the local processor when it may access the shared bus after a request has been made. This is necessary to prevent more than one local processor from accessing the system bus at the same time, resulting in bus contention and possible system failure.

ARBITRATION

Contention by several processors for use of shared resources can create sticky timing problems unless care is exercised in the design of appropriate arbitration logic to resolve timing conflicts. Schemes for bus arbitration vary in speed, cost, and flexibility and involve parallel, serial, transparent, pseudo-transparent, polled, and flag operations.

Parallel Priority Resolution

Parallel priority resolution is most useful in systems with 4 or more masters, where its speed outweighs the disadvantage of the additional hardware. A scheme for system bus arbitration using parallel priority resolution is illustrated in Figure 8.

A master's priority is determined by using a 74F148 priority encoder. Each master's arbitration logic generates a $\overline{\text{REQ}}$ to the priority encoder. When there is contention, the master whose $\overline{\text{REQ}}$ is connected to the highest priority input will be granted access.

A 74F138 is used to decode the encoder outputs to generate the $\overline{\text{EI}}$ (enable input) to the arbitration logic of the master which has been granted access. $\overline{\text{CLEAR}}$ is used to remove all masters from the bus during reset or when an error condition is present. $\overline{\text{ARB CLOCK}}$ is used to synchronize all bus arbitration inputs and outputs to prevent race conditions and to facilitate a standard interface

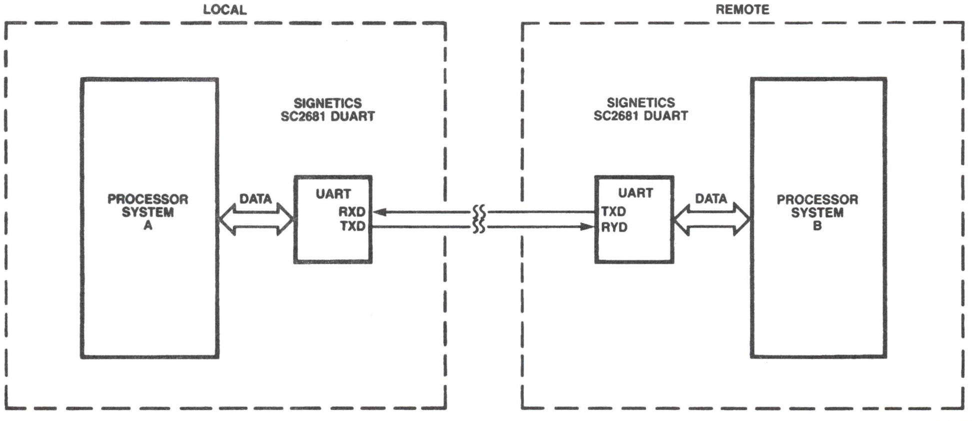
LOCAL
REMOTE
SIGNETICS SC2681 DUART
SIGNETICS SC2681 DUART
PROCESSOR SYSTEM A
DATA
UART
RXD
TXD
UART
TXD
RYD
DATA
PROCESSOR SYSTEM B
BD02360S

Figure 5. Serial Communications Link Provides Economical Inter-processor Communications

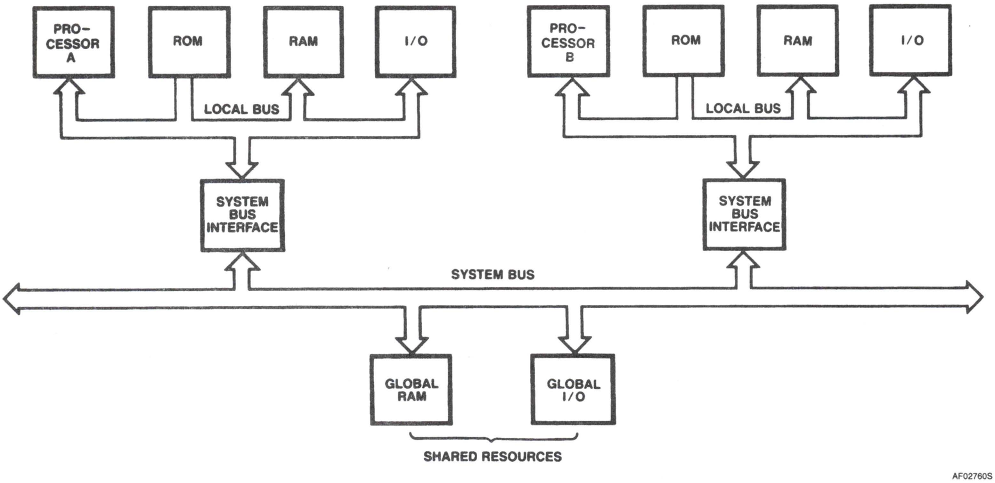
PRO-CESSOR A
ROM
RAM
I/O
PRO-CESSOR B
ROM
RAM
I/O
LOCAL BUS
LOCAL BUS
SYSTEM BUS INTERFACE
SYSTEM BUS INTERFACE
SYSTEM BUS
GLOBAL RAM
GLOBAL I/O
SHARED RESOURCES
AF02760S

Figure 6. Shared Bus Provides Most Powerful Multiple Processor Architecture

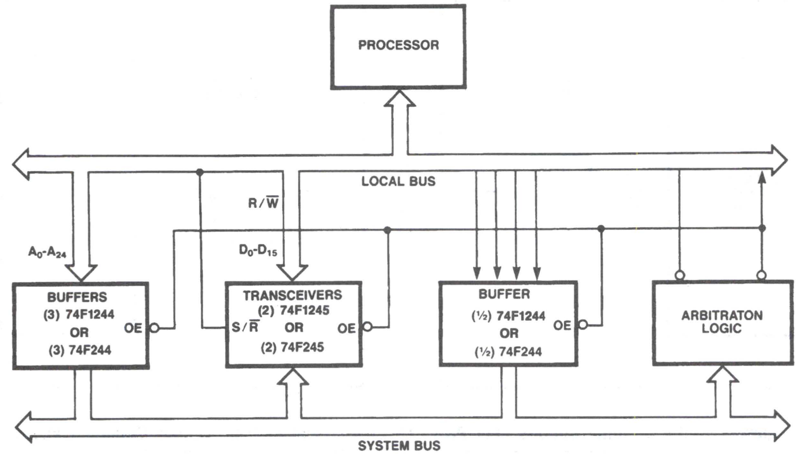
PROCESSOR
LOCAL BUS
R/W̄
A0-A24
D0-D15
BUFFERS
(3) 74F1244
OR
(3) 74F244
OE
TRANSCEIVERS
(2) 74F1245
S/R̄
OR
(2) 74F245
OE
BUFFER
(½) 74F1244
OR
(½) 74F244
OE
ARBITRATON
LOGIC
SYSTEM BUS
AF02711S

Figure 7. Typical System Bus Interface

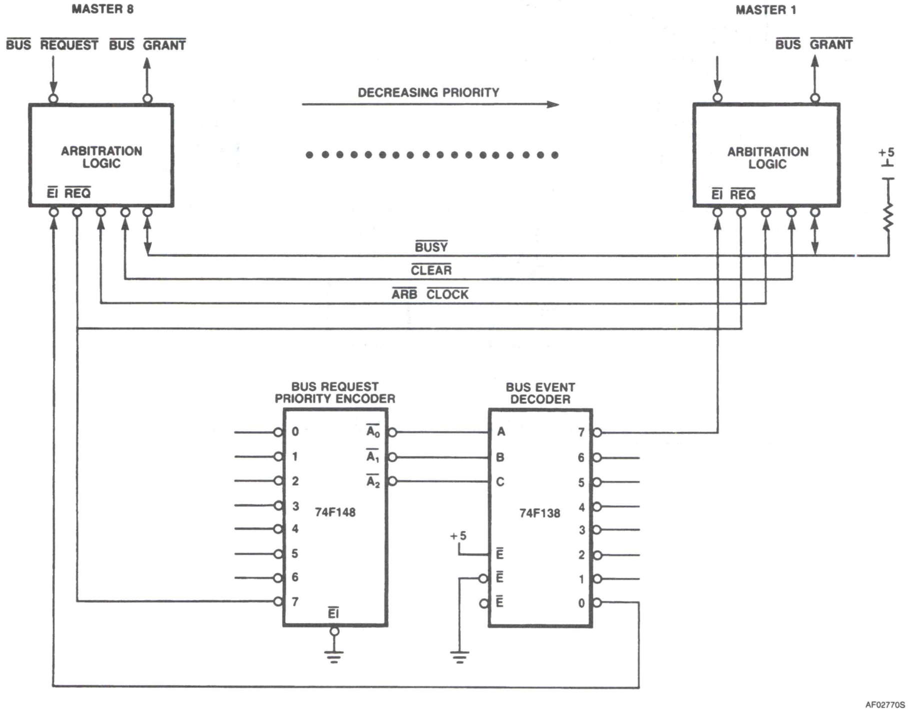
MASTER 8
BUS REQUEST BUS GRANT
DECREASING PRIORITY
MASTER 1
BUS GRANT
ARBITRATION
LOGIC
EI REQ
ARBITRATION
LOGIC
EI REQ
+5
BUSY
CLEAR
ARB CLOCK
BUS REQUEST
PRIORITY ENCODER
74F148
0
1
2
3
4
5
6
7
A0
A1
A2
EI
BUS EVENT
DECODER
74F138
A
B
C
+5
E
E
E
7
6
5
4
3
2
1
0
AF02770S

Figure 8. System Bus Arbitration Using Parallel Priority Resolution

Multiple μP Interfacing With FAST ICs AN207

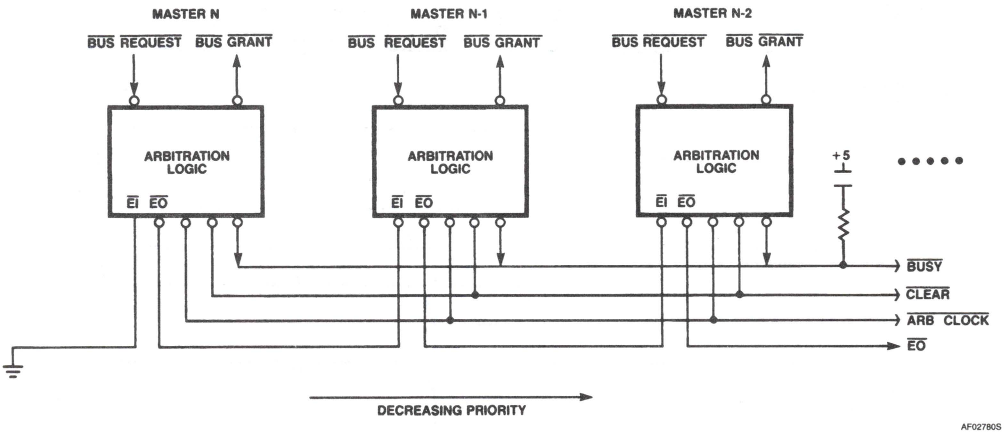
MASTER N
BUS REQUEST
BUS GRANT
MASTER N-1
BUS REQUEST
BUS GRANT
MASTER N-2
BUS REQUEST
BUS GRANT
ARBITRATION LOGIC
ARBITRATION LOGIC
ARBITRATION LOGIC
EI EO
EI EO
EI EO
+5
BUSY
CLEAR
ARB CLOCK
EO
DECREASING PRIORITY
AF02780S

Figure 9. System Bus Arbitration Using Serial Priority Resolution

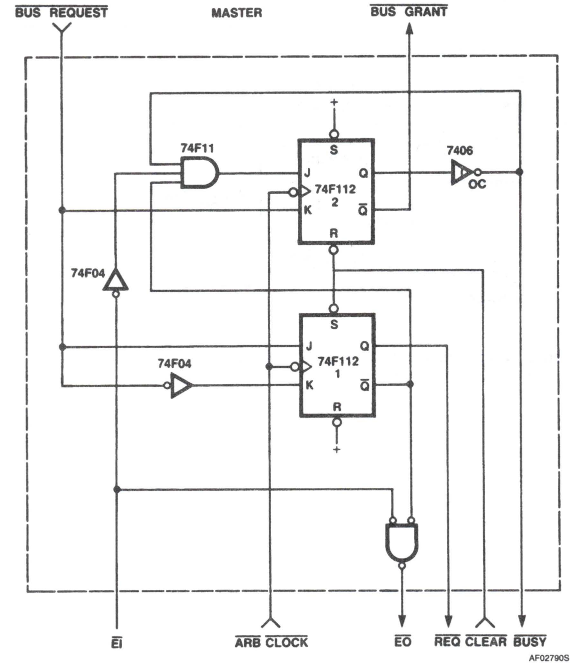
BUS REQUEST
MASTER
BUS GRANT
74F11
S
J
Q
74F112
2
K
Q̄
R
7406
OC
74F04
S
J
Q
74F112
1
K
Q̄
R
74F04
+
+
EI
ARB CLOCK
EO
REQ
CLEAR
BUSY
AF02790S

Figure 10. Arbitration Logic Supports Serial Or Parallel Priority Resolution Techniques

design. $\overline{\text{BUSY}}$ is generated by the master currently accessing the bus to indicate that the bus is in use. Even after a master has been granted access by the priority resolution, it must still wait for the current master to vacate the bus, i.e., $\overline{\text{BUSY}}$ going inactive. The arbitration logic generates a $\overline{\text{BUS GRANT}}$ to a master when $\overline{\text{EI}}$ is asserted and $\overline{\text{BUSY}}$ is not.

Serial Priority Resolution

Serial priority resolution eliminates the need for encoder/decoder hardware at the expense of speed. In Figure 9 a master's priority is determined by its physical location in a daisy chain configuration. A master negates its $\overline{\text{EO}}$ (enable output) when its $\overline{\text{EI}}$ (enable input) is negated or when it wants to access the bus. This negates $\overline{\text{EO}}$ for all masters further down the line *to go inactive*. If a master requests the bus, and no higher priority master is requesting the bus, as indicated by $\overline{\text{EI}}$ being asserted, the master may access the bus when the current master is finished. The ARB clock rate is limited to the speed at which the daisy chain signals can propagate through all masters.

Arbitration Logic

Arbitration logic suitable for either parallel or serial priority resolution is illustrated in Figure 10. The logic shown synchronizes a master's $\overline{\text{BUS REQUEST}}$ input to $\overline{\text{ARB CLOCK}}$ using flip-flop 1, asserting $\overline{\text{REQ}}$ and negating $\overline{\text{EO}}$. If $\overline{\text{EI}}$ is asserted and $\overline{\text{BUSY}}$ is not, the master may access the bus on the next falling edge of $\overline{\text{ARB CLOCK}}$. This arbitration is provided by flip-flop 2. $\overline{\text{BUS GRANT}}$ and $\overline{\text{BUSY}}$ are asserted. When the access is complete, the master negates $\overline{\text{BUS REQUEST}}$ inactive. On the falling edge of $\overline{\text{ARB CLOCK}}$, $\overline{\text{REQ}}$ negated and, if $\overline{\text{EI}}$ is asserted $\overline{\text{EO}}$ is asserted. On the next falling edge $\overline{\text{BUSY}}$ and $\overline{\text{BUS GRANT}}$ are negated. The timing diagram for this sequence is illustrated in Figure 11. Note that a master must wait for the current master to complete a transfer and negate $\overline{\text{BUSY}}$ before it may access the bus.

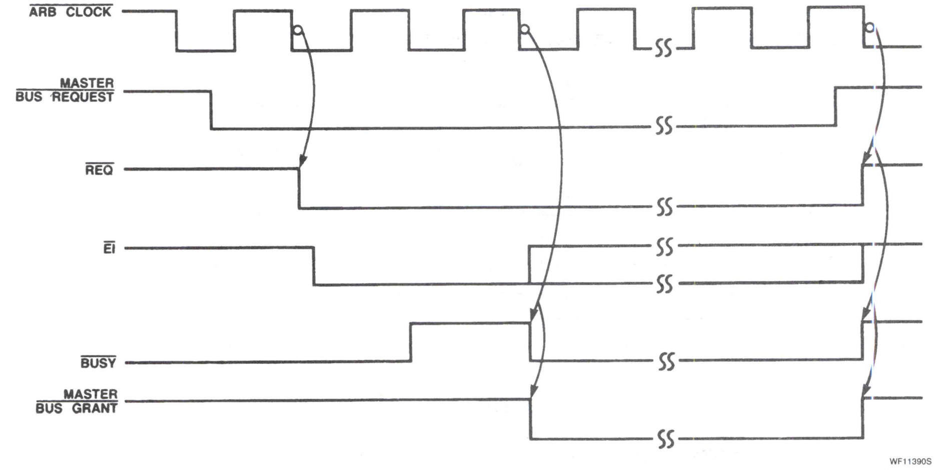
ARB CLOCK
MASTER BUS REQUEST
REQ
EI
BUSY
MASTER BUS GRANT
WF11390S

Figure 11. Timing Diagram for Arbitration Logic

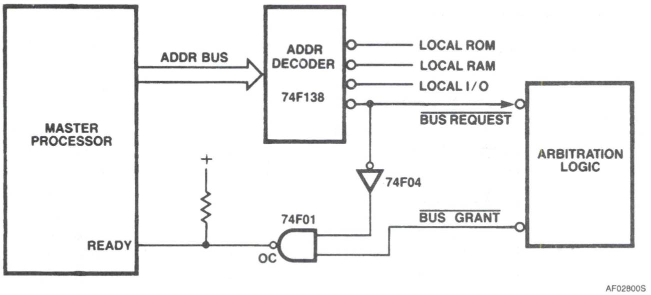
MASTER PROCESSOR
ADDR BUS
ADDR DECODER
74F138
LOCAL ROM
LOCAL RAM
LOCAL I/O
BUS REQUEST
ARBITRATION LOGIC
74F04
74F01
BUS GRANT
READY
OC
+
AF02800S

Figure 12. Pseudo-Transparent Access to Shared Bus

Multiple µP Interfacing With FAST ICs

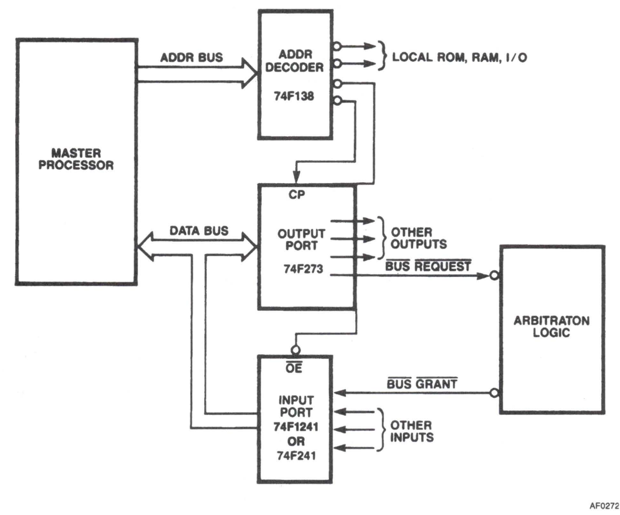
MASTER PROCESSOR
ADDR BUS
ADDR DECODER
74F138
LOCAL ROM, RAM, I/O
CP
DATA BUS
OUTPUT PORT
74F273
OTHER OUTPUTS
BUS REQUEST
ARBITRATON LOGIC
OE
BUS GRANT
INPUT PORT
74F1241 OR 74F241
OTHER INPUTS
AF02721S

Figure 13. Polled Access to Shared Bus

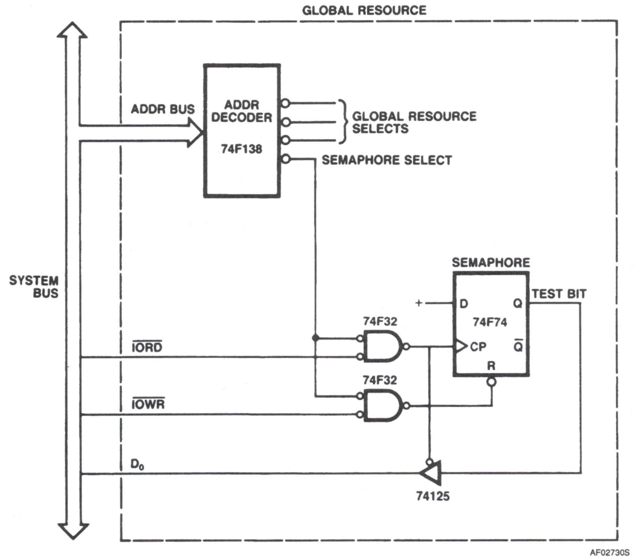
GLOBAL RESOURCE
ADDR BUS
ADDR DECODER
74F138
GLOBAL RESOURCE SELECTS
SEMAPHORE SELECT
SEMAPHORE
SYSTEM BUS
+
D
Q
TEST BIT
74F32
74F74
CP
Q̄
R
IORD
74F32
IOWR
D0
74125
AF02730S

Figure 14. Semaphore (Flag) Register Permits Access to Shared Resource Without Monopolizing Shared Bus

Pseudo-Transparent Priority Resolution

The logic of Figure 12 uses "cycle stealing" to permit single byte transfers with pseudo-transparent arbitration. When the address decoder determines that a master requires access to shared bus, it asserts $\overline{\text{BUS REQUEST}}$. The processor's READY line is held negated, "freezing" the processor until the arbitration logic asserts $\overline{\text{BUS GRANT}}$. Then READY is asserted and the shared bus cycle occurs. The processor is unaware of arbitration and unaware that the bus is shared. With this technique, a watchdog timer should be used to ensure that the processor doesn't "hang up" if faulty bus operation prevents access. Access occurs one cycle at a time, preventing any one master from "hogging" the bus.

Polled Access to Shared Bus

The logic in Figure 13 uses an output port to request access to the bus, and polls an input port to determine when access has been granted. Once access is granted, the master retains the bus until it negates the $\overline{\text{BUS REQUEST}}$ output port bit. Large block moves may occur without fear of another master changing the data as with cycle-by-cycle arbitration. However, this approach greatly slows down the response time of the system, because of the waiting while each master performs. All other masters must wait, even if they do not require the use of the same shared resource.

Semaphore (Flag) Arbitration

The logic of Figure 14 improves on the polled access technique by permitting access to a shared resource when that resource is available. A master first reads the semaphore register associated with the resource it wishes to access. The master may not access the resource unless the semaphore bit is false. When the semaphore bit is false, reading the register automatically sets the bit true. When the master reads a false semaphore, it may then access the resource. All other masters reading the semaphore will see it set and will not access the resource. The master may access the resource until it is no longer needed. By writing to the semaphore register, it is automatically reset, allowing other masters to access the resource. Only the one resource, not the entire shared bus, is monopolized by one master at a time. The hardware performs a function similar to a software read-modify-write operation.

The timing for the semaphore operation is shown in Figure 15. If the semaphore bit is false and the register is read, the bit is set true at the end of the read cycle (rising edge of $\overline{\text{IORD}}$). The semaphore bit is reset by doing a "dummy" write to the semaphore register. The bit is set false at the beginning of the cycle ($\overline{\text{IOWR}}$ going low).

INTERFACING THE MC68000 TO THE MULTIBUS™*

One of the best examples of a multi-processor shared bus is the MULTIBUS. One of the most popular 16 bit processors in new designs today is the MC68000. Yet, to our knowledge, there are currently (mid-83) no LSI MULTIBUS arbiter ICs available to allow a designer to easily interface the two. There are arbiter ICs available, but they were designed for other processors and are cumbersome and limited in performance when interfaced to the 68000.

---

*MULTIBUS is a trademark of Intel Corporation.

The following is the design for a 68000 MULTIBUS interface. The design supports serial or parallel arbitration and performs with a 10MHz bus clock. Operation is similar to the example described previously. Tables 1 and 2 define the MC68000 bus control signals and the MULTIBUS arbitration signals. The timing diagram for MC68000 read and write cycles is shown in Figure 16.

Figure 17 illustrates the control circuitry for the MC68000 to MULTIBUS interface. The master initiates a MULTIBUS transfer by asserting $\overline{\text{MULTIREQ}}$ active. This is usually the output of address decode circuitry. $\overline{\text{AS}}$ clears the request at the end of the transfer. Flip-flops 1, 2, and 3 sample and synchronize the bus request to the falling edge of $\overline{\text{BCLK}}$. Since $\overline{\text{MULTIREQ}}$ is asynchronous to $\overline{\text{BCLK}}$, flip-flop 2 serves as a synchronizer and is clocked on the rising edge of $\overline{\text{BCLK}}$. All inputs to the arbiter are thus synchronous so that race conditions at flip-flop inputs are avoided.

If the bus is not in use ($\overline{\text{BUSY}}$ is not asserted), and no higher priority master requests the bus ($\overline{\text{BRPN}}$ is asserted), the master is granted access on the next falling edge of $\overline{\text{BCLK}}$. Flip-flop 4 provides this function. If these conditions are not satisfied, $\overline{\text{DTACK}}$ is used to force the CPU to wait. Once the master is granted access, it sets $\overline{\text{BUSY}}$ active to indicate that the bus is in use. $\overline{\text{BUSEN}}$ (bus enable) also becomes active and gates the master's address, data, and control buses onto the MULTIBUS. One half cycle later, on the rising edge of $\overline{\text{BCLK}}$, flip-flop 5 sets CMDEN (Command Enable) active. This allows RD or WR strobes to be asserted on the MULTIBUS. This delay is necessary because the MULTIBUS requires data and address valid 50ns before read or write commands. DS is used to generate the read or write strobes.

The MULTIBUS transfer is completed when $\overline{\text{XACK}}$ is asserted terminating the 68000 cycle by asserting $\overline{\text{DTACK}}$. The master maintains control of the MULTIBUS until another master requests access, as indicated by asserted $\overline{\text{CBRQ}}$. If the current master is not performing a MULTIBUS transfer, it loses the bus on the next falling edge of $\overline{\text{BCLK}}$. CMDEN, $\overline{\text{BUSEN}}$, and $\overline{\text{BUSY}}$ are negated. Flip-flop 4 provides this function.

Table 1. MC68000 Bus Control Signals. (Refer To The Signetics 68000 Microprocessor Data Sheet For More Information.)

CLK	Clock. Time reference for 68000 microprocessor bus control.
$\overline{\text{AS}}$	Address Strobe. Indicates that address on address bus is valid.
$\overline{\text{UDS}}$, $\overline{\text{LDS}}$	Upper and Lower Data Strobe. Indicates that the processor is reading from or writing to the upper data byte $(D_7 - D_{15})$ and/or the lower data byte $(D_0 - D_7)$.
R/$\overline{\text{W}}$	Read/Write. Indicates whether the current bus cycle is a read or a write cycle.
$\overline{\text{DTAK}}$	Data Transfer Acknowledge. Input to the 68000 indicating that the data transfer can be completed, on the high to low transition.
$\overline{\text{BCLK}}$	Bus Clock. All arbitration signals listed below must be synchronized to the negative edge of this clock. It is independent of any processor clock.
$\overline{\text{BPRN}}$	Bus Priority In. Indicates that no higher priority master is requesting the bus. Similar to $\overline{\text{EI}}$ in previous examples.
$\overline{\text{BPRO}}$	Bus Priority Out. Used in serial priority resolution circuits. Similar to $\overline{\text{EO}}$ in previous examples.
$\overline{\text{BUSY}}$	Bus Busy. Driven by current bus master to indicate that the bus is in use.
$\overline{\text{BREQ}}$	Bus Request. Used in parallel priority resolution circuits. Similar to $\overline{\text{REQ}}$ in previous examples.
$\overline{\text{CBRQ}}$	Common Bus Request. Driven by all potential bus masters requesting bus. Used to save time by allowing the present bus master to avoid arbitration after each cycle if no other requests are active.
$\overline{\text{XACK}}$	Transfer Acknowledge. Indicates that the MULTIBUS data transfer is completed on high to low transition.

The logic that interfaces the MC68000 to the MULTIBUS is shown in Figure 18. 74F533 inverting octal 3-State latches are used to gate the 20 bit address and 16 bits of data onto the MULTIBUS. Note that the data and address bus is negative true. 74F240 octal 3-State inverting buffers are used to gate 16 bits of data onto and off of the MULTIBUS. Data direction is determined by the MC68000's R/W line. A 74F139, 2 to 4 decoder is used to decode I/O and RD/WR to generate the 4 MULTIBUS commands. I/O is the output of address decode circuitry which decodes I/O addresses. A 74F244 is used to gate the commands onto the MULTIBUS.

Signetics FAST logic family is used in this design to increase speed and bus drive capability while minimizing MULTIBUS loading.

REDUNDANT MICROPROCESSORS ENHANCE RELIABILITY

Figure 19 illustrates how two 6809E microprocessors are used in a parallel redundancy scheme to prevent faulty operation from damaging external systems. Two systems with identical processors, RAM, ROM, and I/O are first synchronized. After synchronization, their data buses are compared every cycle. If the data on the two buses is different, an error has occurred and the system shuts down.

A common clock is used to drive the 6809E processor in each system so that a timing reference is established. Upon reset, both processors execute a sync instruction and the critical output circuits are turned off. When both processors have executed the sync instruction, as indicated by BA = 0 and BS = 1, the START button is used to interrupt the processors and they begin program execution in synchronism. The critical outputs are also turned on. On the falling edge of E, the data buses of the two systems are compared using the 74F521 octal comparator. If the data does not match, at least one system is operating incorrectly. The 74F74 flip-flop latches the error condition and turns off the critical outputs.

A similar technique should be used on outputs to ensure that an output goes active only when the output of both systems goes active.

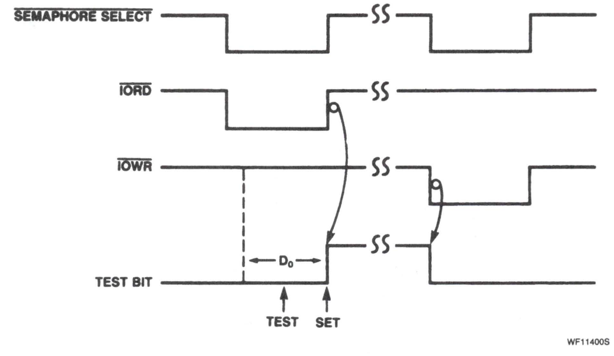
SEMAPHORE SELECT
IORD
IOWR
TEST BIT
D0
TEST
SET
WF11400S

Figure 15. Timing Diagram for Semaphore Operation

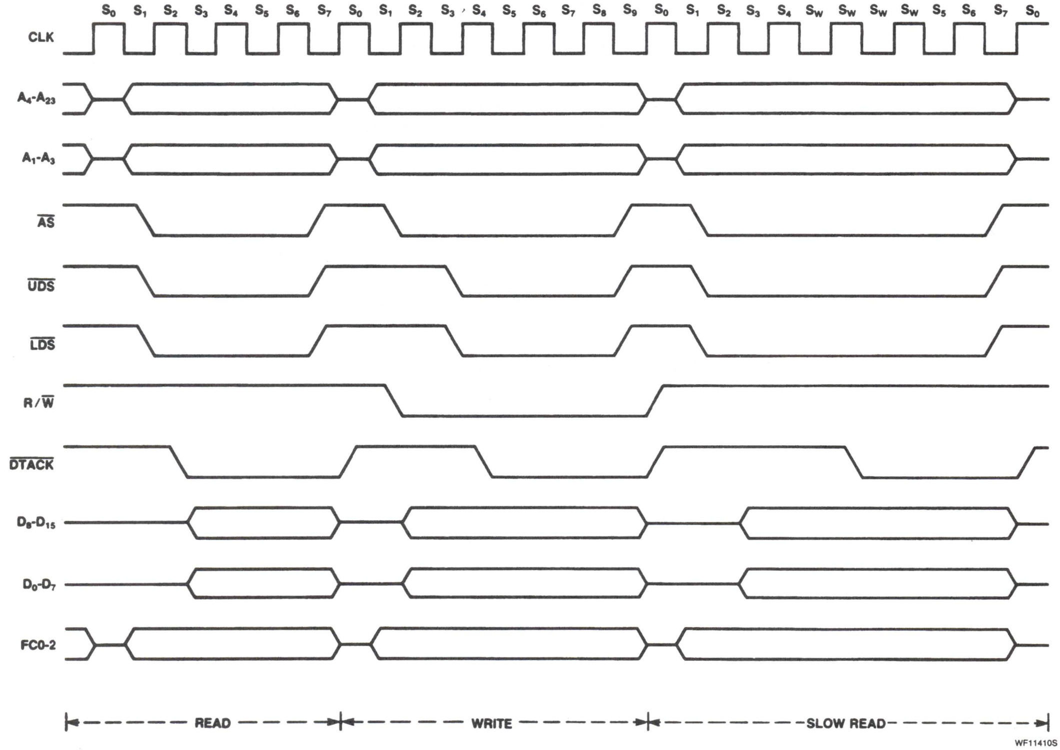
S0 S1 S2 S3 S4 S5 S6 S7 S0 S1 S2 S3 S4 S5 S6 S7 S8 S9 S0 S1 S2 S3 S4 Sw Sw Sw Sw S5 S6 S7 S0
CLK
A4-A23
A1-A3
AS
UDS
LDS
R/W
DTACK
D8-D15
D0-D7
FC0-2
READ
WRITE
SLOW READ
WF11410S

Figure 16. MC68000 Read and Write Cycle Timing Diagram

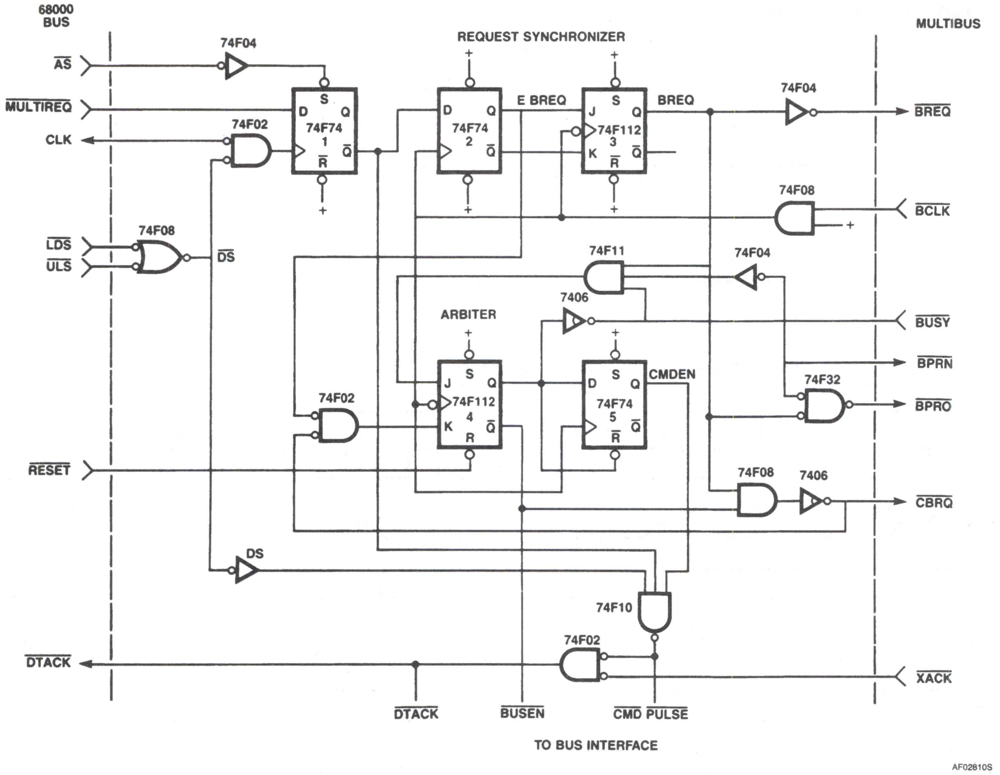
68000 BUS
MULTIBUS
REQUEST SYNCHRONIZER
74F04
AS
MULTIREQ
CLK
74F02
74F74 1
74F74 2
E BREQ
74F112 3
BREQ
74F04
BREQ
74F08
BCLK
LDS
ULS
74F08
DS
74F11
74F04
7406
BUSY
ARBITER
BPRN
74F112 4
74F74 5
CMDEN
74F32
BPRO
74F02
RESET
74F08
7406
CBRQ
DS
74F10
74F02
DTACK
XACK
DTACK
BUSEN
CMD PULSE
TO BUS INTERFACE
AF02810S

Figure 17. MC68000 MULTIBUS Interface Control Circuitry

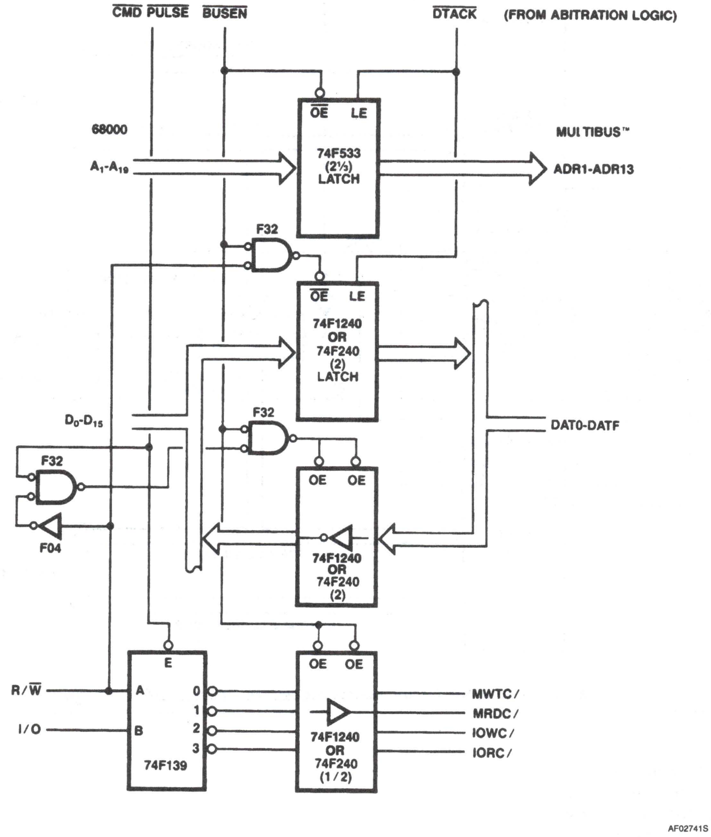
CMD PULSE
BUSEN
DTACK
(FROM ABITRATION LOGIC)
68000
A_1-A_{19}
OE LE
74F533 (2½) LATCH
MULTIBUS™
ADR1-ADR13
F32
OE LE
74F1240 OR 74F240 (2) LATCH
D_0-D_{15}
DAT0-DATF
F32
F32
F04
OE OE
74F1240 OR 74F240 (2)
R/W
I/O
E
A
B
0
1
2
3
74F139
OE OE
74F1240 OR 74F240 (1/2)
MWTC/
MRDC/
IOWC/
IORC/
AF02741S

Figure 18. MC68000 to MULTIBUS Interface Logic

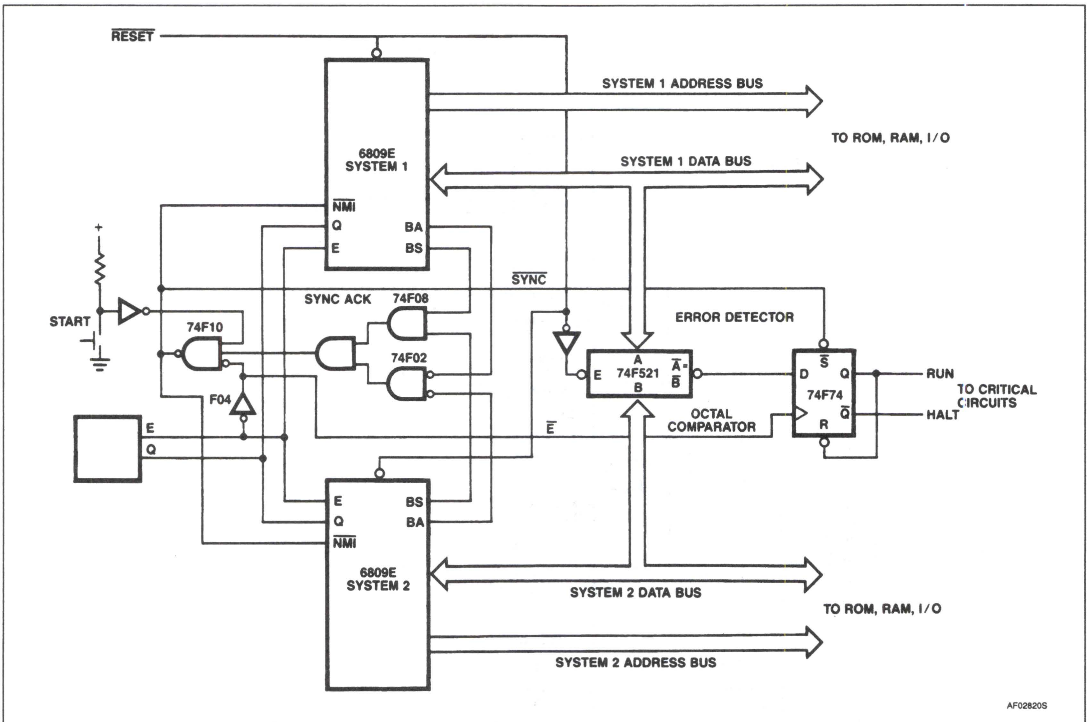
RESET
6809E
SYSTEM 1
SYSTEM 1 ADDRESS BUS
TO ROM, RAM, I/O
SYSTEM 1 DATA BUS
NMI
Q
E
BA
BS
SYNC
SYNC ACK
74F08
ERROR DETECTOR
START
74F10
74F02
F04
A
E 74F521
B
A=B
D
S
Q
74F74
R
Q
RUN
HALT
TO CRITICAL CIRCUITS
OCTAL COMPARATOR
E
Q
E
6809E
SYSTEM 2
BS
BA
SYSTEM 2 DATA BUS
TO ROM, RAM, I/O
SYSTEM 2 ADDRESS BUS
AF02820S

Figure 19. Redundant 6809E Microprocessors Prevent I/O Damage

BIBLIOGRAPHY

Many of the applications illustrated in this note were contributed or influenced by entries in Signetics' Interface Circuit design contest. Special thanks are due to the individuals whose entries were referenced in whole or in part in this note.

Signetics

FAST Products

AN208
Interrupt Control Logic Using FAST ICs

Application Note

INTRODUCTION

This application note shows how Signetics FAST circuits can be used to implement interrupt control logic for a variety of microprocessors. The circuits presented serve a variety of functions, which include:

- Masking: How to selectively enable interrupt inputs
- Prioritizing: Which interrupt is serviced when more than one interrupt occurs
- Vector Generation: How the interrupt service routine is selected

An interrupt is an asynchronous input to a microprocessor that suspends current program execution and causes a jump to an interrupt service routine. Interrupts are especially useful in real-time systems and have become a standard feature in microprocessor designs.

REASONS FOR USING INTERRUPTS

The use of interrupts generally increases the efficiency of the system. Without interrupts, the microprocessor must poll each peripheral to determine when it is ready for service. The time spent polling cuts down available processing time, and polling is unnecessary when the peripheral devices are not ready for service. With interrupts, the peripheral device informs the processor when it is ready; thus no time is wasted.

Interrupts also provide faster response to service requests from a peripheral. The high data rate of many devices, (e.g. disk drives) requires immediate response to prevent loss of data. As another example, a power-fail interrupt can be used to initiate an orderly shutdown in the remaining moments.

Interrupts can also be used for error handling. If a parity error is detected in the memory, for example, an interrupt can be generated to suspend the operation of the program or invoke an error-handling routine.

INTERRUPT LATCHING

Figure 1 shows a circuit that captures asynchronous events and generates an interrupt to the microprocessor. The 74F533 inverting octal latch is used to "freeze" the state of the interrupt inputs. This is necessary to catch short interrupt request pulses. When all interrupt requests are inactive, the latch enable (LE) input of the 74F533 is asserted. When any request is asserted, the interrupt signal to the microprocessor ($\overline{\text{INT}}$) is asserted and the latch is disabled. Thus, the state of the interrupt inputs is latched.

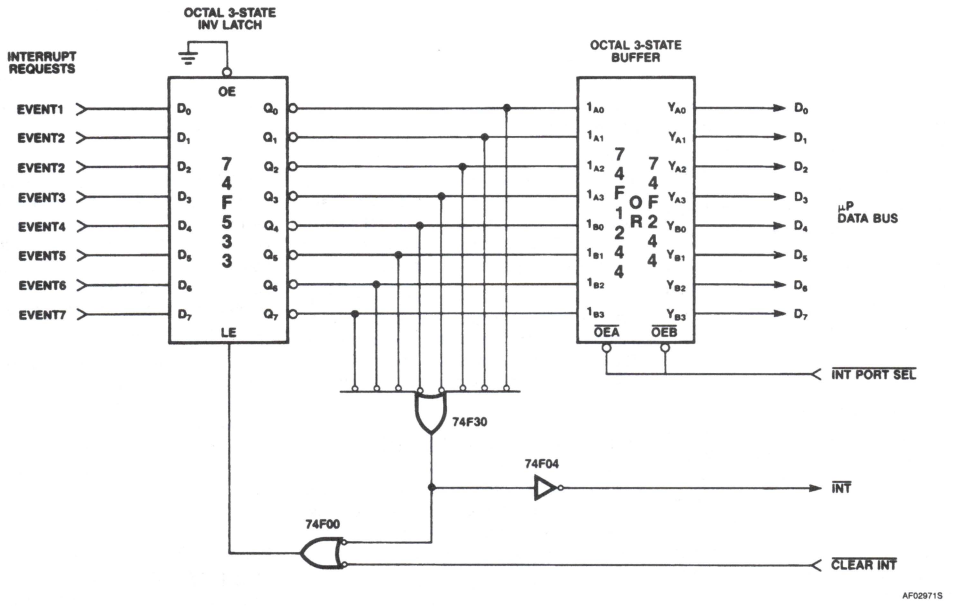
OCTAL 3-STATE INV LATCH
INTERRUPT REQUESTS
EVENT1
EVENT2
EVENT2
EVENT3
EVENT4
EVENT5
EVENT6
EVENT7
OE
D0
D1
D2
D3
D4
D5
D6
D7
74F533
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
LE
OCTAL 3-STATE BUFFER
1A0
1A1
1A2
1A3
1B0
1B1
1B2
1B3
74F1244 OR 74F244
YA0
YA1
YA2
YA3
YB0
YB1
YB2
YB3
OEA
OEB
D0
D1
D2
D3
D4
D5
D6
D7
µP DATA BUS
INT PORT SEL
74F30
74F04
INT
74F00
CLEAR INT
AF02971S

Figure 1. Interrupt Latching

Interrupt Control Logic Using FAST ICs

AN208

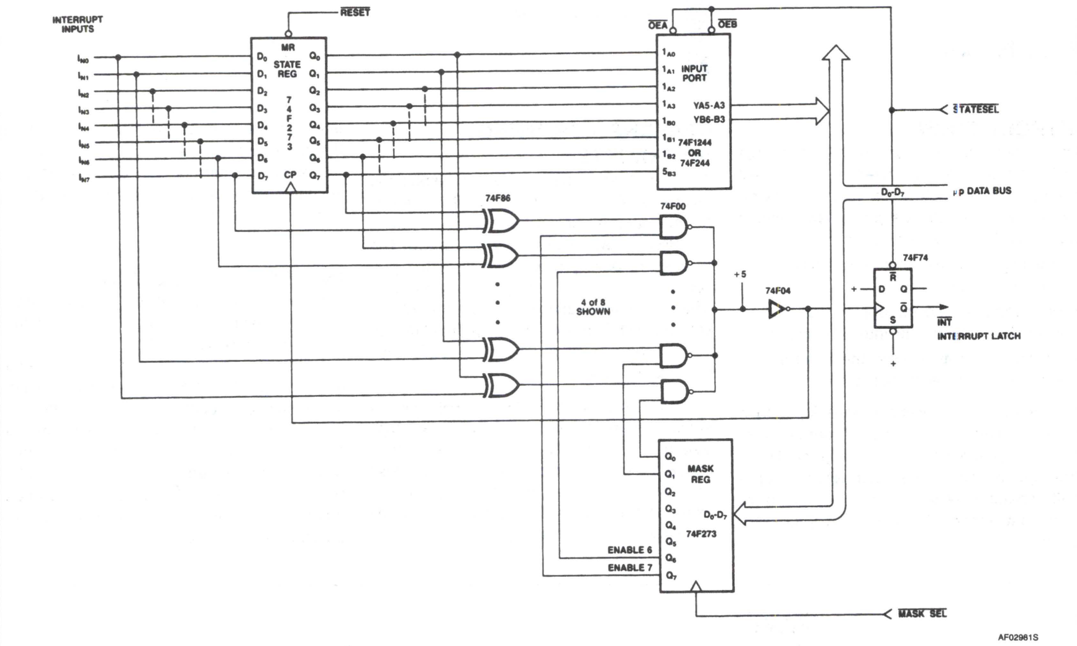
INTERRUPT INPUTS
I_{N0}
I_{N1}
I_{N2}
I_{N3}
I_{N4}
I_{N5}
I_{N6}
I_{N7}
$\overline{RESET}$
MR
STATE REG
74F273
D_0 D_1 D_2 D_3 D_4 D_5 D_6 D_7
Q_0 Q_1 Q_2 Q_3 Q_4 Q_5 Q_6 Q_7
CP
$\overline{OEA}$
$\overline{OEB}$
INPUT PORT
1_{A0} 1_{A1} 1_{A2} 1_{A3} 1_{B0} 1_{B1} 1_{B2} 5_{B3}
YA5-A3
YB6-B3
74F1244 OR 74F244
$\overline{STATESEL}$
D_0-D_7
µp DATA BUS
74F86
74F00
4 of 8 SHOWN
+5
74F04
74F74
$\overline{R}$
D
Q
$\overline{Q}$
S
+
$\overline{INT}$
INTERRUPT LATCH
MASK REG
74F273
D_0-D_7
ENABLE 6
ENABLE 7
$\overline{MASK\ SEL}$
AF02981S

Figure 2. Interrupt Masking

During its interrupt service routine, the microprocessor reads the interrupt latch outputs via the74F1244 or 74F244 octal 3-State buffer to determine which event caused the interrupt. This scheme is most useful with microprocessors such as the 68000 family that do not have vectored interrupts.

At the end of the interrupt service routine, the microprocessor resets the latch by pulsing the /CLEARINT output line. This would typically be generated by decoding a write to a particular address.

INTERRUPT MASKING

Figure 2 shows an interrupt controller that allows each interrupt input to be individually enabled or disabled (masked). A 74F273 octal D flip-flop stores the state of the interrupt inputs whenever any input changes.

Exclusive-OR gates 74F86 compare the inputs of the state register to its outputs; whenever an input changes, the corresponding exclusive-OR gate output goes High.

Another 74F273, connected as an output port, serves as the mask register. The microprocessor writes a bit pattern to this port to determine which interrupts are enabled. The outputs of the exclusive-OR gates are then ANDed with the mask register outputs, so that interrupt inputs with a zero in their mask bit are ignored.

Whenever any unmasked input changes state, the state register is clocked, and the interrupt latch is set. The microprocessor reads the state register via the 74F1244 or 74F244 3-State buffer acting as an input port, and the interrupt latch is cleared.

Caution: This circuit can be fooled if an interrupt input changes twice before the microprocessor reads the state register. Therefore, this design should be used only for relatively slow-changing interrupt inputs.

INTERRUPT PRIORITIZING

In the previous circuits, the hardware does not select which interrupt has highest priority. If two or more interrupts are simultaneously asserted, the microprocessor software must decide which to process first.

Figure 3 shows a circuit with prioritization logic to select the highest priority interrupt. Interrupt inputs are sampled by the 74F377 octal flip-flop. This register is also used to freeze the state of the interrupt inputs when the output of the priority encoder is being read by the microprocessor. If one (or more) interrupt input is asserted, the output of the 74F148 priority encoder will indicate the number of the highest priority active interrupt.

The $\overline{GS}$ output of the encoder is effectively the OR of all the inputs, and produces the interrupt signal to the microprocessor. The microprocessor then reads the interrupt number via the 74F1244 or 74F244 3-State buffer connected as an input port. The microprocessor can use the interrupt number as an index pointer into a branch table, to access the appropriate service routine.

A 74F138 3-to-8 decoder decodes the interrupt number to generate individual reset signals for each interrupt source. The decoder is enabled when the microprocessor reads the interrupt number, so the interrupt output of the device being serviced is automatically reset.

RESTART VECTOR GENERATION FOR 8080 – FAMILY PROCESSORS

The 8080, 8085, NSC800, and Z80 all have interrupt modes in which a vector is automatically read from the interrupting device. (For the 8080, this is the only mode; the other processors also have additional modes.) This vector is treated as an instruction; the single-byte CALL instructions called RESTARTs are

Interrupt Control Logic Using FAST ICs AN208

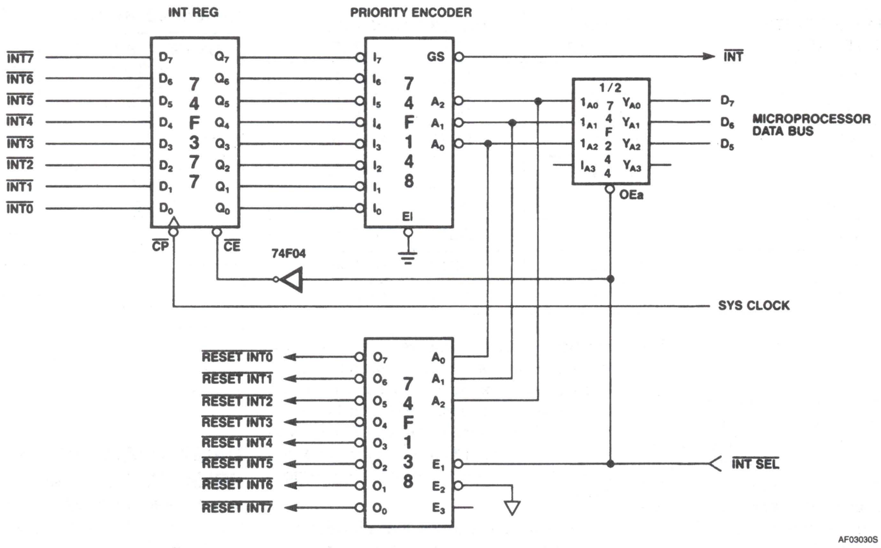
INT REG
PRIORITY ENCODER
74F377
74F148
1/2 74F244
74F138
74F04
INT7
INT6
INT5
INT4
INT3
INT2
INT1
INT0
CP
CE
GS
EI
OEa
INT
MICROPROCESSOR DATA BUS
SYS CLOCK
INT SEL
RESET INT0
RESET INT1
RESET INT2
RESET INT3
RESET INT4
RESET INT5
RESET INT6
RESET INT7
AF03030S

Figure 3. Interrupt Prioritizing

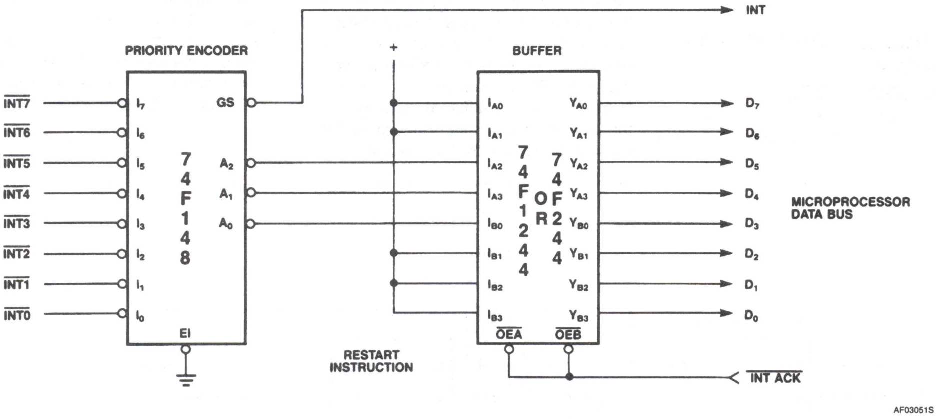
PRIORITY ENCODER
74F148
BUFFER
74F1244 OR 74F244
INT
INT7
INT6
INT5
INT4
INT3
INT2
INT1
INT0
GS
EI
+
RESTART INSTRUCTION
OEA
OEB
INT ACK
MICROPROCESSOR DATA BUS
AF03051S

Figure 4. Restart Vector Generation Circuit

generally used for the vectors. The format of the restart instructions is 11CBA111 (binary), where CBA represents the three-bit identifier. Figure 4 illustrates a restart vector generation circuit.

The 74F148 priority encoder generates the interrupt request to the microprocessor when any interrupt input is asserted. It also provides the three-bit identifier to the appropriate inputs of the 74F1244 or 74F244. When the microprocessor performs an interrupt acknowledge cycle, the restart instruction is read via the 74F244 octal buffer. Table 1 shows the vectors generated for each input. Interrupt input 7 produces an identification code of 000, since the priority encoder outputs are active-Low.

Note that the interrupt inputs are not latched by this circuit, and thus must remain asserted until the interrupt acknowledge cycle is completed.

The Z80 microprocessor has several modes of interrupt operation. The mode described above is called mode 1. Mode 2 is a table-driven mode in which the vector supplied by the peripheral is used as a pointer to a table. The service routine address is then read from the table.

Figure 5 shows a circuit for generating the vectors for Z80 mode 2 interrupts. The 74F148 priority encoder generates a three-bit binary number corresponding to the highest priority active interrupt. This number is read by the microprocessor during the interrupt

Interrupt Control Logic Using FAST ICs AN208

Table 1. 8080-Family Interrupt Vector Generation

HIGHEST PRIORITY ACTIVE INPUT	VECTOR GENERATED	INSTRUCTION NAME	
		8080	Z80
INT7	11000111	RST0	RST 0
INT6	11001111	RST1	RST 8
INT5	11010111	RST2	RST 16
INT4	11011111	RST3	RST 24
INT3	11100111	RST4	RST 32
INT2	11101111	RST5	RST 40
INT1	11110111	RST6	RST 48
INT0	11111111	RST7	RST 56

acknowledge cycle via the 74F244 octal 3-State driver.

Table 2 shows the vectors generated by the circuit. The least significant data input of the 74F1244 or 74F244 is grounded, and the code from the priority encoder provides the next three bits. This is necessary because each interrupt vector must point to a two-byte entry in the service routine address table. The four most significant bits are set by the switches. This allows the same circuit to be used in several places in a system by setting the switches differently on each.

VECTORED INTERRUPTS FOR 68000 – FAMILY MICROPROCESSORS

The 68000 microprocessor and its derivatives (68002 and 65002) do not have a built-in mechanism for handling vectored interrupts. When an interrupt occurs, the microprocessor fetches the address of the service routine from memory locations FFF8 and FFF9 (for the 65002, locations FFFE and FFFF). Normally these are ROM locations, and the interrupt service routine address is therefore fixed.

Figure 6 shows a circuit that provides vectored, prioritized interrupts for these microprocessors. When the microprocessor reads from address FFF8 or FFF9, this circuit disables the normal address buffers and substitutes a different address via a second set of 74F1244 or 74F244 octal 3-State drivers. Bits 1, 2 and 3 of the substituted address are determined by the highest priority active interrupt input. Thus, the service routine address is fetched from a different memory location for each interrupt input. The high-order address bits are set by the switches.

Table 2. Interrupt Vectors Generated By Circuit In Figure 5

HIGHEST PRIORITY ACTIVE INPUT	VECTOR GENERATED (HEX)
INT7	X 0
INT6	X 2
INT5	X 4
INT4	X 6
INT3	X 8
INT2	X A
INT1	X C
INT0	X E

NOTE:
1. X = Switch settings

DAISY CHAIN INTERRUPT PRIORITY SYSTEM

In the previous examples, a priority encoder was used to set the priority of each interrupt source. Another way to set priority is with an interrupt priority daisy chain, as shown in Figure 7. The priority of each device is determined by its physical location in the chain. Support for an interrupt daisy chain is built into the peripheral chips for some microprocessor families, such as the Z80. This example shows how a similar daisy chain can be implemented for other microprocessors such as the 8085 or 68000.

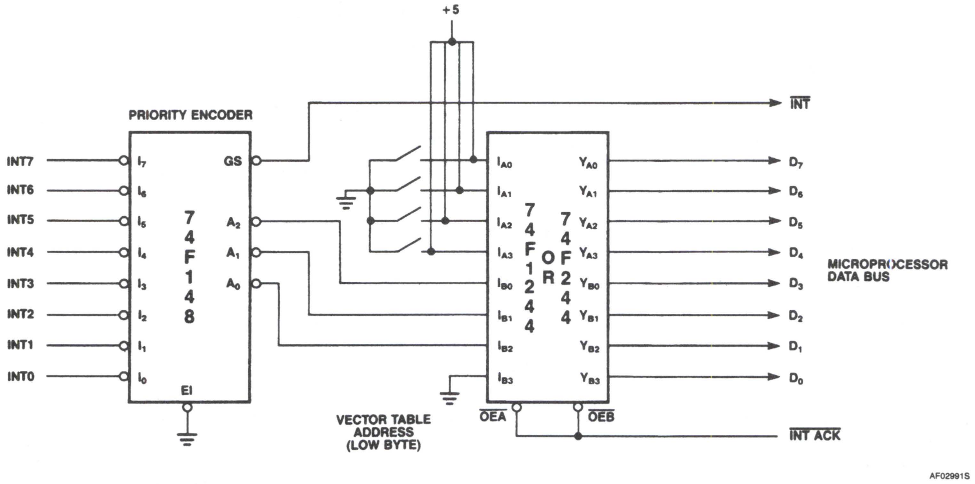

Figure 5. Vector Generation for Two Interrupt Modes

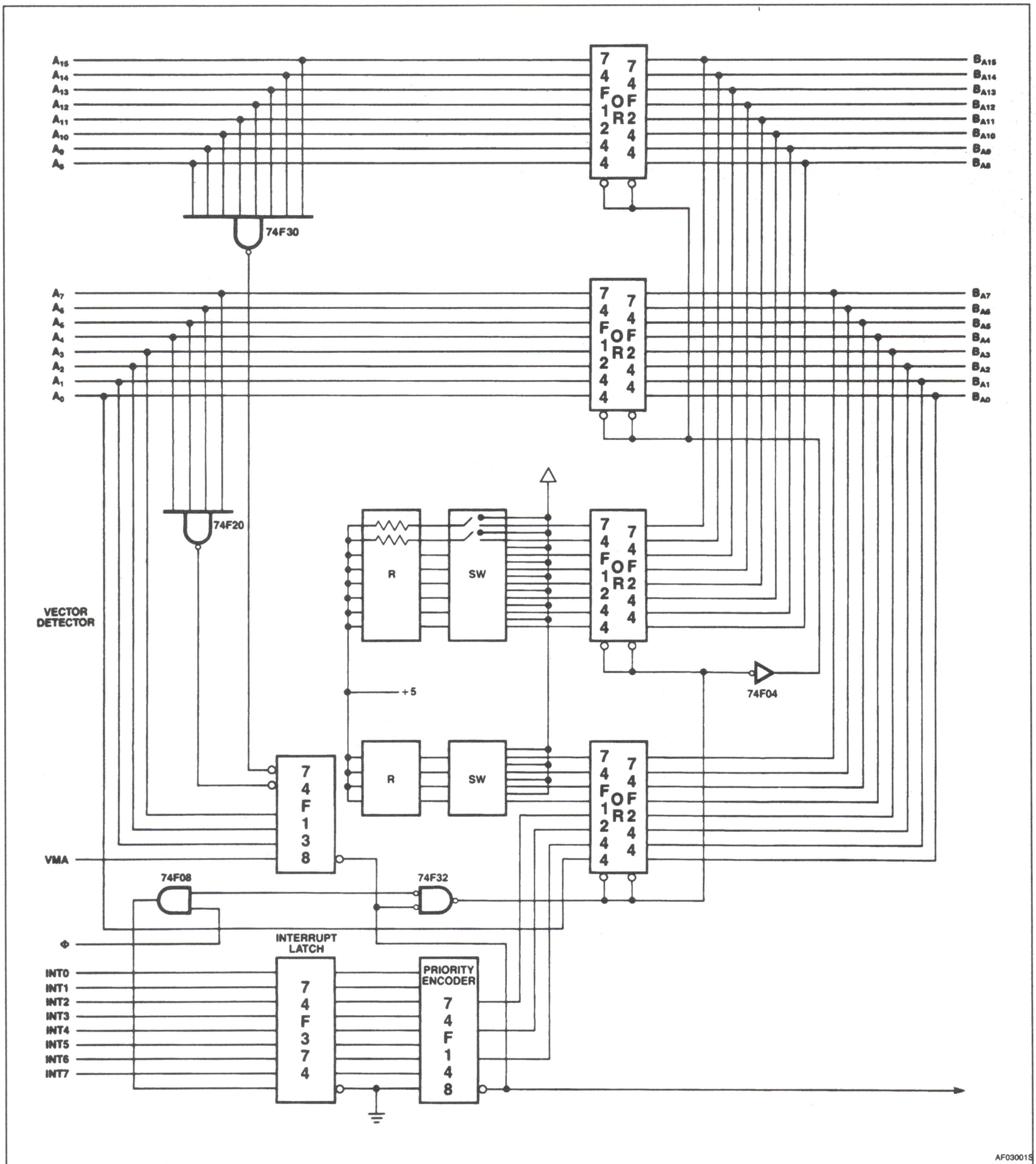
A15
A14
A13
A12
A11
A10
A9
A8
74F30
74F1244
74F2244
BA15
BA14
BA13
BA12
BA11
BA10
BA9
BA8
A7
A6
A5
A4
A3
A2
A1
A0
BA7
BA6
BA5
BA4
BA3
BA2
BA1
BA0
74F20
VECTOR DETECTOR
R
SW
+5
74F04
74F138
VMA
74F08
74F32
Φ
INTERRUPT LATCH
74F374
PRIORITY ENCODER
74F148
INT0
INT1
INT2
INT3
INT4
INT5
INT6
INT7
AF03001S

Figure 6. Prioritized Interrupt Vector Generator

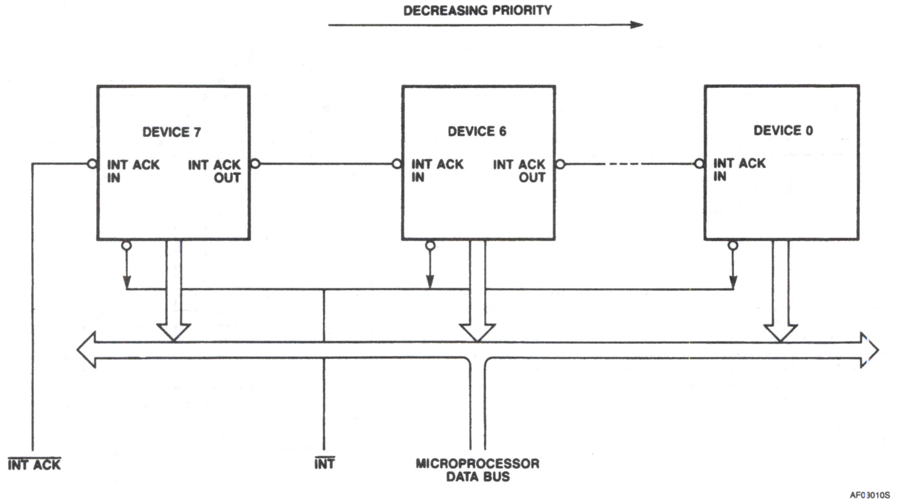
DECREASING PRIORITY
DEVICE 7
INT ACK IN
INT ACK OUT
DEVICE 6
INT ACK IN
INT ACK OUT
DEVICE 0
INT ACK IN
$\overline{\text{INT ACK}}$
$\overline{\text{INT}}$
MICROPROCESSOR DATA BUS
AF03010S

Figure 7. Daisy Chain Interrupt

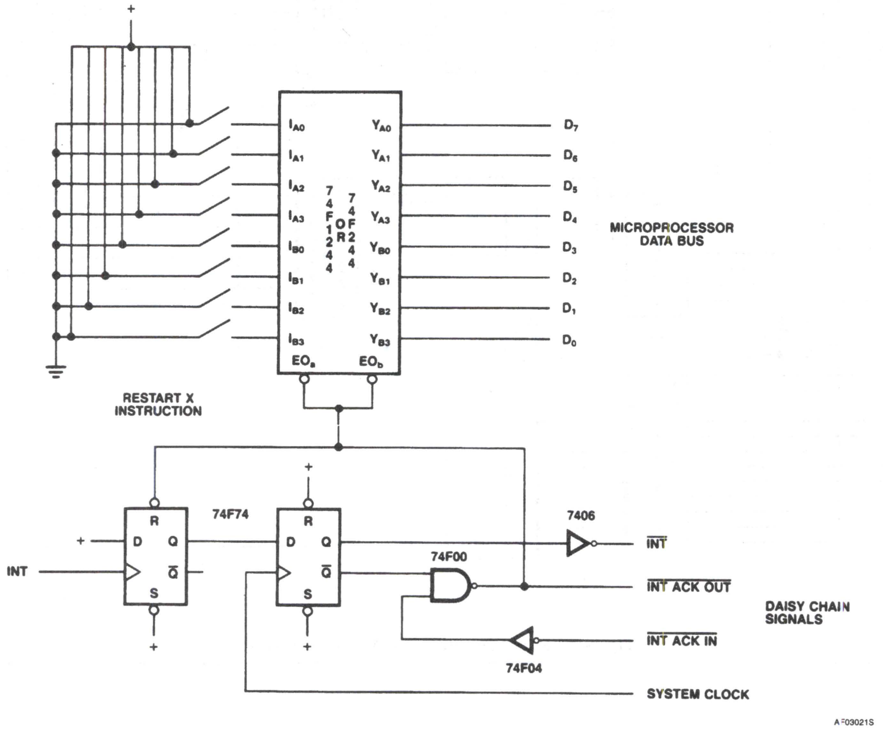
+
I_{A0}
I_{A1}
I_{A2}
I_{A3}
I_{B0}
I_{B1}
I_{B2}
I_{B3}
EO_a
EO_b
74F1244 OR 74F244
Y_{A0}
Y_{A1}
Y_{A2}
Y_{A3}
Y_{B0}
Y_{B1}
Y_{B2}
Y_{B3}
D_7
D_6
D_5
D_4
D_3
D_2
D_1
D_0
MICROPROCESSOR DATA BUS
RESTART X INSTRUCTION
74F74
R
D
Q
$\overline{Q}$
S
INT
7406
74F00
74F04
$\overline{\text{INT}}$
$\overline{\text{INT ACK OUT}}$
$\overline{\text{INT ACK IN}}$
DAISY CHAIN SIGNALS
SYSTEM CLOCK
AF03021S

Figure 8. Logic Circuit for Implementation of Daisy Chain Interrupt

Interrupt Control Logic Using FAST ICs

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When one or more device asserts an interrupt, the microprocessor responds by asserting $\overline{\text{INTACK}}$ active. This signal connects directly to the highest priority device's $\overline{\text{INTACK IN}}$ input. If that device had not asserted an interrupt, then it passes the interrupt acknowledge signal to the next device via its $\overline{\text{INTACK OUT}}$ signal. Thus, the interrupt acknowledge is passed along from one device to the next until it reaches the highest priority device that generated an interrupt. That device then places its interrupt vector on the data bus.

Figure 8 shows an implementation of this system. The two 74F74 flip-flops latch the interrupt request and synchronize it with the system clock. The signal at $\overline{\text{INTACK IN}}$ is passed to $\overline{\text{INTACK OUT}}$ unless the interrupt latch is set. The 74F244 drives the interrupt vector (restart instruction) to the data bus when $\overline{\text{INTACK IN}}$ is active and the interrupt latch is set. Switches allow the interrupt instruction to be selected for each device.

68000 INTERRUPT STRUCTURE

The 68000 16-bit microprocessor provides an extremely versatile interrupt structure. There are seven interrupt priority levels with up to 256 different vectors per level. The 68000 has a three-bit interrupt input which specifies the interrupt level. A code of 000 means no interrupt; any other code produces an interrupt, and the level corresponds to the code.

Figure 9 shows the timing diagram for the interrupt acknowledge cycle. When the 68000 recognizes the interrupt, it places the interrupt acknowledge code on the function code outputs $/FC_0 - /FC_2$, and outputs the interrupt level being serviced on address lines A_0, A_1 and A_2. The interrupting device then places the interrupt vector on the data bus from which it is read by the 68000.

Figure 10 shows a circuit that allows the user, under program control, to generate an interrupt of any priority level and to supply any interrupt vector. The program uses a MOVE instruction to output the desired interrupt level and vector. The circuit then generates the interrupt. This allows subroutines to be implemented as interrupt service routines. It is also useful for testing interrupt service routines.

All signals are VERSABUS™ signals, with the exception of INT ADDR* which is the output of the address decoder, and RD/$\overline{\text{WR}}$* which must be derived from the VERSABUS™ control signals. Note that the address and data buses are active low; VERSABUS™ notation is used (active low signal names are followed by an asterisk "*"). DS0* and DS1* are basically the same as the 68000's $\overline{\text{UDS}}$ and $\overline{\text{LDS}}$. IACKIN* and IACKOUT* are priority daisy chain signals as described previously. IPL1* through IPL7* are the seven interrupt signals which are fed through a priority encoder on the CPU board (not shown) to generate the binary-encoded interrupt signals to the 68000.

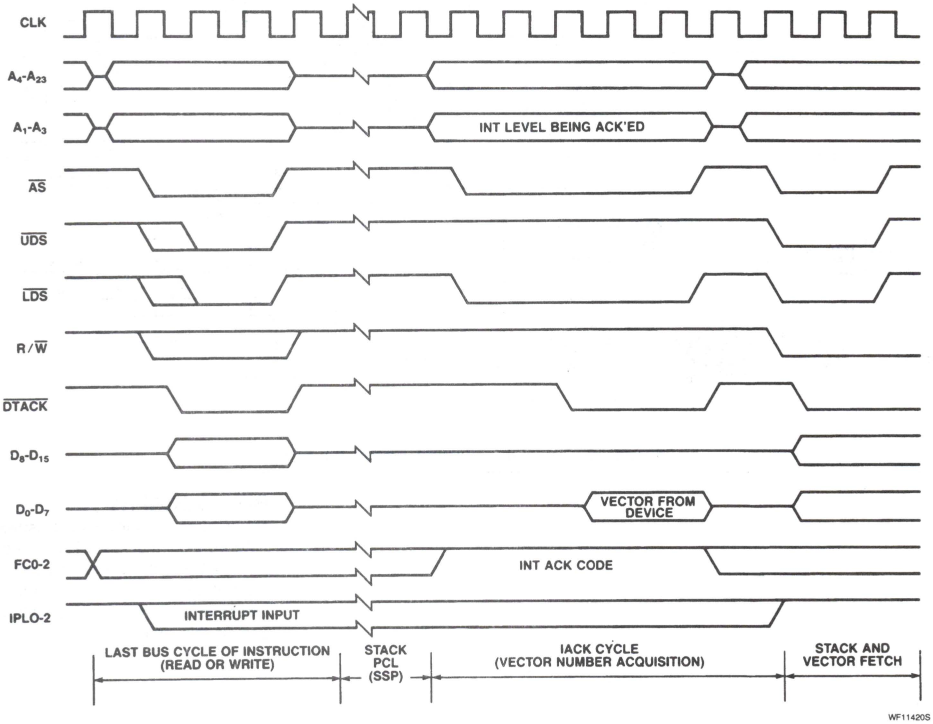

Figure 9. 68000 Interrupt Timing Diagram

Interrupt Control Logic Using FAST ICs

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The operation of the circuit is as follows:

- The software performs a move instruction to the address decoded as INTADDR*, with the interrupt vector in $D_0 - D_7$ and the interrupt level in D_8, D_9 and D_A.
- Flip-flop I is set, releasing the clear from the 74F175 priority register C. The new interrupt level is clocked into the register and an interrupt of that level is generated by the 74F138 decoder D.
- At the same time, the interrupt vector is loaded into the 74F373 latch L.
- After an appropriate delay 74F73A flip-flops P and Q generate XACK*, and the cycle completes.

When the 68000 recognizes the interrupt, the following sequence occurs:

- The priority level being serviced, as indicated by the state of A_0, A_1 and A_2, is compared to the contents of the interrupt priority latch C by the 74F85 comparator B. (Note that the $\overline{Q}$ outputs of the 74F175 are used to invert the active low address signals.)
- If the levels match, the interrupt vector is placed on the data bus, XACK* is generated, and the cycle terminates. Flip-flop I is reset, which removes the interrupt by clearing the interrupt request register.

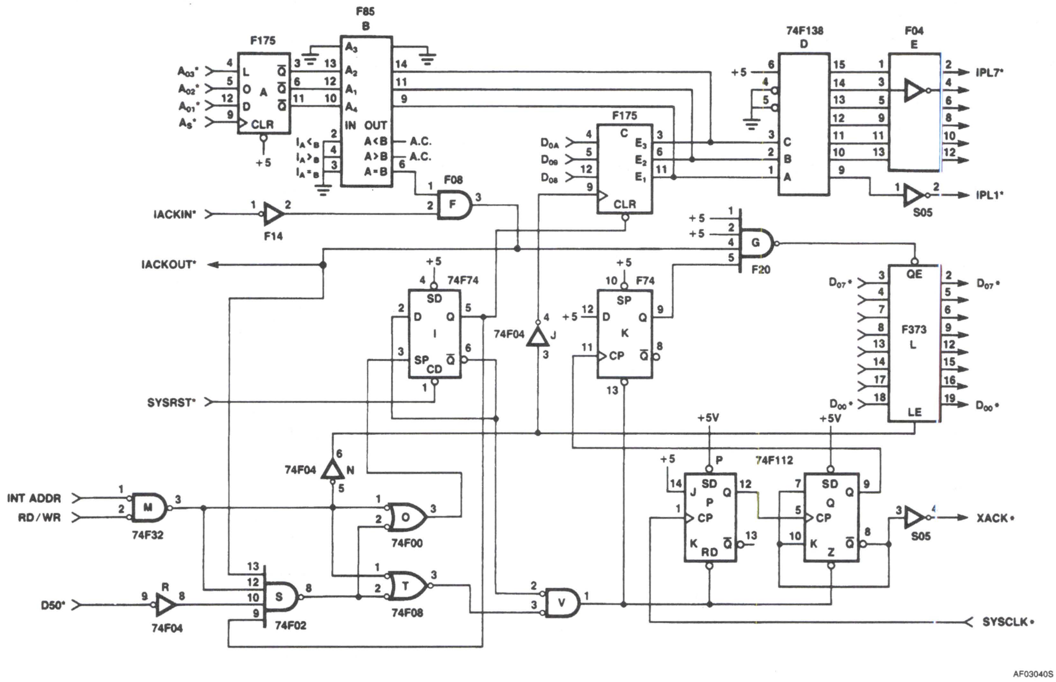
F85
B
F175
A03*
A02*
A01*
As*
L
D
A
CLR
+5
A3
A2
A1
A4
IN OUT
IA<B
IA>B
IA=B
A<B
A>B
A=B
A.C.
A.C.
F08
F
IACKIN*
F14
IACKOUT*
74F74
SD
D Q
I
SP CD Q̄
SYSRST*
F175
C
D0A
D09
D08
E3
E2
E1
CLR
74F04
J
F74
SP
D Q
K
CP Q̄
74F138
D
C
B
A
F04
E
IPL7*
IPL1*
S05
G
F20
D07*
D00*
QE
F373
L
LE
+5V
74F112
SD
J Q
P
CP
K RD Q̄
SD
Q
CP
K Z Q̄
XACK*
S05
SYSCLK*
74F04
N
INT ADDR
RD/WR
M
74F32
O
74F00
T
74F08
D50*
R
74F04
S
74F02
V
AF03040S

Figure 10. Complete Interrupt Circuit for 68000

BIBLIOGRAPHY

Many of the applications illustrated in this note were contributed or influenced by entries in Signetics' Interface Circuit design contest. Special thanks are due to the individuals whose entries were referenced in whole or in part in this note.

Signetics

FAST Products

AN212

Package Lead Inductance Considerations In High-Speed Applications

Application Note

Authors: Stephen C. Hinkle,
Jeffrey A. West

INTRODUCTION

As circuits become faster, more concern needs to be focused on packaging and interconnects in order to fully utilize device performance. One area of concern is with the package leads between the chip and the board environment. The current flowing into or out of an integrated circuit is conducted through a lead frame trace and bonding wire connecting the integrated circuit to outside circuitry. These leads are circuit elements, inductors, and have a definite effect on the circuit performance because they generate noise in High-speed applications.

Inductance is the measure of change in the magnetic field surrounding a conductor resulting from the variation of the current flowing through the conductor. The change in current through the inductor induces a counter electromotive force, EMF, which opposes that change in current.

An example is a buffer driver discharging a 50pF load. At a switching rate of about 3V in 2ns, the current generated by discharging that capacitor at that rate is:

$$I = C\frac{dV}{dt} \simeq 50pF * \frac{3v}{2ns} = 75mA.$$

All this current flows through the ground lead of the package. Changing the current through this lead generates a ground lead voltage or ground bounce. A typical lead inductance has been measured to be about 10nH. Switching 75mA through a ground lead with an inductive value of 10nH causes a ground bounce of about:

$$V = L\frac{dI}{dt} \simeq 10nH * \frac{75mA}{1ns} = 750mV.$$

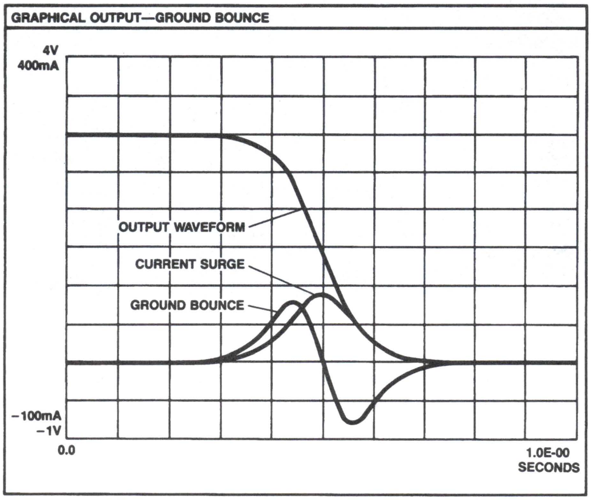

Figure 1

Figure 1 illustrates the current surge and ground bounce during switching. This was modeled using the equations:

$$V(t) = \frac{3V}{1 + e^{(t-to)/K}}$$

$$I_C(t) = C\frac{dV(t)}{dt}$$

$$V_L(t) = L\frac{dI_C(t)}{dt} = LC\frac{d^2V(t)}{dt^2}$$

If more than one output is switched at a time this ground bounce can get very large. Changing the ground reference on the chip can have significant effects on circuit performance. A V_{CC} bounce can also be calculated when the 50pF load capacitors are being charged and can also have serious effects on circuit performance.

Some of the problems caused by package lead inductance are:

1. Adding delay through buffer parts
2. Changing the state of flip-flop parts
3. Output glitching on unswitched outputs
4. Circuit oscillations

GENERAL PROBLEMS ASSOCIATED WITH GROUND BOUNCE IN High-SPEED CIRCUITS

Adding Delay Through Buffer Parts

Delay through a buffer part is not only a function of the gate itself but is also a function of how many gates in the package are switching at once. Switching more than one output at a time adds to the current being forced through the ground lead of the package. The ground potential seen by the chip rises because of the lead inductance. This rise in ground potential raises the threshold of the gate and tends to turn the gate back OFF slowing the discharge rate of the load capacitor. The gate doesn't finish switching until the ground bounce settles out.

Package Lead Inductance Considerations In High-Speed Applications

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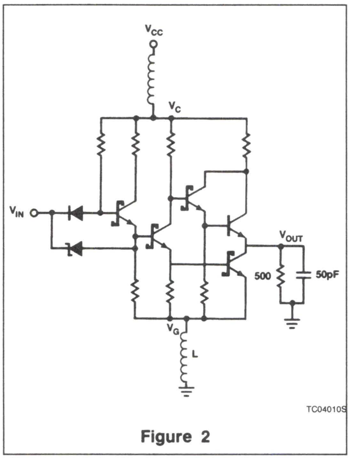

Figure 2

Figure 2 shows an example of a buffer connected to a test load. Probing on the ground pad, V_G, shows the effect ground lead inductance has on the ground pad potential.

Figures 3 and 4 show the ground and V_{CC} bounce during switching on an 'F240 Buffer. The effect of ground bounce on this part is to slow the propagation delays from 3ns with only one output switching to 5ns with all 8 outputs switching at once. AC specifications are usually generated with only one gate switching at a time. For example the 'F240 T_{PHL} limits are 2.0ns minimum, 3.5ns typical and 4.7ns maximum. Therefore when using AC specifications based on single gate switching, a derating factor for multiple switching should be used. A derating factor of 250 to 300ps per output switching has been suggested as a reasonable number and some customers are using this in their internal specifications.

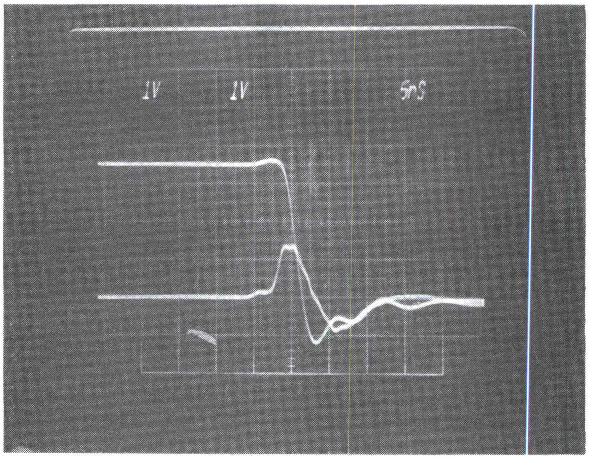

Figure 3

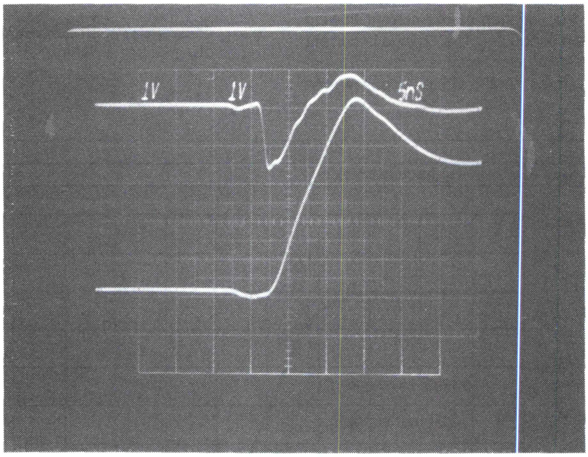

Figure 4

Integrated Circuits Containing Flip-Flops

Integrated circuits containing flip-flops might be seriously affected by inductive ground bounce because of the possibility of the flip-flops changing states. To explore this effect, the 'F374, an Octal D-type flip-flop, was analyzed by comparing test results from the conventional corner mount V_{CC} and ground package to that of a side mount V_{CC} and ground version. A test setup was used where alternate 1's and 0's were clocked into seven of the eight flip-flops to obtain simultaneous output switching and worst case ground bounce. The eighth flip-flop input was held at a DC bias of 2.0V. This should result in its output being held at a constant 1 level.

Package Lead Inductance Considerations In High-Speed Applications

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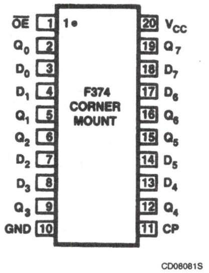


74F374 Failure Analysis

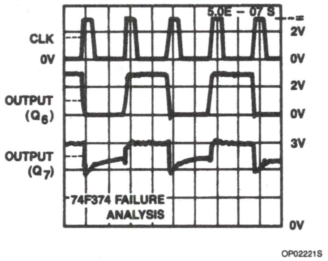
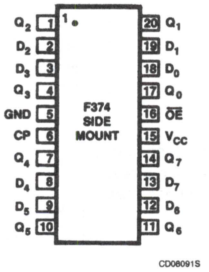


Figure 5



74F374XL

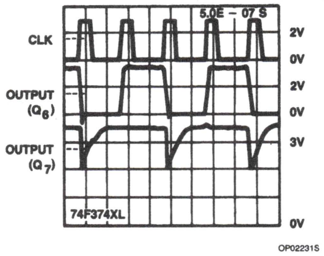


Figure 6

Figure 5 shows the corner mount results. The ground bounce is sufficient to couple the output of the eighth flip-flop (Q_7) to less than 2.0V during the transition of the other seven outputs represented by Q_6. The output then charges to a marginal V_{OH} level.

Figure 6 shows the results from the side mount version. Output glitching during the transition of the other seven outputs is still present, but due to the approximately 50% reduction in lead inductance over the corner mount version, the output is allowed to charge back to its original V_{OH} level.

Output Glitching During Multiple Switching

In some cases the effects of ground bounce can be minimized if properly taken into consideration during the design and layout of the integrated circuit. Note in Figure 7, the glitch that was present on the output of the 'F11, a triple 3-input AND gate, during an early transition of the other two outputs. A newer version of the 'F11 is shown in Figure 8. Note that the glitch has been greatly minimized.

Circuit Oscillations

A fourth area of concern is the possibility of circuit oscillations during slow input transitions through threshold. This would be of importance if the delay through the part is on the order of the natural period of oscillations of the ground inductance and the load capacitance.

During testing, a particular problem has been seen when the inputs are driven by a power supply by way of a cable. Because there is a delay through the cable, it takes time for the power supply to sense a change in the impedance at the input near threshold. This delay sets up oscillations between the power supply and the input of the part when the input is held near threshold.

Inductance Measurements And Verification

To verify that lead inductance caused these problems, the lead inductance was measured and circuit simulations done to show circuit behavior. Measurement of lead inductance was accomplished using an HP S-parameter test set. These measured values of lead inductance were used in a circuit simulation program. The results of the simulation show voltage and current wave forms similar to the measured waveforms.

Package Lead Inductance Considerations In High-Speed Applications

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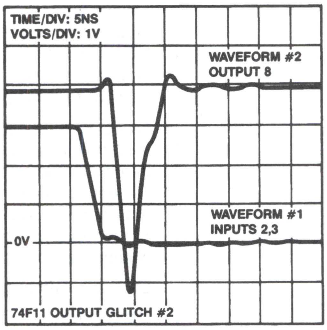

Figure 7

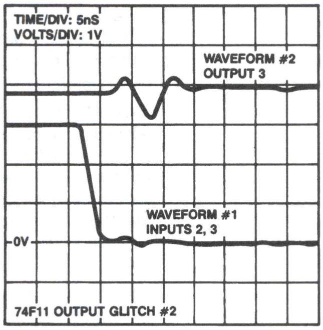

Figure 8

Derivation of the S-parameter Method

The general form for voltage and current along a transmission line is:

$$\bar{V}(z) = V^+e^{-\gamma z} + V^-e^{\gamma z}$$
$$\bar{I}(z) = I^+e^{-\gamma z} - I^-e!s$$

Where V^+, V^-, I^+, I^- are constants, usually complex, determined by the boundary conditions, z is the distance from the load and gamma (γ) is a complex term involving a real or loss term and an imaginary or phase shift term.

$$\gamma = \alpha + j\beta$$
$$\gamma \simeq 1/2(R\sqrt{C/L} + G\sqrt{L/C}) + j\omega\sqrt{LC}.$$

Considering the lossless case where $R = 0$ and $G = 0$, $\gamma = j\beta$ and only results in a phase shift. The equations for voltage and current then become:

$$\bar{V}(z) = V^+e^{-j\beta z} + V^-e^{j\beta z}$$
$$\bar{I}(z) = I^+e^{-j\beta z} - I^-e^{j\beta z}$$

To find Z_1 set $z = 0$. (See Figure 9).

$$\bar{Z}_1 = \bar{V}_1/\bar{I}_1 = (V^+ + V^-)/(I^+ - I^-)$$

since, $I^+ = V^+/Z_0$ and,

$$I^- = V^-/Z_0,$$
$$\bar{Z}_1 = (V^+ + V^-)/(V^-/Z_0 - V^+/Z_0), \text{ or,}$$
$$\bar{Z}_1 = Z_0 \frac{1 + V^-/V^+}{1 - V^-/V^+}$$

V^-/V^+ is called the reflection coefficient and is usually complex,

$$\Gamma = V^-/V^+.$$

The impedance at the load then becomes:

$$\bar{Z}_1 = Z_0 \frac{1 + \Gamma}{1 - \Gamma}$$

On the S-parameter test set, the magnitude of the reflection coefficient, $|\Gamma|$, is measured in dB at a particular angle,

$$\Gamma_{real} = 10^{(|\Gamma_{dB}|/20)} \angle \theta.$$

For an inductor,

$$\bar{Z}_1 = Z_0 \frac{1 + \Gamma}{1 - \Gamma} = R + j\omega L ,$$

usually $R \simeq 0$ and L can be solved for directly.

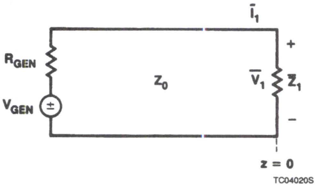

Figure 9

Package Lead Inductance Considerations In High-Speed Applications

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Table 1

PACKAGE	REFLECTION COEFFICIENT	INDUCTANCE
16-pin (300mil-wide)		
8 to 16	−0.50 ∠ 162°C	25.62nH
4 to 12	−0.32 ∠ 172°C	11.51nH
24-pin (600mil-wide)		
12 to 24	−0.56 ∠ 157°C	32.78nH
6 to 18	−0.29 ∠ 157°C	18.33nH
24-pin (300mil-wide)		
12 to 24	−0.47 ∠ 160°C	28.39nH
6 to 18	−0.34 ∠ 170°C	14.27nH

Example

A 16-pin package measuring from pin 8 to 16 has a reflection coefficient $\Gamma_{dB} = -0.5 \angle 162°$, Z_0 of the system is 50Ω and the measurement frequency is 50MHz.

$$\Gamma_{dB} = -0.5 \angle 162°$$

$$\Gamma_{real} = 0.944 \angle 162° = -0.898 + j0.292$$

$$\overline{Z}_1 = Z_0 \frac{1+\Gamma}{1-\Gamma} = 50*\frac{0.102+j0.292}{1.898-j0.292}$$

$$= 50*\frac{0.309 \angle 70.7°}{1.920 \angle -8.74°}$$

$$= 8.05 \angle 79°$$

$$\overline{Z}_1 = 1.475+j7.914$$

$$L = 7.914/(2\pi*50\text{MHz}) = \underline{25.19\text{nH}}.$$

Alternately, using the approximation R = 0, so $|Z_1| = \omega L$:

$$L = \frac{8.05}{2\pi*50\text{MHz}} = \underline{25.62\text{nH}}$$

Three packages were used to measure lead inductance, a 16-pin CERDIP, a 24-pin CERDIP and a 24-pin skinny CERDIP. V_{CC} and ground were double bonded to an 80 × 80 mil blank die. Table 1 shows the results of the measurements.

These values are the total inductance V_{CC} to ground. Each lead inductance would be about one half these members.

Simulation of Measured Values

Both ground and V_{CC} bounce for the 'F240 were simulated using the inductive values measured. The results were similar to the measured data of the 'F240, Figures 3 and 4. The simulation of the 'F240 is shown in Figure 10. This shows the pad V_{CC}, the pad ground (V_G) and the inputs (V_{IN}) and outputs (V_{OUT}) when all 8 buffers are switched simultaneously.

SUMMARY

A major contributor to noise in High-speed circuits is package lead inductance. Integrated circuits are packaged with lead frame traces and bonding wire. These leads act as inductors. Voltage generated across these leads follow the law:

$$V = L\frac{di}{dt}$$

This represents noise to an integrated circuit chip and can cause performance degradation. The faster the switching rates become, the more lead inductance can affect circuit performance.

As circuits become faster, more care should be taken in packaging and chip layout. In some cases like the 'F11, a better layout can help remove potential problems but in most cases like the 'F240, the noise is strictly a function of the package. Care should be taken in integrated circuit packages to minimize lead lengths. Side mount V_{CC} and ground pins, smaller packages such as the surface mounted SO, and High levels of board integration are a few possibilities which would help minimize lead lengths.

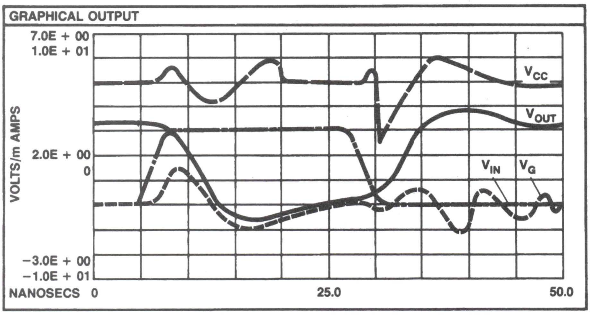


Figure 10

Section 8
Surface Mounted ICs

Surface Mounted ICs

INTRODUCTION

Economic survival is driving the electronics industry to use cheaper, faster, more reliable and more dense systems and components. Assembly technologies, such as SMD (Surface Mounted Device) technology, developed and used in hybrids and for military electronics for over two decades, is being adapted to commercial electronics as part of this evolution. With SMD technology, components are soldered directly to a metalized footprint on the surface of the board or substrate rather than being inserted through holes drilled in the board and then soldered. Because of this evolution, package styles specially designed to facilitate surface mounting are now in high demand.

The reasons for the change to SMD technology vary from one customer to another; but the primary motivator is higher profits through lower manufacturing and material costs, or an improved product, or both.

Improved Electrical Performance

Because SMD packages are much smaller than their DIP counterparts, they have much less capacitance and inductance, and provide improved AC performance, especially in high-speed environments. They help to minimize problems associated with ground bounce and multiple output switching found with standard DIP packages. The SO package is especially suitable for high-speed families such as FAST and High-Speed CMOS where package inductance can induce or compound problems not normally found in slower technologies.

Ease Of Automation

SMD pick-and-place machines offer higher yields, faster cycle rates (3 – 10x faster), and much higher throughput volumes than automatic insertion machines for DIP packages.

Greatly Increased Densities

Greatly increased densities can be achieved through surface mounting. The packages themselves are much smaller (as much as 70%) and can be placed much closer together. Furthermore, both sides of the board can be used with SMDs.

Reduced Board Costs

The number of layers, total size of the board, and the number of plated through holes can be reduced, thus lowering the total cost of the board (many companies claim savings of 30 to 50%).

Easier Board Rework

In those instances where rework is necessary, it is much faster and cheaper with SMDs.

Improved Reliability

Not only are the components proving to be at least as reliable as their DIP counterparts but, surface mounted assemblies show fewer failures in stress tests than equivalent through hole assemblies.

Lower Shipping, Storage And Handling Costs

SMD components are up to 70% smaller and weigh up to 90% less than DIPs (up to 95% savings in storage area for Tape & Reel SMD components vs DIPs and up to 90% savings in component weight). Surface mount assemblies offer additional savings in both weight and space, both of which can be linked to increased profits.

SMD packages for integrated circuits fall into two categories: Swiss Outline, also known as Small Outline (SO), and the Plastic Leaded Chip Carrier (PLCC).

SO PACKAGE

The SO package was developed by N.V. Philips Corp, originally for the Swiss watch industry. In the mid 1970s Signetics introduced linear ICs in SO packages to the US market (hybrid and telecommunications). As demand grew, other technologies such as FAST, Low Power Schottky, Schottky, TTL, CMOS, High-Speed CMOS (HC and HCT), ECL, ROMs, RAMs, PROMs, were made available in SO packages.

The SO is a dual-in-line plastic package with leads spaced 0.050″ apart and bent down and out in a Gull-Wing format. It comes in two widths: 0.150″ SO, and 0.300″ SOL (SO-Large) depending on the pin count.

As ICs became more complex and the number of pins grew, the standard dual-in-line packages grew longer and wider, presenting new electrical and mechanical problems. Some of these were resolved with the introduction of the ceramic leadless chip carrier (LCC). These were square, ceramic packages without leads which can be socketed or soldered directly to a substrate if the thermal coefficient of expansion of the chip carrier and the substrate are to be matched.

In 1980, the Plastic Leaded Chip Carrier (PLCC) was introduced as a cheaper alternative to the LCC. However, this was at the same time that SMD was winning acceptance in commercial electronics and the PLCC was seen as an ideal SMD package for the higher pin count devices (those with more than 28 leads). The PLCC is a square, plastic package with leads on four sides, spaced down and under in a J-Bend configuration. It is available in the higher pin counts: 20, 28, 44, 52, 68, 84 with even higher pin counts under development.

The smallest square PLCC is the 20 pin package. There are many reasons for this; the primary one is that below 20 pins, the package would be as thick as it is square,

Table 1

PIN COUNT	SO	SOL	PLCC
8	x		
14	x		
16	x	x	
18		x	x (rectangular)
20		x	x
24		x	
28		x	x
44			x
52			x
68			x
84			x

Surface Mounted ICs

resulting in a cube-like package which would be very difficult to handle in an automated environment.

Logic and linear devices are available in SO while the more complex parts such as microprocessors, microcontrollers, complex peripherals, large memory devices, and other higher pin count integrated circuits will be found in the PLCC.

ASSEMBLY

The assembly of these SMD packages is virtually the same as for the older DIP packages using the same materials and most of the same equipment and assembly technologies.

The only differences in the process are the smaller lead frames, different lead bends (gull-wing for SO and J-Bend for the PLCC), and closer spacing resulting in a much smaller package for the same basic die.

RELIABILITY

Reliability studies of SMD components, conducted not only by Signetics and Philips, but by many of our competitors and customers, have revealed that these packages are at least as reliable as the standard plastic DIP packages that have been used over the past 20 years. In several cases, test results of the SMD packages have been better than their DIP counterparts.

STANDARDIZATION

The SO package is an industry standard format. In June 1985, the JEDEC (Joint Electronics Engineering Council) of the EIA (Electronics Industries Association) issued a Solid State Product Outlines Standard for each of the SO formats: MS-012 AA-AC for the 0.150″ body width SO and Ms-013 AA-AE for the 0.300″ body width SOL. In addition to the JEDEC Standard, de facto standardization has been achieved in the industry in that most of the major US and European IC manufacturers (more than 15 companies currently) use this standard.

The PLCC is also a standardized format, with a JEDEC Registered Outline #MO-047 AA-AH. It also is multiple sourced with over 10 US IC manufacturers using this standard.

Points worth noting: All SO And SOL packages have 0.050″ lead spacing and a Gull-Wing lead bend, while all PLCC packages have the same lead spacing and a J-Bend lead bend.

TAPE AND REEL

One revolutionary phenomenon in SMD is the development of Tape and Reel for the IC packages. Philips and several other companies making automatic placement equipment recognized the need for a feed system which allows for positive indexing large volumes of components at high-speed in order to get maximum efficiency out of the new pick-and-place machines. Tubes are limited to a relatively small number of parts (dictated by tube length) and depend on gravity to feed components to the placement head. After several proposed tape formats, Philips, Signetics, many of the component and placement equipment manufacturers, and board manufacturers convened under the auspices of EIA (Electronic Industries Association) and agreed on an industry standard specification for Tape and Reel for both SO and PLCC packages. The proposed EIA specification RS 481A is being used by Signetics and Philips, both of whom have shipped components on Tape and Reel since late 1984.

Surface Mounted ICs

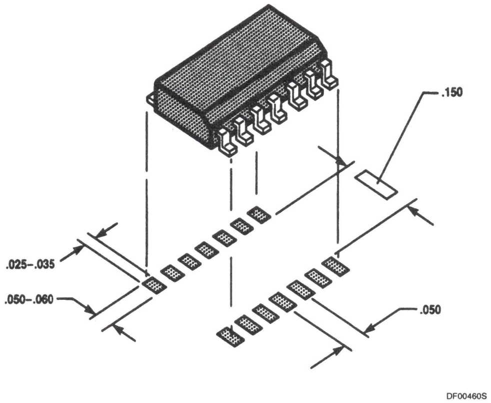
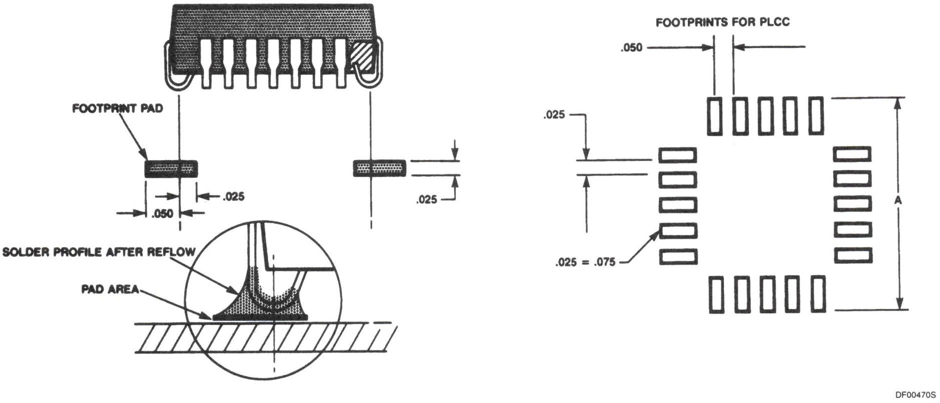

.150
.025–.035
.050–.060
.050
DF00460S

Figure 1. Manufacturers' Recommended Footprint


FOOTPRINT PAD
.025
.050
.025
SOLDER PROFILE AFTER REFLOW
PAD AREA
FOOTPRINTS FOR PLCC
.050
.025
.025 = .075
A
DF00470S

PINS	A
20	.425
28	.525
44	.725
52	.825
68	1.025

Figure 2. Footprint Design for The PLCC-IC

Signetics

FAST Products

Section 9
Package Outlines

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F Hermetic CERDIP 9-16

Signetics

Package Outlines

FAST Products

PACKAGE OUTLINES FOR PLASTIC PACKAGES

The following information applies to all plastic packages unless otherwise specified on individual package outline drawings.

1. Dimensions are shown in Metric units (Millimeters) and English units (Inches).
2. Lead material: Copper Alloy, solder (63%Sn/37%Pb) dipped.
3. Body material: Plastic (Epoxy)
4. Thermal resistance values are determined by temperature sensitive parameter (TSP) method. This method uses the forward voltage drop of a calibrated diode to measure the change in junction temperature due to a known power application. The substrate diode of a Bipolar technology device is generally the diode used in these tests. Die size and test environment have significant effects on thermal resistance values.

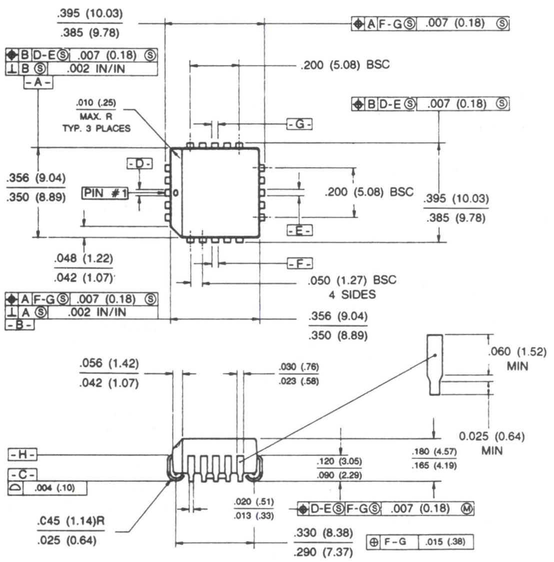
PLASTIC PACKAGES OUTLINES

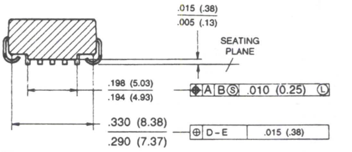
Package Type	Number of Leads	Package Feature	Package Ordering Code	Package Outline Code	Thermal Resistance θ_{JA}/θ_{JC} (°C/W)	Die Size (square mils)	Test Conditions	
							Test Ambient	Test Fixture
SO[1] (Copper Leadframe)	14 pin (SO-14)	3.9mm (0.15″) Body width	D	DH1	124/37	2,500	Still air at room temperature	Device soldered to Philips glass epoxy test board (1.12″ × 0.75″ × 0.059″) with 0.008 – 0.009″ stand-off. Accuracy: ± 15%
	16 pin (SO-16)		D	DJ1	113/36			
	16 pin (SOL-16)	7.5mm (0.30″) Body width	D	DJ2	98/30	5,000		Device soldered to Philips glass epoxy test board (1.58″ × 0.75″ × 0.059″) with 0.008 – 0.009″ stand-off. Accuracy: ± 15%
	20 pin (SOL-20)		D	DL2	90/28			
	24 pin (SOL-24)		D	DN2	76/26			
	28 pin (SOL-28)		D	DQ2	70/24	10,000		
PLCC[2] (Copper Leadframe)	44 pin (PLCC-44)	0.650″ Square body	A	AX1	50/20	15,000	Still air at room temperature	Device soldered to Philips glass epoxy test board (2.24″ × 2.24″ × 0.062″) with 0.008 – 0.009″ stand-off. Accuracy: ± 15%
DIP[3] (Copper Leadframe)	14 pin (DIP-14)	0.300″ Lead row centers	N	NH1	89/44	2,500	Still air at room temperature	Device in Textool ZIF socket with 0.040″, stand-off. Accuracy: ± 15%
	16 pin (DIP-16)		N	NJ1	86/43			
	20 pin (DIP-20)		N	NL1	74/32	5,000		Device in Textool ZIF socket with 0.040″, stand-off. Accuracy: ± 15%
	24 pin SLIM DIP (DIP-24)		N	NN1	65/36			
	24 pin (DIP-24)	0.600″ Lead row centers	N	NN3	59/30			
	28 pin (DIP-28)		N	NQ3	52/27	10,000		
	40 pin (DIP-40)		N	NW3	45/19	15,000		

NOTES:
1. SO = **S**mall **O**utline
2. PLCC = **P**lastic **L**eaded **C**hip **C**arrier
3. DIP = **D**ual-**I**n-Line **P**ackage

Package Outlines

AL1 PLASTIC PLCC-20


.395 (10.03)
.385 (9.78)
B D-E Ⓢ .007 (0.18) Ⓢ
⊥ B Ⓢ .002 IN/IN
-A-
.010 (.25) MAX. R TYP. 3 PLACES
A F-G Ⓢ .007 (0.18) Ⓢ
.200 (5.08) BSC
B D-E Ⓢ .007 (0.18) Ⓢ
-G-
-D-
.356 (9.04)
.350 (8.89)
PIN #1
.200 (5.08) BSC
.395 (10.03)
.385 (9.78)
-E-
.048 (1.22)
.042 (1.07)
-F-
.050 (1.27) BSC 4 SIDES
A F-G Ⓢ .007 (0.18) Ⓢ
⊥ A Ⓢ .002 IN/IN
-B-
.356 (9.04)
.350 (8.89)
.060 (1.52) MIN
.056 (1.42)
.042 (1.07)
.030 (.76)
.023 (.58)
0.025 (0.64) MIN
-H-
-C-
.004 (.10)
.120 (3.05)
.090 (2.29)
.180 (4.57)
.165 (4.19)
.045 (1.14)R
.025 (0.64)
.020 (.51)
.013 (.33)
D-E Ⓢ F-G Ⓢ .007 (0.18) Ⓜ
.330 (8.38)
.290 (7.37)
⊕ F-G .015 (.38)

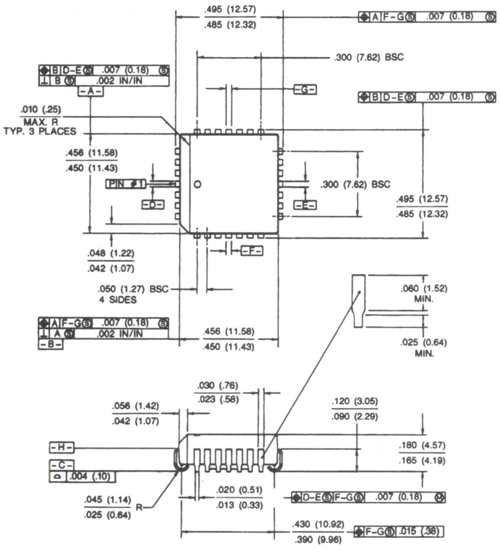

.015 (.38)
.005 (.13)
SEATING PLANE
.198 (5.03)
.194 (4.93)
A B Ⓢ .010 (0.25) Ⓛ
.330 (8.38)
.290 (7.37)
⊕ D-E .015 (.38)

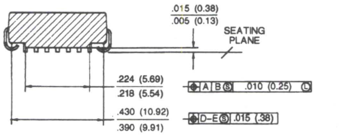
NOTES:

1. Package dimensions conform to JEDEC specification MO-047-AA for plastic leaded chip carrier 20 leads, .050 inch lead spacing, square. (issue A, 10/31/84).
2. Controlling dimensions: inches. Metric are shown in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M-1982.
4. "A" and "B" are reference datums on the molded body at plane "H" and do not include mold flash. Mold flash protrusion shall not exceed .006" (.15mm) on any side.
5. Datum "D-E" and "F-G" are determined where these center leads exit from the body at plane "H".
6. Pin numbers continue counterclockwise to pin #20 (top view).
7. Signetics order code for product packaged in a PLCC is the suffix A after the product number.

PO00631S

AQ1 PLASTIC PLCC-28


.495 (12.57)
.485 (12.32)
A F-G Ⓢ .007 (0.18) Ⓢ
.300 (7.62) BSC
B D-E Ⓢ .007 (0.18) Ⓢ
⊥ B Ⓢ .002 IN/IN
-A-
-G-
B D-E Ⓢ .007 (0.18) Ⓢ
.010 (.25) MAX. R TYP. 3 PLACES
.456 (11.58)
.450 (11.43)
PIN #1
.300 (7.62) BSC
-D-
-E-
.495 (12.57)
.485 (12.32)
.048 (1.22)
.042 (1.07)
-F-
.050 (1.27) BSC 4 SIDES
.060 (1.52) MIN.
A F-G Ⓢ .007 (0.18) Ⓢ
⊥ A Ⓢ .002 IN/IN
-B-
.456 (11.58)
.450 (11.43)
.025 (0.64) MIN.
.030 (.76)
.023 (.58)
.056 (1.42)
.042 (1.07)
.120 (3.05)
.090 (2.29)
-H-
.180 (4.57)
.165 (4.19)
-C-
.004 (.10)
.045 (1.14)
.025 (0.64)
R
.020 (0.51)
.013 (0.33)
D-E Ⓢ F-G Ⓢ .007 (0.18) Ⓜ
.430 (10.92)
.390 (9.96)
F-G Ⓢ .015 (.38)


.015 (0.38)
.005 (0.13)
SEATING PLANE
.224 (5.69)
.218 (5.54)
A B Ⓢ .010 (0.25) Ⓛ
.430 (10.92)
.390 (9.91)
D-E Ⓢ .015 (.38)

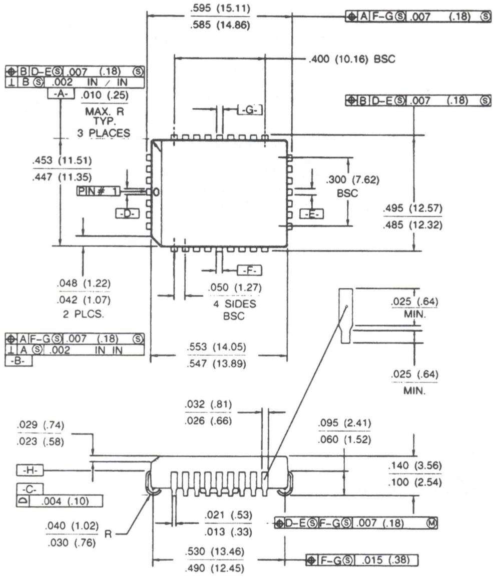
NOTES:

1. Package dimensions conform to JEDEC specification MO-047-AB for plastic leaded chip carrier 28 leads, .050 inch lead spacing, square. (issue A, 10/31/84).
2. Controlling dimensions: inches. Metric are shown in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M-1982.
4. "A" and "B" are reference datums on the molded body at plane "H" and do not include mold flash. Mold flash protrusion shall not exceed .006" (.15mm) on any side.
5. Datum "D-E" and "F-G" are determined where these center leads exit from the body at plane "H".
6. Pin numbers continue counterclockwise to pin #28 (top view).
7. Signetics order code for product packaged in a PLCC is the suffix A after the product number.

PO00611S

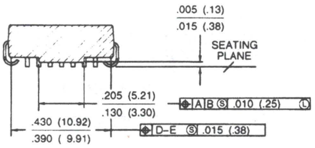
Package Outlines

AR2/PLASTIC PLCC-32


.595 (15.11)
.585 (14.86)
A F-G S .007 (.18) S
.400 (10.16) BSC
B D-E S .007 (.18) S
B S .002 IN / IN
-A- .010 (.25)
MAX. R
TYP.
3 PLACES
-G-
B D-E S .007 (.18) S
.453 (11.51)
.447 (11.35)
PIN # 1
.300 (7.62)
BSC
-D-
-E-
.495 (12.57)
.485 (12.32)
-F-
.048 (1.22)
.042 (1.07)
2 PLCS.
.050 (1.27)
4 SIDES
BSC
.025 (.64)
MIN.
A F-G S .007 (.18) S
A S .002 IN IN
-B-
.553 (14.05)
.547 (13.89)
.025 (.64)
MIN.
.032 (.81)
.026 (.66)
.029 (.74)
.023 (.58)
.095 (2.41)
.060 (1.52)
-H-
.140 (3.56)
.100 (2.54)
-C-
.004 (.10)
.021 (.53)
.013 (.33)
D-E S F-G S .007 (.18) M
.040 (1.02)
.030 (.76)
R
.530 (13.46)
.490 (12.45)
F-G S .015 (.38)

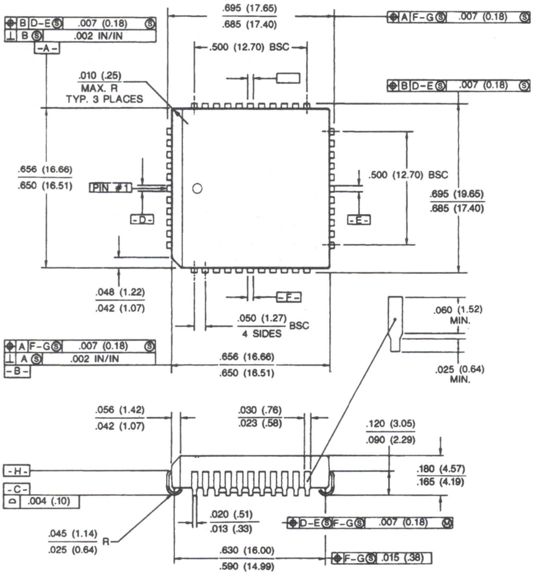
NOTES:

1. Package dimensions conform to JEDEC specification MO-047-AB for plastic leaded chip carrier 28 leads, .050 inch lead spacing, square. (issue A, 10/31/84).
2. Controlling dimensions: inches. Metric are shown in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M-1982.
4. "A" and "B" are reference datums on the molded body at plane "H" and do not include mold flash. Mold flash protrusion shall not exceed .006" (.15mm) on any side.
5. Datum "D-E" and "F-G" are determined where these center leads exit from the body at plane "H".
6. Pin numbers continue counterclockwise to pin #28 (top view).
7. Signetics order code for product packaged in a PLCC is the suffix A after the product number.


.005 (.13)
.015 (.38)
SEATING
PLANE
.205 (5.21)
.130 (3.30)
A B S .010 (.25) L
.430 (10.92)
.390 (9.91)
D-E S .015 (.38)

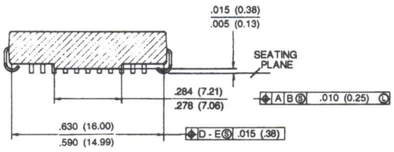
PO00170S

AX1/PLASTIC PLCC-44


B D-E S .007 (0.18) S
B S .002 IN/IN
-A-
.695 (17.65)
.685 (17.40)
A F-G S .007 (0.18) S
.500 (12.70) BSC
.010 (.25)
MAX. R
TYP. 3 PLACES
B D-E S .007 (0.18) S
.656 (16.66)
.650 (16.51)
PIN #1
.500 (12.70) BSC
.695 (19.65)
.685 (17.40)
-D-
-E-
.048 (1.22)
.042 (1.07)
-F-
.050 (1.27)
4 SIDES
BSC
.060 (1.52)
MIN.
A F-G S .007 (0.18) S
A S .002 IN/IN
-B-
.656 (16.66)
.650 (16.51)
.025 (0.64)
MIN.
.056 (1.42)
.042 (1.07)
.030 (.76)
.023 (.58)
.120 (3.05)
.090 (2.29)
-H-
.180 (4.57)
.165 (4.19)
-C-
.004 (.10)
.020 (.51)
.013 (.33)
D-E S F-G S .007 (0.18) M
.045 (1.14)
.025 (0.64)
R
.630 (16.00)
.590 (14.99)
F-G S .015 (.38)

NOTES:

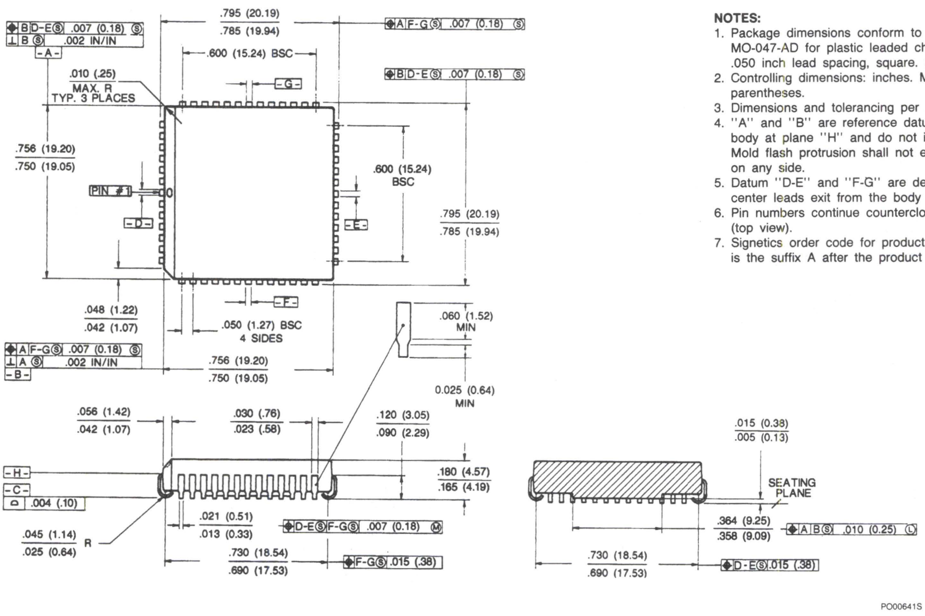
1. Package dimensions conform to JEDEC specification MO-047-AL for plastic leaded chip carrier 44 leads, .050 inch lead spacing, square. (issue A, 10/31/84).
2. Controlling dimensions: inches. Metric are shown in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M-1982.
4. "A" and "B" are reference datums on the molded body at plane "H" and do not include mold flash. Mold flash protrusion shall not exceed .006" (.15mm) on any side.
5. Datum "D-E" and "F-G" are determined where these center leads exit from the body at plane "H".
6. Pin numbers continue counterclockwise to pin #44 (top view).
7. Signetics order code for product packaged in a PLCC is the suffix A after the product number.


.015 (0.38)
.005 (0.13)
SEATING
PLANE
.284 (7.21)
.278 (7.06)
A B S .010 (0.25) L
.630 (16.00)
.590 (14.99)
D-E S .015 (.38)

PO00601S

Package Outlines

AA1 PLASTIC PLCC-52

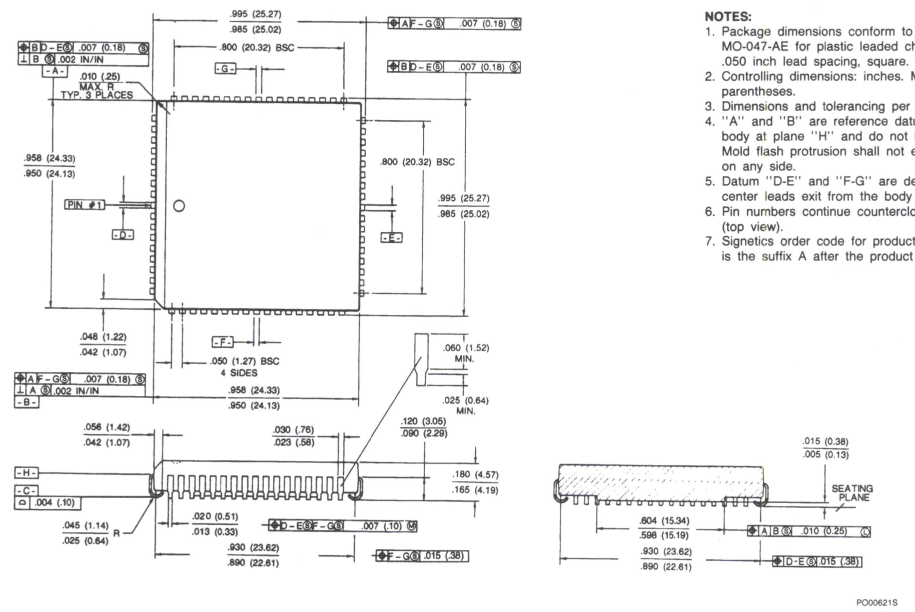


⊕ B D-E Ⓢ .007 (0.18) Ⓢ
⊥ B Ⓢ .002 IN/IN
-A-
.795 (20.19)
.785 (19.94)
.600 (15.24) BSC
⊕ A F-G Ⓢ .007 (0.18) Ⓢ
.010 (.25) MAX. R TYP. 3 PLACES
-G-
⊕ B D-E Ⓢ .007 (0.18) Ⓢ
.756 (19.20)
.750 (19.05)
PIN #1
.600 (15.24) BSC
-D-
-E-
.795 (20.19)
.785 (19.94)
.048 (1.22)
.042 (1.07)
-F-
.050 (1.27) BSC 4 SIDES
.060 (1.52) MIN
⊕ A F-G Ⓢ .007 (0.18) Ⓢ
⊥ A Ⓢ .002 IN/IN
-B-
.756 (19.20)
.750 (19.05)
0.025 (0.64) MIN
.056 (1.42)
.042 (1.07)
.030 (.76)
.023 (.58)
.120 (3.05)
.090 (2.29)
.015 (0.38)
.005 (0.13)
-H-
-C-
⏥ .004 (.10)
.180 (4.57)
.165 (4.19)
SEATING PLANE
.021 (0.51)
.013 (0.33)
⊕ D-E Ⓢ F-G Ⓢ .007 (0.18) Ⓜ
.364 (9.25)
.358 (9.09)
⊕ A B Ⓢ .010 (0.25) Ⓛ
.045 (1.14)
.025 (0.64)
R
.730 (18.54)
.690 (17.53)
⊕ F-G Ⓢ .015 (.38)
.730 (18.54)
.690 (17.53)
⊕ D-E Ⓢ .015 (.38)
PO00641S

NOTES:

1. Package dimensions conform to JEDEC specification MO-047-AD for plastic leaded chip carrier 52 leads, .050 inch lead spacing, square. (issue A, 10/31/84).
2. Controlling dimensions: inches. Metric are shown in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M-1982.
4. "A" and "B" are reference datums on the molded body at plane "H" and do not include mold flash. Mold flash protrusion shall not exceed .006" (.15mm) on any side.
5. Datum "D-E" and "F-G" are determined where these center leads exit from the body at plane "H".
6. Pin numbers continue counterclockwise to pin #52 (top view).
7. Signetics order code for product packaged in a PLCC is the suffix A after the product number.

AB1 PLASTIC PLCC-68



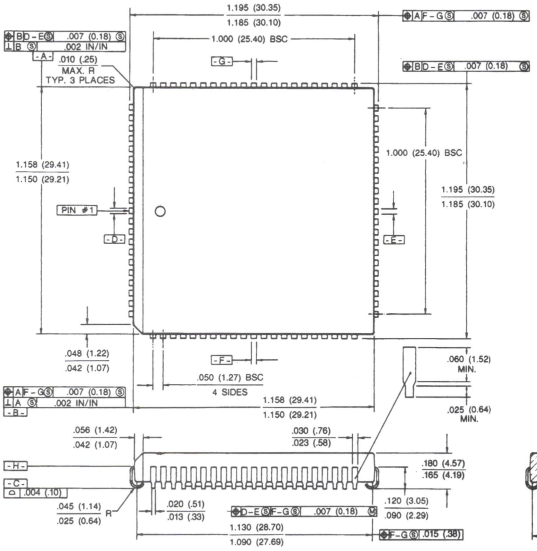
.995 (25.27)
.985 (25.02)
⊕ A F-G Ⓢ .007 (0.18) Ⓢ
⊕ B D-E Ⓢ .007 (0.18) Ⓢ
⊥ B Ⓢ .002 IN/IN
-A-
.800 (20.32) BSC
-G-
⊕ B D-E Ⓢ .007 (0.18) Ⓢ
.010 (.25) MAX. R TYP. 3 PLACES
.958 (24.33)
.950 (24.13)
.800 (20.32) BSC
PIN #1
.995 (25.27)
.985 (25.02)
-D-
-E-
.048 (1.22)
.042 (1.07)
-F-
.060 (1.52) MIN.
.050 (1.27) BSC 4 SIDES
⊕ A F-G Ⓢ .007 (0.18) Ⓢ
⊥ A Ⓢ .002 IN/IN
-B-
.958 (24.33)
.950 (24.13)
.025 (0.64) MIN.
.056 (1.42)
.042 (1.07)
.030 (.76)
.023 (.58)
.120 (3.05)
.090 (2.29)
.015 (0.38)
.005 (0.13)
-H-
.180 (4.57)
.165 (4.19)
-C-
⏥ .004 (.10)
SEATING PLANE
.045 (1.14)
.025 (0.64)
R
.020 (0.51)
.013 (0.33)
⊕ D-E Ⓢ F-G Ⓢ .007 (.10) Ⓜ
.604 (15.34)
.598 (15.19)
⊕ A B Ⓢ .010 (0.25) Ⓛ
.930 (23.62)
.890 (22.61)
⊕ F-G Ⓢ .015 (.38)
.930 (23.62)
.890 (22.61)
⊕ D-E Ⓢ .015 (.38)
PO00621S

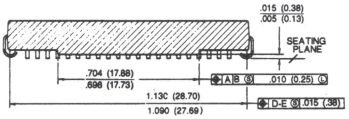
NOTES:

1. Package dimensions conform to JEDEC specification MO-047-AE for plastic leaded chip carrier 68 leads, .050 inch lead spacing, square. (issue A, 10/31/84).
2. Controlling dimensions: inches. Metric are shown in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M-1982.
4. "A" and "B" are reference datums on the molded body at plane "H" and do not include mold flash. Mold flash protrusion shall not exceed .006" (.15mm) on any side.
5. Datum "D-E" and "F-G" are determined where these center leads exit from the body at plane "H".
6. Pin numbers continue counterclockwise to pin #68 (top view).
7. Signetics order code for product packaged in a PLCC is the suffix A after the product number.

Package Outlines

AC1 PLASTIC PLCC-84


1.195 (30.35)
1.185 (30.10)
1.000 (25.40) BSC
A F-G S .007 (0.18) S
B D-E S .007 (0.18) S
B S .002 IN/IN
-A- .010 (.25)
MAX. R
TYP. 3 PLACES
-G-
B D-E S .007 (0.18) S
1.000 (25.40) BSC
1.158 (29.41)
1.150 (29.21)
1.195 (30.35)
1.185 (30.10)
PIN #1
-D-
-E-
.048 (1.22)
.042 (1.07)
-F-
.050 (1.27) BSC
4 SIDES
.060 (1.52)
MIN.
A F-G S .007 (0.18) S
A S .002 IN/IN
-B-
1.158 (29.41)
1.150 (29.21)
.025 (0.64)
MIN.
.056 (1.42)
.042 (1.07)
.030 (.76)
.023 (.58)
-H-
-C-
D .004 (.10)
.180 (4.57)
.165 (4.19)
.045 (1.14)
.025 (0.64)
R
.020 (.51)
.013 (.33)
D-E S F-G S .007 (0.18) M
.120 (3.05)
.090 (2.29)
1.130 (28.70)
1.090 (27.69)
F-G S .015 (.38)


.015 (0.38)
.005 (0.13)
SEATING
PLANE
.704 (17.88)
.696 (17.73)
A B S .010 (0.25) L
1.130 (28.70)
1.090 (27.69)
D-E S .015 (.38)

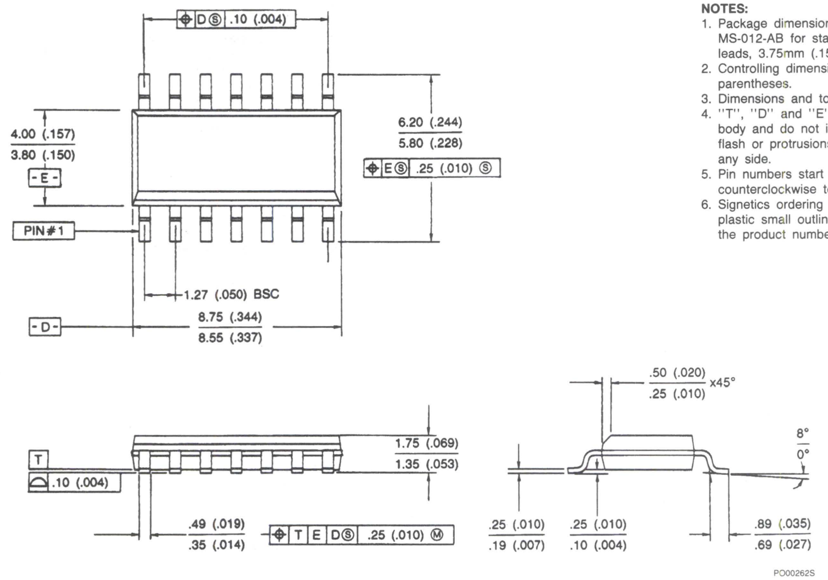
NOTES:

1. Package dimensions conform to JEDEC specification MO-047-AF for plastic leaded chip carrier 84 leads, .050 inch lead spacing, square. (issue A, 10/31/84).
2. Controlling dimensions: inches. Metric are shown in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M-1982.
4. "A" and "B" are reference datums on the molded body at plane "H" and do not include mold flash. Mold flash protrusion shall not exceed .006" (.15mm) on any side.
5. Datum "D-E" and "F-G" are determined where these center leads exit from the body at plane "H".
6. Pin numbers continue counterclockwise to pin #84 (top view).
7. Signetics order code for product packaged in a PLCC is the suffix A after the product number.

PO00591S

Package Outlines

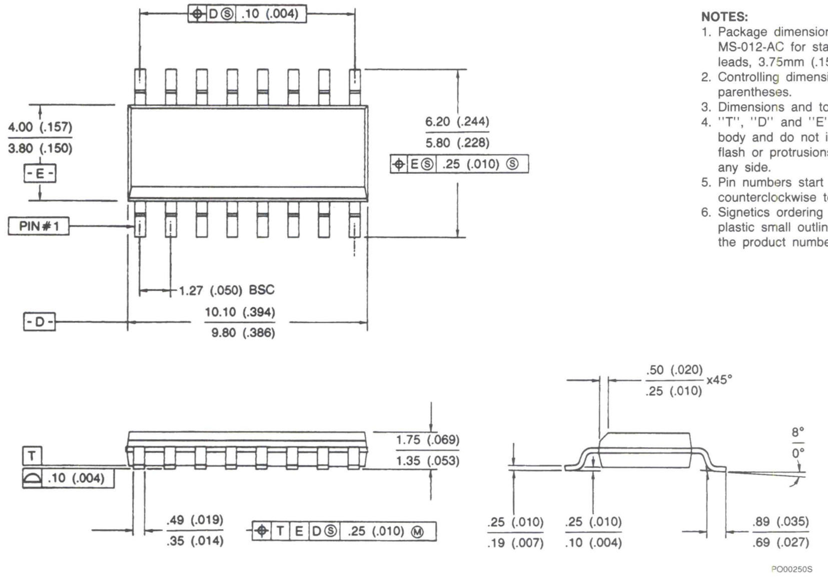
DH1/PLASTIC SO-14


⊕ D Ⓢ .10 (.004)
4.00 (.157)
3.80 (.150)
-E-
PIN#1
6.20 (.244)
5.80 (.228)
⊕ E Ⓢ .25 (.010) Ⓢ
1.27 (.050) BSC
-D-
8.75 (.344)
8.55 (.337)
.50 (.020)
.25 (.010)
x45°
T
.10 (.004)
1.75 (.069)
1.35 (.053)
8°
0°
.49 (.019)
.35 (.014)
⊕ T E D Ⓢ .25 (.010) Ⓜ
.25 (.010)
.19 (.007)
.25 (.010)
.10 (.004)
.89 (.035)
.69 (.027)
PO00262S

NOTES:

1. Package dimensions conform to JEDEC specification MS-012-AB for standard small outline (SO) package, 14 leads, 3.75mm (.150") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #14 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

DJ1/PLASTIC SO-16

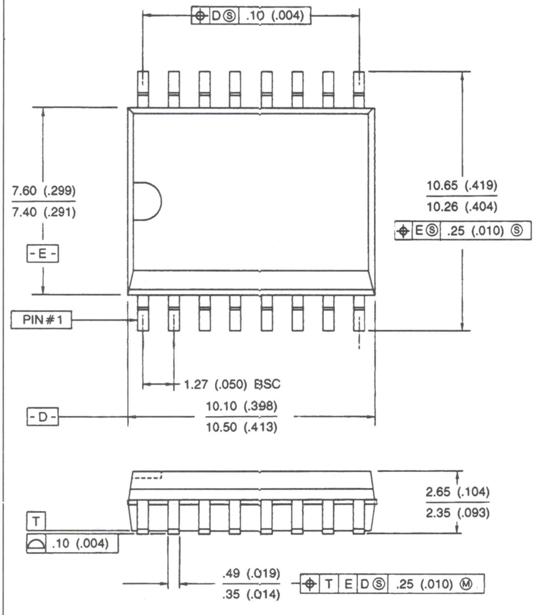

⊕ D Ⓢ .10 (.004)
4.00 (.157)
3.80 (.150)
-E-
PIN#1
6.20 (.244)
5.80 (.228)
⊕ E Ⓢ .25 (.010) Ⓢ
1.27 (.050) BSC
-D-
10.10 (.394)
9.80 (.386)
.50 (.020)
.25 (.010)
x45°
T
.10 (.004)
1.75 (.069)
1.35 (.053)
8°
0°
.49 (.019)
.35 (.014)
⊕ T E D Ⓢ .25 (.010) Ⓜ
.25 (.010)
.19 (.007)
.25 (.010)
.10 (.004)
.89 (.035)
.69 (.027)
PO00250S

NOTES:

1. Package dimensions conform to JEDEC specification MS-012-AC for standard small outline (SO) package, 16 leads, 3.75mm (.150") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #16 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

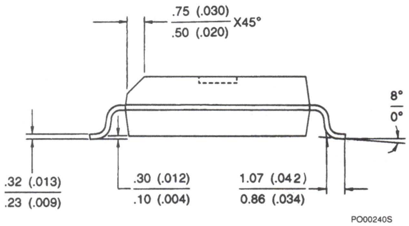
Package Outlines

DJ2/PLASTIC SOL-16

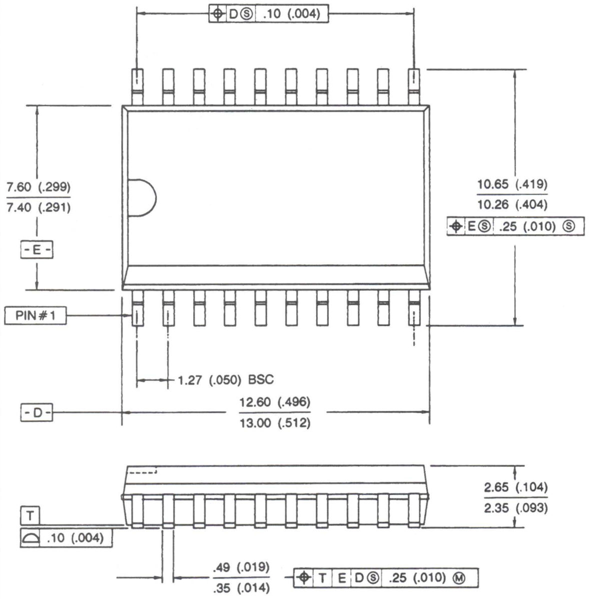

⌖ D Ⓢ .10 (.004)
10.65 (.419)
10.26 (.404)
⌖ E Ⓢ .25 (.010) Ⓢ
7.60 (.299)
7.40 (.291)
-E-
PIN #1
1.27 (.050) BSC
-D-
10.10 (.398)
10.50 (.413)
2.65 (.104)
2.35 (.093)
T
.10 (.004)
.49 (.019)
.35 (.014)
⌖ T E D Ⓢ .25 (.010) Ⓜ

NOTES:

1. Package dimensions conform to JEDEC specification MS-013-AA for standard small outline (SO) package, 16 leads, 7.50mm (.300") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #16 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

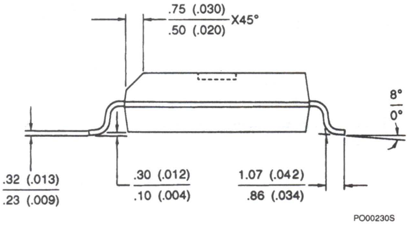

.75 (.030)
.50 (.020)
X45°
8°
0°
.32 (.013)
.23 (.009)
.30 (.012)
.10 (.004)
1.07 (.042)
0.86 (.034)
PO00240S

DL2/PLASTIC SOL-20


⌖ D Ⓢ .10 (.004)
10.65 (.419)
10.26 (.404)
⌖ E Ⓢ .25 (.010) Ⓢ
7.60 (.299)
7.40 (.291)
-E-
PIN #1
1.27 (.050) BSC
-D-
12.60 (.496)
13.00 (.512)
2.65 (.104)
2.35 (.093)
T
.10 (.004)
.49 (.019)
.35 (.014)
⌖ T E D Ⓢ .25 (.010) Ⓜ

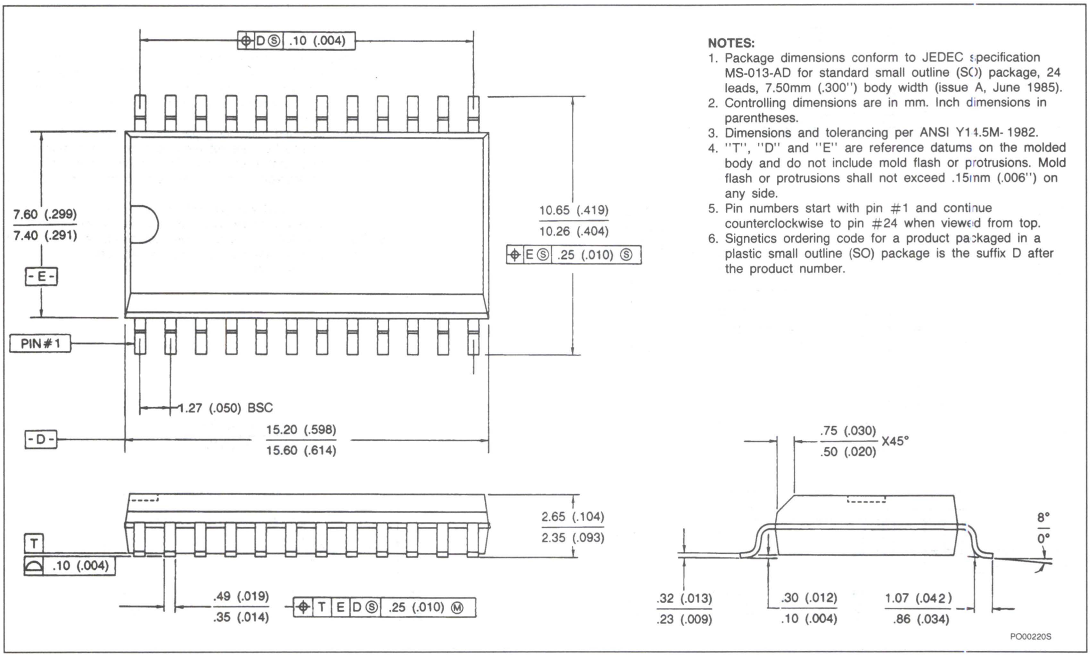
NOTES:

1. Package dimensions conform to JEDEC specification MS-013-AC for standard small outline (SO) package, 20 leads, 7.50mm (.300") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #20 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.


.75 (.030)
.50 (.020)
X45°
8°
0°
.32 (.013)
.23 (.009)
.30 (.012)
.10 (.004)
1.07 (.042)
.86 (.034)
PO00230S

Package Outlines

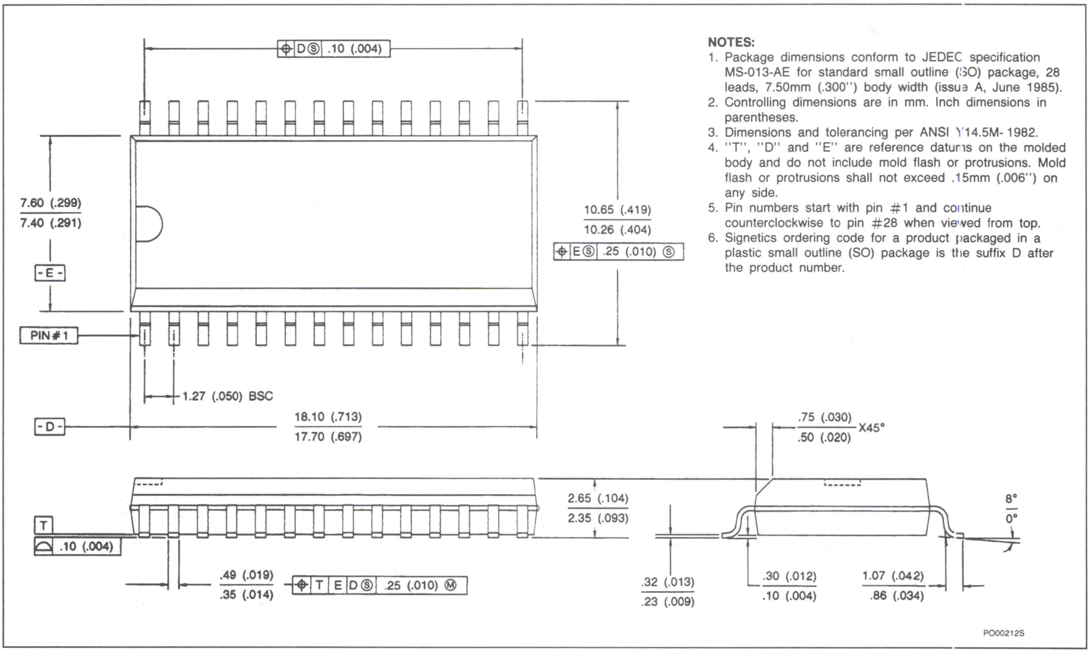
DN2/PLASTIC SOL-24



⊕ D Ⓢ .10 (.004)
7.60 (.299)
7.40 (.291)
-E-
PIN # 1
10.65 (.419)
10.26 (.404)
⊕ E Ⓢ .25 (.010) Ⓢ
1.27 (.050) BSC
-D-
15.20 (.598)
15.60 (.614)
2.65 (.104)
2.35 (.093)
T
.10 (.004)
.49 (.019)
.35 (.014)
⊕ T E D Ⓢ .25 (.010) Ⓜ
.75 (.030)
.50 (.020)
X45°
8°
0°
.32 (.013)
.23 (.009)
.30 (.012)
.10 (.004)
1.07 (.042)
.86 (.034)
PO00220S

NOTES:
1. Package dimensions conform to JEDEC specification MS-013-AD for standard small outline (SO) package, 24 leads, 7.50mm (.300") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #24 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

DQ2/PLASTIC SOL-28

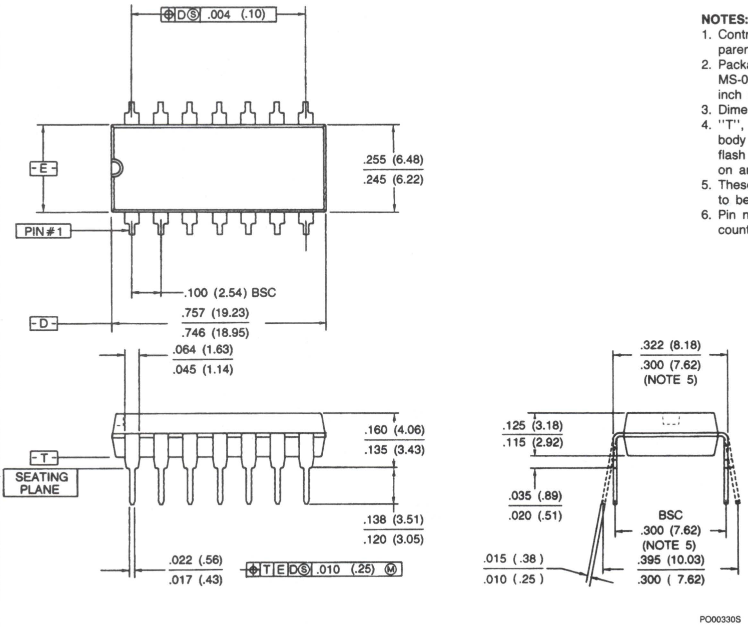


⊕ D Ⓢ .10 (.004)
7.60 (.299)
7.40 (.291)
-E-
PIN # 1
10.65 (.419)
10.26 (.404)
⊕ E Ⓢ .25 (.010) Ⓢ
1.27 (.050) BSC
-D-
18.10 (.713)
17.70 (.697)
2.65 (.104)
2.35 (.093)
T
.10 (.004)
.49 (.019)
.35 (.014)
⊕ T E D Ⓢ .25 (.010) Ⓜ
.75 (.030)
.50 (.020)
X45°
8°
0°
.32 (.013)
.23 (.009)
.30 (.012)
.10 (.004)
1.07 (.042)
.86 (.034)
PO00212S

NOTES:
1. Package dimensions conform to JEDEC specification MS-013-AE for standard small outline (SO) package, 28 leads, 7.50mm (.300") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #28 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

Package Outlines

NH1/PLASTIC DIP-14

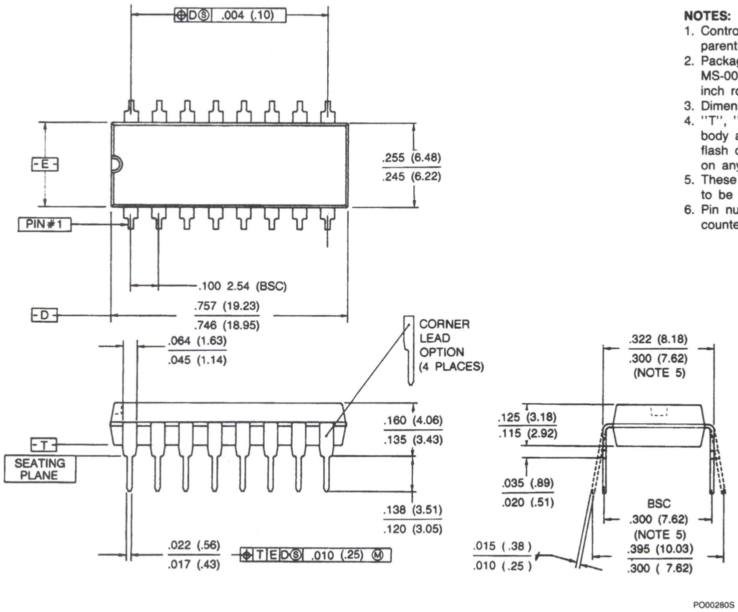


D S .004 (.10)
-E-
.255 (6.48)
.245 (6.22)
PIN #1
.100 (2.54) BSC
-D-
.757 (19.23)
.746 (18.95)
.064 (1.63)
.045 (1.14)
.322 (8.18)
.300 (7.62)
(NOTE 5)
.160 (4.06)
.135 (3.43)
.125 (3.18)
.115 (2.92)
-T-
SEATING PLANE
.035 (.89)
.020 (.51)
.138 (3.51)
.120 (3.05)
BSC
.300 (7.62)
(NOTE 5)
.022 (.56)
.017 (.43)
T E D S .010 (.25) M
.015 (.38)
.010 (.25)
.395 (10.03)
.300 (7.62)
PO00330S

NOTES:

1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-001-AC for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 14 leads (issue B. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #14 when viewed from the top.

NJ1/PLASTIC DIP-16



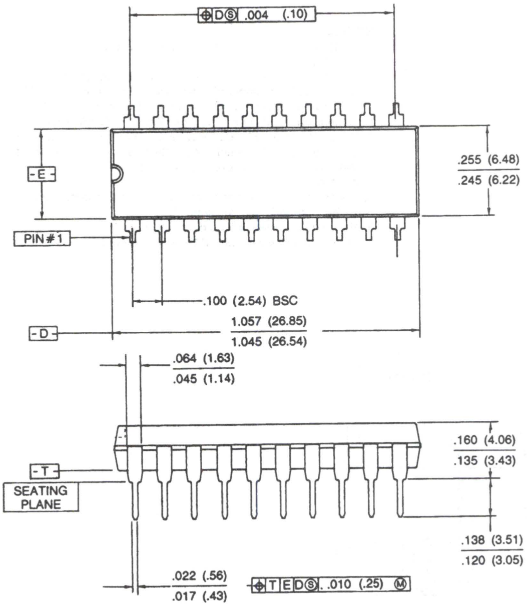
D S .004 (.10)
-E-
.255 (6.48)
.245 (6.22)
PIN #1
.100 2.54 (BSC)
-D-
.757 (19.23)
.746 (18.95)
CORNER LEAD OPTION (4 PLACES)
.064 (1.63)
.045 (1.14)
.322 (8.18)
.300 (7.62)
(NOTE 5)
.160 (4.06)
.135 (3.43)
.125 (3.18)
.115 (2.92)
-T-
SEATING PLANE
.035 (.89)
.020 (.51)
.138 (3.51)
.120 (3.05)
BSC
.300 (7.62)
(NOTE 5)
.022 (.56)
.017 (.43)
T E D S .010 (.25) M
.015 (.38)
.010 (.25)
.395 (10.03)
.300 (7.62)
PO00280S

NOTES:

1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-001-AA for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 16 leads (issue B. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #16 when viewed from the top.

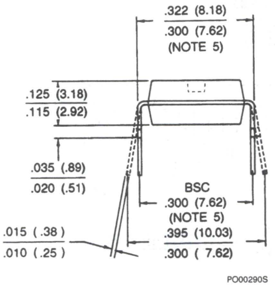
Package Outlines

NL1/PLASTIC DIP-20

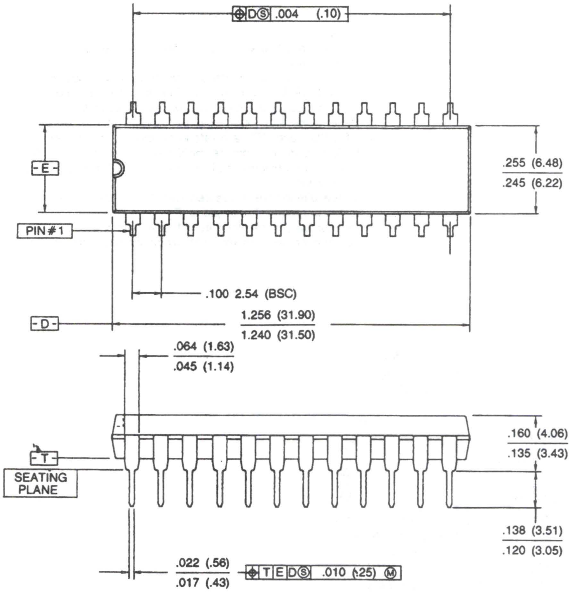

⊕ D Ⓢ .004 (.10)
-E-
PIN # 1
.255 (6.48)
.245 (6.22)
.100 (2.54) BSC
-D-
1.057 (26.85)
1.045 (26.54)
.064 (1.63)
.045 (1.14)
-T-
SEATING PLANE
.160 (4.06)
.135 (3.43)
.138 (3.51)
.120 (3.05)
.022 (.56)
.017 (.43)
⊕ T E D Ⓢ .010 (.25) Ⓜ

NOTES:

1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-001-AE for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 20 leads (issue B. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #20 when viewed from the top.

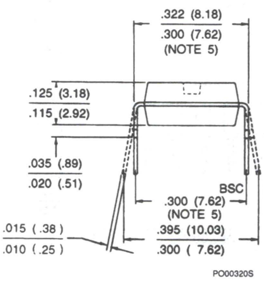

.322 (8.18)
.300 (7.62)
(NOTE 5)
.125 (3.18)
.115 (2.92)
.035 (.89)
.020 (.51)
BSC
.300 (7.62)
(NOTE 5)
.015 (.38)
.010 (.25)
.395 (10.03)
.300 (7.62)
PO00290S

NN1/PLASTIC DIP-24


⊕ D Ⓢ .004 (.10)
-E-
PIN # 1
.255 (6.48)
.245 (6.22)
.100 2.54 (BSC)
-D-
1.256 (31.90)
1.240 (31.50)
.064 (1.63)
.045 (1.14)
-T-
SEATING PLANE
.160 (4.06)
.135 (3.43)
.138 (3.51)
.120 (3.05)
.022 (.56)
.017 (.43)
⊕ T E D Ⓢ .010 (.25) Ⓜ

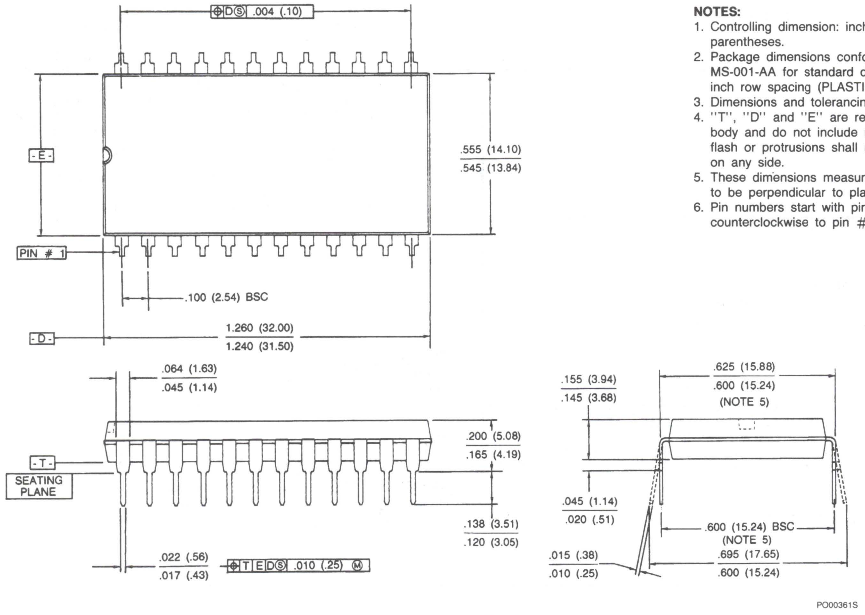
NOTES:

1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-001-AR for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 24 leads (issue B. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #24 when viewed from the top.


.322 (8.18)
.300 (7.62)
(NOTE 5)
.125 (3.18)
.115 (2.92)
.035 (.89)
.020 (.51)
BSC
.300 (7.62)
(NOTE 5)
.015 (.38)
.010 (.25)
.395 (10.03)
.300 (7.62)
PO00320S

Package Outlines

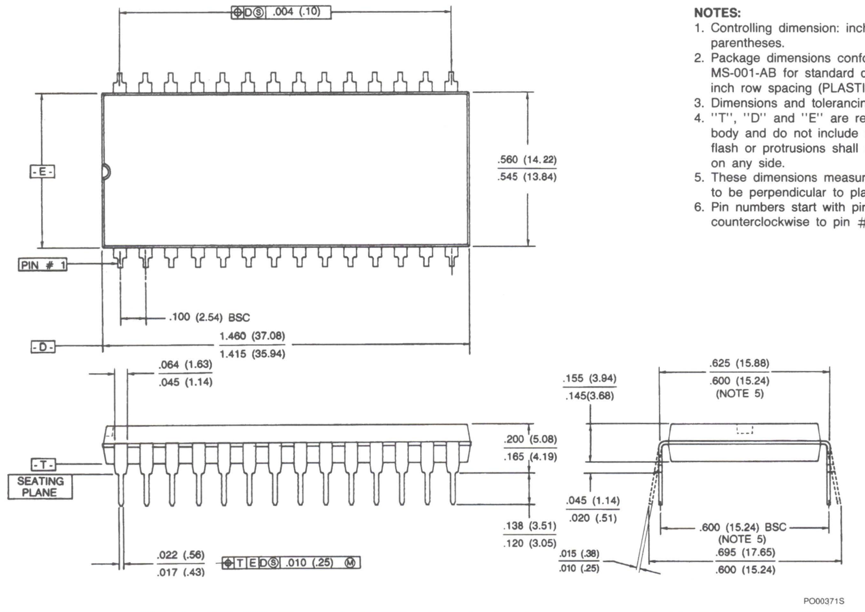
NN3/PLASTIC DIP-24


⊕ D Ⓢ .004 (.10)
- E -
.555 (14.10)
.545 (13.84)
PIN # 1
.100 (2.54) BSC
- D -
1.260 (32.00)
1.240 (31.50)
.064 (1.63)
.045 (1.14)
.200 (5.08)
.165 (4.19)
- T -
SEATING PLANE
.138 (3.51)
.120 (3.05)
.022 (.56)
.017 (.43)
⊕ T E D Ⓢ .010 (.25) Ⓜ
.155 (3.94)
.145 (3.68)
.625 (15.88)
.600 (15.24)
(NOTE 5)
.045 (1.14)
.020 (.51)
.600 (15.24) BSC
(NOTE 5)
.015 (.38)
.010 (.25)
.695 (17.65)
.600 (15.24)
PO00361S

NOTES:

1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-001-AA for standard dual in-line (DIP) package .600 inch row spacing (PLASTIC) 24 leads (issue B. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #24 when viewed from the top.

NQ3/PLASTIC DIP-28

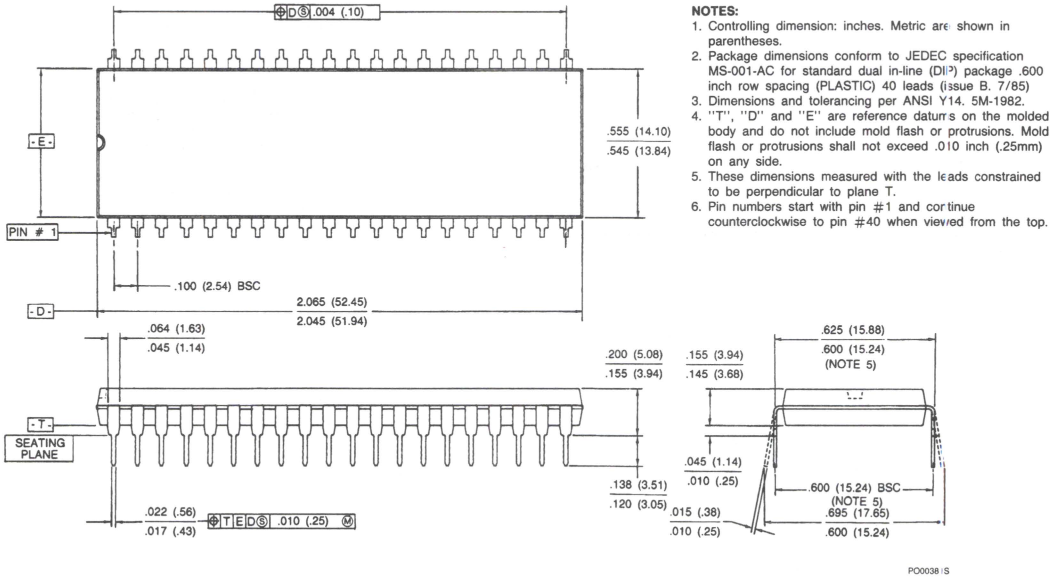

⊕ D Ⓢ .004 (.10)
- E -
.560 (14.22)
.545 (13.84)
PIN # 1
.100 (2.54) BSC
- D -
1.460 (37.08)
1.415 (35.94)
.064 (1.63)
.045 (1.14)
.200 (5.08)
.165 (4.19)
- T -
SEATING PLANE
.138 (3.51)
.120 (3.05)
.022 (.56)
.017 (.43)
⊕ T E D Ⓢ .010 (.25) Ⓜ
.155 (3.94)
.145(3.68)
.625 (15.88)
.600 (15.24)
(NOTE 5)
.045 (1.14)
.020 (.51)
.600 (15.24) BSC
(NOTE 5)
.015 (.38)
.010 (.25)
.695 (17.65)
.600 (15.24)
PO00371S

NOTES:

1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-001-AB for standard dual in-line (DIP) package .600 inch row spacing (PLASTIC) 28 leads (issue B. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #28 when viewed from the top.

Package Outlines

NW3/PLASTIC DIP-40


⊕ D Ⓢ .004 (.10)
-E-
PIN # 1
.555 (14.10)
.545 (13.84)
.100 (2.54) BSC
-D-
2.065 (52.45)
2.045 (51.94)
.064 (1.63)
.045 (1.14)
.200 (5.08)
.155 (3.94)
.155 (3.94)
.145 (3.68)
.625 (15.88)
.600 (15.24)
(NOTE 5)
-T-
SEATING PLANE
.045 (1.14)
.010 (.25)
.138 (3.51)
.120 (3.05)
.600 (15.24) BSC
(NOTE 5)
.015 (.38)
.010 (.25)
.695 (17.65)
.600 (15.24)
.022 (.56)
.017 (.43)
⊕ T E D Ⓢ .010 (.25) Ⓜ
PO0038 IS

NOTES:

1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-001-AC for standard dual in-line (DIP) package .600 inch row spacing (PLASTIC) 40 leads (issue B. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #40 when viewed from the top.

Package Outlines

PACKAGE OUTLINES FOR HERMETIC CERDIP

1. Controlling dimensions are given in inches, and millimeters in parentheses.
2. Dimensioning and tolerancing per ANSI Y14.5M – 1982.

2.1 ⊕ is a geometric characteristic symbol meaning: the accuracy of a position.

2.2 "T", "D", and "E" are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to mismatch.

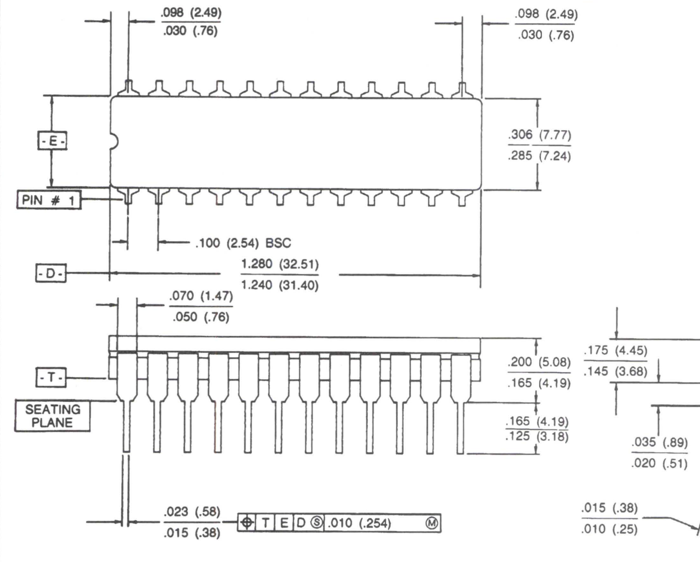
2.3 "S" is a modifying symbol and means: regardless of features.

2.4 "M" is a modifying symbol and means: at a maximum material condition.

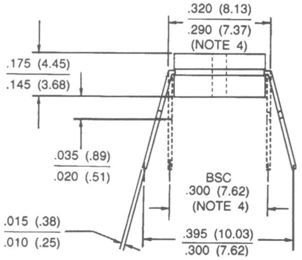
3. BSC means: Basic
4. These dimension measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with pin #1 and continue counter-clockwise when viewed from the top.
6. Lead material: ASTM alloy F – 38 (Alloy 42) or equivalent – tin plated or solder dipped.
7. Body Material: Ceramic with glass seal at leads.
8. Thermal resistance values are determined by temperature sensitive parameter (TSP) method. This method uses the forward voltage drop of a calibrated diode to measure the change in junction temperature due to a known power application.
9. Test conditions:
   Test ambient – still air
   Power dissipation – 1.0W
   Test fixture
   θ_{JA} – Textool ZIF socket with .040" stand-off
   θ_{JC} – water cooled heat sink

Package Outlines

FN1 24-PIN HERMETIC CERDIP (300mil-wide)



.098 (2.49)
.030 (.76)
.098 (2.49)
.030 (.76)
-E-
.306 (7.77)
.285 (7.24)
PIN # 1
.100 (2.54) BSC
-D-
1.280 (32.51)
1.240 (31.40)
.070 (1.47)
.050 (.76)
.200 (5.08)
.165 (4.19)
-T-
SEATING PLANE
.165 (4.19)
.125 (3.18)
.023 (.58)
.015 (.38)
T E D S .010 (.254) M
.175 (4.45)
.145 (3.68)
.035 (.89)
.020 (.51)
.015 (.38)
.010 (.25)



.320 (8.13)
.290 (7.37)
(NOTE 4)
BSC
.300 (7.62)
(NOTE 4)
.395 (10.03)
.300 (7.62)

NOTES:
1. Controlling dimension: inches. Millimeters are shown in parentheses.
2. Dimensions and tolerancing per ANSI Y14.5M – 1982.
3. "T", "D", and "E" are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch.
4. These dimensions measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #24 when viewed from the top.

853-0586 84000

FO00401S

Section 10
Sales Offices

Sales Offices

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Caracas
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Key Customer Interest

Fast Manual

Last name First name

Address

Company name

City State Zip

Department or Division

( )
Area code Phone number Extension

A. Please send additional information on surface mount technology. ☐ **Yes** ☐ **No**

B. Please send additional information on the following functions which are not shown in this data manual.

---

1. Your company and its products/services fit into the following category:

☐ Aerospace
☐ Consumer Products
☐ Computers
☐ Computer Peripherals
☐ Communications Products
☐ Basic Chemicals/Petroleum
☐ Instruments & Controls
☐ Office & Business Machines
☐ Telecommunications Products
☐ Bio/Medical Products
☐ Transportation
☐ Electrical Equipment
☐ Utilities
☐ Research & Development
☐ Industrial Equipment
☐ Defense & Military
☐ Government Agency
☐ Electronics System Integration
☐ Components & Sub-Assemblies
☐ Test & Measurement Equipment
☐ Auto/Truck/Bus Manufacturing
☐ Scientific Equipment
☐ Educational Institution
☐ Other ______

2. Your location is the:

☐ Company Headquarters
☐ Regional Headquarters
☐ Division Headquarters
☐ Military Facility
☐ Sales Office
☐ R & D Lab
☐ Engineering/Design Facility
☐ Distribution Facility
☐ Manufacturing Facility
☐ Repair/Retrofit Facility
☐ Other ______

3. Number of employees at your location: ☐ 1–250 ☐ 251–500 ☐ 501–1000 ☐ More than 1000

4. Number of engineers at your location: ______

5. Approximate annual company billings: ☐ Don't Know ☐ Under $5mm ☐ $5mm to $10mm ☐ $10mm to $100mm ☐ Over $100mm

6. Would you like a sales engineer to call you? ☐ YES ☐ NO

7. Please indicate your area(s) of product interest:

☐ **DIGITAL LOGIC (7)**
☐ **MEMORY (8)**
☐ **MICROPROCESSOR (9)**
☐ **SURFACE MOUNT DEVICES (10)**
☐ **VME INTERFACE DEVICES (11)**
☐ **MILITARY PRODUCTS (12)**
☐ **OTHER** products or applications **(13)** ______
☐ **LINEAR PRODUCTS (14)**
☐ **ASIC/SEMICUSTOM (15)**
☐ **MICROCONTROLLER (16)**
☐ **PROGRAMMABLE LOGIC DEVICES (PLD) (17)**

8. Your primary job responsibility/title is (check one only):

MANAGEMENT
☐ Senior Corp Manager
☐ Engineering Management
☐ Financial
☐ Purchasing/Procurement
☐ Production
☐ Project
☐ Other

ENGINEERING
☐ Section Leader
☐ Group Leader
☐ Project Engineer
☐ Design
☐ Aerospace
☐ Applications
☐ Component Evaluation
☐ Software
☐ Mechanical
☐ Materials Specifications
☐ Production
☐ Systems
☐ Ocean/Naval
☐ Quality Assurance
☐ Other

PURCHASING/PROCUREMENT
☐ Electronics Buyer
☐ General Purchasing Agent
☐ Production Component Buyer
☐ Engineering Buyer
☐ Other

EDUCATION/INSTRUCTION
☐ Professor
☐ Asst. Professor
☐ Instructor
☐ Industrial Instructor
☐ Student
☐ Research Scientist

CONSULTING
☐ Government
☐ Military
☐ Product Design
☐ Software Development
☐ Electronics Systems Design
☐ Systems Integration
☐ Component Evaluation
☐ Other

9. Do you recommend, specify, approve or direct purchasing of electronic components?

☐ Yes
☐ No

If yes, which of these:
☐ Digital Logic
☐ Linear
☐ ASIC/Semi Custom
☐ PLDs
☐ Memory
☐ Microprocessor
☐ Microcontroller
☐ VME Interface Devices
☐ SMD
☐ Military
☐ Other

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